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(54) **Title**: SPIN TORQUE MAGNETIC INTEGRATED CIRCUIT

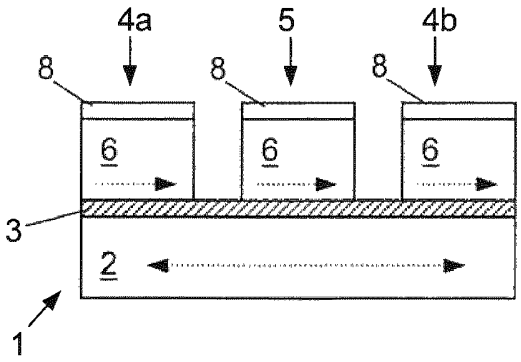

Fig. 1a

(57) **Abstract**: The invention relates to a spin torque magnetic integrated circuit (1), comprising a shared free layer (2) with a magnetic anisotropy such as a shape anisotropy or a crystal anisotropy with at least two stable magnetic states disposed on a substrate, a first non-magnetic layer (3) disposed on a first side of the free layer (2), input regions disposed on the non-magnetic layer (3), at least one output region (5) disposed on the non-magnetic layer (3), comprising at least one output layer (6), capping layers (8) to electrically contact the input regions (4a, 4b) and output region (5), wherein two input regions (4a, 4b) are disposed on the non-magnetic layer (3), at least one of the input regions (4a, 4b) comprises at least one magnetic input reference layer (6), and the orientation of the magnetization vectors of the input reference layers, the output reference layer, and the orientation of the magnetic anisotropy of the free layer are collinear. The invention further relates to a flip flop circuit comprising such a circuit, a shift register comprising such a flip flop, and methods to operate these circuits.

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Spin Torque Magnetic Integrated Circuit

The invention relates to a spin torque integrated circuit according to the preamble of claim 1, a flip flop circuit comprising such a circuit, a shift register comprising such a flip flop, and methods to operate these circuits.

Scaling CMOS technology has provided high density, high speed, and low power consumption electronic circuits. However, due to the constant shrinking of device dimensions the leakage currents - especially at standby – have become a serious issue. A possible solution to circumvent the standby power problem is to introduce non-volatile information storage in logic circuits. By this circuits can be shut down completely without loss of information and energy is only consumed when logic states are changed.

Ideally, a complete circuit could be powered off, while all data are protected, and instantly available when the power is up again. For achieving this goal one needs to introduce non-volatility in basic building blocks like Flip Flops (FF). Non-Volatile FFs (NVFF) store intermediate computing data in nonvolatile mode and offer these immediately when the circuit is re-powered.

Due to its high endurance, fast speed, low power consumption, and small area Spin-Transfer Torque Memory (STTM) devices are attractive candidates for realizing such NVFF.

The document WO 2011/075257 A2 discloses a spin torque magnetic integrated circuit, comprising a ferromagnetic free layer with a magnetic anisotropy with at least two stable magnetic states disposed on a substrate, a first non-magnetic layer disposed on a first side of the free layer, several input regions disposed on the non-magnetic layer, each comprising a ferromagnetic fixed input reference layer, several output regions disposed on the non-magnetic layer, comprising at least one ferromagnetic fixed output reference layer, and capping layers to electrically contact the input regions and output region.

However, the disclosed circuit is not suited for sequential logic needed for flip flop operations because it is an essential requirement of the described circuit that a multitude of input regions – that is, more than two – is provided, and the output signal exclusively depends on the majority of the input signals.

Therefore, the objective of the invention is to provide a non-volatile magnetic integrated circuit that enables sequential operations such as flip flop or shift register operation, while saving die space as compared to conventional circuits. A further objective is to provide methods to operate such circuits to enable sequential operations.

To overcome the above described problem, a spin torque magnetic integrated circuit is presented in which only two input regions are disposed on the non-magnetic layer, at least one of the input regions comprises at least one magnetic input reference layer, and the orientation of the magnetization vectors of the input reference layers, the output reference layer, and the orientation of the magnetic anisotropy of the free layer are chosen in such a way that they are collinear. This allows to use two and only two input regions for operation, and makes flip flop operation possible. Flip flop logic is realized in the magnetic domain by creating constructive or destructive superposition of two spin disturbances which are synchronously generated at the input regions. The operation result is saved via the magnetization orientation in the shared free layer, and can be read out by suitable sensing circuits.

The disclosed magnetic flip flop circuit is superior to conventional flip flop circuits, because instead of eight CMOS transistors (non clocked) or twelve CMOS transistors (clocked) for a classic RS flip flop or seven transistors and two magnetic tunnel junction memory elements for a non-volatile flip flop, only one non-volatile magnetic flip flop is needed. Thus the invented non-volatile magnetic flip flop saves die space and eases large scale integration. In contrast to CMOS RS flip flops there are no forbidden input combinations and thus circuit design is eased further.

Stacking and arrangement of several of these devices and their intrinsic logic allow the creation of an extremely dense shift register. By arranging the flip flops in two or more levels and applying two phase shifted clocking signals, the flip flops couple in a way that the information held by one shared free layer is successively passed via spin-transfer torque effect to the corresponding next shared free layer. By this means, shift register operation can be achieved.

Both input regions may comprise at least one magnetic input reference layer. The magnetization vectors of the input reference layers may have the same direction or the opposite direction as the magnetization vector of the output reference layer, depending on the polarity of the input signals. The input reference layers and the output reference layers might comprise ferromagnetic, anti-ferromagnetic, or synthetic anti-ferromagnetic layers. According to an embodiment of the invention, only a single input reference layer comprises a ferromagnetic, anti-ferromagnetic, or synthetic anti-ferromagnetic fixed layer.

According to an embodiment of the invention, the easy axis of the magnetic anisotropy of the free layer, the input reference layer, and the output reference layer may be oriented substantially in-plane with the substrate. This might be necessary if the respective layers have a magnetic shape anisotropy, such as for a bar shape or an elliptic shape.

According to a further embodiment of the invention the easy axis of the magnetic anisotropy of the free layer, the input reference layer, and the output reference layer may be oriented substantially out-of-plane in relation to the substrate. This might be possible if the respective layers have a magnetic crystal anisotropy.

Accordingly, the shape of the shared free layer may be bar like or elliptical in order to create an in-plane shape anisotropy needed for operation, but could be in principal of an arbitrary geometry if the anisotropy is material-induced such as for an out-of-plane anisotropy.

It is further provided that a second non-magnetic layer might be disposed on a second side of the free layer, and at least one electrically contactable input and/or output region comprising at least one magnetic fixed reference layer is disposed on the second non-magnetic layer. This enables to double the STT at operation in case of a geometrically symmetric stack and opposing reference layer magnetization, and therefore to reduce the switching current.

It is further provided that the layout of the free layer might have a y-shape where the two input regions and the output region are located on separate legs, and the angle between the input regions is between 0° and 180°, preferably between 30° and 120°.

The width of the shared free layer may be between 10 nm to 100 nm, its length between 2 to 10 times the width, preferably between 3 to 5 times the width, and its thickness may be in the range from 0.5 nm to 50 nm. Particularly, the width of the free layer can be between 10nm and 100nm, its length between 20nm and 1000nm, preferably between 30nm and 500nm, and its thickness between 0.5nm and 50nm.

The shared free layer may be composed of a ferromagnetic, an anti-ferromagnetic or a synthetic anti-ferromagnetic material. An out-of-plane crystal anisotropy may be realized if the shared free layer comprises terbium cobalt iron (TbCoFe) or cobalt platinum (CoPt) layers. Furthermore, a synthetic anti-ferromagnetic stack with crossing layers can form or be part of the shared free layer.

The non-magnetic layer may comprise an insulator such as an oxide like aluminum dioxide (Al_2O_3) or magnesium oxide (MgO). The non-magnetic layer may also comprise a metal such as copper or aluminum. Its thickness may range from 0.5 nm to 10 nm. The non-magnetic layer may be deposited above and/or below the shared free layer. It may comprise a single layer or a layer stack. It fulfils several purposes. On one hand, it works as a spin tunnel barrier and on the other hand it may be utilized to either electrically insulate or electrically contact a certain region.

It is further provided that the non-magnetic layer may cover the shared free layer completely or partially. Particularly, it might be advantegeous for certain embodiments if the non-magnetic layer covers the shared free layer only in the signal input regions and the signal output region.

The signal input region and the signal output region comprise a reference layer which may comprise a layer stack fixing its magnetization. For instance a pinning layer, a coupling layer, and a pinned layer or an (synthetic) antiferromagnetic layer, a coupling layer, and a ferromagnetic layer might be used. It may comprise partly another shared free layer in order to couple to another non-volatile magnetic integrated circuit.

The output region may be placed in the middle between two input regions, or on either side of the signal input region. Additionally one may supply the non-volatile magnetic integrated circuit and the non-volatile shift register with a small power source which will ensure safely defined states when the main power fails or the whole device is turned off.

There may also be a corresponding contact layer structure on the opposite side of the shared free layer to guarantee a perpendicular current flow to maximize the STT effect. This layer structure may be similar to the upper layer stack in order to reduce the switching current by a second STT contribution. Preferably, the spin torque from the second interface may be parallel to the spin torque from the first interface, otherwise the STT contributions would at least partially cancel each other out.

The stable magnetization states of the signal input regions and the signal output regions is preferably collinear to the magnetization in the shared free layer and either parallel or anti-parallel oriented.

The invention further relates to a method to operate a spin torque magnetic integrated circuit according to the invention, wherein the method comprises the following steps:
First, electrical current or voltage signals representing logic states are applied simultaneously at the two signal input regions. Then, the electrical current or voltage signals and any sensing currents or voltages are removed for a certain time period to relax the magnetic state of the integrated circuit. Within a time period, the logic state of the shared free layer is read out by a sense amplifier utilizing a sensing current or sensing voltage. Preferably, the time period is long enough to let the free layer relax to about 80% of its final state.

According to the invention, the logic state of the shared free layer might be read out by sensing the difference in electrical resistance for parallel and anti-parallel orientation of the input or output regions to the reference layer magnetization. Particularly, the logic state of the shared free layer might be read out by passing the magnetization via STT operation to an adjacent shared free layer of a second non-volatile magnetic integrated circuit.

The invention relates further to an integrated circuit comprising a first integrated circuit as described above, and a second circuit as described above, wherein at least one reference layer of the second circuit comprises a part of the free layer of the first circuit. The first circuit and the second circuit might be arranged in different levels, and they are preferably stacked to save die space. Particularly, the reference layer of a signal input region of the second circuit might comprise the shared free layer of the first circuit. In such an arrangement, it is possible to stack several integrated circuits operated as flip flops together, so that a shift register operation is achieved.

It is further provided that at least a third integrated circuit is provided, where at least one of the reference layers of the third circuit comprise the shared layer of any of the first or second circuit. This can be repeated as often as necessary, to realize a shift register with the desired number of stages.

The invention is further related to a method to operate such an arrangement comprising two integrated circuits connected together and operating as flip flops, wherein a first clock signal is applied to the input region of the first circuit and a second clock signal is applied to the input region of the second circuit and the first clock signal and the second clock signal are phase-shifted, wherein the first clock signal and the second clock signal are preferably provided in such a way that there is a relaxation time window between the pulses of the clock signals in which the first circuit and the second circuit are unpowered.

Further features of the invention become evident from the description of the embodiments, the figures, and the claims.

A detailed description of several embodiments of the invention is given below.

Fig. 1a-1c: Schematic cross-section of a spin torque integrated circuit according to the invention;

Fig. 2a-2c: Schematic cross-section of a spin torque integrated circuit according to the invention;

Fig. 3a-3c: Schematic cross-section of a spin torque integrated circuit according to the invention;

Fig. 4: Truth table of a non-volatile magnetic flip flop according to the invention;

Fig. 5: Truth table of a non-volatile magnetic flip flop according to the invention;

Fig. 6: Top view of an alternative non-volatile magnetic flip flop layout according to the invention;

Fig. 7a: Circuit diagram of a proposed non-volatile shift register operating with AB flip flop logic;

Fig. 7b: Top view of a first non-volatile shift register layout according to the invention;

Fig. 7c: Schematic cross-section of a first non-volatile shift register according to the invention;

Fig. 7d: Timing diagram of a non-volatile shift register according to the invention;

Fig. 8a: Schematic top view of a second non-volatile shift register according to the invention,

Fig. 8b: Schematic cross-section of the second non-volatile shift register layout.

Figs. 1 to 3 show several embodiments of non-volatile magnetic integrated circuits 1 comprising a shared free layer 2, a first non-magnetic layer 3, two signal input regions 4a, 4b, and at least one signal output region 5. The shared free layer 2 may be deposited as whole or partially above a substrate. It exhibits a magnetic anisotropy which may be a shape anisotropy and/or a crystal anisotropy, which defines two stable magnetic states. In the embodiments of Figs. 2a, 2b, 3a, and 3b, the magnetic anisotropy of the shared free layer 2 is a crystal anisotropy. The easy axis of the anisotropy is either oriented in-plane, as in Fig. 1a and 1b, or out-of-plane, as in Fig. 2a and 2b.

The non-magnetic layer 3 works as a spin tunnel barrier and it may also be utilized to either electrically insulate or electrically contact a certain region. Therefore, it may consist of an oxide e.g. aluminum dioxide (Al_2O_3), magnesium oxide (MgO), etc. or of a metal e.g. copper, aluminum, etc. In Figs. 1a to 1b it is deposited above the shared free layer 2 and covers the shared free layer 2 completely. Its thickness ranges from 0.5 nm to 10 nm. In Figs. 2a and 2b, it is deposited only partially on the the shared free layer 2 in the region where the reference layers 6 are deposited. In Figs. 3a and 3b, a second non-magnetic layer 9 is deposited on the back side of the shared free layer 2.

The signal input regions 4a, 4b and the signal output region 5 are disposed on the non-magnetic layer 3. Each of these layers contains a reference layer 6 which may comprise a layer stack fixing its magnetization. The reference layer may comprise the shared free layer of a different magnetic circuit in order to couple to another non-volatile magnetic integrated circuit 1. Additionally, the signal input regions 4a, 4b and the signal output region 5 comprise a capping layer 8 to electrically contact the structure.

Figs. 3a and 3b show that there may also be corresponding contact layer structures 8 on the back side of the shared free layer 2 to guarantee a perpendicular current flow to maximize the STT effect. This layer structure is similar to the upper layer stack in order to reduce the switching current by a second STT contribution.

If the layer structure is identical its magnetization should point in the opposite direction of the first layer. In a further embodiment not shown, the layer structure on the back side of the shared free layer 2 is different from the upper layer structure.

Figs. 1c, 2c, and 3c show further embodiments of the integrated circuits according to the invention, in which the direction of the magnetization vectors in the input regions 4a, 4b are anti-parallalel.

The stable magnetization states of the signal input regions 4a, 4b and the signal output region 5 are shown by the dotted arrows and are collinear to the magnetization in the shared free layer 2 and either parallel or anti-parallel oriented.
To operate the described circuit 1, the method according to the invention is described below, making use of the truth tables in Fig. 4 and Fig. 5. The method comprises the following steps: First, electrical current or voltage signals A and B representing logic states are applied simultaneously at the two signal input regions. For instance, a positive current or voltage pulse denotes logic 1 and a negative current or voltage pulse represents logic 0.

Applying a current or voltage pulse to a signal input region 4a causes a STT operation in the shared free layer 2 at the region where the shared free layer 2 overlaps with the signal input region 4a. The onset of the input pulse generates a spin disturbance which travels through the shared free layer 2 heading to the opposite boundary of the shared free layer 2 where it is reflected and additionally pushed by STT exerted in the second signal input region 4b.

Due to this kind of oscillating motion, the spin disturbance gains power over time and the localized precessing motions successively increase up to the point where they overcome the energy threshold separating the two stable states. Once the magnetization is flipped the STT changes from enhancing the precessional motion to damping the precessional motion so it will relax to its new stable state fast.

In Fig. 4 and Fig. 5, the signals in the two signal input regions 4a, 4b are denoted A and B. The symbol Q_i denotes the output of time step i. There are two types of flip flop logic available. AB flip flop logic is shown in Fig. 4, and RS flip flop is shown in Fig. 5.

The AB flip flop sets its state Q_i to 1 if both inputs (A and B) are set to 1, sets its state to 0 if both inputs are set to 0, and holds its state $Q_i = Q_{i-1}$ if they are unequal. For this flip flop the magnetization vectors of the input reference layers must both have the same direction.

Two spin disturbances are synchronously generated. They can exhibit the same phase angle, corresponding to Case 1 and 4 in Fig. 4 or Case 2 and 3 in Fig. 5. If they are generated by oppositely oriented spin transfer torques, the disturbances have a 180° phase shift, corresponding to Case 2 and 3 in Fig. 4 or Case 1 and 4 in Fig. 5.

In the cases where the two spin disturbances posses no phase shift, the disturbances superimpose constructively which leads to an enhanced switching speed, while when the two disturbances are inverse to each other they superimpose destructively which represses the precession built up and prevents switching.
Thus, by applying simultaneous positive or negative voltage/current pulses the magnetization state of the shared free layer 2 can be set, reset, or held unchanged as needed for flip flop operation.

The RS flip flop is realized by inverting one of the signal inputs, e.g. A in Fig. 5. It sets its state Q_i to 1 if $R = \bar{A} = 0$ (R denotes reset) and $S = B = 1$ (S denotes set), sets its state Q_i to 0 if $R = 1$ and $S = B = 0$, and holds its state $Q_i = Q_{i-1}$ if they are equal as shown in Fig. 5. The inversion can be realized in several ways. One may invert the input current or voltage pulse polarity or may make the STTs act in opposite directions. In one embodiment, the magnetic vectors of the input reference layers 6 have opposite directions. In a further embodiment, one may utilize a synthetic anti-ferromagnetic stack with crossing layers (upper (lower) layer goes down (up) joining layer from an adjacent synthetic anti-ferromagnetic stack) for the shared free layer 2.

Within a time period, the logic state of the shared free layer is read out by a sense amplifier utilizing a sensing current or sensing voltage. If the reading currents or voltages are small enough to prevent undesired switching events, the signal input regions 4a, 4b can be used for sensing the logic state Q_i represented by the magnetization of the shared free layer 2. It may be read out by sensing the difference in electrical resistance for parallel and anti-parallel orientation to the reference layer magnetization and a sense amplifier.

Alternatively, the logic state Q_i may be passed on via STT to an adjacent shared free layer 2 of a neighboring non-volatile magnetic integrated circuit 1. After reading, the electrical current or voltage signals and any sensing currents or voltages are removed for a certain time period to relax the magnetic state of the spin torque magnetic integrated circuit.

Fig. 6 shows an alternative embodiment of a non-volatile magnetic integrated circuit 1 featuring a y-shaped layout. The angle between the signal input regions 4a and 4b is approximately 90°. If the circuit is used for flip flop operation, the two simultaneously generated spin disturbances are scattered at the leg intersection and only a part of the incoming spin disturbances contributes to switch the leg containing the signal output region 5, which is electrically inactive during write operation, and the before described resonance effect is strongly reduced causing higher switching currents. However, it may be useful when due to space constraints it is necessary to place the signal output region 5 separate from the signal input regions 4a, 4b.

For demonstration purposes simulations a set of simulations of non exclusive embodiments of non-volatile magnetic integrated circuits 1 have been carried out. Metal non-magnetic layers 3 causing a current spin polarization of P = 0.3, a magnetization saturation $M_S = 4 \times 10^5$ A/m, an outof-plane uni axial crystal anisotropy $K = 1 \times 10^5$ J/m^3, an exchange constant $A_{exch} = 2 \times 10^{-11}$ J/m, a shared free layer thickness of 3 nm, a device width of 30 nm, and a device length of 120 nm were assumed. The device was found starting to be operational at $\approx 10^{10}$ A/m^2 until $\approx 10^{12}$ A/m^2.

For the y-shape embodiment shown in Fig. 6 it takes between one and two orders of magnitude larger current densities depending on leg angle and length. Switching speed depends on the applied current density and ranges from tens of nanoseconds to picoseconds.

In a further embodiment, in order to reduce the required current densities, oxide non-magnetic layers 3 such as MgO are used. This raises the spin current polarization to about 0.6 – 1. In a further embodiment, a further tunnel barrier is provided below the shared free layer 2 to add a further STT contribution supporting the switching process.

In order to further illustrate practical applications of the invented non-volatile magnetic integrated circuit 1, several non-limiting embodiments of shift register topologies and their operation are shown.

Figs. 7a-7c show a first working example of a non-volatile shift register 7 comprising three non-volatile magnetic integrated ciruits 100, 200, 300, where the contact layers 8 have been omitted for clarity. For the sake of simplicity only three circuits 100, 200, and 300 are shown, but the extension to larger non-volatile shift registers is straightforward.

Fig. 7a shows the circuit diagram of the shift register 7 with the integrated circuits 100, 200, and 300 connected in series and working as flip flops. The input signal 403 is attached to the input regions 104a, 104b of the first circuit 100. The output region of the first circuit 100 is equivalent to the input region 204a of the second circuit 200, and the output region 205 of the second circuit 200 is equivalent to the input region 304a of the third circuit 300. The second input regions 204b, 304b of the circuits 200 and 300 are driven by independent clock signals 401 and 402.

Fig. 7b shows a schematic top view of the layout of the shift register 7, and Fig. 7c shows a schematic cross section along the cut A-A of Fig. 7b. The circuits 100, 200, and 300 are placed in two distinct levels. In further embodiments, they could also be arranged in multiple levels. A first flip flop circuit 100 has signal input regions 104a and 104b and a signal output region 105. The signal output region 105 is arranged in such a way that it operates as signal input region 204a of the second circuit 200. The second circuit 200 has a second signal input region 204b, and a signal output region 205. The signal output region 205 works as a signal input region 304a of the third circuit 300. This scheme can be repeated as long as necessary to achieve the desired number of stages of the shift register.

Fig. 7d shows a timing diagram of the shift register. Clock signals 401, 402 comprise a periodic signal with a first pulse, a relaxation window Tr1, Tr2 without any signal, and a second pulse with opposite polarity to the first pulse within its period. The relaxation windows Tr1, Tr2 are required for relaxation. The time slot in between electrically decouples the two distinct levels. Two pulses, positive and negative, are needed to copy the state from the preceding non-volatile magnetic flip flop 100 into the subsequent non-volatile magnetic flip flop 200.

Additionally, there may be further time slots without any signal to allow data readout (e.g. serial to parallel data conversion).

A current or voltage pulse input signal 403 is applied to the signal input regions 104a and 104b. During the write operation of the non-volatile magnetic flip flop 100 the non-volatile magnetic flip flop 200 is electrically inactive. After the corresponding writing pulses there is a sufficiently relaxation window Tr1, such as several nanoseconds, where no signal is applied in order to relax the magnetization in the shared free layer to the desired state. The length of the relaxation window depends on the application, but is generally in the in the regime of picoseconds to tens of nanoseconds. Then the circuit 100 is in read mode and and its shared free layer 102 is used as a reference layer for the input of the second circuit 200 while the second signal input region 204b receives a first clock signal 401.

The information stored in shared free layer 102 is passed to the shared free layer 202 via STT effect by a spin polarized current flowing from the reference layer in the signal output region 105 stack through the non-magnetic layer 203.

As an alternative embodiment, the non-magnetic layer 103 can comprise a metallic material. In this case, non-magnetic layer 103 can be contacted directly and the space between the signal input regions 104a, 104b and signal output region 105 can be used for feeding leads.

Since in read mode only the signal output region 105 is powered, only half the spin torque is exerted on shared free layer 102 and the spin disturbance path to a reflecting boundary and the power gain region is doubled. Thus, it takes much longer to flip the shared free layer 102 than to flip the shared free layer 202 which is in write mode with two active signal input regions 204a, 204b. This enables a non-disturbing readout.

The current or voltage pulses applied to the signal input region 204a must be synchronous to clock signal 401 at signal input region 204b but their polarity must be fixed. This is required due to the two intrinsic flip flop logic types (AB and RS) and the additional degree of freedom, which is introduced by employing the shared free layer 102 as reference layer in order to fix it to AB flip flop logic.

After a time slot Tr2 for relaxing the shared free layer 202, which is already taken care of by the clock signal 401, the non-volatile magnetic flip flop 200 is switched from write to read mode.

This means the signal input regions 204a and 204b are without power, while the signal output region 205 is used to transfer its magnetization state via STT operation to the signal input region 304a and shared free layer 302 through the non-magnetic layer 303 to the subsequent non-volatile magnetic flip flop 300.

Again the input signal for signal input region 304a is synchronous to a second clock signal 402 and only exhibits one type of polarity. The clock signal 402 is shifted with respect to clock signal 401 in order to guarantee that either the first (preceding) level of flip flops or the second (subsequent) level of flip flops is in write (read) mode.

Thus, with every clock cycle of clock signal 401 and clock signal 402 a signal input 403 written in non-volatile magnetic flip flop 100 is successively copied into non-volatile magnetic flip flop 200 and from there to the non-volatile magnetic flip flop 300 and so on. By changing the phase and/or polarities of the clock signal 401, clock signal 402, and the other input signals the signal flow in the shift register can be reversed.

Figs. 8a – 8b show a second embodiment of a non-volatile shift register 7 according to the invention. Its operation principle is similar to the first embodiment, but it allows in-plane as well as out-of-plane anisotropies, because the layout of the circuits 100, 200, 300 does not have to be crossed. The non-volatile magnetic integrated circuits 1 are again arranged in two levels but instead of placing them crossed they are ordered along a line. Furthermore, signal input regions 104b, 204b, 304b changed place with signal output regions 105, 205, 305.

The signal input 403 is written into the circuit 100 synchronously to the clock signal 402. Since all non-volatile magnetic flip flops are operated in AB logic mode both input signals must exhibit the same polarity to set or reset the respective flip flop. Thus, applying a positive pulse sets the circuit 100 and the information is held, until it is reset. The information is copied to the second circuit 200, when clock signal 401 and the signal from signal output region 105, which is synchronous to signal 401 and has a fixed polarity, have the same polarity.

The information stored in circuit 200 is copied to non-volatile magnetic flip flop 300 over the output region 305, when clock signal 402 and the signal from signal output region 205, which is synchronous to signal 402 and has a fixed polarity, have the same polarity. Thus, information written into the non-volatile magnetic integrated circuit 100 by the input signal 403 is successively pushed through the whole shift register.

With the aid of these two working examples a person skilled in the art is able to amend the presented topologies in a way that fits his needs without any difficulties (e.g. 90° corners etc.).

By employing the above described devices and circuits one is able to realize truly instant on devices, save die space, ease large scale integration, operate at high speeds, and enable low power consumption. Since the described invention is CMOS compatible it may be used in hybrid circuits as well as spintronics only circuits working completely in magnetic domain via STT and spin disturbances.

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List of reference numerals

1, 100, 200, 300	Spin torque magnetic integrated circuit
2, 102, 202, 302	Shared free layer
3, 203, 103, 303	Non-magnetic layer
4a, 104a, 204a, 304a,	First input region
4b, 104b, 2014b, 304b	Second input region
5, 105, 205, 305	Output region
6	Reference layer
7	Shift register
8	Capping layer
9	Second non-magnetic layer
401, 402	Clock signal
403	Signal input

Claims

1. Spin torque magnetic integrated circuit (1), comprising:
   - a shared free layer (2) with a magnetic anisotropy such as a shape anisotropy or a crystal anisotropy with at least two stable magnetic states disposed on a substrate,
   - a first non-magnetic layer (3) disposed on a first side of the free layer (2),
   - input regions disposed on the non-magnetic layer (3),
   - at least one output region (5) disposed on the non-magnetic layer (3), comprising at least one output layer (6),
   - capping layers (8) to electrically contact the input regions (4a, 4b) and output region (5),

   characterized in that

   only two input regions (4a, 4b) are disposed on the non-magnetic layer (3),
   at least one of the input regions (4a, 4b) comprises at least one magnetic input reference layer (6), and
   the orientation of the magnetization vectors of the input reference layer, the output reference layer, and the orientation of the magnetic anisotropy of the free layer are collinear.

2. Spin torque magnetic integrated ciruit according to claim 1, characterized in that both input regions (4a, 4b) comprise at least one magnetic input reference layer (6).

3. Spin torque magnetic integrated circuit according to claim 1 or 2, characterized in that at least one magnetization vector of the input reference layers of the input regions (4a, 4b) has the same direction or the opposite direction as the magnetization vector of the reference layer of the output region (5).

4. Spin torque magnetic integrated circuit according to any of the preceding claims, characterized in that the easy axis of the magnetic anisotropy of the free layer, the input reference layer, and the output reference layer are oriented substantially in-plane with the substrate.

5. Spin torque magnetic integrated circuit according to any of the preceding claims, characterized in that the easy axis of the magnetic anisotropy of the free layer, the input reference layer, and the output reference layer are oriented substantially out-of-plane in relation to the substrate.

6. Spin torque magnetic integrated circuit according to any of the preceding claims, characterized in that a second non-magnetic layer (9) is disposed on a second side of the free layer (2), and at least one electrically contactable input and/or output region comprising at least one magnetic fixed reference layer is disposed on the second non-magnetic layer (9) to reduce the switching current.

7. Spin torque magnetic integrated circuit according to any of the preceding claims, characterized in that the non-magnetic layer covers the shared free layer only partially, particularly only in the signal input regions and signal output regions.

8. Method to operate a spin torque magnetic integrated circuit according to any of the preceding claims in sequential logic operation, such as flip-flop or shift register operation,
characterized in that
the method comprises the following steps:
- electrical current or voltage signals representing logic states are applied simultaneously at the two signal input regions (4a, 4b);
- the electrical current or voltage signals and any sensing currents or voltages are removed for a certain time period to relax the magnetic state of the spin torque magnetic integrated circuit;
- within a time period, the logic state of the shared free layer is read out by a sense amplifier utilizing a sensing current or sensing voltage.

9. Method according to claim 8, characterized in that the logic state of the shared free layer is read out by sensing the difference in electrical resistance for parallel and anti-parallel orientation of the input or output regions to the reference layer magnetization.

10. Method according to claim 8, characterized in that the logic state of the shared free layer is read out by passing the magnetization via STT operation to an adjacent shared free layer (2) of a second non-volatile magnetic integrated circuit (1).

11. Spin torque magnetic integrated circuit comprising
    - a first circuit according to any of the claims 1 to 7, and
    - a second circuit according to any of claims 1 to 7,

    characterized in that at least one reference layer (6) of the first circuit comprises a part of the free layer (2) of the second circuit.

12. Spin torque magnetic integrated circuit according to claim 11, characterized in that the first circuit and the second circuit are arranged in different levels, preferably stacked.

13. Spin torque magnetic integrated circuit according to claim 11 or 12, characterized in that the reference layer (6) of a signal input region (4) of the second circuit comprises the free layer (2) of the first circuit.

14. Spin torque magnetic integrated circuit according to any of claims 11 to 13, characterized in that at least a third circuit according to any of the claims 1 to 7 is provided, where at least one reference layers of the third circuit comprises the shared layer of any of the first or second circuit.

15. Method to operate a spin torque magnetic integrated circuit according to any of claims 11 to 14 in sequential logic operation, such as flip-flop or shift register operation, characterized in that the method comprises the following steps:
    - a first clock signal (401) is applied to the input region of the first circuit;
    - a second clock signal (402) is applied to the input region of the second circuit;
    - where the first clock signal and the second clock signal are phase-shifted, and
    - the first clock signal (401) and the second clock signal (403) are provided in such a way that there is a relaxation time window between the pulses of the clock signals during which the first circuit and the second circuit are unpowered.

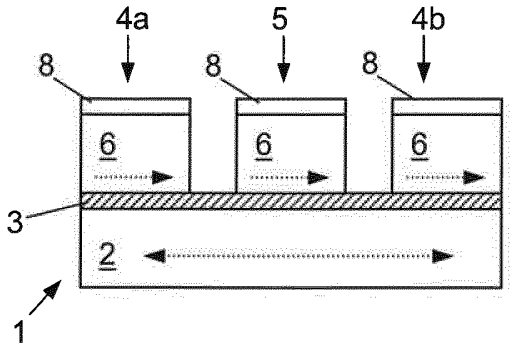


Fig. 1a

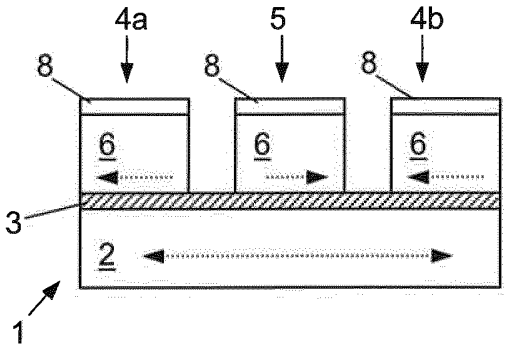


Fig. 1b

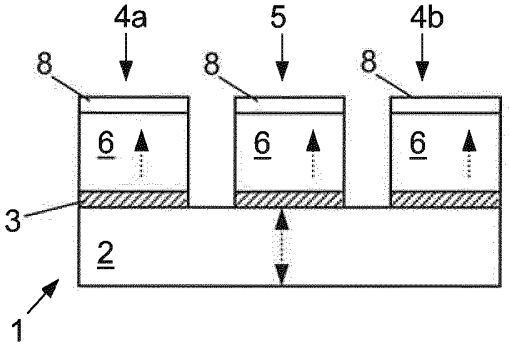


Fig. 2a

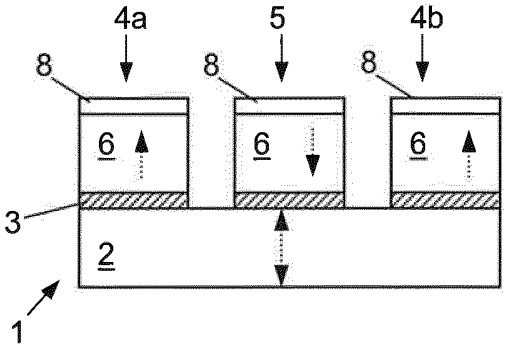


Fig. 2b

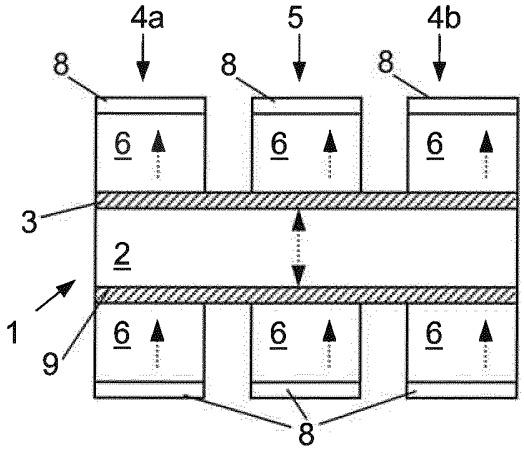


Fig. 3a

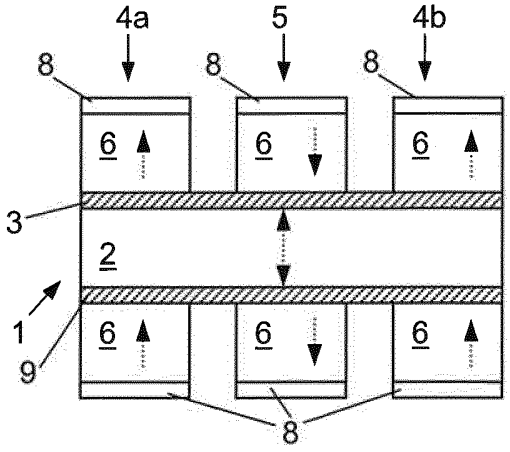


Fig. 3b

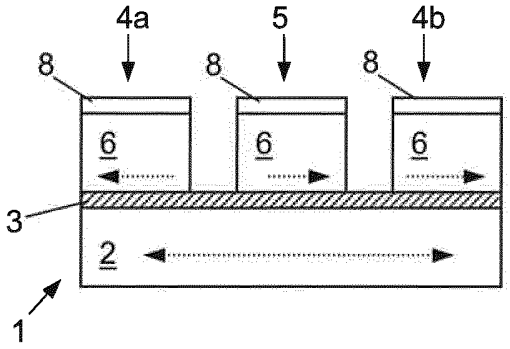


Fig. 1c

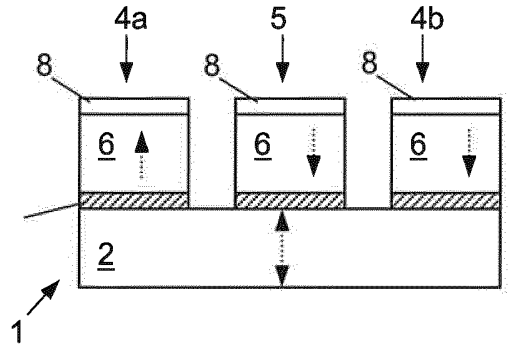


Fig. 2c

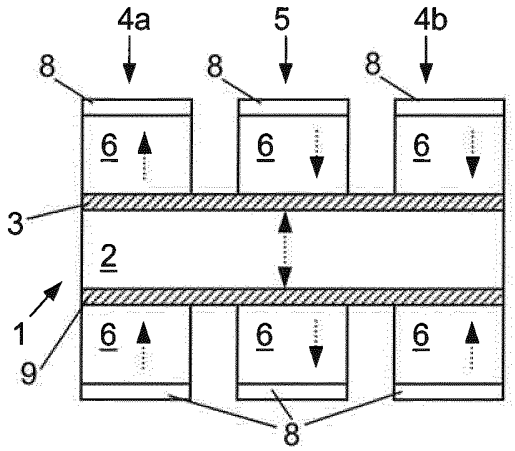


Fig. 3c

Case	A	B	Q_i
1	0	0	0
2	0	1	Q_{i-1}
3	1	0	Q_{i-1}
4	1	1	1

Fig. 4

Case	$R(\overline{A})$	S(B)	Q_i
1	0	0	Q_{i-1}
2	0	1	1
3	1	0	0
4	1	1	Q_{i-1}

Fig. 5

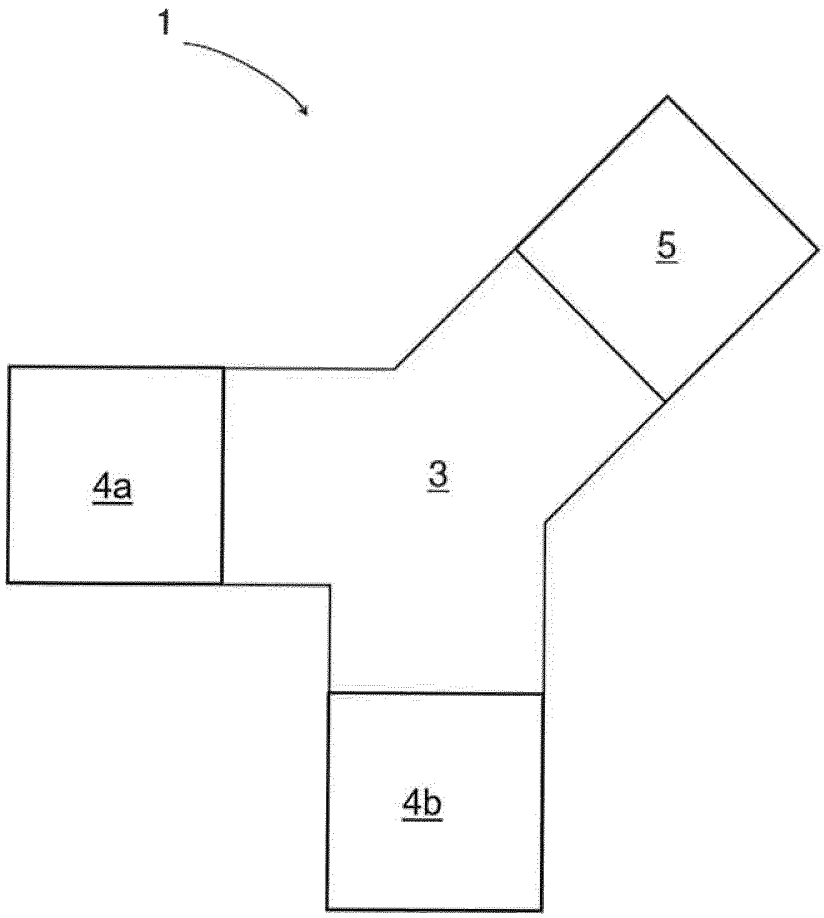


Fig. 6

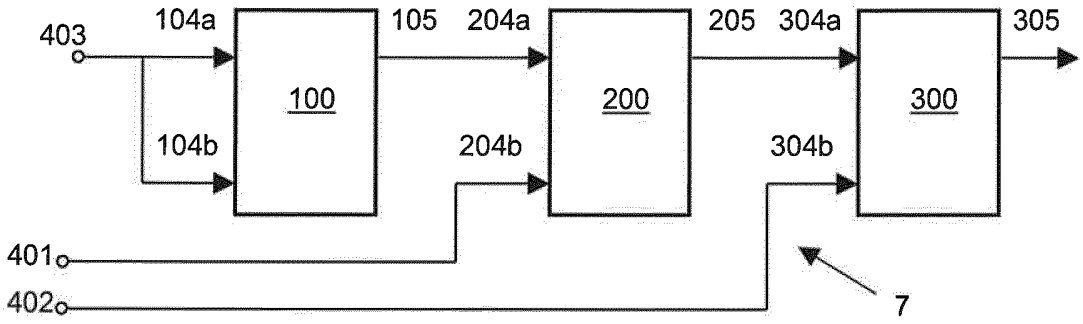


Fig. 7a

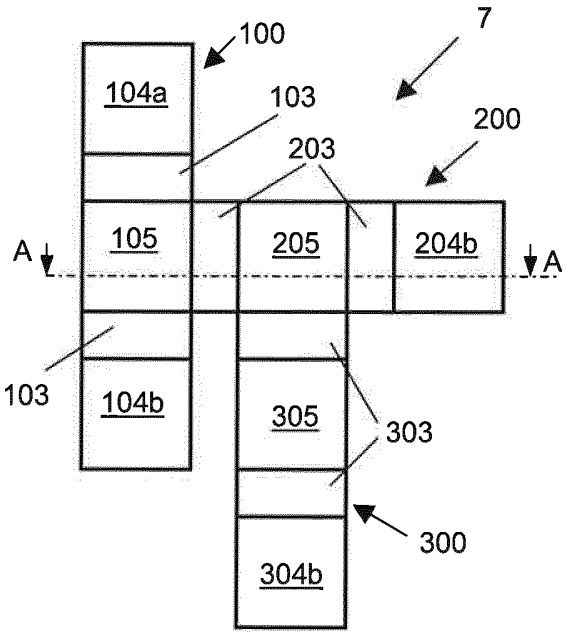


Fig. 7b

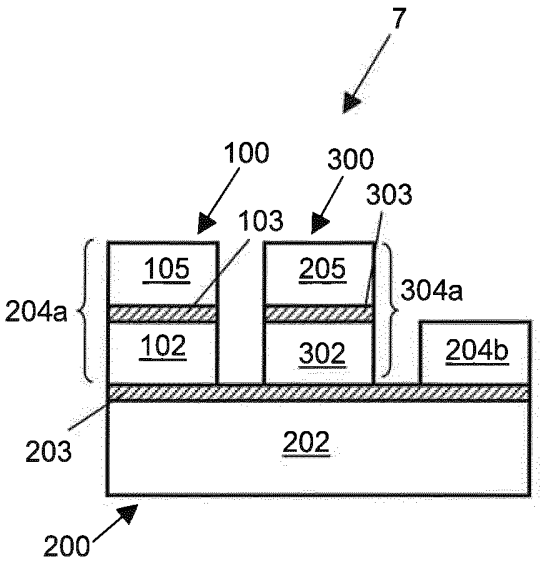


Fig. 7c

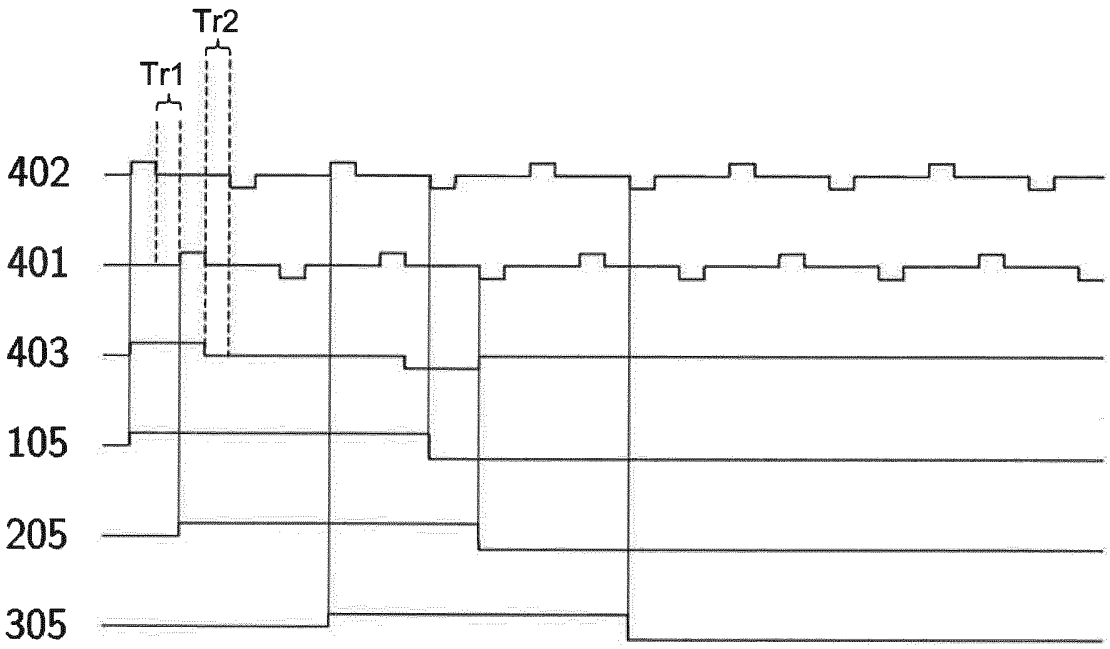


Fig. 7d

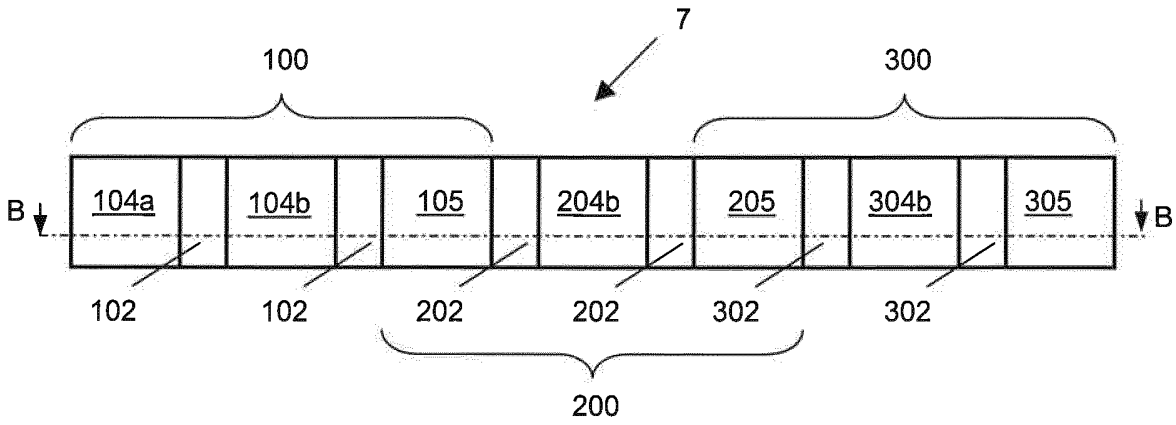
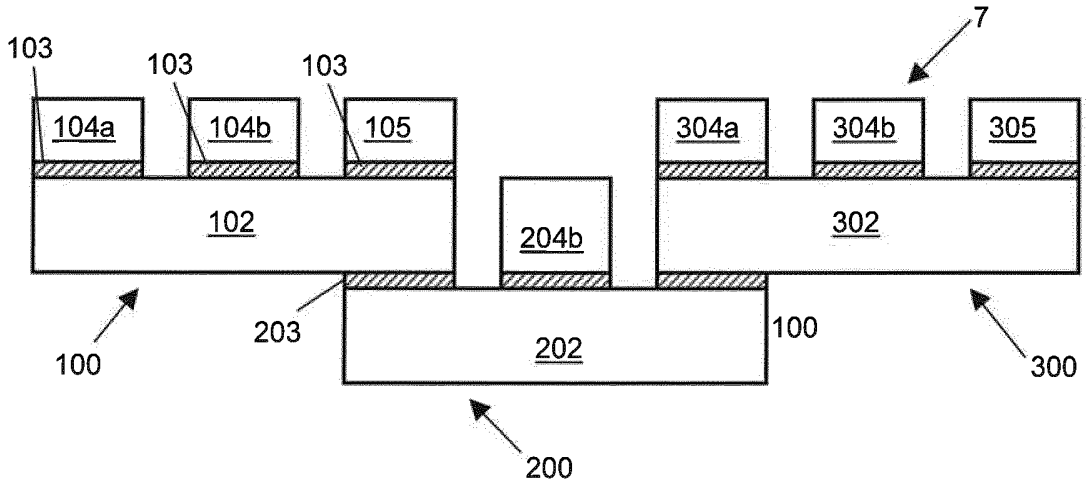

7
100
300
B
104a
104b
105
204b
205
304b
305
B
102
102
202
202
302
302
200

Fig. 8a


103
103
103
7
104a
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200

Fig. 8b

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2014/054985

A. CLASSIFICATION OF SUBJECT MATTER
INV. B82Y25/00 G01R33/09 G11B5/39 H01F10/32 G11C11/15
H01F41/30 H01L43/08 H01L43/12
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B82Y G01R G11B H01F G11C H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/147816 A1 (NIKONOV DMITRI E [US] ET AL) 23 June 2011 (2011-06-23) paragraph [0019] - paragraph [0021]; figure 1	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 April 2014	23/04/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Angermeier, Detlef

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2014/054985

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 2513904 A2	24-10-2012
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