Review on SiC MOSFETs High-Voltage Device Reliability Focusing on Threshold Voltage Instability

K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger

(Invited Paper)

***Abstract*— An overview over issues and findings in SiC power MOSFET reliability is given. The focus of this article is on threshold instabilities and the differences to Si power MOSFETs. Measurement techniques for the characterization of the threshold voltage instabilities are compared and discussed. Modeling of the threshold voltage instabilities based on capture–emission-time (CET) maps is a central topic. This modeling approach takes the complete gate bias/temperature history into account. It includes both gate stress polarities and is able to reproduce the short-term threshold variations during application-relevant 50-kHz bipolar ac-stress. In addition, the impact on circuit operation is discussed.**

***Index Terms*— Bias temperature instability (BTI), capture–emission-time (CET), high temperature gate stress (HTGS), hysteresis, SiC.**

I. Introduction

The introduction is divided into three sections. Section I-A is about the properties and advantages of SiC, Section I-B about the history and challenges, whereas Section I-C covers the SiC dMOSFET properties.

A. Properties and Advantages of SiC

From the application point of view, the most advantageous features of SiC, compared to silicon, are its high breakdown field, its high thermal conductivity, and its wide bandgap, see Table I. Given that there would be a suitable package, the high bandgap of SiC would, in principle, allow operation as a semiconductor up to temperatures of 1000 °C, while Si becomes intrinsic above roughly 400 °C [1, Ch 3]. The breakdown voltage of a MOSFET is limited by the epilayer thickness and doping as well as the breakdown field of the semiconductor. When attempting to increase the drain breakdown voltage, the thickness of the drift zone (see Fig. 1) has to be increased and its doping has to be reduced.

Consequently, the specific $R_{ds,ON}$ (product $R_{ds,ON}$ times active area) will increase. To reach a certain target $R_{ds,ON}$, one has to increase the size of the MOSFET, which, on the other hand, increases capacitances with the square of the breakdown voltage [2]. Inversely, the specific $R_{ds,ON}$ of the MOSFET improves with the square of the semiconductors breakdown field, and moreover, the higher allowed doping level in the drift zone further improves $R_{ds,ON}$. The potential for high-voltage applications is above 600 V (already several 1.7 and 3.3 kV devices entering the market [4]), and the specific $R_{ds,ON}$ of SiC compared to Si is shown in Fig. 1. In the application,

TABLE I
Comparison of Material Properties for Si, SiC, and GaN [2]

Properties	Si	4H-SiC	GaN
Energy Gap [eV]	1.12	3.26	3.5
Electron Mobility $[\mathrm{cm}^2/\mathrm{Vs}]$	1400	900	600
Hole Mobility $[\mathrm{cm}^2/\mathrm{Vs}]$	600	100	200
Breakdown Field $[\mathrm{V/cm}^2 \cdot 10^6$	0.3	3	3
Thermal Conductivity $[\mathrm{W/cm°C}]$	1.5	4.9	1.3
Saturation Drift Velocity $[\mathrm{cm/s}]$	1	2.7	2.7

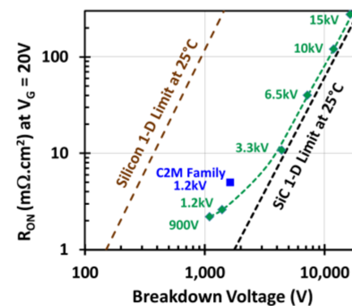

Fig. 1. Specific ON-resistance ($R_{ON,sp}$) of next-generation SiC MOSFETs measured at a gate bias of 20 V, as a function of breakdown voltage at $T = 25$ °C. Adapted from [3].

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seeing the electrical properties of the switch, the advantages of a SiC MOSFET are that the capacitances are lower, which improves the dynamic losses, and that $R_{ds,ON}$ is lower, which reduces the static losses allowing a higher switching speed [5]. This gives a higher efficiency and allows higher switching frequencies. In particular, for applications such as switching converters, the size is reduced due to smaller heat-sinks and, inversely proportional to switching frequencies, a smaller size of inductors and capacitors is achieved. The corresponding reduction in system cost has the potential to compensate the higher cost of the SiC switch [6]. Because of all these benefits, the actual SiC market grows at a rate of 40% per year [7], and more and more manufacturers are entering the market (e.g., Wolfspeed, Rohm, Infineon, ST, Littlefuse, Fuji, Mitsubishi, Toshiba, and Renesas) [4].

B. History and Challenges of SiC

Due to its exceptional hardness, synthetic SiC has been used for a century as an abrasive and as a ceramic material. Its first application in power electronics was as a voltage-dependent resistor in lightning arrestors followed by SiC Schottky diodes. Although all the electronic advantages have been known for a long time, it was not until 2008 that SemiSouth Laboratories (closed in 2013) introduced the first commercial 1200 V JFETs and 2011 until CREE introduced a 1200 V MOSFET [8]. Main factors slowing down the commercialization of SiC MOSFETs were point-defects at the SiC/SiO_2 interface and extrinsic defects within the gate oxide bulk. Currently available MOSFETs still have a channel mobility much lower than the SiC bulk mobility and a much higher extrinsic gate oxide defect density than Si MOSFETs. However, during the recent years, channel properties have improved sufficiently enough to be able to make devices with competitive $R_{ds,ON}$ times active area, and the gate oxide extrinsic problem has been solved by applying efficient electrical screening measures [9]. What remains a challenge of the SiC technology is the much more difficult and expensive crystal growth process compared to Si. However, also in this respect, there were and are steady improvements, as shown, for example, in [10] and [11]. There is, for sure, a growing interest in SiC MOSFET devices, which is, for instance, reflected by the number of publications, which is according to google scholar continuously doubling every 5 years, with no sign of saturation.

C. SiC dMOSFET Properties

Fig. 2 shows the construction of a dMOSFET with a trench channel. The total $R_{ds,ON}$-resistance of the MOSFET is a sum of channel, JFET, drift-zone, and substrate resistances. The relative contributions of the components are different between SiC- and Si-MOSFETs. This has also implications for reliability, as will be discussed in Section I. Currently available commercial SiC MOSFETs are mostly planar, but there are also trench devices coming up [2], [12]. The advantages of trench MOSFETs, such as lower chip size for same $R_{ds,ON}$, are described in detail in [2], [9], and [13].

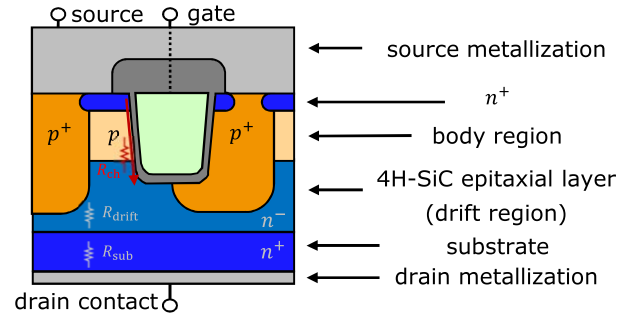

Fig. 2. Schematic cross section of a trench SiC MOSFET.

II. Reliability Overview

In some high-voltage applications, SiC MOSFETs will replace Si IGBTs. An IGBT, however, cannot be directly compared to a MOSFET. Thus, in this article, we will focus on an summary of the most important characteristics and the reliability of SiC- compared to Si-dMOSFETs and thus mainly give a review on the peculiarities of SiC MOSFETs.

The reliability tests on wafer level and for packaged products reported so far are the same as the ones typically applied to Si power MOSFETs and IGBTs e.g., power cycle tests, temperature cycle tests, temperature humidity storage (forward and reverse bias), high- and low-temperature storage, positive and negative high-temperature bias, high-temperature reverse bias [14], [15] as well as short-circuit robustness tests [16], [17]. To the best of authors' knowledge, there are no major, SiC-specific reliability issues except the ones related to gate oxide and interface. There are some reports about special reliability issues regarding the degradation of the body diode [18], [19] and soft error rates, which are similar to Si devices. A well-known degradation mechanism in MOSFETs is the degradation due to channel hot carriers. For SiC, so far there are less than a handful reports [20], [21] without any striking results. For a long time, a serious problem of SiC MOSFETs has been the gate oxide quality [9]. However, it has been demonstrated by the application of smart screening techniques, the extrinsic failure rates of SiC MOSFETs can be reduced to the same low failure rate as Si-MOSFETs or IGBTs. Efficient gate oxide screening is, however, only possible with a much thicker gate oxide than what is typically needed to fulfill intrinsic lifetime targets. A detailed discussion on intrinsic and extrinsic gate oxide reliability of SiC MOS structures can be found in Ch. 7 of [1, Ch. 7].

III. Measurement Techniques

Next, we discuss and compare, in detail, different techniques and instruments, which are suitable and have been applied to measure the threshold voltage instabilities. A dominant part of threshold shifts and instabilities in SiC are due to fast components [22], [23]. This is also true for the most advanced generations of SiC MOSFETs; thus, these fast components cannot be neglected. Typical switching periods of converters are on the order of 10 μs, so we want to define "fast" in this chapter as being faster than 10 μs. Furthermore, as for Si [24], we differentiate between threshold voltage shifts

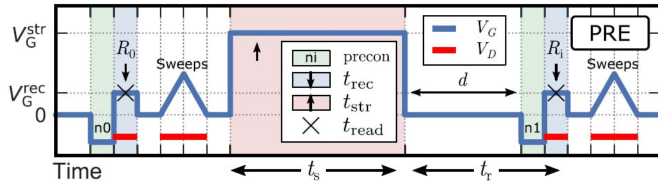

Fig. 3. Preconditioned BTI pattern with accumulation pulse (green) before the initial readout R_0 and the readout R_i after stress to maintain identical switching conditions. From [26].

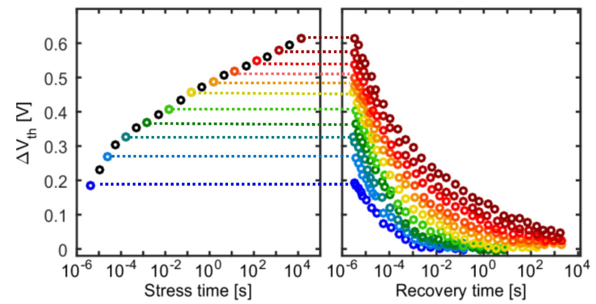

Fig. 4. V_{th} drift during gate stress (left) and recovery (right) of a typical planar device at $T = 25$ °C positive bias stress with multiple pairs of stress and recovery data. Data from [27].

fully recovering within typical experimental time windows ($\leq$100 ks) and degradation that is not recovering within this time and is thus, in the following, referred to as permanent component.

For SiC, a large, fast recovering threshold hysteresis has been reported a decade ago [22]. For a close description and also modeling of SiC bias temperature instability (BTI)-induced threshold voltage shifts, see Section V. The phenomena and challenges regarding the measurement techniques are similar to the ones of BTI of logic MOSFETs [25]. In the past, BTI and fast measurement techniques for BTI have drawn lots of attention, and more than 4000 articles have been published since 2000. It is important that knowledge is transferred between the negative BTI (NBTI)-community and the SiC-community. The chapter is structured according to the type of V_{th} readout applied in different measurement techniques (not all slow techniques are treated).

A. Slow $I_d V_g$-Sweeps

A standard technique, using a parameter analyzer, to read V_{th} after the stress is to apply a $I_d V_g$-sweep lasting from milliseconds to seconds. An inherent preconditioning is performed, due to the start voltage of the V_g-ramp at a high negative or positive gate bias.

B. Preconditioning Technique

For most purposes, it is useful to do an additional preconditioning [9]. In [9], [26], and [27] a measure-stress-measure (MSM) sequence is presented using preconditioning gate pulses before measuring V_{th}, as shown in Fig. 3. The basic idea behind the proposed MSM sequence is to remove the fully reversible hysteresis effect from the extracted V_{th} drift by restoring a defined charge state at the interface before each threshold voltage read-out. This is achieved by using a 100 ms negative preconditioning gate pulse before measuring $V_{th,up}$ and a 100 ms positive preconditioning gate pulse before measuring $V_{th,down}$ [28]. For all cases, it has to be ensured that the preconditioning pulses and sweep rate are precisely reproducible. Within the negative preconditioning pulse, the recoverable component of positive BTI (PBTI) is fully recovered and only the more permanent component is remaining as a threshold voltage shift after long-term positive gate stress. It is clear that the method is not suitable to determine fast ΔV_{th}-components due to the removed stress history, which is especially relevant to resolve the threshold voltage hysteresis within single ac pulses (see Section VI). Furthermore, it cannot be used to measure and extract the distribution of capture and emission times (CETs) (see Section III-C). However, it is able to determine the more permanent ΔV_{th}-components, which lead to long-term drift of device characteristics. Advantages are the capability to precisely compare the threshold hysteresis between different samples or the evolution of the hysteresis after (any) stress [9], [27], [28]. One other advantage of this technique is its straightforward practicability by any standard measurement equipment or parameter analyzer. The time delay between the end of stress and the readout is almost irrelevant for the drift result [28], allowing parallel stressing in a furnace. This is particularly beneficial for industrial qualification tests.

C. Fast MSM Technique

MSM techniques with a fast readout are the most commonly used techniques. They have been used for Si and also for N/PBTI. The main advantage is that standard, commercial instruments can be used. Stress pulses from microseconds to days are applied. Immediately, after the stress pulse, a preset gate bias (around V_{th}) is applied and the drain current is measured. V_{th} is calculated from the measured I_d [27]. The rise- and fall-times of the stress-pulse have to be carefully set and considered. Undershoot and overshoot between stress-pulse and measurement have to be avoided. Prior to measuring, a clever forecast of the preset gate bias is useful in order to avoid that—due to a large ΔV_{th}—the measurement ends up far off the threshold in the $I_d V_g$-curve. The parameter limiting and characterizing a measurement is the measuring delay, the delay between the end of the stress pulse and the measurement. An example for the technique is shown in Fig. 4, with a 2 μs measuring delay [27]. As seen from Fig. 4, the technique using commercial analyzers with several pairs of stress and recovery sequences is perfectly able to extract CETs [29] and as such enables the possibility to analytically model the stress and recovery time dependence of the threshold voltage shift by CET maps (see also Section V). A variant of this technique, used in this article and described in I, is the generation of the gate readout voltage by a feedback-loop, which enforces a constant, preset I_d.

D. Fast $I_d V_g$-Sweeps

V_{th} read-outs from a $I_d V_g$-sweep like in Section III-A, but with a full ramp recorded in a microsecond with fast

I_d acquisition have been proposed and performed in many publications [22], [30]–[33]. In all cases, the drain current is measured using a pulse generator and an oscilloscope. The quality of the fast-$I_d V_g$ measurement depends on the speed and on the V_g-span of the ramp. In principle, an $I_d V_g$-curve contains a lot more information compared to a single-point readout (see Section III-C), e.g., about mobility degradation. On the other hand, it has to be considered that during the $I_d V_g$-sweep, the ΔV_{th} is not a constant and, as discussed in Section V, highly accelerated by the applied gate voltage. Consequently, the presented technique, in principle, is suitable to measure CET maps, as long as the trapping/detrapping during the ramps is considered. This, however, is not an easy task. Reliability engineers should consider if there are simpler, less demanding measuring techniques producing the same results. A special, smart variant has been employed in [34] for V_{th} measurements during bipolar ac stress. Both the rise and the fall of the ac-signal are linear microseconds-ramps. Full $I_d V_g$-curves can be recorded during these transitions. In addition, the threshold hysteresis can be measured from the difference between the up- and the down-ramp.

E. Ultrafast $I_d V_g$-Sweeps

$I_d V_g$-sweeps with ramp times of nanoseconds and below have been reported to study BTI of logic FETs. The technique is influenced by signal-distortions due to imperfect impedance matching. In fact, the accuracy in measured ΔV_{th} hardly reaches 10 mV, which is a problem, e.g., $V_{\text{dd}} = 1$ V, which is not so critical for power MOSFETs. Nonetheless, such techniques applied to SiC MOSFETs are not reported yet because, e.g., for a sample with a 100 pF gate capacitance, at a gigahertz frequency (corresponding to a nanosecond-ramp), the gate impedance would be 1 mΩ only. Therefore, the application of the technique clearly would require special samples.

F. Universal Recovery Curve

V_{th} is extracted after stress at different current levels [9]. The higher the current level, the higher the positive recovery field and the faster thermal equilibrium is restored due to electron capture. Thus, scaling the time from the very low current levels (1 nA) up to 1 mA, an universal curve of V_{th} can be extracted and a scaled time equivalent to a recovery time is obtained [9]. This technique needs repeated stress at different measurement conditions.

G. On the Fly (OTF) Technique

The "on-the-fly" technique [35] also named as "nonrelaxational" [36] has been used to study BTI not only in Si but also in SiC MOSFETs [37]. The readout of ΔV_{th} is performed at stress gate voltage. Therefore, recovery, even the one caused by a short μs-measuring delay, is omitted. However—as already mentioned as a huge drawback in the NBTI Si literature [38]—is that it is impossible to measure an initial (zero-hour) V_{th}. The initial measurement is already modified by the degradation induced due to the measurement at the stress level. This is especially critical for SiC, because as an example, ΔV_{th} induced due to a 1 μs stress is 100 mV (for SiC), but the OTF technique produces (and misses) the same 100 mV during its initial measurement (compare Section V). Note that this systematic error (100 mV in the example) is unknown and cannot be determined by the OTF experiment. Moreover, OTF determines the V_{th} far off the actual threshold voltage, which introduces further problems as discussed in [33]. For instance, the technique cannot distinguish between V_{th} and mobility degradation. However, in contrast to the N/PBTI-case, OTF can be a very useful technique for the SiC-case. From a practical point of view, a more important parameter than ΔV_{th} is $R_{\text{ds,ON}}$ and its degradation. OTF is the only technique to directly measure the short-term variations of $R_{\text{ds,ON}}$ during ac gate bias switching exactly like in the application.

H. Resistive Heater Technique

As shown in Section V, it is a specialty of SiC that charge trapping with very short time constant $\leq$100 ns contributes a major part to the overall ΔV_{th}. No measurement technique so far has been able to resolve these short time constants. It would be very useful to shift these short time constants into the measuring window (see Fig. 10) by "freezing" the emission, preferred at cryogenic temperatures. A temperature decrease would bring a gain in time (Arrhenius temperature acceleration) and would thus give the chance to study the defects with the short emission time constants. Resistive-heater techniques, enabling to cool down MOSFETs from 300 °C or more to substrate temperature, have been employed in the past for Si MOSFETs [39], [40]. To the best of authors' knowledge, no approach to use these resistive heater techniques to SiC has been reported.

I. Electrical Defect Spectroscopy

Investigations on the bias- and temperature-dependence of charge-capture and -emission single, individual defects [time-dependent defect spectroscopy (TDDS)] have given considerable insights in the nature of "BTI" defects [24], [41]. There is no obvious reason why this technique could not be applied to SiC MOSFETs. Still no results have been reported yet.

J. Fast MSM Technique With Home Made Instrument

Commercial instruments provide superior accuracy and stability. On the other hand, the application of complex and fast stress and measure patterns is mostly prevented by the commercial firmware. In particular, to perform application-relevant tests such as pulsed bipolar ac measurements require the termination of the stress sequence at a predefined position within the stress sequence and thus require the use of an arbitrary pulse generator with, e.g., 25 V output, the capability to drive a nF-capacitive load with several amplifiers, and a synchronization with the current measurement system. We, therefore, prefer a home-made instrument designed to fulfill all requirements for SiC-MOSFET characterization. The microcontroller allows, especially for repetitive sequences,

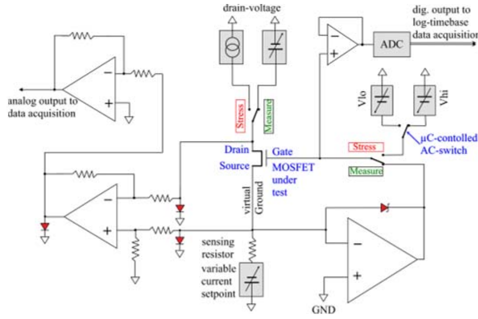

Fig. 5. Simplified measurement setup. The setup consists of three main components: 1) a stress-signal generator, consisting of digital analog converters (DACs) generating V_{high} and V_{low} and analog switches driven by the pulsewidth modulation (PWM)-unit of a microcontroller; 2) an analog measuring unit, consisting of analog switches and an operational amplifier in a feedback loop in order to control V_{gs} in a way to make Id constant; and 3) an "OTF"-measuring unit, consisting of a constant current (≈≤ 1 A) fed into drain and a differential amplifier for measuring V_{ds} (corresponding to $R_{\text{ds,ON}}$ during the V_{gs}-on-phase. Most important for fast settling times is that all amplifier inputs/outputs have voltage limiting circuits (represented by diodes in red) to prevent amplifier saturation. All switches are fast solid-state analog switches with appropriate ON-resistance.

a timing exactly reproducible within 10 ns. Fig. 5 shows the specialized test setup. In addition to the shown simplified measurement setup, the setup contains two (for high and low current) source measuring units (not shown) to measure I_{d} and I_{g}. The measurement setup is described in detail in [42].

K. Characterization Considerations

The previous points A-I just cover the determination of V_{th} and thus do not provide $I_d V_g$-curves in the regime of high V_g and high currents. Commonly, $I_d V_g$ (or V_{ds})-curves of power MOSFETs are measured by pulsing V_g or V_{ds} in order to avoid self-heating of the MOSFET with a high current only flowing for a submillisecond time. For a Si-MOSFET, other than self-heating, there is no problem correlated with timing. Any threshold hysteresis is below the resolution limit [43]. In contrast, the hysteresis of SiC MOSFETs (see Fig. 11) is significant and existing for all SiC (even the most modern) technologies and without proper consideration of all measurement parameters of the $I_d V_g$-curves, the hysteresis affects reproducibility and comparability of measured parameters. We recommend to precisely specify how, e.g., the data-sheet value of $R_{\text{ds,ON}}$ has been measured. Fig. 6 shows the difference in $I_d V_g$-curves between a Si- and a SiC-MOSFET. As mentioned in Section I, $R_{\text{ds,ON}}$ of the Si MOSFET at high V_g is dominated by the resistance of the drift zone. In contrast, $R_{\text{ds,ON}}$ of the SiC-MOSFET is dominated by the channel resistance. Due to the low transconductance for the Si-MOSFET at high gate voltages, the dependence of $R_{\text{ds,ON}}$ on a degradation ΔV_{th} vanishes. In contrast, $R_{\text{ds,ON}}$ of the SiC-MOSFET is "at least at $T = 25$ °C" directly proportional to the gate overdrive $(V_g - V_{\text{th}})$ (see Fig. 6). Fig. 7 shows two pulsed $I_d V_g$-curves recorded with a short (10 μs) and a long pulse (100 μs) length as well as two different base levels. Due to the V_{th}-hysteresis, the drain current decreases during the pulse (see Fig. 14), thus I_d

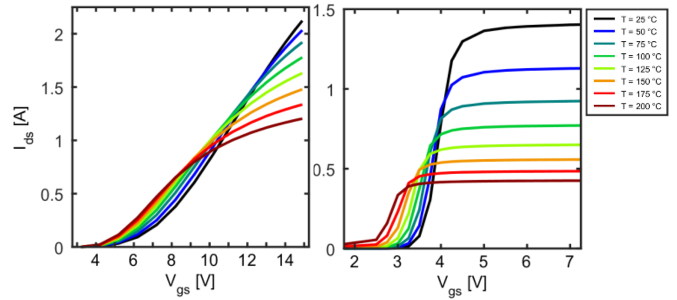

Fig. 6. Comparison of trench SiC (left) and Si (right) MOSFET $I_d V_g$-curves in dependence on the temperature.

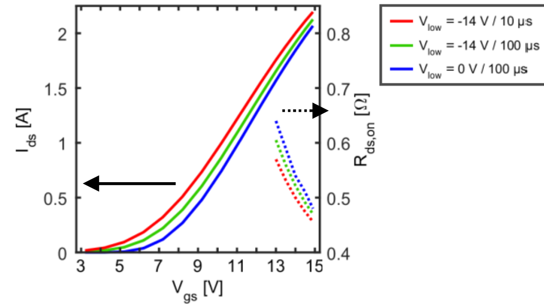

Fig. 7. Dependence of I_{ds} and $R_{\text{ds,ON}}$ on the pulse base level V_{low} and on the pulselength of a trench MOSFET. Note that effects and errors due to rise/fall times overshoot are carefully observed and avoided.

averaged over the pulselength is significantly higher for the short pulse. Furthermore, to avoid self-heating the MOSFET is kept in a state of low I_d at $V_g = V_{\text{base}}$ for a time much longer than the pulselength. As a consequence of the hysteresis, the measured I_{ds} and $R_{\text{ds,ON}}$ is significantly lower for the negative pulse base. There are numerous reports ([9], [27], [28], [36], [44], [45]), which compare measured values of ΔV_{th}, power-law coefficients of ΔV_{th} versus stress time, dependence on measuring delay [27] (the time between the end of stress and the V_{th} measurement) [46], of instrument, sweep rates [47], and so on. Very similar phenomena have already been discussed at length in the NBTI literature. Considering that ΔV_{th} is due to fast capture and emission of charge in traps, meaning that there is fast drift and recovery of ΔV_{th}, these phenomena are well understood. Considering the phenomena shown in Section VI, the requirements to correctly study these effects in SiC MOSFETs are as follows.

1) A complete and well-defined stress history, considering the complete function V_{gs} versus time and also temperature from the start to the actual determination of V_{th}, with highest possible time resolution (e.g., μs).
2) The measuring delay (time between the end of stress and V_{th} determination) has to be as short as possible. Common switching frequencies are around 100 kHz, corresponding to a 10 μs ac period. Thus, relevant stress and recovery times are in the order of microsecond. Measuring delays of 10 μs are already too long when assessments of short-term stress are desired.
3) In order to predict and simulate threshold voltage shifts, for example, from long negative dc stress and bipolar ac stress, the measurement should be able to provide

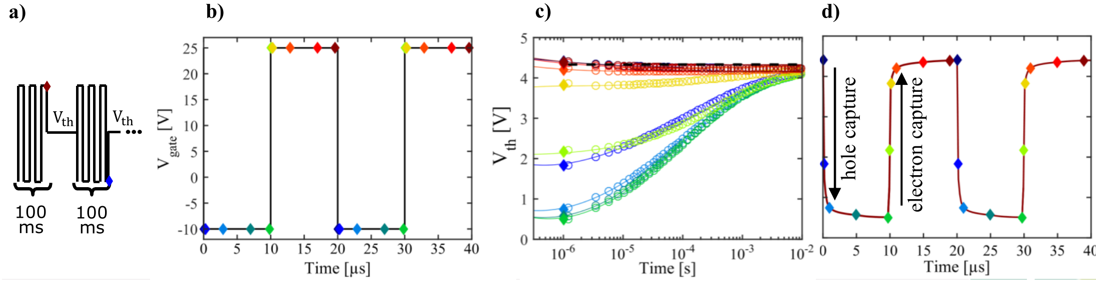

Fig. 8. Explanation of the measurement technique, example with real data of a trench MOSFET (T = 175 °C, V_{high} = 25 V, V_{low} = −10 V, and f = 50 kHz). (a) AC stress is interrupted at different points in time of the ac stress. Directly after interrupting the stress, the threshold voltage is measured from 1 μs to 10 ms recovery time. Between each measurement point another ac stress of 100 ms is applied in order to restore the premeasurement trap occupation state. (b) Example 50 kHz bipolar ac signal is shown with different points of interruption as described for (a). (c) V_{th} recovery traces after each interruption of the ac signal are shown on a logarithmic time scale. (d) First measurement points (after 1 μs measurement delay) are shown with the corresponding timing position during the ac signal. Line serves as guide to the eye. The threshold voltage hysteresis is mostly due to capture and emission (neutralization) of positive charges. From [23].

the data required to extract (negative and positive) CET (or activation energy) maps [42].

Only measurement techniques, including C, D, E, and J, can be adapted to fulfill all of the three requirements. Measurement techniques H and I can be used to achieve further understanding.

IV. AC Measurement Setup

Measurements of V_{th} under real application conditions with a time resolution below the ac switching period are to our knowledge only reported by our group [23], [42], [46]. To measure the behavior of V_{th} in real-time during the ac stress, we interrupt the ac gate stress at different positions in time during the ac signal [see Fig. 8(b)] and apply the measurement technique as described in Section III-J. A full V_{th} recovery trace (1 μs up to 10 ms) back to the initial V_{th} is recorded for each interruption of the ac gate signal [see Fig. 8(c)]. The measurement disrupts the trap occupation state caused by the bipolar ac signal. To fully restore the premeasurement trap occupation state before each interruption of the ac gate signal, 100 ms of ac stress are applied [see Fig. 8(a)]. This stress is long enough to fully restore the trap occupation state and is short enough that only the traps with short CETs are activated, no slowly recovering components are activated and thus applying another ac stress of 100 ms does, therefore, not increase the long-term V_{th}. The actual measured hysteresis can then be shown as, e.g., a function of the ac period with the threshold voltage extracted at the shortest possible delay (here 1 μs) with respect to the timing of the interruption of the gate stress. Note that the major part of the hysteresis is only detected if the gate is actually switched from inversion to accumulation as shown in Fig. 8(d)].

V. DC Gate Stress Measurements

We want to highlight and help to understand new features and peculiarities of threshold voltage variations of SiC MOSFETs. First, we will discuss differences and similarities in the effects, their modeling, and the relevance of the threshold voltage instabilities in Si and SiC MOSFETs.

1) Under the positive gate bias, there is capture or trapping of the negative charge in the oxide or interface leading to a positive ΔV_{th}. This effect is accelerated with increasing gate voltage and referred to as PBTI.
2) Under the negative gate bias, there is capture or trapping of the positive charge in the oxide or interface leading to a negative ΔV_{th}. This effect is accelerated with decreasing gate voltage and referred to as NBTI.
3) Recovery after both positive and negative gate bias stress occurs when the stress is terminated. This recovery is accelerated when the voltage is switched into the direction opposite to the stress voltage.

In this section, we refrain from speculations on the physical origin of these effects, but an overview about others discussing the nature of the traps is given in Section VIII. Results presented in Section V are based on measurements of trench MOSFETs. Both planar and trench SiC MOSFETs show NBTI and PBTI [9], [28], [48], [49], in Section VI, we show a comparison of the hysteresis for planar and trench SiC MOSFETs. We have shown in [46] that for both Si and SiC, the threshold voltage shifts due to BTI can be well understood as the collective response of an ensemble of independent defects [29]. The kinetics of charge capture and emission can be studied as discussed in Section III-C with MSM measurements of stress and recovery pairs. Each MSM measurement should consist of a huge set of stress times, e.g., ranging from 100 ns, 1 μs, 10 μs, ... to 200 ks and recovery times after each stress period of up to 100 ks or if possible even shorter/longer times (see Section III-J). A good description is achieved with so-called CET maps and the analytic modeling of the kinetics of charge capture and emission, in consistence with previous work on Si, is described by two Gaussian distributions [29]: one distribution for the defects having short CETs (called recoverable component) and another for the charged defects having emission times mostly permanent in typical experimental time windows from CETs 1 μs–100 ks. For Si, the temperature activation of the CETs of a single trap is commonly modeled according to the Arrhenius equation [39]

$$E_{a(c,e)} = k_B T \cdot \ln\left(\frac{\tau}{\tau_0}\right). \quad (1)$$

The Arrhenius equation can be used to translate CET maps into temperature-independent activation energy map inheriting the

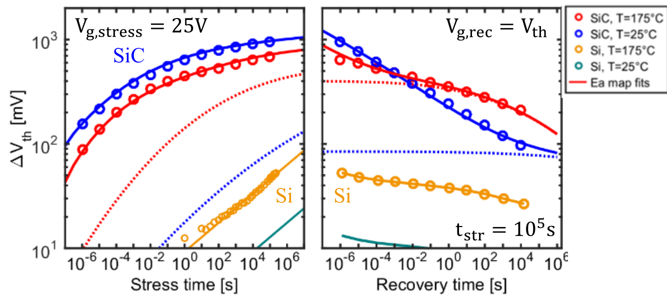

Fig. 9. (a) Comparison of Si and SiC trench MOSFETs with same t_{ox} and same E_{ox} during the positive gate bias stress with 1 μs measurement delay. SiC shows higher but fast recovering ΔV_{th} with a reversed temperature dependence compared to Si: ΔV_{th} at lower temperatures (T = 25 °C) is larger than at higher temperatures (T = 175 °C). (b) Recovery after 200 ks stress with the same stress voltage. Recovery at lower temperatures is faster than at higher temperatures. A crossing of the measured ΔV_{th} is observed at 5 ms. The lines in both figures show the simulations obtained by the analytic activation energy map in Fig. 10, with the dashed lines showing only the contribution of the permanent component [42].

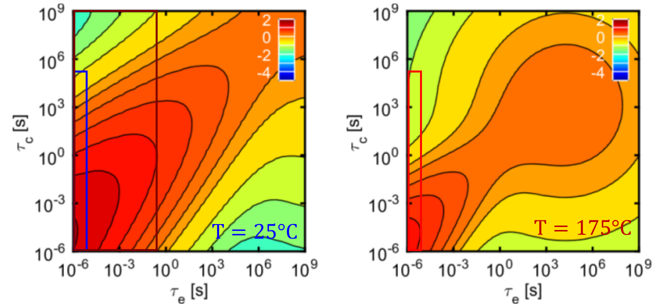

Fig. 10. PBTI CET maps (derived from Fig. 9) shown as a function of the CET constants at (a) T = 25 °C and (b) T = 175 °C. All maps are shown on a logarithmic color scale, 0 corresponds to ΔV_{th} of 10^0 mV/10^{-1}s^2. Fitting the data, we obtain the two characteristic temperature-independent constants $\tau_{(0,r)} = \tau_{(0,p)} = 10^{-15}$ s. The rectangles mark the defects that are recovering within the decade of 1- to 10-μs recovery time after 100-ks dc stress at T = 25 °C and T = 175 °C, respectively, indicated in Fig. 9.

temperature dependence of the CET maps. To fully describe and model the long-term degradation under application conditions, voltage-dependent activation energy maps for each NBTI and PBTI stress are required. A detailed description of the modeling can be found in [42]. Thus, MSM measurements at different temperatures and voltages have been performed. Here, the most important features of PBTI and NBTI including the obtained model are shown (lines are always obtained from simulations with the CET maps).

A. Positive DC Gate Stress Measurements (PBTI)

It is crucial to understand differences in Si and SiC MOSFETs threshold voltage reliability to eliminate possible risks. In Fig. 16, we compare ΔV_{th} of Si and SiC-MOSFETs after positive gate bias stress with the same gate oxide thickness t_{ox} and same oxide field E_{ox}. Si-MOSFETs show, generally, a lower ΔV_{th} due to a lower trap density compared to SiC, but the threshold voltage shift of Si devices is dominated by the permanent component (for long stress times, e.g., >100-ks less than 50% of the drift recovers). On the other hand, ΔV_{th} of SiC-MOSFETs is dominated by the fast recovering ΔV_{th} (for long stress times, e.g., >100 ks more than 80% of the drift recovers). Since ΔV_{th} observed in SiC-MOSFETs (see Fig. 9) recovers almost immediately (within 1 μs) when the gate is switched to negative voltages after the termination of stress, it is not necessarily application-relevant. Another peculiarity that is only visible at short measurement delays ($\leq$1 ms) is that the measured ΔV_{th} at lower temperatures is higher than at high temperatures [45], [50]. At a first glance, this might appear unintuitive as BTI is known to increase with increasing temperature. But, due to the thermal activation of not only stress but also recovery, traps with emission time constants around 1 μs at T = 25 °C have emission time constants shorter than the measurement delay at T = 175 °C, thus measurements at high temperatures also cannot resolve the threshold voltage shift of the fast components. In contrast to Si, SiC contains more traps with short CET constants [see fast increase for short stress times in Fig. 9(a)], so ΔV_{th} vanishes as quickly as it appears within milliseconds [Fig. 9(b)]. After 5 ms recovery time, a crossing of the measured ΔV_{th} is observed. Slow measurement techniques, as presented in Sections III-A–III-G, will miss this temperature dependence. Furthermore, the extraction of single activation energies leads to negative or positive activation energies dependent on the measurement delay. Nonetheless, long-term degradation is dominated by the more permanent component and thus especially for long-term ac stress, where defects with short emission time constants are constantly recovering within the low phase of the ac stress, the degradation is highest at high temperature. A higher ΔV_{th} at lower temperatures has not been observed for Si, because the defect density in the PBTI CET map increases from short to long capture time constants τ_c [29], [51], whereas, as shown in Fig. 10, the density of defects of recoverable component in SiC MOSFETs increases toward short CET constants (see Fig. 10). To summarize, charge capture due to gate stress is, of course, thermally activated, thus ΔV_{th} increases with temperature. The temperature dependence is fully described by the Arrhenius temperature acceleration according to (1). Furthermore, we have shown that this seemingly paradoxical dependence of ΔV_{th} on the recovery time and temperature can be well understood with the PBTI CET maps. To avoid loss of information and provide a comparability of different stress temperatures, ΔV_{th} after high-temperature stress should also be measured at room temperature or even cryogenic temperatures with a measurement delay as short as possible [24]. In particular, measurement techniques involving polyheaters as presented in Section III-H would be beneficial for SiC. Lifetime estimation according to the JEDEC [52] procedure allows a measurement delay of 48 h because of the strong recovery dependence, the fast recovering components are neglected [27], [48]. Furthermore, there is no clearly defined measurement sequence introducing huge differences in the measurement results, which causes an incomparability of the results. Modeling of the stress voltage dependence with CET maps has been demonstrated in [42]. As observed in many

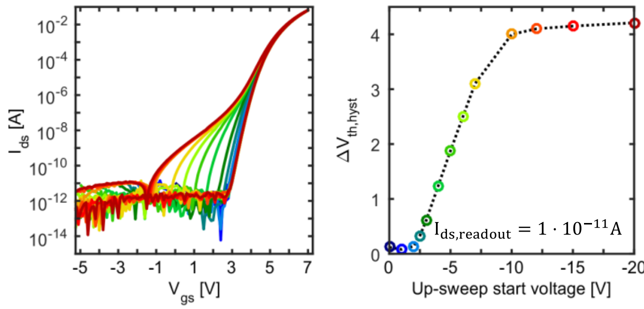

Fig. 11. (a) I–V curves of a SiC trench MOSFET with different start voltages of the up-sweep from accumulation (red) to inversion (blue). The colors in (b) show the starting voltage of the measurements in (a) and $V_{ds} = 0.1$ V. (b) Hysteresis extracted at $I_d = 10^{-11}$ A.

publications [27], [36], [44], [53], ΔV_{th} increases linearly with stress voltage, whereas the power-law exponent for all voltages remains constant. The distribution of the CET constants does not change significantly with the stress voltage, but the number of active traps increases. With the use of PBTI CET maps, all parameters needed for lifetime predictions are provided, and the measurement delay is considered within the model. As such, long-term degradation under ac switching conditions can be easily simulated (see Section VI).

B. Negative dc Gate Stress Measurements (NBTI)

An important aspect to consider is the fact that SiC MOSFETs are typically operated with, e.g., bipolar ac voltages or negative dc gate voltage. Since the threshold voltage shifts due to the negative stress voltages dominate the hysteresis under bipolar ac gate signals, it is of particular importance to analyze and model the threshold voltage after negative gate bias stress. The subthreshold hysteresis seen in the difference in the subthreshold regime of $I_d V_g$-curves up-sweep and down-sweep measurements [28] is caused by fast capture of positive charge during negative stress (see Fig. 11). Within the up-sweep of an $I_d V_g$-curve, the $\Delta V_{th,hyst}$ can only be extracted in the subthreshold regime, due to the measurement delay of ≈ 100 ms within each step and also the increased V_{gs} leading to an acceleration of the recovery. Already above V_{th}, both up and down $I_d V_g$-curves lie on top of each other. $I_d V_g$-curves are barely suitable to correctly estimate the threshold voltage variations during application like ac stress, because the measurement is highly influenced by the sweep rate, integration time, the step width as well, and, of course, V_{gs}-dependent recovery within the up-sweep.

Our advanced measurement technique does not need a post-measurement data evaluation as, e.g., the universal recovery curve measurement (see Section III-F) and provides additional information on the time dynamics determined by the CET constants for several stress times with recovery times ranging from 1 μs to 100 ks. We observe a large and very fast negative ΔV_{th} under negative gate bias stress (see Fig. 12). The negative ΔV_{th} already saturates after 100 s at $T = 175$ °C and we observe a decrease of the saturation stress time with increasing temperature. Recovery after negative stress occurs with very short emission time constants, at $T = 175$ °C full recovery is observed after measurement times of 10 ms. Thus, conventional, slow measurement techniques as presented in Section III are unable to detect these fast threshold voltage shifts or only very small drifts are observed. We apply the same concept as for the PBTI CET maps to the negative gate bias MSM measurements as shown in Fig. 12 and calculate the NBTI CET map for $V_g = -5$ V for each temperature as shown in Fig. 13. Obviously, the density of traps with small CET constants is very high for negative dc stress. In contrast to the PBTI CET maps, the distribution of the traps does not contain a permanent component, and the emission time constants are narrowly distributed. This means that, despite of the short-term behavior, no additional long-term drift is observed. This varies from manufacturer to manufacturer and is a matter of the interface passivation process and, e.g., a permanent component of NBTI has been reported for other manufacturers [9], [37], [44], [50].

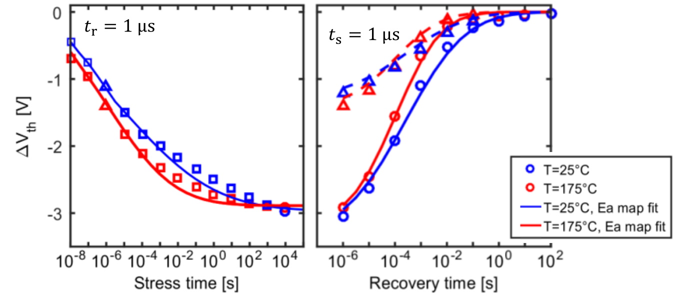

Fig. 12. Threshold voltage shift after negative stress and its recovery at ($V_g = -5$ V/ V_{th}) at $T = 25$ °C and $T = 175$ °C of a SiC trench MOSFET. Left: saturation of V_{th} after stress at $V_g = -5$ V with increasing stress time (symbols correspond to the measurement data with a measurement delay of 1 μs). The recovery time to return to the initial V_{th} at $Vg = V_{th}$ (right) is shown for $t_s = 1$ μs (triangles) and $t_s = 10$ ks (circles) and is shorter than 100 s for both temperatures. Lines are simulations obtained by the NBTI CET maps shown in Fig. 13. From [42].

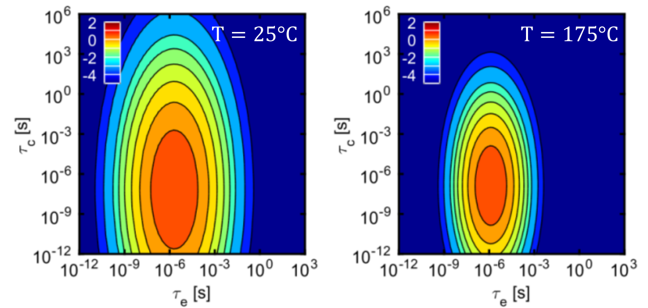

Fig. 13. NBTI CET map ($V_g = -5$ V/V_{th}) at (a) $T = 25$ °C and (b) $T = 175$ °C obtained by fits to MSM measurements as shown in Fig. 12 with recovery traces for stress-times from 100 ns up to 100 ks. The charged trap density g is shown in dependence of the capture and emission activation energies and is shown on a logarithmic color scale [mV/s^2]. Activation energies for charge capture and charge emission are below 100 meV.

The temperature dependence is slight, but as shown in Fig. 13, the distribution of the CET constants at $T = 25$ °C is a little bit broader than at $T = 175$ °C. Previously, this has been sometimes attributed to be consistent with Shockley–Read–Hall (SRH) theory for the carrier exchange [9], [54], [55] (see discussion on the trap origin in Section VIII). With increasing

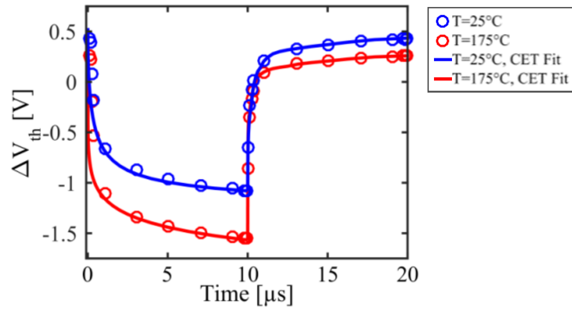

Fig. 14. ΔV_{th} hysteresis of a SiC trench MOSFET at a bipolar ac signal with $V_{\mathrm{low}} = -5$ V, $V_{\mathrm{high}} = 25$ V, $T = 25$ °C (blue) and $T = 175$ °C (red) with $f = 50$ kHz. Symbols are experimental data recorded with a measurement delay of 1 μs. The solid lines show the calculated results for each temperature obtained by the combination of the NBTI and PBTI CET maps shown in Figs. 10 and 13. From [42].

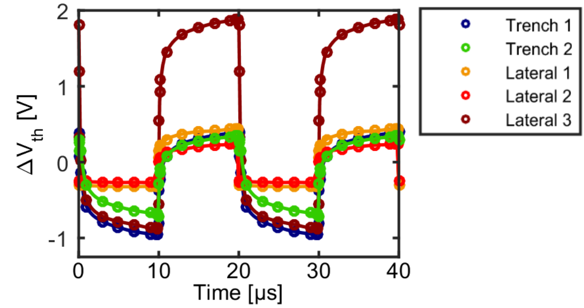

Fig. 15. ΔV_{th} hysteresis of lateral and trench SiC MOSFETs of four different manufacturers at a bipolar ac signal with $V_{\mathrm{low}} = -5$ V, $V_{\mathrm{high}} = 15$ V, $T = 25$ °C with $f = 50$ kHz. Symbols are experimental data recorded with a measurement delay of 1 μs. Lines serve as guide to the eye.

negative gate stress, the saturation level is also increased as shown in Fig. 11. In addition, the time to saturation is accelerated, still no permanent components are observed. Furthermore, there is also a dependence of the emission time constants on the recovery voltage. In particular, it is necessary to study the time constants of the recovery with recovery voltage for negative as well as positive stress to provide a model for the bipolar ac stress with variable voltage levels. As shown in [9] and [42], the recovery time after the negative stress is exponentially decreasing with increasing positive gate recovery voltage. On the other hand, when switching from the positive to the negative gate voltage, the recovery time from the positive stress is drastically decreasing with increasing negative gate voltage. This leads to a drawback of our measurement technique, as shown in Fig. 12, the threshold voltage is increasing during recovery, and thus, the measurement at V_{th} accelerates the recovery.

VI. AC Gate Stress Measurements

In the next step, we study the threshold voltage hysteresis introduced by an application like bipolar ac gate signal with a frequency of 50 kHz. The 50 kHz is within the common frequency range for applications of SiC MOSFETs. The goal of these measurements is to measure the hysteresis and compare the results to our CET map simulation approach. To measure the behavior of V_{th} in real-time during the ac stress, we interrupt the ac stress at different positions in time during the ac signal (compare Section IV). The most application-relevant V_{th} of these measurements is the hysteresis at the shortest possible measurement delay of 1 μs with respect to the timing position during the ac signal. Exemplary, in Fig. 14, measured V_{th} during a 50 kHz ac signal is shown for $V_{\mathrm{high}} = 25$ V with $V_{\mathrm{low}} = -5$ V following the measurement principle as described in Fig. 8. Short-term hysteresis of the threshold voltage of up to 1.5 V is observed. The fast decrease in V_{th} during the negative gate stress is caused by the previously described capture of holes with capture times below 1 μs dependent on the negative gate voltage [46]. For Si MOSFETs, the short-term threshold hysteresis during ac stress is only a few millivolts, due to a very small portion of traps with short CET constants. The capture times of SiC for hole capture are more faster than for electron capture, which is visible in the fast saturation during the negative stress as shown in Fig. 12 and the CET maps for NBTI in Fig. 13 and PBTI in Fig. 10. Dependencies on V_{low} and V_{high} and the temperature are shown and discussed in detail in [42]. To obtain the V_{th} response to a rectangular ac signal, the concept of CET maps is especially beneficial, a derivation of the occupancy level of the defects after the ac stress can be found in [56]. Due to the bipolar ac stress, the simulation results are obtained by the superposition of the negative and positive ΔV_{th} calculated using the corresponding PBTI and NBTI CET maps. In addition, the accelerated recovery of the negative ΔV_{th} with increased recovery voltage has to be considered when switching from the negative to the positive gate voltage and vice versa. Combining both effects, we obtain the absolute measured hysteresis (delay 1 μs), which shows an excellent agreement with the measurement results for both temperatures. With the knowledge of all dependencies of both the NBTI and PBTI CET maps, we provide a very good and accurate approach for the consideration of the hysteresis in circuit simulators.

In Fig. 15, we compare the hysteresis of lateral and trench MOSFETs of different manufacturers of state-of-the-art technologies. Both trench MOSFETs show very similar behavior. For the devices “Lateral 1 and 2,” the NBTI contribution is roughly half compared to the trench devices, the device “Lateral 3” shows a similar NBTI contribution as the trench devices, but a four times larger $+\Delta V_{\mathrm{th}}$ due to PBTI. The magnitude of the hysteresis and voltage dependencies are different for each manufacturer, nonetheless, all evaluated SiC MOSFETs show NBTI as well as PBTI effects and thus inherit a hysteresis, which might be undetected for longer measurement delays. Another important application of the CET maps is the calculation of ΔV_{th} after long-term ac stress. In Fig. 16, we compare the measurements of ΔV_{th} after dc stress at two different temperatures (25 °C and 175 °C) to ΔV_{th} after ac stress with $V_{\mathrm{high}}/V_{\mathrm{low}}$ 25 V/5 V as well as the 25 V/0 V at $T = 175$ °C at a frequency of 50 kHz with a measurement delay of 1 μs. Simulation results are obtained by the PBTI CET maps shown in Fig. 10. The ac simulations can be directly obtained by the multiplication of the PBTI CET map at $T = 175$ °C with the defect occupancy map for the corresponding ac stress pattern, additionally, the recovery acceleration with decreasing recovery voltage has

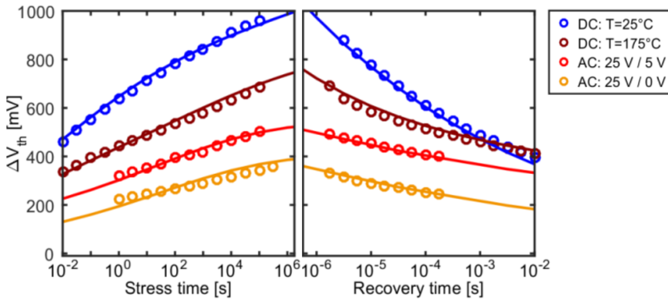

Fig. 16. Simulation (lines) from PBTI CET map (shown in Fig. 9) and measurements of ΔV_{th} of a SiC trench MOSFET after 25 V dc $T = 25$ °C and dc $T = 175$ °C, 25/5 V ac and 25/0 V ac gate stress at $T = 175$ °C in dependence on stress time right with measurement delay 1 μs and on the left dependence on the recovery time. The ac measurements were performed at a frequency of 50 kHz and a duty cycle of 50% equivalent to alternating $t_{\mathrm{S}} = 10$ μs and $t_{\mathrm{rec}} = 10$ μs. The solid lines are simulations obtained from the PBTI CET map. To simulate the 25 V/0-V ac signal, the stress time $t_{\mathrm{S}} = 10$ μs and the equivalent recovery time $t_{\mathrm{rec,\,0\,V}} = 3 \cdot t_{\mathrm{rec},\,V_{\mathrm{th}}}$. Simulation and measurements show a very good agreement. From [42].

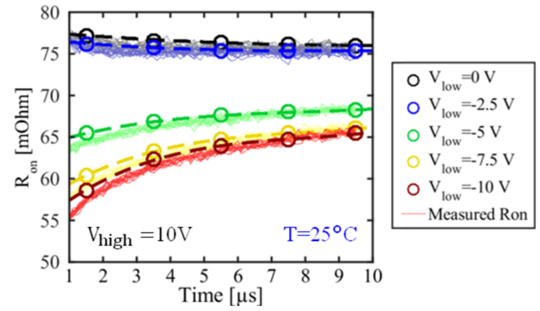

Fig. 17. $R_{\mathrm{ds,ON}}$ of a SiC trench MOSFET (not measured at typical conditions) during the V_{high} period of the ac stress for different values of V_{low} with $V_{\mathrm{high}} = 10$ V and $I_{\mathrm{d}} = 100$ mA at $T = 25$ °C. Thin lines: directly measured $R_{\mathrm{ds,ON}}$ for 50 successive periods. Circles: $R_{\mathrm{ds,ON}}$ calculated from measured static $I_{\mathrm{d}}V_{\mathrm{g}}$ curves and ΔV_{th} from bipolar ac measurements such as shown in Fig. 14. The dashed lines are a guide to the eye connecting the circles. The change in $R_{\mathrm{ds,ON}}$ is therefore, fully recoverable during ac stress. From [42].

to be considered. We observe that ΔV_{th} after ac conditions 25 V/5 V as well as ac 25 V/0 V have the same power-law exponent as the dc stress (see Fig. 9 on the left), whereas the degradation after ac 25 V /0 V stress is $\approx 40\%$ lower than at 25/5 V and 70% lower compared to dc stress. We achieve a very good agreement of all map simulations and the measurement data of the ac stress.

VII. Impact on Circuit Operation and Verification

For Si, the V_{th} hysteresis during a bipolar ac signal is a few millivolts and is thus uncritical. For SiC, an increasing short-term threshold voltage hysteresis is seen when switching the gate to more negative bias in the low phase of the gate pulse. Fortunately, this effect is not permanent and recovers quickly within a fraction of the high phase of the gate bias pulse. Also, we observed that the threshold voltage hysteresis itself does not significantly increase after the end of life. In real applications, in contrast to the measurement, the portion of ΔV_{th}, which is recovered within the measurement delay, is still active during the application [23]. Therefore, we also perform recovery-free on-the-fly measurements (see Section III-G) to study the impact of ΔV_{th} on $R_{\mathrm{ds,ON}}$ during application conditions. To show that ΔV_{th} is the only reason for $\Delta R_{\mathrm{ds,ON}}$ and possible changes in the mobility apparently do not play a role, we chose $V_{\mathrm{high}} = 10$ V, because at higher gate voltages (i.e., typically used are voltages higher than 15 V), ΔV_{th} recovers too fast to cause a clearly measurable change in $R_{\mathrm{ds,ON}}$. Nonetheless, $V_{\mathrm{high}} = 10$ V is not a typical condition for switching the device on. In Fig. 17, we present the measured $R_{\mathrm{ds,ON}}$ during the V_{high} period (transistor is "on") of the ac stress for different V_{low} voltages. For the comparison of $R_{\mathrm{ds,ON}}$ with ΔV_{th}, we use a temperature of $T = 25$ °C, because the impact of ΔV_{th} on $R_{\mathrm{ds,ON}}$ at high temperatures decreases due to the strong temperature dependence of the epilayer resistance and thus decreasing transconductance at higher temperatures (see Fig. 6). $R_{\mathrm{ds,ON}}$ increases back to its initial value with recovering V_{th}. The measured ΔV_{th} during the ac stress at $T = 25$ °C and $V_{\mathrm{high}} = 10$ V is used to calculate the change in $R_{\mathrm{ds,ON}}$ using the static $I_d V_g$ curve in the linear regime ($R_{\mathrm{ds,ON}}$ dependent on the gate voltage) as reference with very high agreement, so we show that the dependence of $R_{\mathrm{ds,ON}}$ during ac stress is only correlated with the observed ΔV_{th} during ac stress and shows the same dependencies as the hysteresis. An even lower $R_{\mathrm{ds,ON}}$ in Fig. 17 is expected for $t \leq 1$ μs (not seen due to finite settling time of measuring amplifier). This has allows four rather positive conclusions: First, ΔV_{th} is the only reason for $\Delta R_{\mathrm{ds,ON}}$. Second, we can perfectly explain and model the change in $R_{\mathrm{ds,ON}}$ during ac stress using CET maps. Third, the change in $R_{\mathrm{ds,ON}}$ is also fully recoverable as V_{th} and fourth, $R_{\mathrm{ds,ON}}$ is lowered during the negative (V_{low}) period of the ac stress and, therefore, helps to switch the SiC-MOSFET faster, thus minimizing the dynamic losses.

VIII. Nature of Traps

Although the focus of this article is more on electrical properties than on the physical nature of traps, this is an important point which will be briefly discussed. Moreover, there might be some sample or process dependence. There are a few studies using electron spin resonance (ESR) or electrical detected magnetic resonance (EDMR) to study the relevant defects at the SiC/SiO_2 interface in SiC devices [57]–[61]. Although these studies have contributed a significant portion to the understanding of the nature of these defects, they are not fully agreeing on the microscopic defect structure and succeed only partially in finding a direct correlation between resonance spectra and performance limiting defects, threshold voltage instabilities, respectively. Sample or process variations could be an explanation for the inconsistencies. Simply based on ΔV_{th} versus stress-time data, some publications try to attribute defects to oxide trap energy levels or depth in the gate oxide and tunneling processes [49]. However, the spectroscopy of individual defects (see NBTI literature [41], [62]) has shown that "slow" defects do not necessarily have a "deep" energy or are deep in the oxide. Tunneling time constants are very fast to be responsible for slow traps, and elastic tunneling models [63], [64] have been discarded long ago for the NBTI-effect [65]. Although for SiC MOSFETs, the gate oxide

thicknesses would be large enough to explain kiloseconds time constants, all ΔV_{th}'s have been found to be thermally activated. This fact is clear evidence against elastic tunneling and rather supports a thermally activated structural relaxation process, just like for NBTI [65]. Overall, from measurements of ΔV_{th} on large and mixed ensembles of defects (recorded on large area samples), it is difficult to distinguish between classes of traps and their properties, particularly their activation energies [56]. Therefore, at the moment SiC defect models and classifications—though they might be plausible in some cases—remain speculative and are not sufficiently backed by evidence. In addition, these ideas do not give a direct hint how to avoid the remaining defects after postoxidation-anneal and/or short-/long-term threshold voltage variations. Nevertheless, we believe that further EDMR/ESR investigations and electrical spectroscopy on individual defects, like for NBTI in Si devices [65], could be the key to unravel the physical nature of the defects responsible for the positive as well as the negative ΔV_{th}. Despite of all the difficulties, some others have already in the past attempted to attribute short-term threshold variations to interface trapped charge and long-term effects to border traps [9], [66], [67]. Interface trapped charges are often defined as point defects at the semiconductor–dielectric interface, which are located energetically within the semiconductor bandgap and are often related to dangling bondlike or vacancy-like centers [68]. A classical characterization technique for fast interface states is charge pumping [69]–[71], which has also been applied to SiC [67], [72], [73]. Border traps are described as traps within the SiO_2 close to the semiconductor–dielectric interface and are often linked to oxygen vacancies [74], hydroxyl E' centers or silicon-oxygen bonds [75]. Differences in the hysteresis of devices with vertical crystal planes of a 4H-SiC (e.g., the a-plane) and planar devices of 4H-SiC (e.g., Si-face) were reported in [76]. Vertical devices show a better channel mobility and the larger hysteresis in these devices has been attributed to a lower density of interface states D_{it} close to the conduction band (reduction of electron trapping at gate voltages higher than the threshold voltage) and a higher D_{it} around midgap (increase in charge trapping in the subthreshold regime of the MOSFET) [9], [73], [76].

IX. Conclusion

A review on threshold variations of high-voltage SiC MOSFETs has been given, with a particular emphasis on differences to Si MOSFETs. In the commercial introduction of SiC MOSFETs, a main task, which had to be solved, was to reduce the SiC/SiO_2 interface defects to an acceptable level in order to improve the channel mobility and minimize the channel resistance. Doing so, also threshold voltage instabilities were significantly reduced, however, especially short-term variations are by today still higher than in Si MOSFETs. We have argued that these short-time variations cause a hysteresis effect, which is unique for SiC MOSFETs but which does not limit the reliability or the performance of the device since it is fully recoverable. Furthermore, the magnitude of the hysteresis does not significantly increase during stress. Besides short-time V_{th} variations, there is also a more permanent drift component for PBTI stress, which may be potentially critical for some applications if not controlled properly. In latest generation SiC MOSFETs, these threshold instabilities have been improved [9], [27], [34], [47], [48], [77], [78]. Nevertheless, they should be considered in circuit design and need to be included in SPICE models. A model to simulate all the threshold instabilities, under any arbitrary stress stimulus of varying gate bias and temperature, is given in this article. The model uses CET-maps; a very good agreement could be shown in the model/experiment comparison. Thus, the simulation model (e.g., implemented in a SPICE model) can easily simulate threshold instabilities encountered in real applications, which are hard to verify experimentally. This enables us, in principle, to predict the V_{th} evolution during the product lifetime. The ability to foresee electrical parameter drifts for different mission profiles is one key to decide on realistic drift margins and to guarantee a certain specification limit/reliability for the entire chip lifetime. Another key for the future is to further improve device processing and gain more understanding of the nature of the traps, which cause these variations. SiC MOSFETs have some peculiarities in the threshold voltage, which are, today, much better understood and much better controlled as they were some years ago. This has opened the door for the commercialization of the SiC MOSFET and made it reliable for industrial and automotive applications. We evaluated different measurement techniques and presented an appropriate technique to consider and model application-relevant threshold voltage instabilities. Thus, we consolidated the understanding of how to correctly assess the V_{th} drift. For this purpose, we recommend our proposed measurement technique to be established in a new SiC JEDEC standard.

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