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Modeling Bias Temperature Instability in Si and SiC MOSFETs using Activation Energy Maps

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To Simon and Bernd.

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Abstract

Microelectronic chips are at the heart of modern electronic devices and are also used in cars for e.g. driver assistance, safety systems, powertrain control, communications, and infotainment systems. The metal-oxide-semiconductor field effect transistor (MOSFET) is the dominant transistor in these digital as well as analog integrated circuits (ICs). MOSFETs act as switches or amplifiers for electrical currents by exploiting the field effect.

Reliable behavior has to be guaranteed throughout the entire lifetime of the device, especially for safety-critical applications. The reliability challenges for devices increase with miniaturization, increased stress fields within the circuit, and with new and innovative materials.

The most prominent mechanism which degrades the device performance and thus seriously affects the reliability is the bias temperature instability (BTI) and depends on the temperature and applied gate bias. A threshold voltage shift is caused by charging and discharging of interface states and structural defects located in the oxide. In the last years, significant progress has been made to identify the physical degradation mechanisms behind BTI. However, physical models are computationally too expensive for circuit simulations. Therefore, efficient and accurate models for the bias temperature instability under real application conditions are still urgently needed in order to assess the device behavior until the end of its lifetime.

In this work, an accurate and efficient BTI compact model for circuit simulations is presented. A circuit-simulator compatible model has to provide high accuracy, low computational effort, acceptable experimental, and low implementation effort. For this model, an accurate description of the threshold voltage shift after any stress, recovery, and temperature pattern is required. The model presented in this work is based on a single activation energy map, which includes the voltage and temperature dependence of stress and recovery. A mathematically efficient approach is used to calculate the degradation with a stress time-independent simulation time. To fulfill the requirement of low experimental effort and fast model parameterization, an efficient measurement technique, the temperature-accelerated measure-stress-measure technique, is developed. The model is validated against measurements with several different AC stress conditions and integrated within a circuit simulator, which is used by Infineon Technologies AG. It is shown that the complex BTI degradation mechanism after any arbitrary stress, recovery, and temperature conditions can be simulated with the developed compact model achieving high accuracy.

In addition, BTI-induced threshold voltage shifts of Silicon Carbide (SiC) MOSFETs are investigated in this work. The wide-bandgap semiconductor SiC increasingly gains importance because SiC MOSFETs can be operated at a higher temperature, higher frequency, and higher power density than Si devices, which allows shrinking of the passive components and heatsinks. As such, full

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SiC system solutions are more efficient, lighter and smaller, and less expensive than their silicon-based counterparts. As in Si MOSFETs, the performance of SiC transistors is seriously affected by defects which can be located in the oxide and at the oxide/semiconductor interface. It has been observed that the BTI induced threshold voltage shifts are more severe for SiC devices than for conventional Si transistors. Besides, SiC MOSFETs show threshold voltage shifts under both positive (*on* state) as well as negative (*off* state) gate bias stress. As such, the standard test procedures typically used to characterize threshold voltage shifts for Si MOSFETs are not sufficient to determine the threshold voltage shifts under application conditions of SiC MOSFETs.

Therefore, a new AC measurement technique for BTI evaluation of SiC MOSFETs is proposed in this work. This thesis highlights the differences between Si and SiC MOSFETs and determines the relevance of threshold voltage variations for the application. A precise model for BTI-induced threshold voltage shifts based on activation energy maps is derived. The presented model is the first published BTI model for application-relevant AC stress of SiC MOSFETs.

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Kurzfassung

Mikroelektronische Schaltungen bilden den Kern elektronischer Bauteile und finden verstärkt Anwendung in der Automobilelektronik beispielsweise in der Fahrsicherheit, Fahrassistenz und in Kontrollmodulen des Antriebsstranges. Der Metall-Oxid-Halbleiter-Feldeffekttransistor ist das zentrale Bauteil in diesen digitalen sowie analogen integrierten Schaltungen. Mittels des Feldeffekts können Metall-Oxid-Halbleiter-Feldeffekttransistoren Ströme ein- und ausschalten oder verstärken.

Die Zuverlässigkeit der MOSFETs muss über die vorgesehene Lebensdauer hinweg garantiert werden. Die Herausforderungen für die Zuverlässigkeit vergrößern sich nicht nur mit zunehmender Miniaturisierung und erhöhten Stressfeldern innerhalb der Schaltungen sondern auch mit neuen und innovativen Materialien.

Der bekannteste Effekt ist die Bias-Temperatur-Instabilität (BTI). Der Effekt verringert die Leistungsfähigkeit der Transistoren mit ernsthaften Auswirkungen auf die Zuverlässigkeit und die Lebensdauer. In Abhängigkeit von der Temperatur und der angelegten Gate-Spannung lässt sich eine Verschiebung der Schwellspannung beobachten, die durch Laden und Entladen von Defekten, an der Halbleiter/Oxid Grenzfläche oder im Dielektrukum, entsteht. Während der letzten Jahre wurden große Fortschritte in der physikalischen Modellierung dieses Alterungsmechanismus erzielt. Für Schaltungssimulationen sind diese physikalischen Modelle jedoch nicht geeignet, da sie zu viel Rechenzeit benötigen. Um das Verhalten des Transistors bis zum Ende seiner Lebenszeit korrekt zu beschreiben sind daher effiziente und zugleich ausreichend genaue Modelle zur Beschreibung der Bias-Temperatur-Instabilität unter realen Applikationsbedingungen unbedingt und dringend notwendig.

In dieser Arbeit wird ein akkurates und effizientes BTI Kompaktmodell, das für Schaltungssimulationen geeignet ist, vorgestellt. Ein Alterungsmodell für Schaltungssimulationen muss folgende Anforderungen erfüllen: Eine hohe Genauigkeit, niedriger Rechenaufwand, akzeptabler experimenteller Aufwand und gute Implementierbarkeit. Dabei ist die Modellierung der Schwellspannung unter jeglichen Spannungsbedingungen unter Berücksichtigung der Temperatur eine notwendige Vorraussetzung. Das in dieser Arbeit entwickelte Modell basiert auf einer Aktivierungsenergiekarte, die die Spannungs- und Temperatur-Abhängigkeit von Stress und Erholungs-Phasen berücksichtigt. Es wird ein mathematisch effizienter Ansatz verwendet um die Alterung zu berechnen. Dabei ist die Simulationszeit unabhängig von der zu simulierenden Stresszeit.

Um die Anforderung des niedrigen experimentellen Aufwands mit einer schnellen Modell-Parametrisierung zu erfüllen wurde eine effiziente Messtechnik, die TA-MSM Technik, entwickelt. Das Modell wird mit Hilfe von Messungen mit verschiedenen AC Stressbedingungen überprüft und ist bereits in einen Schaltungssimulator der Infineon Technologies AG integriert. In der vorliegenden Arbeit wird gezeigt, dass der komplizierte Alterungsmechanismus BTI mit einer

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hohen Genauigkeit mit dem entwickelten Kompaktmodell simuliert werden kann für beliebige Temperatur-, Stress- und Erholungs-Bedingungen.

Des Weiteren wurden in dieser Arbeit Verschiebungen der Schwellspannung von Siliziumkarbid-Transistoren untersucht. Der Halbleiter SiC besitzt eine große Bandlücke und wird zunehmend wichtiger, da SiC MOSFETs bei höherer Temperatur, höherer Frequenz und höherer Leistungsdichte betrieben werden können, was die Verkleinerung von passiven Komponenten und Kühlkörpern ermöglicht. Dadurch sind auf SiC basiernede Systemlösungen effizienter, leichter, kompakter und auch kostengünstiger als Systeme, die rein auf Siliziumtechnologie aufgebaut sind. Die Leistung von Siliziumkarbid-Transistoren ist ebenso wie die von Silizium Transistoren beeinträchtigt durch Defekte, die sich im Oxid als auch an der Oxid/Halbleiter-Grenzfläche befinden. Untersuchungen haben gezeigt, dass in Siliziumkarbid-Transistoren größere Verschiebungen der Schwellspannung aufgrund von BTI auftreten als für Silizium Transistoren. Des Weiteren zeigen Siliziumkarbid-Transistoren sowohl Verschiebungen der Schwellspannung unter positiven Gatespannungen (im eingeschalteten Zustand) als auch negativen Gatespannungen (im ausgeschalteten Zustand). Die typischen standardisierten Tests um die Veränderung der Schwellspannung für Silizium-Transistoren zu messen sind ungeeignet für Siliziumkarbid-Transistoren, da die Veränderung der Schwellspannung unter Applikationsbedingungen nicht mit diesen Tests bestimmt werden kann.

Daher wird in dieser Forschungsarbeit eine neue Messtechnik für die Beurteilung der Zuverlässigkeit von SiC MOSFETs unter AC Applikationsbedingungen demonstriert. Die Forschungsarbeit untersucht Unterschiede zwischen Silizium- und Siliziumkarbid-Transistoren und bestimmt die Bedeutung von Veränderungen der Schwellspannung für die Applikation. Des Weiteren wurde ein präzises Modell für BTI von Siliziumkarbid Transistoren basierend auf Aktivierungsenergiekarten entwickelt. Das in dieser Forschungsarbeit vorgestellte Modell ist das erste Modell für BTI unter Applikationsbedingungen von Siliziumkarbid MOSFETs.

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Acronyms

AWG	arbitrary waveform generator
BSIM	Berkeley short-channel IGFET model
BTI	bias temperature instability
cc	constant current
CET	capture and emission time
CV	capacitance-voltage
cv	constant voltage
CVD	chemical vapor deposition
DFT	density functional theory
DSO	digital storage oscilloscope
DUT	device under test
EDMR	electrically detected magnetic resonance
eMSM	extended measure-stress-measure
EOL	end-of-life
EPR	electron paramagnetic resonance
ESR	electron-spin resonance
fWLR	fast wafer level reliability
GaAs	gallium arsenide
GaN	gallium nitride
HCD	hot-carrier degradation
HCS	hot-carrier stress
HDL	Harry Diamond Laboratories
INV	inverter logic gate
MSM	measure-stress-measure
NBTI	negative bias temperature instability
NMP	non-radiative multi-phonon
NOR	not OR logic gate
NRA	nuclear reaction analysis
OTF	on-the-fly
PBTI	positive bias temperature instability
PCM	process control monitor
PID	plasma induced damage
POA	post oxidation anneal
PVD	physical vapor deposition
R-D	reaction-diffusion
RTN	random telegraph noise

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SiC	silicon carbide
SILC	stress-induced leakage current
SIMS	secondary ion mass spectrometry
SMU	source measurement unit
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	static random access memory
STM	scanning tunneling microscopy
TA-MSM	temperature accelerated measure-stress-measure
TCAD	technology computer aided design
TDDB	time-dependent dielectric breakdown
TDDS	time-dependent defect spectroscopy
TEM	transmission electron microscopy
WKB	Wentzel-Kramers-Brillouin

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List of Symbols

Symbol	Unit	Description
A	m^2	Gate area
A_p	1	Amplitude of the quasi-permanent component
A_r	1	Amplitude of the recoverable component
B_c	eV	Barriers for charge capture
B_e	eV	Barriers for charge emission
C	F	Capacitance
C_{ox}	F	Oxide capacitance
dc	1	Duty cycle
D_{it}	cm^{-3}	Interface state density
$\Delta R_{ds,on}$	Ω	On resistance shift
Δt_r	s	Recovery pulse time
Δt_s	s	Stress pulse time
ΔV_{th}	V	Threshold voltage shift
ΔV_{th}^{sub}	V	Sub-threshold voltage shift
ΔV_{th}^{hyst}	V	Hysteresis threshold voltage shift
n	1	Power-law exponent
ε_{ox}	F/m	Dielectric constant of the gate dielectrics
ε_r	1	Relative permitivity
E_a	eV	Activation energy
$E_{a,H}^{app}$	eV	Horizontal single activation energy
$E_{a,V}^{app}$	eV	Vertical single activation energy
E_C	eV	Conduction band energy
E_c	eV	Activation energy of charge capture
E_e	eV	Activation energy of charge emission
E_F	eV	Fermi-level
E_G	eV	Bandgap
E_{ox}	eV	Electric oxide field
f	Hz	Frequency
g	V/s^2	Density of defects
g_m	S	Transconductance
I_{ds}	A	Drain current
$I_{d,lin}$	A	Drain current in the linear regime
$I_{d,sat}$	A	Drain current in the saturation regime
I_{gs}	A	Gate current
I_{sub}	A	Substrate current

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k_{12}	$1/\mathrm{s}$	Transition rate between state 1 and state 2
k_{21}	$1/\mathrm{s}$	Transition rate between state 2 and state 1
l_{des}	m	MOSFET gate length
μ_{c}	eV	Mean activation energy of charge capture
$\mu_{\mathrm{c,0}}$	eV	Mean activation energy of charge capture at 0 V
$\mu_{\Delta\mathrm{e}}$	eV	Shift of the mean activation energy of charge emission
$\mu_{\Delta\mathrm{e,0}}$	eV	Shift of the mean activation energy of charge emission at 0 V
μ_{e}	eV	Mean activation energy of charge emission
μ_{eff}	$\mathrm{cm}^2/(\mathrm{Vs})$	Effective channel mobility
η	m	Step height
N_{V}	1	Number of voltage classes
O	1	Occupation probability
P	V	Permanent component of the threshold voltage shift
R	V	Recoverable component of the threshold voltage shift
r	1	Correlation parameter
ρ	1	Correlation coefficient
$R_{\mathrm{ds,on}}$	Ω	On resistance
$R_{\mathrm{on,sp}}$	Ω	Specific on resistance
σ_{c}	eV	Standard deviation of the mean value of the capture activation energy
σ_{e}	eV	Standard deviation of the mean value of the emission activation energy
τ_0	s	Temperature-independent time constant
$\tau_{0,\mathrm{p}}$	s	Temperature-independent time constant of the quasi-permanent component
$\tau_{0,\mathrm{r}}$	s	Temperature-independent time constant of the recoverable component
t_{AC}	s	AC stress time
τ_{c}	s	Capture time constant
τ_{e}	s	Emission time constant
t_{eof}	s	Time until end-of-life
t_{d}	s	Measurement delay
t_{rec}	s	Recovery time
Θ_{rec}	s	Equivalent recovery time
$t_{\mathrm{r,trans}}$	s	Transformed recovery time
t_{str}	s	Stress time
Θ_{str}	s	Equivalent stress time
$t_{\mathrm{s,trans}}$	s	Transformed stress time
T_{meas}	°C	Measurement temperature
T_{ref}	°C	Reference temperature
T_{str}	°C	Stress temperature
t_{ox}	m	Oxide thickness
$V_{\mathrm{bin},i}$	V	Voltage used for binning
V_{dd}	V	Nominal operation voltage
V_{ds}	V	Drain voltage
$V_{\mathrm{ds,meas}}$	V	Drain voltage during measurement
$V_{\mathrm{ds,str}}$	V	Drain voltage during stress
V_{fb}	V	Flat band voltage
V_{gs}	V	Gate voltage
$V_{\mathrm{gs,str}}$	V	Gate stress voltage
$V_{\mathrm{gs,rec}}$	V	Gate recovery voltage
V_{h}	V	High level voltage
V_{l}	V	Low level voltage
V_{in}	V	Input voltage

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V_{max}	V	Maximum voltage
V_{min}	V	Minimum voltage
V_{out}	V	Output voltage
V_{ov}	V	Gate overdrive voltage
V_{p}	V	Gate pulse voltage
V_{ss}	V	Ground voltage
V_{th}	V	Threshold voltage
$V_{th,0}$	V	Initial threshold voltage
V_{th}^{sub}	V	Sub-threshold voltage
w_{des}	m	MOSFET gate width

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Physical Constants

Symbol	Name	Value
ε_0	Vacuum Permitivity	$8.854187817 \times 10^{-12}\mathrm{Fm}^{-1}$
k_B	Boltzmann's constant	$1.380662 \times 10^{-23}\mathrm{J}^{-1}\mathrm{K}^{-1}$
q	Elementary charge	$1.6021892 \times 10^{-19}\mathrm{C}$

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Chapter 1

Introduction

Microelectronic chips are at the heart of modern electronic devices consisting primarily of metal-oxide-semiconductor field-effect transistors (MOSFETs). By exploiting the field effect, the voltage applied to the gate terminal determines the conductivity of the device which can be used for switching or amplifying electronic signals. The MOSFET is the dominant transistor in digital circuits as well as analog integrated circuits and the scaling and miniaturization of the MOSFETs enables high-density integrated circuits such as memory chips and microprocessors. Another type of MOSFET is a power MOSFET, which is designed to handle significant power levels and is utilized in cars, trains, power supply systems, solar inverters and many other fields.

The computation speed and the lifetime of the devices is strongly influenced by imperfections of the MOSFETs oxide layer [1, 2]. Thus every new device technology has to overcome several qualification tests before it can be released and sold to the customer [3]. Furthermore, the reliability of the devices is monitored during fabrication for example by fast wafer level reliability (fWLR) monitoring [4]. As such, the influence of process changes on the reliability of the MOSFETs is monitored. Especially for security- and safety-relevant applications, e.g. in the automotive industry, it is of utmost importance to ensure the promised lifetime [5]. In the following, a motivation for this work as well as a short summary of the main reliability risks of modern transistors is presented.

1.1 Motivation

During the last decades, the density of transistors approximately has doubled every two years following Moore's law [6] which has lead to improved performance of the microelectronic chips and decreasing costs per transistor. Therefore, the widths and lengths as well as the operating voltage of the transistors have reduced and a thinning of the insulating layer was required. As a consequence of the scaling, the electric fields inside the devices have increased significantly because the operation voltages could not be scaled in the same manner as the device geometry [7]. With the decreasing device dimensions and the increased electric fields, reliability challenges have also increased and gained more importance [8, 9]. This has resulted in quite some challenges for the design of integrated circuits [10]. The reliability-relevant degradation mechanisms can be separated into two different classes:

- Degradation effects that cause permanent local failures or complete destruction of the device such as micro-cracks, electro-migration or the time-dependent dielectric breakdown (TDDB) [11, 12]. Furthermore, there are permanent failures induced by radiation that cause e.g. single event latch-up or failures due to ionizing radiation [13, 14].

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- Degradation effects that cause slow changes of the transistor parameters over time. At high temperatures, the most relevant degradation effect of this class is the bias temperature instability (BTI) causing an increase of the MOSFETs threshold voltage [15]. The mobility, as well as the threshold voltage, is affected by hot-carrier degradation (HCD), where high energy (hot) carriers affect the atomic structure by breaking bonds at the interface [16]. BTI and HCD are due to charging and discharging of interface states as well as of oxide defects. In addition, new defects inside the oxide and along the interface are created and can act as trap-assisted tunneling (TAT) centers. This increases the tunneling current through the oxide after device stress causing stress-induced leakage current (SILC). As a consequence of these aging mechanisms, the power demand is increased and the switching time is affected and may cause circuit timing failures [17].

Every important device parameter has a certain drift margin which has to be satisfied during reliability testing [18]. The drift margin determines the lifetime of the product. Reliability challenges such as BTI, HCD, TDDB, and SILC have increased due to the decreasing device dimensions [7, 10]. Possible degradation induced failures of numerous devices within guaranteed operation times may generate tremendous costs [19]. Hence, research and industry are currently developing tools and methodologies to reduce the physical effects and in addition to cope with the degradation e.g. by introducing redundancy in the system design or by parameter adaptions like the decrease of the maximum operation voltage [KWC1].

In order to assess the device behavior under operating conditions until the end of its lifetime, aging models are needed to simulate the whole circuit. In addition, electronic design automation (EDA) tools are needed to analyze the impact of device and interconnect reliability on the circuit behavior [KWC1]. Thereby the functionality of the circuit has to be ensured through the entire lifetime of the product. In the last decade, significant progress has been made to enable accurate simulations of circuits based on the Simulation Program with Integrated Circuit Emphasis (SPICE), and aging models have been implemented into the design flow as add-ons to SPICE-based circuit simulations [9, 17]. Lifetimes of the products are in the range of several years e.g. 10 – 20 years for automotive applications. Naturally tests with realistic stress scenarios can surely not be measured. Due to practicability and cost reasons, reliability tests have to be completed within hours or even faster (e.g. fWLR within seconds) and therefore, tests have to be accelerated with e.g. increased temperature or supply voltage. To determine the actual lifetime of the device from accelerated test conditions, aging models are needed for each aging mechanism to perform extrapolations for long term stress under use conditions.

Instead of long-term degradation measurements, assessment of the expected circuit degradation behavior may be simulated within a circuit simulator [19, KWC1, KWJ1]. Thus, all aging mechanisms influencing the functionality and reliability of the device have to be known, understood, and modeled. As a result, either the processes can be changed to optimize device performance or the circuit design has to be adapted. A precondition for these countermeasures is an accurate aging model suitable for circuit simulations to minimize reliability risks.

In the following, to give a basic understanding a lateral planar MOSFET used in CMOS technology is described and the relevant properties and parameters are introduced. In addition, the most important device reliability challenges BTI, HCD, TDDB, and SILC are briefly described.

1.1.1 The Transistor

A transistor is composed of semiconductor material usually with at least three terminals for connection to an external circuit. The transistor is used to amplify or switch electronic signals and electrical power. The cross-section of a conventional pMOSFET (lateral planar transistor used in CMOS technology) with source, drain, and gate terminals is shown in Fig. 1.1. Two highly p-doped regions, source, and drain are separated by an n-doped body region. An insulating

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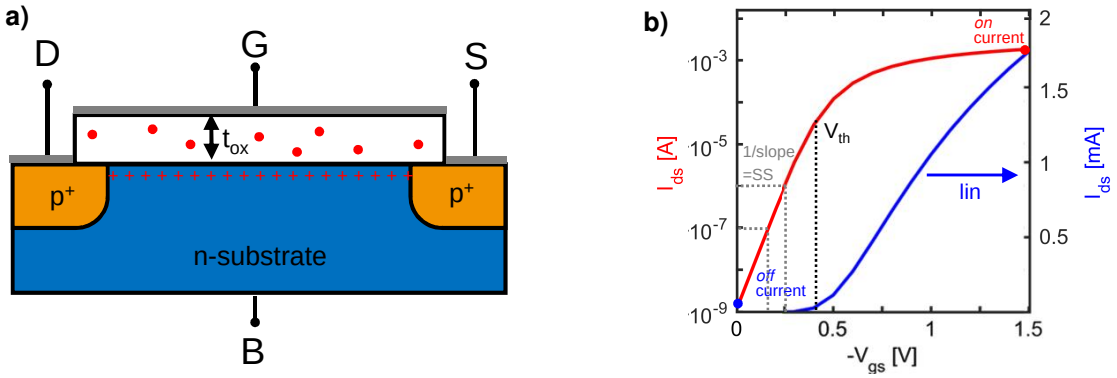

Figure 1.1: Cross-section of a pMOSFET and a typical transfer characteristics. **a)** Cross-section of a pMOSFET with two highly p-doped drain and source regions separated by an n-doped body region. The gate contact is separated from the body by an insulating layer (e.g. SiO_2 or SiON). **b)** Typical transfer characteristics of a pMOSFET: Drain-source current I_{ds} versus gate-source voltage V_{gs}. Logarithmic and (red, left scale) linear (blue, right scale) scale. The most important parameters characterizing the MOSFET are the *off*- and *on*-currents, the sub-threshold swing SS, and the threshold voltage V_{th}.

layer (e.g. silicon dioxide SiO_2 or amorphous silicon oxynitride SiON) separates the gate and the body. The MOSFET capacitor is formed by the gate electrode (metal or polysilicon), the insulating layer and the substrate. The capacitor prevents a current flow and therefore enables a loss-less control of the MOSFET. In the case of a pMOSFET a negative gate-source voltage V_{gs} is required to switch the device *on*. A supply voltage V_{dd} between the drain and the source ($V_{ds} = V_{dd}$) is required to control the drain-source current I_{ds} with the gate voltage V_{gs}.

Typically, measurements of I_{ds} of a MOSFET by sweeping the gate voltage V_{gs} at a fixed drain voltage V_{ds} are called "transfer characteristics" or $I_{ds}V_{gs}$-curves as shown in Fig. 8.3 b). Characteristic parameters of the $I_{ds}V_{gs}$-curve are the *off*-current at $V_{gs} = 0\,\mathrm{V}$, the threshold voltage V_{th}, the *on*-current at $V_{gs} = V_{dd}$, and the sub-threshold swing (SS; reciprocal value of the sub-threshold slope in Fig. 1.1 b). Several definitions of V_{th} exist: The transition from accumulation to inversion (microscopic description) and the macroscopic description where V_{th} is extracted from the $I_{ds}V_{gs}$-characteristics and is based, e.g. on a drain current I_{ds} threshold or on the maximum transconductance. The transconductance g_m is the small-signal conductance for input gate voltage and output drain current dependent on V_{gs} at constant V_{ds}:

$$g_m = \frac{dI_{ds}}{dV_{gs}}. \tag{1.1}$$

Imperfections of the amorphous SiO_2 are introduced either during device fabrication or occur at the interfaces between different materials. Besides, the devices are aggressively scaled down and the gate dielectric thickness has been decreased correspondingly, which led to very high gate leakage currents [20, 21]. In order to prevent boron diffusion from the gate to the channel, nitrogen was introduced into the gate stack [22]. Another advantage of nitrogen is that the dielectric thickness, the location, and the profile of nitrogen incorporation can be independently controlled within limits for plasma nitrided oxides (PNO) [23]. However, there are also some disadvantages regarding reliability [15, 23, 24].

1.1.2 Bias Temperature Instabilities

Bias temperature instabilities (BTI) are a crucial reliability issue for MOSFETs [1, 25, 26]. Most prominent is negative bias temperature instability (NBTI) at negative gate voltages where the charging of defects in the oxide or interface with positive charges leads to a negative shift of the

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flat band voltage V_{fb} as well as to a negative shift of the threshold voltage V_{th} of pMOSFETs. Already in the 1950s and 1960s, experimental investigations have been performed on SiO_2 under elevated bias voltage and temperature conditions [27–29]. In 1966, Miura *et al.* [30] observed an increase of electron concentration at flat band bias conditions after positive gate bias stress of a MOS structure and linked the measurements to the presence of gate oxide vacancies. This degradation mechanism is now referred to as BTI [31].

Until the introduction of nitrogen, not much attention has been paid to understand this mechanism [25]. More than 30 years later, nitrogen in the gate stack led to a dramatic increase of this instability for negative gate voltages [32, 33] in pMOSFETs and the publication rate on BTI has drastically increased which led to more than 10000 publications as of today [34].

BTI does not cause hard failures such as short circuits across the oxide but leads to a shift of the threshold voltage V_{th} and a degradation of the channel mobility. The resulting changes in the transfer characteristics of the device can cause severe problems, especially when the specification margins of the technology and product are very narrow. When applying a stress gate bias $V_{gs,str}$ for a stress time t_{str} and monitoring the threshold voltage V_{th} after the end of the stress, an immediate recovery after stress is observed as defects charge during the stress and can discharge during recovery at lower gate bias. The threshold voltage shift is calculated as $\Delta V_{th}(t_{str}) = V_{th}(t_{str}) - V_{th,0}$ with $V_{th,0} = V_{th}(t_{str} = 0)$ the threshold voltage before stress.

The fast recovery after end of stress has been neglected until 2003 when Ershov *et al.* reported a *recoverable* and a *permanent* component [35]. For long recovery times, the threshold voltage recovers towards its initial value. The remaining ΔV_{th} at the end of the measurement has been considered as quasi-permanent contribution (typically $\approx t_{rec} \geq 100\,\text{ks}$) whereas the recovering part at the beginning of the measurement is referred to as recoverable component ($t_{rec} \approx 1\,\mu\text{s}$). This experimental separation strongly depends on the measurement delay. Until today, there is no experimental technique to determine these components separately. Note that the permanent component also shows recovery for long recovery times and we will refer to it as "quasi-permanent" component in this work. Whereas for older technologies, pMOSFETs suffered most for NBTI and nMOSFETs where less affected by positive bias temperature instability (PBTI), several modern technologies are seriously affected by both positive as well as negative gate bias stress e.g. MOSFETs with high-κ gate stacks [36], FinFETs [37] or silicon carbide (SiC) transistors [38]. In this work, NBTI is first studied on conventional Silicon (Si) pMOSFETs with a SiON oxide. Furthermore, SiC-based nMOSFETs with SiO_2 oxides are studied. Here, PBTI as well as NBTI play an important role and are thus studied in detail in this work.

1.1.3 Hot Carrier Degradation

This work focuses on BTI, but the studied circuits are also affected by the degradation due to highly energetic ("hot") carriers known as hot carrier degradation (HCD). The term *hot* refers to the kinetic energy of the carriers. The carriers are accelerated by high channel electric fields due to high drain voltages. HCD affects device parameters such as the drain current, the threshold voltage and the *on*-resistance. Hot carriers damage the Si/SiO_2 interface by dissociating neutral Si-H bonds and leaving electrically active dangling Si-H bond behind as illustrated in Fig. 1.2. This process typically requires kinetic energy higher than 3 eV. One of the first successful HCD models was the so-called "lucky-electron" model [39], which is still frequently used for long channels or high electric fields. Nonetheless, even for low operating voltages and for newer technologies with nanometer dimensions HCD is a severe degradation mechanism, thus also *colder* carriers have to be considered as a cause of HCD [8, 40]. Takeda *et al.* have identified four main modes of hot carrier stress [41]:

1. Channel hot-electron (CHE) injection: Single particle mechanism, which occurs mainly at $V_{ds} = V_{gs}$ conditions due to "lucky electrons". Lucky electrons are electrons which gain

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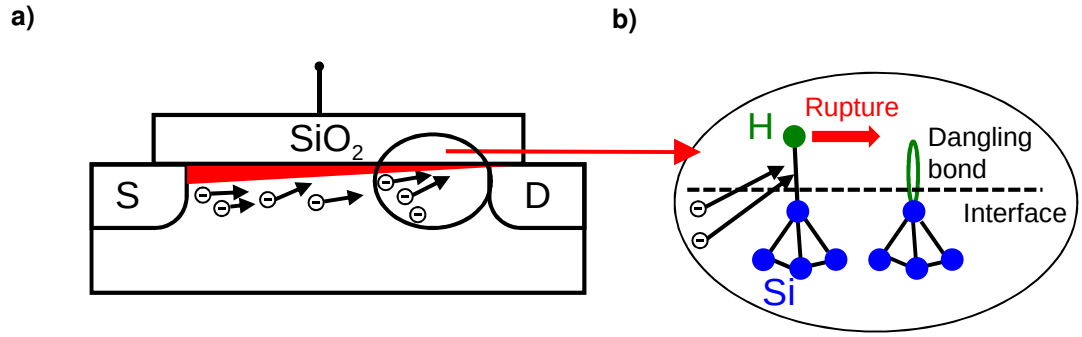

Figure 1.2: A schematic illustration of the principles of hot carrier degradation. **a)** If a drain-source bias is applied to the MOSFET, the electric field along the interface is non-uniformly distributed with the highest electric field at the drain side. **b)** The collision of accelerated carriers with the Si/SiO_2 interface leads to a dissociation of the Si-H bond. As a consequence, electrically active dangling bonds are created and can be charged and discharged by carriers, which leads to a reduction of the channel mobility. After: [42].

sufficient energy to trigger a bond dissociation mechanism, which is dominant in large-area devices. For newer technology nanoscale transistors, one single particle energy is not sufficient to directly dissociate the Si-H bond, but a multiple particle process is necessary with a series of collisions [42].

2. Substrate hot-electron (SHE) injection: Due to high bulk voltages, a large electric field in the substrate can accelerate carriers from the Si substrate into the SiO_2. If the energy of the carriers is high enough, a dissociation of the Si-H bond is caused.

3. Drain avalanche hot-carrier (DAHC) injection: A high vertical field is caused near the drain due to the channel pinch-off which causes impact ionization. The generated electrons and holes can be injected into the oxide or contribute to the substrate current.

4. Secondarily generated hot-electron (SGHE) injection: Impact ionization due to DAHC stress may cause injection of secondary minority carriers.

Dependent on the device dimensions, worst-case conditions of HCD are different [42]. Thus, in a long-channel nMOSFET the highest degradation is caused at the highest substrate current I_{sub} (maximum impact ionization, typically at $V_{gs} \approx 0.5V_{ds}$) [43]. Long-channel pMOSFETs suffer most at the maximum gate current I_{gs} [44]. Furthermore, the degradation is highest at low temperatures. For short-channel devices, multiple vibrational excitation gains importance, therefore the highest degradation is at the highest carrier flux ($V_{gs} = V_{ds}$, for both n- and pMOSFETs) [16]. Contrary to the long-channel devices, the HCD degradation for those short-channel devices is more severe at high temperatures [8]. An empirical power-law model for HCS is presented in Section 4.2.

1.1.4 Time-Dependent Dielectric Breakdown

The purpose of the gate oxides of MOSFETs is to insulate the gate from the channel. However, not only quantum mechanical tunneling and high energetic carriers can lead to deviations from this ideal property, but also trapping of carriers from the channel and as well as release of these carriers to the gate occurs. These defects act as tunneling centers and induce a gate leakage current. Leakage currents through the dielectric of the MOSFET may cause a breakdown of the insulator during stress at high electric fields. The effect strongly depends on the stress time and

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oxide thickness. TDDB is consistently described by the creation of traps that act as tunneling centers [45].

1.1.5 Stress-Induced Leakage Current

An increased tunneling current is not only observed at high electric fields but also at low electric fields after stress of the MOSFET, called SILC [46]. Leakage currents at low electric fields are related to defects created in the oxide layer during high-field stress [47], due to trap-assisted tunneling where two or more defects located in the oxide act as tunneling centers.

1.2 Scope

The focus of this work is on bias temperature instabilities as it is one of the most critical reliability issues and focuses on BTI of Si MOSFETs as well as SiC MOSFETs [15, 38]. In the last years, a significant process has been made to identify the physical degradation mechanisms behind BTI and the *gate-sided hydrogen release model* [48] has been developed. Nonetheless, the model parametrization is challenging and computationally far too expensive for circuit simulations. Efficient and accurate analog bias temperature instability models are therefore still urgently needed to evaluate aging within circuit simulators. Models suitable for circuit simulations have to especially provide high accuracy, low simulation effort, acceptable experimental, and low implementation effort. In particular, modeling the recovery after arbitrary gate stress is a considerable challenge [26, 49, 50].

One goal of this thesis has been to find an analytic description of BTI-induced threshold voltage shifts relying on established physics: The model has to include all dependencies (stress voltage, recovery voltage, temperature). To reduce the experimental effort a new measurement technique is introduced. All model parameters (temperature-, stress, and recovery voltage-dependence) are obtained from experiments. No defect database or time-consuming single defect measurements are required as for other published compact models [51, 52]. A further requirement for circuit simulations is efficient analytic modeling of BTI for any desired lifetime with arbitrary stress voltages and temperatures under consideration of the full stress history of the device. The model developed and presented in this thesis fulfills all requirements for circuit simulations.

The second goal of this thesis has been the investigation and modeling of the bias temperature instability of SiC MOSFETs. SiC-based MOSFETs are increasingly entering the high power device market [38] and have several benefits: They can be operated at higher temperature, higher frequency, and higher power density as they offer significantly reduced static and dynamic losses. As in Si MOSFETs, the reliability and performance of SiC transistors is seriously affected by interface as well as oxide defects. Also, the BTI induced threshold voltage shifts are more severe for SiC devices than for their silicon counterparts. Furthermore, SiC MOSFETs show threshold voltage shifts under both positive (*on* state) as well as negative (*off* state) gate bias stress. A correct and consistent description of the threshold voltage shifts is generally important for the development and simulation of reliable integrated circuits. One target of this thesis is to highlight the differences between Si and SiC MOSFETs, determine the relevance of threshold voltage variations for the application, and derive a precise model for BTI-induced threshold voltage shifts. Application conditions of SiC MOSFETs include both NBTI and PBTI. Therefore, the standard test procedures typically used to characterize threshold voltage shifts for Si MOSFETs are not sufficient to determine the threshold voltage shifts under application conditions of SiC MOSFETs. Therefore, a new AC measurement technique for BTI evaluation under application conditions of SiC MOSFETs is proposed and the modeling of the induced threshold voltage shift is demonstrated.

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1.3 Structure of the Thesis

The thesis is structured in four parts. The first part is a general part providing the theoretical foundations of the thesis: After this introduction, in Chapter 2 state-of-the-art measurement techniques are introduced. The fundamental properties of BTI are described in Chapter 3 and an overview of BTI models is given in Chapter 4. Besides, the capture and emission time map framework is described upon which the model developed in this thesis is built.

After the theoretical foundations, the second part deals with BTI in silicon-based MOSFETs: In Chapter 5 the measurement setup and the experimental techniques of Si MOSFETs applied in this thesis are presented. The voltage-dependent activation energy map model and its extension developed in this thesis to be suitable for circuit simulations is presented and validated in Chapter 6 and Chapter 7.

The third part deals with BTI in SiC-based MOSFETs: In Chapter 8 properties and reliability issues of SiC MOSFETs are discussed. In Chapter 9 the measurement setup and the experimental techniques of SiC MOSFETs applied in this thesis are presented. The model for PBTI, NBTI, and application-relevant AC stress of SiC MOSFETs is presented in Chapter 10. The fourth part concludes the thesis. A discussion on the physical meaning of single value activation energies for BTI in Si and SiC MOSFETs is given in Chapter 11. Finally, the work is summarized and an outlook is given in Chapter 12.

1.4 Contributions Made in This Thesis

The main work of the first topic on bias temperature instability of Si MOSFETs is to find an analytic description which relies on established physics but is efficient to model BTI under arbitrary stress conditions including all dependencies suitable for circuit simulations.

- Section 6.1: For the acceleration of the measurements, a new measurement setup has been built-up and the temperature accelerated measure-stress-measure (TA-MSM) technique has been developed as described in Section 5.2 and published [KWC2].
- Section 6.1.3: Voltage dependent activation energy map modeling using the TA-MSM technique has been achieved covering a wide range of stress voltages. The model is presented in [KWJ2].
- Section 6.3: A new phenomenon has been investigated within this thesis: The quasi-permanent and reverse recovery effect as reported in [KWC3].
- Section 7: Extension of the activation energy maps to consider the full stress history of the device and enable simulations under any arbitrary $V_{\mathrm{gs}}(t)$ with varying time-dependent stress/recovery voltage and temperature. The model is published in [KWJ3].
- Section 7.7: Analytic calculation of the threshold voltage shift for any desired lifetime with arbitrary stress/temperature (solely periodicity is a requirement). Integration in the Infineon SPICE circuit simulator is demonstrated in [KWJ4].

The second topic covered by this thesis is the modeling of BTI for SiC MOSFETs.

- Chapter 9: To perform measurements of V_{th} under real application conditions with a time resolution below the AC switching period, a measurement setup has been built and published in [KWC4].
- Section 10.1: Activation energy map modeling of PBTI of SiC MOSFETs has been developed and is published in [KWJ5].

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- Section 10.2: The first activation energy map model of NBTI of SiC MOSFETs has been developed and presented in [KWC5].
- Section 10.3 and Section 10.4: The first model of the subthreshold-voltage hysteresis and application-relevant AC stress has been demonstrated and published in [KWC5].

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Part I

Theory

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Chapter 2

Measurement Techniques for Si and SiC Devices[1]

In this section, the most relevant state-of-the-art measurement techniques for the characterization of Si and SiC BTI-induced effects are described and compared. After a general introduction to the measurement of transfer characteristics and the extraction of the threshold voltage, the section is structured according to the type of V_{th} readout. The different measurement techniques are presented and different kinds of challenges for measurements of silicon carbide threshold voltage instabilities are discussed.

2.1 Transfer Characteristics

Changes in the $I_{ds}V_{gs}$-curves are often used to quantify BTI, because they are strongly influenced by charges in the oxide [53]. For the characterization of changes due to hot-carrier stress (HCS), $I_{ds}V_{gs}$-curves are also an often chosen method to characterize non-recoverable charges [54]. In addition, $I_{ds}V_{gs}$-curves are used for pre- and post-stress characterization and transistor parameters such as the threshold voltage V_{th}, transconductance g_m, the sub-threshold swing SS.

2.1.1 Measurement of the Threshold Voltage.

One possibility for a fast measurement to minimize the recovery after NBTI stress is solely considering shifts of the threshold voltage V_{th} instead of recording full $I_{ds}V_{gs}$-curves. As shown in Fig. 2.1 a), the $I_{ds}V_{gs}$-curve is shifted after stress towards higher threshold voltages and the drain current is reduced. Two experimental extraction methods for the threshold voltage [53, 55] - the constant voltage (cv) and constant current (cc) method are briefly discussed and explained in the following. A more detailed discussion of the measurement techniques can be found in [KWJ7].

The constant gate voltage (cv) method:

The drain current I_{ds} is recorded at a constant gate voltage, typically near V_{th} as illustrated in Fig. 2.1 b). Immediately after stress with a stress bias ($V_{gs,str}$ with V_{ds}^{str}) the recovery bias (V_{gs}^{cv} and V_{ds}^{rec}) is applied for the time t_{rec}. The reduced drain current recovers towards its initial value. Subsequently, to obtain the ΔV_{th}, the drain current is converted into ΔV_{th} using the initial $I_{ds}V_{gs}$-curve [56].

[1] The description of the peculiarities of SiC measurement techniques is based on [KWJ6]

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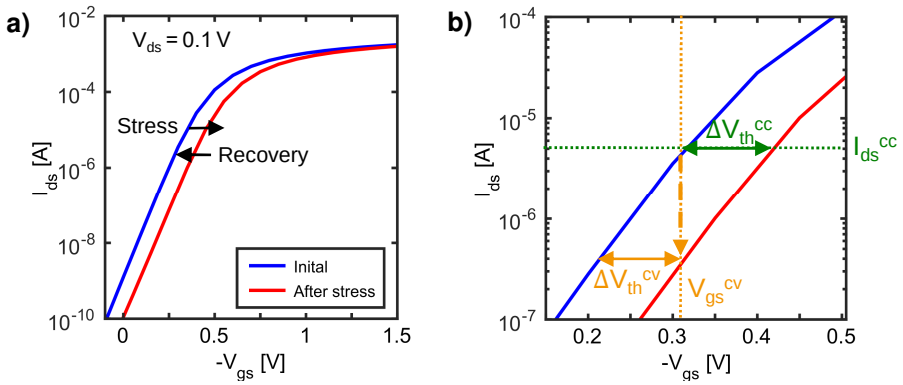

Figure 2.1: $I_{ds}V_{gs}$ characteristics of a pMOSFET at $T = 25°C$ and $V_d = -0.1$ V before (blue) and after stress (red) of a pMOSFET. **a:** Difference of the $I_{ds}V_{gs}$-curves before and after stress. After the end of a BTI stress, the parameters recover towards their initial values. **b:)** Comparison of the extracted ΔV_{th} with the constant gate voltage method (cv) and the constant drain current method (cc). **cv-method:** The drain current I_{ds}^{cv} at a constant recovery voltage V_{gs}^{cv} is monitored. Postprocessing step: I_{ds}^{cv} is transformed to V_{gs}^{cv}. **cc-method:** The gate voltage V_{gs}^{cc} is monitored while the drain current is held at I_{ds}^{cc}.

Typically, in the constant voltage setup, the drain current is measured with a transimpedance amplifier. A feedback resistor defines the measurement range for I_{ds} during stress as well as during the measurement [KWJ8, 57]. Since the drain current I_{ds} can vary a few orders of magnitude between stress and measurement, the feedback resistor has to be changed between stress and recovery. Unfortunately, this switch introduces an additional delay [KWJ8]. Furthermore, the feedback resistor has to be chosen prior to the measurement to ensure a proper measurement resolution during the measurement which is not always trivial for heavy degradation as it requires estimating the final degradation of the device.

The constant current (cc) method:

The threshold voltage can be directly measured by recording the gate voltage controlled by a feedback loop of an operational amplifier forcing a constant threshold drain current [KWJ8]. Immediately after stress, the recovery bias is switched to V_{ds}^{rec} while the drain current is held at I_{ds}^{cc}. The advantage of forcing the threshold current is that the ΔV_{th} is directly obtained using the cc method and does not require a transformation. The cc setup requires one voltage source during stress and a current source during recovery. To avoid changes in the state of the degradation, it is necessary to ensure a constant gate stress voltage and a switch without overshoots from stress to recovery (as also discussed in [58]). Because the threshold voltage is extracted directly from the measurement and no post-processing has to be performed, throughout this work for the Si MOSFETs and SiC MOSFETs, the constant current method is applied with the measurement setup as described in Section 5.1.2 and Section 9.3. Furthermore, we achieve readout delays of $t_d \approx 1\,\mu s$ with our constant drain current measurement setup, which is more difficult to achieve with the constant gate voltage method [58].

2.1.2 Slow $I_{ds}V_{gs}$-Sweeps

A standard technique to quantify degradation is the readout of V_{th} after stress by applying a $I_{ds}V_{gs}$-sweep lasting from milliseconds to seconds. This can be performed using a commercial semiconductor parameter analyzer. By applying this technique, due to the start voltage of the V_{gs}-ramp at a high negative or positive gate bias, an inherent pre-conditioning is performed. An example of a slow $I_{ds}V_{gs}$ sweep on a lateral SiC MOSFET is shown in Fig. 2.2.

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To compare the stress-induced threshold voltage shift after PBTI or NBTI stress with this technique, it is important to keep the sweep parameters well-defined and constant (starting and stop voltage as well as sweep rate). Nonetheless, when applying e.g. negative voltages after PBTI stress or vice versa, positive voltages after NBTI stress, the stress-induced degradation recovers during the measurement. Especially for SiC MOSFETs, slow $I_{ds}V_{gs}$-sweeps are not a useful technique to study NBTI, because due to the fast recovery barely any degradation is observed when performing slow $I_{ds}V_{gs}$-sweeps.

2.1.3 Measurement of the Hysteresis

Even for the most advanced SiC MOSFETs differences between $I_{ds}V_{gs}$ up- and down-sweeps (from accumulation to inversion and vice versa) are observed and show a hysteresis of up to several volts [59–61]. No significant hysteresis is observed for Si MOSFETs at typical sweep rates, therefore this sub-chapter focuses only on SiC MOSFETs. An example of a hysteresis measurement is shown in Fig. 2.2. For proper characterization of this hysteresis, the following aspects have to be considered:

- The hysteresis is mainly determined by the negative starting voltage V_{gs} of the $I_{ds}V_{gs}$-sweep. The hysteresis is mainly visible in the sub-threshold region due to fast recovery with increasing gate voltage [59]. Therefore, the hysteresis within an $I_{ds}V_{gs}$-curve sweep should be extracted at the lowest possible gate voltage above the drain current resolution limit of the measuring unit.

- The hysteresis then amounts to:

$$\Delta V_{th}^{sub} = V_{th}^{sub}(up) - V_{th}^{sub}(down) \tag{2.1}$$

  with readout in the sub-threshold voltage regime V_{th}^{sub} at a defined current setpoint $I_{d,setpoint}$. In the example shown in Fig. 2.2, the sub-threshold voltage of the up-sweep is shifted by ≈ -4 V.

- Furthermore, due to the longer integration time and thus larger recovery time, the hysteresis is less pronounced for slower sweep rates.

Thus, for proper comparison of threshold voltage shifts before and after stress it is mandatory that all sweep parameters are known and kept the same. The correlation of the hysteresis and its dependence on the sweep parameters is discussed for SiC MOSFETs in Section 10.3.

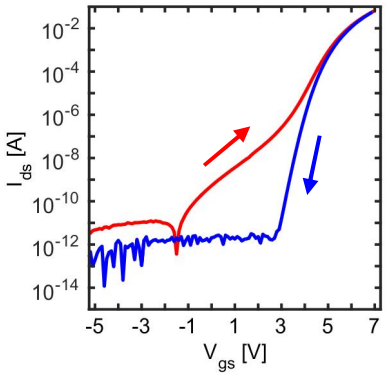

Figure 2.2: Zoom in of $I_{ds}V_{gs}$-up- and down-sweeps for a V_{gs} sweep from −20 V to 7 V of a trench SiC MOSFET [62, 63]. A drain-current hysteresis between up- and down-sweep is visible. The sub-threshold voltage of the up-sweep is shifted ≈ -4 V.

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2.1.4 Fast $I_{ds}V_{gs}$-Sweeps

Threshold voltage read-outs from a full $I_{ds}V_{gs}$-sweep recorded in a microsecond with fast I_{ds} acquisition have been proposed [64–68]. In all cases, the drain current is measured using a pulse generator and an oscilloscope. A special variant has been employed in [69] for V_{th} measurements during bipolar AC stress. Both the up- and down-sweeps are linear microseconds-ramps. Full $I_{ds}V_{gs}$-curves can be recorded during these transitions. In addition, the threshold hysteresis can be extracted from the difference between the up- and the down-ramp. Furthermore, $I_{ds}V_{gs}$-sweeps with ramp times of nanoseconds and below have been reported to study BTI of logic FETs [70–72]. The technique is influenced by signal-distortions due to imperfect impedance matching. In fact, the accuracy in measured ΔV_{th} hardly reaches 10 mV. This is a problem for e.g. nominal operation voltage $V_{dd} = 1$ V, which is not so critical for power MOSFETs but for CMOS technologies. Nonetheless, such techniques applied to SiC MOSFETs have not been reported yet because e.g. for a sample with a 100 pF gate capacitance, at a GHz frequency (corresponding to an nanosecond-ramp), the gate impedance would be 1 mOhm only [KWJ6]. Therefore, the application of this technique clearly would require special samples.

The quality of the fast-$I_{ds}V_{gs}$ measurement depends on the speed and on the V_{gs}-span of the ramp. In principle, an $I_{ds}V_{gs}$-curve contains a lot more information compared to a single-point readout (see Section 2.2), e.g. about mobility degradation. On the other hand, it has to be considered that during the $I_{ds}V_{gs}$-sweep the ΔV_{th} is not a constant and depends on the sweep parameters. As a consequence, fast-$I_{ds}V_{gs}$-sweeps are in principle suitable to extract defect properties such as capture and emission times, as long as the trapping/de-trapping during the ramps is considered. This, however, complicates the measurement setup as well as the data evaluation. Therefore, in this work, we use the $I_{ds}V_{gs}$-sweeps only for the pre-characterization as well as for the post-stress characterization to analyze the full $I_{ds}V_{gs}$ for potential mobility changes.

2.2 Measure-Stress-Measure Scheme

The measure-stress-measure (MSM) technique is one of the most commonly used techniques and has been used for years to study Si NBTI and PBTI. The idea of the MSM scheme is to measure the initial threshold voltage $V_{th,0}$ of a MOSFET. Then, stress is applied to the gate voltage for a certain time at elevate voltages and temperatures. Finally, the degraded V_{th} is measured afterward for a certain time to observe the recovering ΔV_{th}. Prior to measuring, an informed forecast of the aging-induced ΔV_{th} is useful in order to avoid that the measurement ends up in an undesired part of the $I_{ds}V_{gs}$-curve, far off the threshold voltage. As seen in Fig. 2.3, the measured threshold voltage shift significantly reduces with increasing measurement delay t_d.

Since 2003 and the first reports about a measurement delay of $t_d = 0.4$ s by Ershov [35], the experimental efforts to reduce the measurement delay have increased. In 2003, Rangan reported $t_d = 1$ ms, Leroux and Shen $t_d = 1\,\mu$s with the cv method in 2004 [73, 74], followed by Reisinger $t_d = 1\,\mu$s with the cc method [58]. Roughly 50% of the threshold voltage shift in Fig. 2.3 b) recovers until the start of a conventional measurement with $t_d = 1$ s compared to the technique introduced by Reisinger with $t_d = 1\,\mu$s. The most recent report by Yu in 2018 is a delay with $t_d = 1$ ns [71, 75]. Not only is the measurement delay crucial for the characterization of BTI but also the recovery itself contains valuable information about the defect kinetics and the composition of recoverable and quasi-permanent components. Instead of recording V_{th} for a short period after stress, in the extended measure-stress-measure (eMSM) technique the recovery period is extended to record the recovery behavior of V_{th} for a long time e.g. up to days [56].

The technique with several pairs of stress and recovery sequences is perfectly able to extract the distribution of capture and emission times [76] and as such provides a good foundation to

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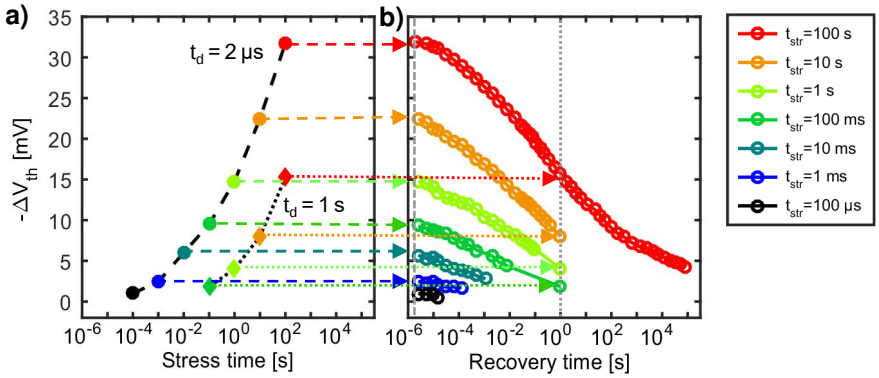

Figure 2.3: MSM sequences for a Si MOSFET: **a)** V_{th} shift during gate stress and recovery **b)** recovery $V_{gs} = -2.8\,V$ and $T = 125°C$ after positive bias stress with multiple pairs of stress and recovery data. The degradation curve is shown for two different measurement delays, $t_d = 1\,\mu s$ and $t_d = 1\,s$. Horizontal arrows connect points in the stress curve to the corresponding recovery measurement. Data from: [58].

analytically model the stress and recovery time dependence of the threshold voltage shift by capture and emission time (CET) maps (see also Section 10.1). The specially designed measurement setup to perform MSM measurements for Si and SiC MOSFETs with a measurement delay of $t_d = 1\,\mu s$ is presented in Section 5.1.2 and Section 9.3, respectively.

2.3 Preconditioning Technique

A deliberately introduced preconditioning step [38] is commonly used within the qualification process of the SiC MOSFETs using preconditioning gate pulses before measuring V_{th} as presented in [38, 77, 78] and sketched in Fig. 2.4. The basic idea behind the preconditioning measure-stress-measure sequence is to remove the fully-reversible hysteresis effect from the extracted V_{th} drift by restoring a defined charge state at the interface before each threshold voltage read-out. This is achieved by using e.g. a 100 ms negative preconditioning gate pulse before measuring $V_{th,up}$ and a 100 ms positive preconditioning gate pulse before measuring $V_{th,down}$ [79].

For all cases it has to be ensured that the preconditioning pulses and sweep rates are precisely reproducible. It is clear that the method is not suitable to determine fast ΔV_{th}-components due to the removed stress history, which is especially relevant to resolve the threshold voltage shift within a switching period (see Section 9.3.1). Furthermore, it cannot be used to measure and

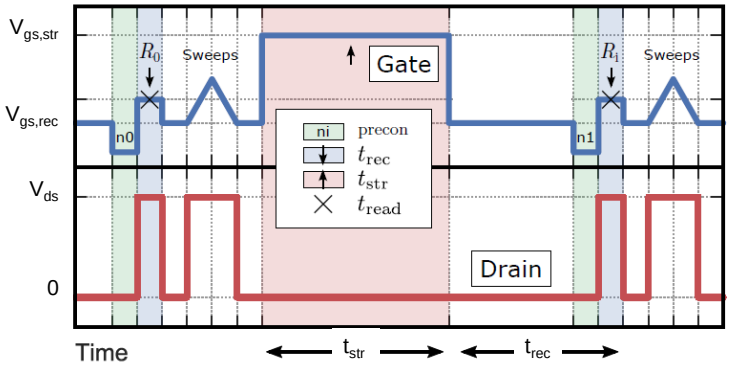

Figure 2.4: Preconditioned BTI pattern with accumulation pulse of length $n = t_{acc}$ (green) before the initial readout R_0 with $I_{ds}V_{gs}$ sweeps and the readout R_i after stress to maintain identical switching conditions. Source: [77]

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extract the distribution of capture and emission times (as it is possible for e.g. the MSM technique presented in Section 2.2). However, it is able to determine the more permanent ΔV_{th}-components, which lead to long-term drift of device characteristics.

Advantages are the capability to precisely compare the threshold hysteresis between different samples or the evolution of the hysteresis after (any) stress [38, 78, 79]. Another advantage of this technique is its straightforward applicability by most standard measurement equipment or parameter analyzer. The time delay between the end of the stress and the readout is almost irrelevant for the measurement result [79], which is particularly beneficial for industrial qualification tests because many devices can be measured in series after parallel stressing in a furnace. A comparison of measurements with the preconditioning technique with our fast MSM technique are shown in Section 10.1.5.

2.4 On-the-fly Measurements

The on-the-fly (OTF) measurement technique, also called "non-relaxational" technique [80], was proposed by Denais *et al.* to overcome the influence of the measurement delay [81]. In OTF measurements, the drain current I_{ds} is measured by applying a modulation to the gate bias close to the stress level. Afterward, to determine ΔV_{th}, a three-parameter MOSFET model is used in order to extract the parameter change [82]. The technique has been used to study BTI in Si and in SiC MOSFETs [83]. It is possible to implement OTF measurements with the standard measurement equipment (see Section 5.1.1). The readout of ΔV_{th} is performed at the stress gate voltage. Therefore recovery, even the one caused by a short µs-measuring delay, is omitted.

However, a huge drawback of the measurement technique is that the initial measurement is already modified by the degradation induced due to the measurement at stress voltage. Therefore, it is impossible to measure an initial (zero-hour) V_{th} [58]. This is especially critical for SiC, because already applying short stress pulses of e.g. a 1 µs causes a threshold voltage shift of around 100 mV. With the measurement at stress, the OTF technique produces and at the same time misses within the initial measurement these 100 mV which thus introduces a systematic error. This error is unknown because it cannot be determined by the OTF experiment.

Moreover, OTF determines the V_{th} at a bias much higher than the actual threshold voltage, leading to a different ΔV_{th} due to additionally occupied states, which are not occupied at operating voltage as discussed in [68, 84]. Furthermore, the technique cannot distinguish between V_{th} and mobility degradation. However, OTF can be a very useful technique to measure the $R_{ds,on}$. OTF is the only technique to directly measure the short-term variations of $R_{ds,on}$ during AC gate bias switching exactly like in the application as described in Section 9.3.2 with the measurement results presented in Section 10.5.

2.5 Resistive Heater Technique

Resistive heater techniques enable to heat up MOSFETs within seconds from e.g. room temperature to 300°C or more by placing small poly stripes to surround the MOSFET under investigation [85]. This is commonly applied in time-critical wafer-level reliability monitoring [86–89] because the resistive heater provides fast heating of the device without the limitations associated with a conventional heating system like a thermo-chuck or a furnace. Since charge trapping starts at very short time constants, it is useful to shift these short time constants into the measuring window (see Section 5.2.2, Fig. 5.4) by "freezing" the emission, preferably at cryogenic temperatures. Decreasing temperature shifts the short capture and emission time constants at lower temperatures into the measurement window and thus provides the opportunity to study these defects. Resistive-heater techniques have been employed in the past for Si MOSFETs within single-transistor characterization [90, 91] or for fWLR monitoring with e.g. small circuits as the

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ring oscillator presented in Section 5.2.3. To our knowledge, no approach to use these resistive heater techniques for SiC MOSFETs has been reported yet, even if it offers a good possibility to study the short emission time constants of SiC-related defects.

2.6 Electrical Defect Spectroscopy

Investigations on the bias- and temperature-dependence of charge capture and charge emission on single, individual defects provided considerable insights into the nature of BTI related defects [92, 93]. These measurements are performed on small-area devices to study single defects and are referred to in the Si literature as time-dependent defect spectroscopy (TDDS). An example of a typical ΔV_{th} recovery measurement is shown in Fig. 2.5. Large-area devices show a continuous recovery of V_{th} towards $\Delta V_{\text{th}} = 0$ V, whereas nanoscale MOSFETs show discrete steps in the V_{th} recovery measurement. The impact of a single charge q on the ΔV_{th} is given by

$$\Delta V_{\text{th}} = \frac{-q}{C_{\text{ox}}}, \text{ with } C_{\text{ox}} = \epsilon \cdot \frac{A}{t_{\text{ox}}} \tag{2.2}$$

where C_{ox} is the oxide capacitance determined by its dielectric constant ϵ_{ox}, the gate area A and the oxide thickness t_{ox}. The number of active traps N_{t} decreases with the device area A, but if the area is reduced, the impact of a single charge on the ΔV_{th} is increased. To observe discrete steps, the steps have to be larger than the resolution of conventional ΔV_{th} measurements (≈ 0.1 mV). Thus, for a SiO_2 oxide with $t_{\text{ox}} = 2.2$ nm thickness, the area of the MOSFET needs to be smaller than about 100 nm $\times$ 100 nm [94].

For large-area devices, the large number of active traps N_{t} ($\gtrapprox 1000$) leads to a continuous recovery trace. Thus, the same BTI traps are responsible for the nanoscale and large-area devices and consequently, the threshold voltage shift can be modeled as the sum of N independent defects with different impact on the ΔV_{th}. With TDDS measurements, via the step height η in the recovery traces, the defects can be identified with a capture and emission time dependent on the temperature, stress, and recovery bias. As SiC devices are generally larger than Si MOSFETs, to our knowledge no single trap studies have yet been reported on SiC MOSFETs. Nonetheless, there is no obvious reason why this technique could not be applied to SiC MOSFETs.

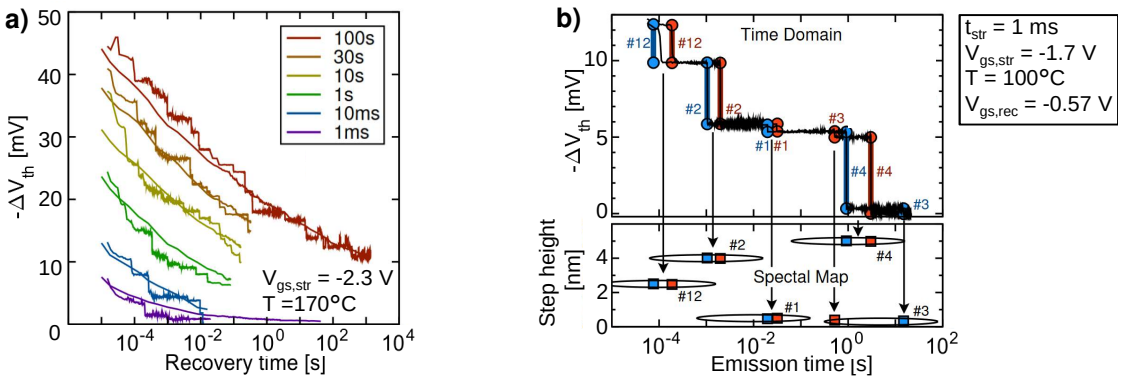

Figure 2.5: a) Step-wise recovery of a single narrow device in comparison with the average over 25 different devices (smooth traces) after different stress times. Discharge of a single hole leads to each step with widely distributed emission times. [95]. **b)** Two typical ΔV_{th} recovery measurements of a small-area MOSFET with unambiguous fingerprints of each defect: the step height and the emission time constant. The analysis of a large number of recovery measurements and the corresponding spectral mapping (bottom) of each defect with its step height and emission time is called TDDS [96].

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Chapter 3

Fundamentals of the Bias Temperature Instability

The performance of n-channel as well as p-channel MOSFETs is seriously affected by bias temperature instabilities, which are one of the most crucial reliability concerns in modern semiconductor devices. In general, BTI is divided into positive BTI (PBTI) and negative BTI (NBTI). The terms negative and positive refer to the bias applied to the gate contact of the device and is typically referred to as stress bias $V_{\mathrm{gs,str}}$. As shown in Fig. 3.1 a) for Si MOSFETs, NBTI is more severe in pMOSFETs, whereas PBTI is pronounced for nMOSFETs. Commonly, due to the higher impact on the device performance and usage (rare application of significant positive voltages to pMOSFETs as well as significant negative voltages to nMOSFETs), the focus of the industry and research lies on NBTI of pMOSFETs. Nonetheless, several modern technologies are significantly affected by both PBTI and NBTI, an example are MOSFETs with high-κ dielectrics [37, 57] and SiC nMOSFETs [KWJ6, 97].

In this chapter, the fundamentals of the bias temperature instability are described. First, in Section 3.1, the impact of BTI on the device characteristics is presented. Second, the impact on the circuit performance is described in Section 3.2. Third, the main properties of BTI such as the temperature and voltage dependence are discussed in Section 3.3. Fourth, empirical, physical as well as compact models describing BTI are presented in Section 4.

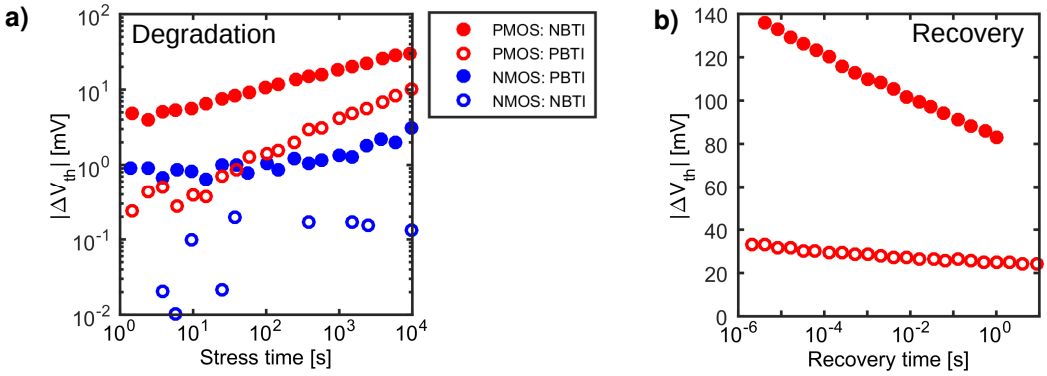

Figure 3.1: a) Threshold voltage shift as a function of the stress time for both nMOSFET and pMOSFET devices under positive and negative bias at $T = 125°\mathrm{C}$. Data from: [50]. **b)** ΔV_{th} recovery after 10^4 s NBTI and PBTI stress of a p-MOSFET (same stress field). Data from: [98].

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3.1 Impact on the Device Characteristics

Typically, the impact of BTI on the device characteristics is described as shift of the threshold voltage V_{th}. Throughout this work, as is commonly done, the threshold voltage shift ΔV_{th} is defined as the voltage difference of the gate bias to drive the same drain-source current between the unstressed and stressed device. Because circuit designs rely on defined current thresholds for the devices in their *on* and *off* state, this definition is well-suited for circuit designers and can also be implemented within a BSIM circuit simulator using the Berkeley short-channel IGFET model (BSIM) parameter *delvt0*. Not only the threshold voltage shifts towards larger absolute gate voltages when subjecting a MOSFET to negative gate stress voltages, but also the transconductance g_{m} and the *on* current reduces. The fractional change of drain current due to the threshold voltage shift is for MOSFETs in the linear region for $V_{\text{ds}} \ll V_{\text{gs}}$ [50, 99]:

$$I_{\text{d,lin}} \approx \frac{w_{\text{des}}\mu_{\text{eff}}C_{\text{ox}}}{l_{\text{des}}}\left(V_{\text{gs}} - V_{\text{th}}\right)\cdot V_{\text{ds}} \rightarrow \frac{1}{I_{\text{d,lin}}}\frac{\text{d}I_{\text{d,lin}}}{\text{d}V_{\text{th}}} = -\frac{\Delta V_{\text{th}}}{V_{\text{gs}} - V_{\text{th}}} \tag{3.1}$$

and for the saturation region [100]:

$$I_{\text{d,sat}} \approx \frac{w_{\text{des}}\mu_{\text{eff}}C_{\text{ox}}}{2l_{\text{des}}}\left(V_{\text{gs}} - V_{\text{th}}\right)^2 \rightarrow \frac{1}{I_{\text{d,sat}}}\frac{\text{d}I_{\text{d,sat}}}{\text{d}V_{\text{th}}} = -\frac{2\Delta V_{\text{th}}}{V_{\text{gs}} - V_{\text{th}}}. \tag{3.2}$$

μ_{eff} denotes the effective channel mobility and l_{des} and w_{des} the effective length and width of the transistor. With technology scaling, the device dimensions and voltages shrink, typically the reduction in V_{gs} is larger than in V_{th}, leading to a higher degradation for smaller technology nodes [100]. The fractional change of the drain current due to a change in mobility is

$$\frac{1}{I_{\text{ds}}}\frac{\text{d}I_{\text{ds}}}{\text{d}\mu_{\text{eff}}} = \frac{\Delta\mu_{\text{eff}}}{\mu_{\text{eff}}}. \tag{3.3}$$

Since the density of interface traps density D_{it} depends approximately inversely on μ_{eff}, the mobility degrades due to interface trap generation [100]. The effect of these changes on the device characteristics after BTI stress on circuits is discussed in the following.

3.2 Impact on Circuits

A typical application in which BTI affects the performance of a circuit is a simple inverter circuit as shown in Fig. 3.2. Dependent on the input voltage, either the PMOS or the NMOS is affected by NBTI or PBTI, respectively. Therefore, in logic CMOS applications, both NBTI and PBTI affect the performance of the circuit. However, for the Si MOSFETs studied in this work as shown in Fig. 3.1 a), the BTI degradation is roughly a factor of 10 higher for the pMOSFETs than the nMOSFETs. Typically for digital and analog circuits, very important parameters are the drain currents $I_{\text{d,lin}}$ and $I_{\text{d,sat}}$. Higher drain currents lead to faster capacitor charging and higher frequency operation in digital circuits. The delay time in digital circuits is

$$t_{\text{d}} = \frac{C\,|V_{\text{dd}}|}{I_{\text{ds}}} = \frac{2l_{\text{des}}C}{W\mu_{\text{eff}}C_{\text{ox}}\left(V_{\text{dd}} - \Delta V_{\text{th}}\right)^2} \tag{3.4}$$

where V_{dd} is the supply voltage, C is the load capacitance, C_{ox} the oxide (or insulator) capacitance. As NBTI leads to a reduction in μ_{eff} and an increase in V_{th}, the delay time increases. As a consequence for e.g. ring oscillators, the switching frequency ($f = 1/t_{\text{d}}$) decreases quadratically to ΔV_{th}.

BTI is also a reliability concern for static random access memory (SRAM) cells, as it leads to an increase in the minimum read voltage and a decrease in the minimum write voltage of

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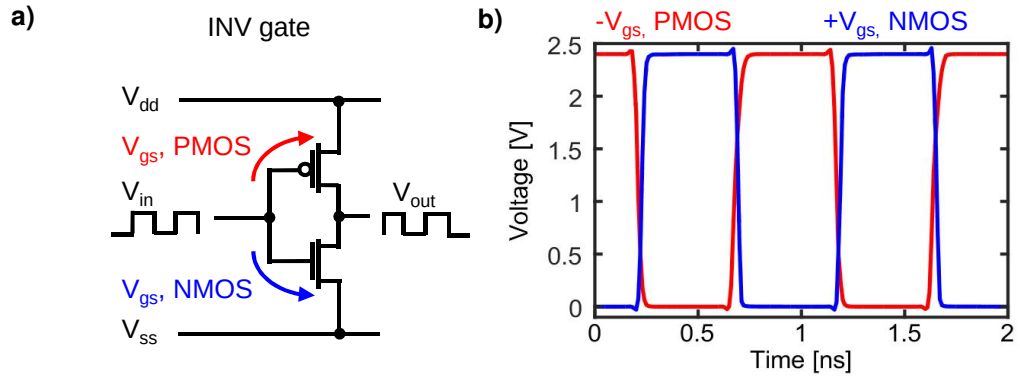

Figure 3.2: a) CMOS inverter consisting of a nMOSFET and a pMOSFET in series with a common gate contact. **b)** Input and output voltages alternate between V_{dd} and V_{ss}. If $V_{in} = V_{dd}$, the nMOSFET is subjected to PBTI stress, whereas if $V_{in} = V_{ss} = 0$, the pMOSFET is subjected to NBTI stress.

the SRAM cell [101, 102]. An example of a critical circuit is a two-stage operational amplifier/comparator, which is a typical analog circuit-block [103]. These analog circuit-blocks often have a so-called "power-down" functionality to save e.g. battery power, the bias of the amplifier is switched off, but the supply voltages are still applied. Critical devices are matched or exactly weighted transistor pairs as they are under asymmetric stress during this "power-down" mode. In this case, one of the two matched transistors ages more than its counterpart, which can lead to severe BTI induced input offset voltages and finally to a malfunction of the circuit [KWC1]. Particularly for these circuits, reliable and accurate aging models for circuit simulations are of utmost importance.

3.3 Properties of the Bias Temperature Instability

An accurate aging model has to cover all important dependencies of the degradation effect. Therefore, in the following, the most important experimental observations are summarized. The dependence of the capture and emission time constants of single defects on the temperature, stress, and recovery bias are discussed and the two-state modeling approach based on the non-radiative multi-phonon (NMP) theory is introduced. Furthermore, the temperature, stress, and recovery bias dependence of large-area defects with distributed capture and emission time constants is described. This chapter focuses on the observations made on Si MOSFETs. Experimental studies of BTI on SiC MOSFETs are discussed in Section 8.3. The physical model behind capture and emission of charge into defects is described in detail in Section 4.3.2.

3.3.1 Single Trap Characteristics and Two-State Modeling

TDDS studies and random telegraph noise (RTN) measurements with simultaneously recorded I_{gs} and I_{ds} as shown in Fig. 3.3 a) reveal that each defect has a different step height η and can be identified with its mean capture time τ_c and its emission time τ_e [21, 92] (see also Fig. 2.5 b). The simplest approximation for the phenomenological behavior of the defects is the description of defects consisting of *two states*, a charged state and an uncharged (neutral) one as shown in Fig. 3.3 b). As illustrated in Fig. 3.3 c), the two states are separated by a potential barrier on the order of 0.4 – 1.5 eV [76]. The energy level of the charged state can be shifted up and down with the applied gate voltage. During capture the barrier B_c and during emission the barrier B_e has to be overcome by thermal excitation which is a stochastic transition and can be described by a Markov process. The transition process from one state to the other is thermally driven and is

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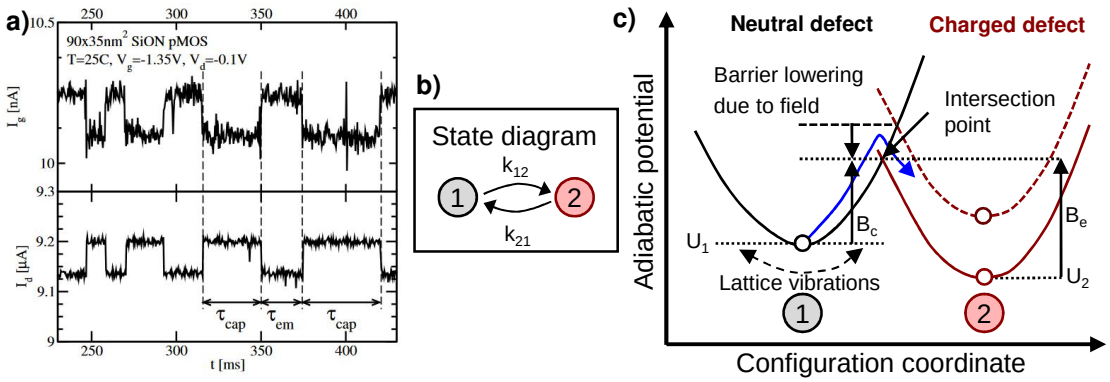

Figure 3.3: a) RTN measurement with simultaneously recorded I_{gs} and I_{ds} traces. A decrease in I_{ds} is observed for hole capture after a period of τ_c and at the same time I_{gs} increases. Vice versa after a period τ_e, a decrease in I_{gs} is observed. Source: [21]. **b)** Two-state diagram with a neutral (gray circle) and a positive charge (red circle) state. The transition rates k_{12} and k_{21} are described by the NMP theory. **c)** Schematic of a configuration coordinate diagram of a defect in the neutral, uncharged state and in the charged state for two different electric fields (the dashed black line corresponds to the lower field). In the semiclassical approximation, the neutral defect has to be thermally excited via lattice vibrations up to the intersection point, then the charge carrier may tunnel to the positive defect and relax to its new equilibrium state. Adapted from: [104, p.80]

described by the transition rates k_{12} and k_{21}, which are the probabilities for the transition from one state to the other within a unit time interval.

The mean charge capture and emission times τ_c and τ_e follows the relations:

$$k_{12} = \frac{1}{\tau_c} \text{ and } k_{21} = \frac{1}{\tau_e}. \tag{3.5}$$

The physical process behind the transition $1 \rightarrow 2$ is ascribed to hole capture (i.e. electron emission) whereas the transition $2 \rightarrow 1$ is ascribed to hole emission (i.e. electron capture). In the case of an electron trap, the roles of electrons and holes are exchanged. The transition rates are described by the NMP theory which relies on calculating the quantum mechanical transition probability between the two atomic configurations. In this picture, the adiabatic energy surfaces are reduced to one-dimensional configuration coordinates and approximated by a harmonic oscillator as shown in Fig. 3.3 c). In a semiclassical approximation the barriers for the charge capture B_c and emission B_e depend on the intersection point of the parabolas belonging to the energy levels U_1 and U_2. If $\Delta U_{12} = U_1 - U_2 \geq 0$ the forward rate exceeds the backward rate $k_{12} \geq k_{21}$ and thus state 2 is the preferred state (defect is charged, "stress"), whereas if $\Delta U_{12} \leq 0$ the backward rate exceeds the forward rate and thus state 1 is the preferred state (defect is uncharged, "recovery"). As such, the capture and emission times depend on the applied gate voltage for stress and recovery, making it an electrochemical reaction. Further modeling details on the defect centric model by Grasser [48] are provided in Section 4.3.2.

Temperature- and Bias-Dependent Time Constants of Single Defects

Large-area devices show a continuous increase in ΔV_{th} during stress, whereas nanoscale transistors show discrete steps in the ΔV_{th} measurement (see Fig. 2.5). In TDDS measurements, the defects can be identified by their capture and emission times as well as their step heights [92]. Numerous detailed TDDS experiments have led to the following conclusions on the capture and emission time constants and their dependencies on temperature, stress, and recovery bias:

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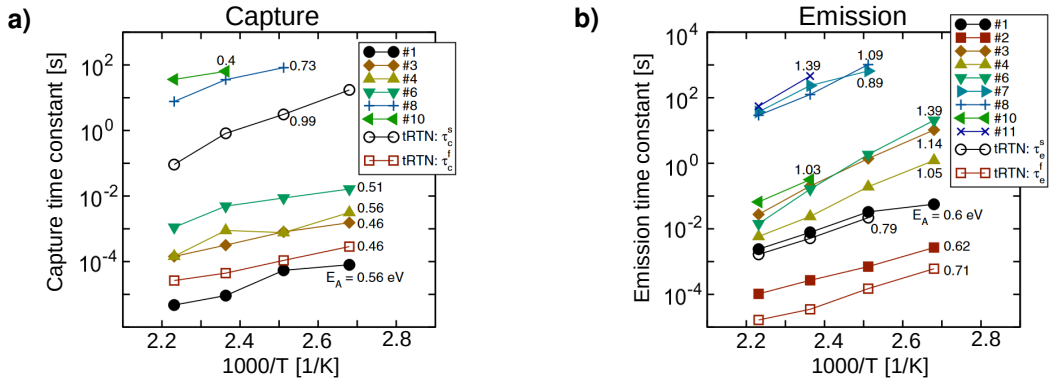

Figure 3.4: Temperature dependence of single defects: **a)** Capture time constants and **b)** emission time constants. An almost linear relationship between the logarithm of the capture/emission time constants and $1/T$ suggests the Arrhenius-like temperature dependence as described in (3.6). Activation energies (written next to the arbitrarily labeled defects) are widely distributed. Source: [92]

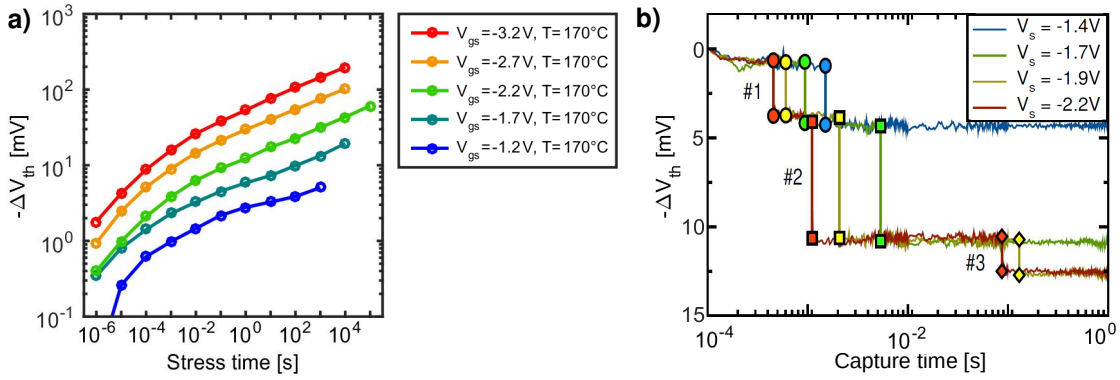

Figure 3.5: Stress bias dependence of NBTI: **a)** Threshold voltage shift dependent on the stress time for different stress voltages for a large-area transistor. Data from: [51]. **b)** The single defects show discrete ΔV_{th} steps with characteristic capture times. The capture time constants of the defects decrease with increasing stress bias. Source: [105]

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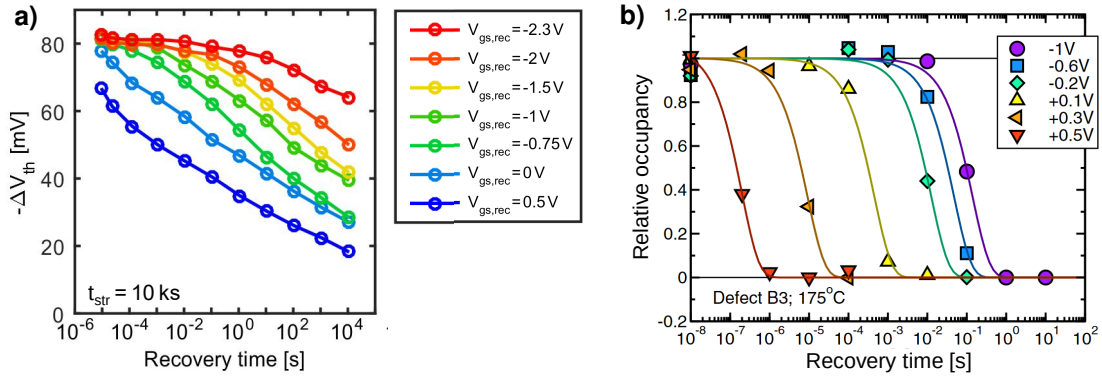

Figure 3.6: Recovery bias dependence of NBTI: **a)** Recovery bias dependence over recovery time for a large-area transistor. The ΔV_{th} recovery after the same stress is accelerated with increasing recovery voltage. Data from: [106]. **b)** Single defects show discrete ΔV_{th} steps with characteristic emission times. Shown is the experimental relative defect occupancy as a function of the pulse duration. The emission time constants of the defects decrease with increasing recovery bias. Also, defects with emission time constants that are unaffected by the recovery bias have been observed. Source: [107]

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- NBTI degradation and recovery is initially due to charging and discharging of individual defects. The capture time constants τ_c and emission time constants τ_e are widely distributed (from sub-microseconds to longer than several days).

- It was found that by varying the temperature (see Fig. 3.4), the emission and capture time constants of single defects are thermally activated approximately following an Arrhenius equation [92, 94, 108–110]:

$$\tau = \tau_0 \cdot \exp\left(\frac{E_a}{k_B T}\right) \tag{3.6}$$

  with an activation energy E_a, Boltzmann's constant k_B and the characteristic temperature-independent constant τ_0. As illustrated in Fig. 3.3, the barrier B_c corresponds to the activation energy of the capture process $E_{a,c}$, whereas the barrier B_e corresponds to the activation energy of the emission process $E_{a,e}$.

- No defects with temperature-independent capture time constants could be found in the experimental window of microseconds to days.

- Capture time constants show a strong field dependence as illustrated in Fig. 3.3 c). The threshold voltage shift increases with increasing stress bias, because a higher stress bias leads to a higher oxide field and thus a higher number of charged defects as seen in Fig. 3.5 a). The increase in stress bias leads to decreasing capture times of the single defects and increases the probability of charging a single defect.

- The emission times of the charge emission events in Fig. 3.6 are recovery bias dependent, but single defects that show bias-independent recovery also exist. The bias independent emission time constants are associated with *fixed oxide traps*, whereas the bias dependent emission times are due to *switching traps* [107]. This observation led to the development of the four-state NMP model, which is presented in Section 4.3.2

It is assumed that within a micrometer-sized device, thousands of defects have a wide distribution of capture and emission time constants being responsible for the power-law-like increase of V_{th} with stress time, as shown in Fig. 3.5 a). Strong acceleration of the recovery can be achieved for recovery voltages towards accumulation [51] as shown in Fig. 3.6 a). The modeling of the distribution of the capture and emission time constants is discussed in Section 4.4.1.

3.3.2 Temperature Dependence of Large-Area Devices

As the name BTI indicates, the degradation mechanism is strongly temperature-activated, meaning that the degradation becomes more severe with increasing temperatures [30, 100, 112, 113]. For most silicon devices already a significant threshold voltage shift can be measured above $T = 100°C$ [15, 50, 114] as shown in Fig. 3.7 a). The poly-heater technique is applied to vary the stress temperature and ensure the same recovery temperature for all measurements [85]. As such, the temperature dependence of the degradation is separated from the temperature dependence of recovery [115].

Recovery of ΔV_{th} degradation caused by NBTI occurs over many decades in time following a $\log(t_{rec})$-like behavior [96]. The recovery temperature has a strong impact on the measured threshold voltage shift as seen in Fig. 3.7 b). Recovery at lower temperatures results in a larger measurable degradation level [90, 91, 111, 116], because already before the first measurement point, most of the degradation has recovered at higher recovery temperatures. Even after a long recovery time most of the degradation is still not recovered at low temperatures.

The defect time constants for capture τ_c and emission τ_e are thermally activated as shown in Fig. 3.4. Following the Arrhenius law (3.6), the defect time constant τ_1 at temperature T_1 changes with temperature T_2 to the defect time constant τ_2.

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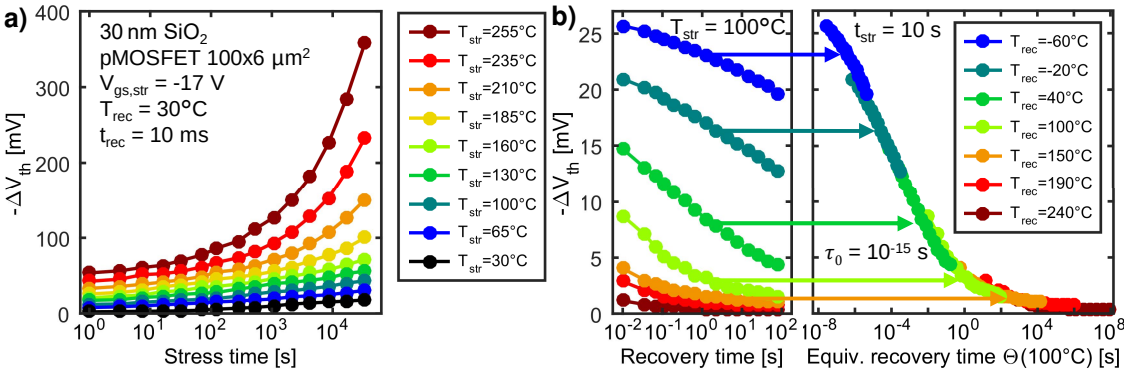

Figure 3.7: a) Dependence on the stress temperature by applying the poly-heater technique with $T_{\text{rec}} = 30°\text{C}$. The stress temperature significantly increases the ΔV_{th} following the Arrhenius law. **b)** Temperature-dependent recovery after the same NBTI stress (identical duration, same oxide field, same stress temperature) for the original recovery time (left) and the equivalent recovery time $\theta(T = 100°\text{C})$. Higher recovery temperatures decrease the observed ΔV_{th} due to accelerated recovery. All recovery traces can be mapped onto one single trace by calculating the temperature-time θ following (3.7). Data from: [111]

Data recorded at a reference temperature T_{ref} is thus equivalent to data recorded at any T considering the time-transformation [90]

$$\theta(T) = \tau_0 \left(\frac{t}{\tau_0} \right)^{T_{\text{ref}}/T} . \tag{3.7}$$

Pobegen *et al.* have demonstrated that the Arrhenius temperature dependence is also valid for a large ensemble of defects [111]. In Fig. 3.7 b), measurements of different temperatures are transformed following (3.7) to a single time scale and all recovery traces are mapped onto one single trace. The benefit of this transformation of the experimental time-window will be further discussed in Section 5.2.2, where a new measurement technique - the TA-MSM technique is introduced.

3.4 Defect Candidates for the Bias Temperature Instability

Despite the huge effort made to identify the underlying defect structures responsible for the reliability phenomena, the origin of the recoverable and quasi-permanent component remains under debate [32]. Although the absolute ΔV_{th} is more pronounced in SiC-based devices, the similar characteristics of BTI in SiC-based devices to Si-based devices indicates similar atomic origins. In the following several microscopic defect candidates are presented and discussed based on experimental results and theoretical calculations on Si MOSFETs. In Section 8.4, a detailed discussion on the nature of the traps in SiC MOSFETs based on current literature is given.
The amorphous SiO_2 used in insulators is non-ideal due to imperfections introduced during the device fabrication and due to imperfections at the interfaces between the different materials. As a consequence, electrically active sites exist which are also called traps. We differentiate between the following traps occurring in thermally grown SiO_2 gate dielectrics as shown in Fig. 3.8 [117]:

- Mobile ionic charges, which may exist due to impurities
- Fixed oxide charges due to structural defects in the SiO_2 near the Si/SiO_2 or in the case of SiC MOSFETs SiC/SiO_2 interface
- Trapped oxide charges in the SiO_2

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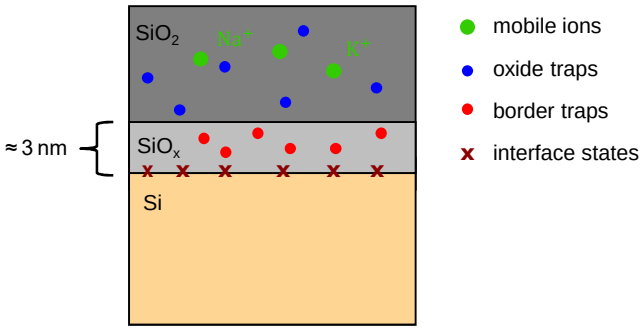

Figure 3.8: Classification of defects in the SiO_2/Si system. Adapted from: [117]

- Border traps, which are located in the first ≈ 3 nm of the SiO_2
- Interface trapped charges, due to the lattice mismatch between crystalline Si or SiC bulk and the SiO_2.

In the following, some experimental techniques and theoretical calculations, which have been employed to identify the responsible defects, are presented and its results are discussed:

- Electron-spin resonance (ESR), which is also often called electron paramagnetic resonance (EPR), provides chemical information about the composition of point defects in semiconductors and insulators. The atomic structure is exposed to a magnetic field and the microwave absorption is studied [118].
- In thermally grown SiO_2, a considerable amount of hydrogen is induced in the manufacturing process of the device. Some recent studies using nuclear reaction analysis (NRA) have been applied to detect hydrogen, as it has been suggested to be important for defect formation [119].
- Transmission electron microscopy (TEM) [120] and scanning tunneling microscopy (STM) [121] provide information about the surface structure and thickness of layers, whereas secondary ion mass spectrometry (SIMS) investigations can be used to analyze the composition of thin films [122].
- Capacitance-voltage (CV) curves provide information about the energy, density and the time constants of the defects [123, 124].
- Theoretical investigations on the atomistic structure of possible defect properties is obtained by the density functional theory (DFT) [125, 126].

Based on the investigations presented above, several types of defects responsible for BTI are discussed and shown in Fig. 3.9. In the following, the most important results of the interface between Si and SiO_2 are summarized:

- The best-known defect candidate in SiO_2 is the *oxygen vacancy*, a defect structure, in which two neighboring Si atoms are bonded to three instead of four oxygen atoms. They have multiple configurations as the E' and E'_γ configuration [127–129].
- A hydrogen atom trapped in an oxygen vacancy has also been suggested as a possible defect candidate, the so-called *hydrogen bridge* configuration. Due to the interstitial hydrogen, the bond between the two neighboring Si atoms is distorted [11, 130].

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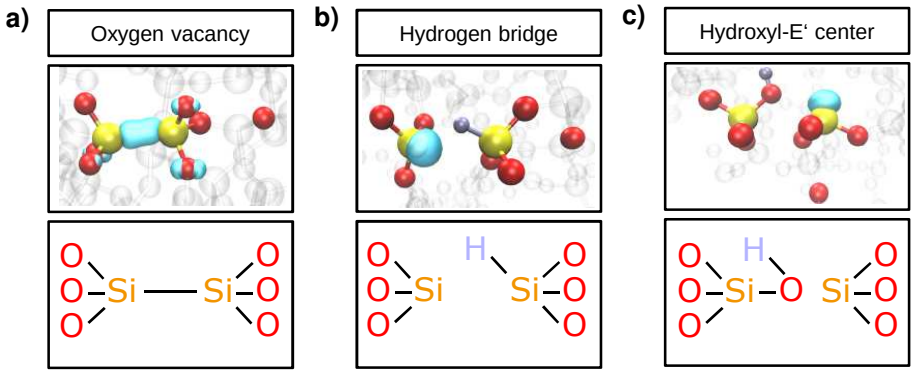

Figure 3.9: Defect candidates in amorphous SiO_2: **a)** The oxygen vacancy, **b)** the hydrogen bridge. **c)** the hydroxyl E' center. Top: Atomic configurations of the neutral stable state 1. The turquoise bubble representes the localized highest occupied orbitals for the neutral charge states and the lowest unoccupied orbital for the positive charge states. Adapted from: [134]. Bottom: Simplified schematic for the initial configuration.

- Dangling bonds of threefold-coordinated Si atoms facing a hydroxyl O-H group are called *hydroxyl* E' centers and have shown good agreement between experimental data and DFT calculations [131]. Like the hydrogen bridge and the oxygen vacancy, the hydroxyl E' center has four possible configurations, two stable and two meta-stable states [125].
- Interface states are commonly associated with P_b centers, where the Si has a *dangling bond*. Dependent on the crystal orientation of the interface, there are three different types of P_b centers available at the SiO_2/Si interface [2, 132, 133].

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Chapter 4

Modeling of Bias Temperature Instabilities

Until today, more than 10000 [34] publications of BTI measurements and proposals of degradation mechanisms have been published. As the central motivation of this work is to provide an accurate and efficient aging model for circuit simulations, the currently published models are discussed with respect to their suitability within a commercial circuit simulation.

4.1 Model Requirements for Circuit Simulations

For this purpose, five requirements that have to be fulfilled are defined as following[1]:

1) The model has to correctly cover degradation as well as recovery time constants from submicroseconds up to 10 years. Additionally, a minimum accuracy for the threshold voltage shift is required.

2) The complete stress history has to be considered within the model to be able to model the actual stress and recovery condition. Temporal changes including changes of the stress and recovery voltage, short-term peaks, over- and undershoots, temperature, and application modes like e.g. standby have to be correctly captured within the model.

3) Different components of BTI may be in different states of degradation or recovery at the same time, dependent on the previous stress history [135, 136]. As a consequence, the model has to treat these defects differently.

4) The model has to be suited for arbitrary stress stimuli e.g. by numerically solving differential equations. But such computations consume time and computing power and are as such unsuitable for the use in circuit simulators. Stress stimuli occurring within the application may be complex but are in general periodic. A computationally efficient model has to be able to take advantage of this periodicity. To be applicable within industrial circuit simulators, the additional computation time of the aging simulation of the whole circuit should not significantly exceed the simulation time of the circuit without aging.

5) A final requirement for the use in commercial simulators is that the experimental and implementation effort to set up the model has to be feasible.

[1] The requirements have been formulated and published by the author of this thesis in [KWJ3]

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In industry, currently, very simple models such as power-law models are widely used, lacking physical background and accuracy. During the past couple of years, research groups at the Institute for Microelectronics (TU Wien), imec (Belgium) and Infineon (Munich and Villach) have developed a defect-centric model with distributed capture and emission time constants of the defects, providing accurate physical agreement with the measurements. The NMP theory [137–139] offers an accurate description of the phenomena related to oxide defects across multiple technologies [140]. The four-state NMP model [141] has been successfully applied to model PBTI as well as NBTI consistent with RTN [142] and SILC [143, 144]. The model has been extended to describe the hydrogen release mechanism [48, KWC3, KWC6].

Although modern devices have been dramatically down-scaled, the computational effort to directly compute the electrical properties of the oxide with time-consuming technology computer aided design (TCAD) simulations are too large to be used for circuit simulations. Therefore, physics-based compact models are beneficial. Capture and emission time (CET) maps were proposed based on a two-state modeling approach to provide a physical approximation of the four-state NMP model [145, 146]. Another modeling approach that enables fast AC circuit simulation based on a defect data-base was proposed recently by Giering *et al.* [52, 147]. Furthermore, a compact-physics framework called "Comphy" has recently been developed by Rzepa *et al.* using an abstraction of the NMP model together with a semi-empirical model for defect generation and transformation to an effective two-state model [51].

4.2 Empirical Models

Typically, empirical models are used if the detailed underlying mechanism is not known or physics-based modeling exceeds the feasible experimental effort, or is too computational expensive. Empirical models provide a simple description of the experimental data. Device degradation can often be modeled using a power-law or exponential-like functions [148, Chapter 2]. Empirical models are widely used in industry for the comparison of different technologies and lifetime estimations. In addition, the implementation into a circuit simulator is easily feasible and the model can e.g. be integrated with a simple assertion function in the SPICE simulation framework. As these models do not provide a physics-based description of the underlying mechanism, extrapolations may be inaccurate and depend e.g. for NBTI on the measurement delay or readout condition [149–151].

Power-law

Already in 1978, the simple power-law was used by Sinha *et al.* to describe BTI as the shift of the flat-band voltage ΔV_{fb} [152]. Typically, the dependence on the stress time of the threshold voltage shift is described by the power-law in time as:

$$\Delta V_{\mathrm{th}} = A t_{\mathrm{str}}^{n}, \tag{4.1}$$

with n the power-law exponent typically reported in the range of 0.1 – 0.3 [50, 100, 151, 153] and A the prefactor containing the stress voltage and temperature dependence. The stress voltage dependence is in this framework often modeled as:

$$A \propto {E_{\mathrm{ox}}}^{\gamma} \approx \left(\frac{V_{\mathrm{ov}}}{t_{\mathrm{ox}}}\right)^{\gamma}, \tag{4.2}$$

with E_{ox} the oxide field, the overdrive voltage $V_{\mathrm{ov}} = \left|V_{\mathrm{gs}} - V_{\mathrm{th}}\right|$. Typically the exponent γ is in the range of 2.5 – 3 for Si devices [50].

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As discussed in Section 3.3.1, the temperature dependence can be described by an Arrhenius law

$$A \propto \mathrm{e}^{-\frac{E_\mathrm{a}}{k_\mathrm{B}T}} \tag{4.3}$$

and the extracted activation energy E_a is typically reported to be in the range of 60 – 80 meV [50, 100]. The threshold voltage shift is then modeled by the simple analytic expression

$$\Delta V_\mathrm{th} = A_0 \left(\frac{\left| V_\mathrm{gs} - V_\mathrm{th} \right|}{t_\mathrm{ox}} \right)^\gamma \mathrm{e}^{-\frac{E_\mathrm{a}}{k_\mathrm{B}T}} t_\mathrm{str}^n. \tag{4.4}$$

As the threshold voltage shift shows a power-law dependence on the stress time, a $\log(t_\mathrm{str})$-$\log(V_\mathrm{th})$ plot shows a straight line. Using (4.4) with a fit to measurement, the parameters can be estimated for each technology and the model can be integrated within a circuit simulator [154, 155]. Nonetheless, the model neglects several effects such as recovery and saturation (deviation from the power-law), time-dependent stress voltages, or non-constant n for different stress conditions.

Time-Dependent Stress Voltages

An extension to the power-law model has been proposed for HCS [156]. The model still neglects recovery, but improves the model accuracy by accounting for changes in the stress voltages [157]. A general equation for the conversion of a power-law constant-bias degradation to degradation formulas valid under time-varying bias has been given by Scholten *et al.* [158]:

$$\Delta P(t) = C \left[\int_0^t f\left(V_i(\hat{t})\right) \mathrm{d}\hat{t} \right]^n. \tag{4.5}$$

This model can be used to calculate the drift of a parameter P (e.g. threshold voltage, linear operating point) in the application with a time-dependent stress voltage $V(t)$. $\Delta P(t)$ denotes the change in a parameter due to a degradation process starting at $t = 0$ and the function $f(V)$ is a function describing the degradation dependent of the terminal voltages.

Empirical Hot Carrier Model

The time-dependent stress voltage approach is used for the modeling of the hot-carrier induced degradation implemented in the Infineon in-house SPICE circuit simulator (see Section 7.7.4). The degradation after HCS is independently considered as a change in the saturation current following a power-law with an exponential dependence on V_ds. Furthermore, an Arrhenius temperature dependence as well as an exponential dependence on the transistor length l_des are considered. The dependence on V_gs is empirically modeled by a $4th$-order polynomial $A(V_\mathrm{gs})$ for the V_gs dependence:

$$\frac{\Delta I_\mathrm{ds}}{I_\mathrm{ds,0}} \propto \left(\mathrm{e}^{-\frac{E_\mathrm{a}}{k_\mathrm{B}T} + \frac{a}{|V_\mathrm{ds}|} + \frac{b}{l_\mathrm{des}}} A(V_\mathrm{gs}) \right) t_\mathrm{str}^n \tag{4.6}$$

with the constants a and b describing the dependence on the drain voltage V_ds and device length l_des, respectively.

Empirical Modeling of Recovery

For waveforms with an approximately rectangular shape (see inverter in Fig. 3.2), empirical modeling approaches consider the recovery with a pre-factor α [159–161]. Mostly the recovery-factor α is used as a pre-factor to the power-law in (4.1) and is assumed to be linearly dependent on the duty cycle [159] with $\alpha \approx 0.4$ for a duty cycle of 50 % [162]. For digital signals with duty cycles

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close to 50 %, the empirical power-law model can be significantly improved by the introduction of α, but especially for duty cycles close to the boundaries 0 or 1, the assumed linear dependency of α on the duty cycle is not valid.

4.3 Physical Models

Despite tremendous research efforts there is still no consensus on the basic physics of NBTI. There are two mechanisms involved [26, 32]:

1. A *diffusion-limited process*, where a Si-H defect at the Si/SiO_2 interface is depassivated during stress forming a P_b center [32]. A hydrogen atom is released and forms a hydroxyl group with a neighboring oxygen atom and diffuses away. This leaves a positively charged oxygen vacancy behind.

2. A *reaction-limited process*, where hole trapping in pre-existing defects occurs with trapping and trap transformation through first-order processes [32].

Over the last decade, it has been under debate whether Si-H bond breaking is reaction-limited by the supply of H or rather diffusion-limited. Two different models are under debate: The reaction-diffusion (R-D) model, which holds that NBTI is a diffusion-limited process [136, 163], and the "Defect-Centric" model, which holds that the mechanism is rather reaction-limited [141, 164]. In the following, the two competing physical models are briefly presented, but the focus lies on the defect-centric model as the reaction-diffusion model is criticized for unphysical parameterization: R-D models postulate that hole trapping stops after 1 s, which is incorrect and the degradation of thin oxides as a diffusion-limited process (unphysical transfer rates [32]).

4.3.1 Reaction-Diffusion

Already in 1977, Jeppson and Svensson discussed several physical degradation mechanisms of NBTI was observed in large-area devices [165]. One discussed mechanism was mechanism one, therefore the later modified model is usually referred to as "reaction-diffusion" model. The mechanism was assumed to be mainly a diffusion-limited process [101, 153, 163, 166]. It has been argued that interface states, which are dangling bonds present at the Si/SiO_2 interface, are responsible for the threshold voltage shift and the power-law dependence of ΔV_{th} with stress time (with $n = 1/4$) can be explained by this model. During the fabrication process, interface states can be passivated by hydrogen (H) and form a Si-H bond. Within the R-D model, it is assumed that during stress this formation can capture a hole weakening the Si-H bond, which can cause a release of the H from the Si atom. The hydrogen is assumed to diffuse in the gate dielectric, leaving an unsaturated, electrically active bond behind. Furthermore, hydrogen atoms can passivate dangling Si bonds and neutralize the interface states.

After further investigation of NBTI, the fast recovery of NBTI over many decades in time has been observed, which led to an adaption of the R-D model: The one-dimensional hydrogen motion was replaced by a three-dimensional hydrogen distribution and diffusion. Furthermore, the diffusion of H and H_2 molecules and their inter-conversion has been considered [136, 167–171]. However, even with this extension, the criticism remains. The validity of the underlying physical interpretation is criticized [164] due to model parameters contradictory to established literature on hydrogen in Si/SiO_2 systems (e.g. diffusion length is in the range of micrometers for a nanometer-sized oxide) [32, 172, 173]. Moreover, a very small barrier is assumed for the recovery process which is inconsistent with forming gas anneal data. Besides, the model is based on elastic tunneling processes, which is in contradiction with the Arrhenius temperature dependence [141]. As such, lifetime simulations do not correctly cover degradation and recovery under the consideration of the complete stress history (requirement 1 and 2 not fulfilled). Meanwhile,

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the model is commercially available [171], but the computation time is too high for lifetime calculations and as such requirement 4) is not fulfilled either.

4.3.2 Defect-Centric Model

The defect-centric model is based on the discrete behavior of individual traps and focuses on hole capture and emission in bulk traps and border traps [164]. First, a *two-stage model* was developed [174]: Based on the initial work by Huard *et al.*, the recoverable component is described as charging and discharging of preexisting oxide defects. This is considered through first-order processes [50] and is described by the NMP theory [137, 175]. The quasi-permanent degradation is modeled phenomenologically with a simple double-well (DW) model [174]. The distributions of the parameters of these two models are then optimized to obtain one set of defects which gives consistent results for all experiments (TDDS as well as extended MSM experiments with different parameters). The trapping model parameters (trap levels and capture and emission times) show good agreement with the physical properties of calculations of atomistic defect configurations obtained by DFT calculations [134]. Later, this model has been refined to a *four-state NMP model*, motivated by observations at single defects with TDDS measurements [141] not consistent with two-state trapping kinetics. Finally, after further study of the quasi-permanent component, the *gate-sided hydrogen release model* was developed [48].

The Two-Stage NMP Model

In 2009, Grasser *et al.* suggested a two-stage model to explain the negative bias temperature instability based on the E' center as shown in Fig. 4.1. The model describes the defect creation via a two-stage process: In stage one, holes can be trapped into near-interfacial E' centers with two neutral and one positive state. The charge trapping is described by the NMP theory. In stage two, the increased hole concentration considerably enhances the creation of e.g. P_b centers at the Si/SiO_2 interface and K_N centers in oxynitrides. Thus unpassivated silicon dangling bonds are created, which are poorly recoverable defects [174]. The charging and discharging is modeled over a field-dependent barrier is thermally activated as described in Section 3.3.1. Each defect occupies either an electrically neutral or a positively charged state. Transitions between the two states occur with characteristic capture and emission times dependent on the stress and recovery bias and temperature as well as characteristic step height η visible in the measurement of V_{th} and I_{ds}. The mean value of the threshold voltage shift can be described as:

$$\Delta V_{th}(t) = \sum_k \eta_k \cdot (w_k(t) - w_k(t_o)) \tag{4.7}$$

with $w_k(t)$ the probability that defect k is charged at the time t. The step-height η_k is the contribution of the defect to the ΔV_{th}.

The total threshold voltage shift is given by the contributions of the interface and oxide defects as:

$$\Delta V_{th}(t) = -\frac{\Delta Q_{ox}(t) + \Delta Q_{it}(t)}{C_{ox}}. \tag{4.8}$$

with Q_{it} the charge of the interface states and Q_{ox} the charge of the oxide states. The microscopic model for ΔQ_{ox} is inspired by the Harry Diamond Laboratories (HDL) switching trap model for E' centers [176, 177]. Before, Tewksbury applied a two-state model to the threshold voltage shift of MOSFETs [178]. In this model, each defect has a capture and emission time constant and the densities of states and forward and backward transition probabilities are considered. In the first proposed two-stage model, the hole trapping of the near-interfacial E' is modeled within the NMP theory [137, 139] and three states of the E' center: Two neutral and one positive state as shown in Fig. 4.1 [179]. The microscopic model for ΔQ_{it} is based on Brower's simple

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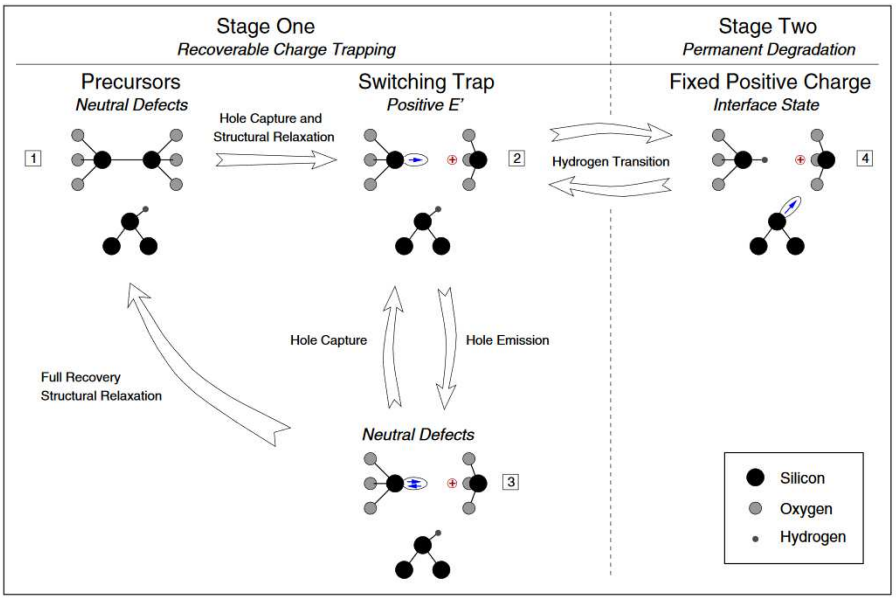

Figure 4.1: Schematic description of the two-stage model: The model for the switching oxide trap (stage 1) for the creation of a E' center is coupled with the creation of a dangling bond at the interface (stage 2) [174]. The E' center has three states which are modeled with NMP transitions and is considered to contribute to the recoverable component of BTI, whereas the interface states and fixed positive charges are assumed to contribute to the quasi-permanent component. From: [174]

thermal model considering rate-limited reactions for passivation and depassivation of P_b centers [180, 181]. The model is extended with a phenomenological field dependence (modification of the passivation and depassivation barriers) [179]. This two-stage model was the first model consistently describing hydrogen relocation for the quasi-permanent and recoverable component with NMP transitions.

The Four-State NMP Model

The extension of the first stage of the two-stage model was motivated by studies employing TDDS on pMOSFETs, which found spontaneously disappearing and reappearing defects. Furthermore, it has been found that single-trap emission times can be either bias-independent (fixed oxide traps) or show a strong bias-dependent emission time (switching traps) [92]. Further studies revealed frequency-dependent NBTI and anomalous RTN [182], which cannot be explained by the 2 or 3 states, respectively, within the two-stage model [141].

The four-state NMP model (see Fig. 4.2) is able to explain all these features: in principle, the model consists of two stable states 1 and 2, and two meta-stable states $1'$ and $2'$ [141]. The states $1/1'$ are neutral and $2/2'$ represent charged defects. Charge capture occurs via the transition from state 1 to state 2 via the meta-stable state $2'$. Hole emission proceeds from state 2 to state 1 via either state $1'$ (switching trap) or $2'$ (fixed oxide trap). The four-state NMP model describes the capture and emission time characteristics and its temperature- and bias-dependence via charge transfer reaction followed by thermal transitions via barriers according to the NMP theory. When a stress bias is applied at the gate, the trap level shifts with respect to the Fermi-level of the channel depending on their trap depth due to the electric field in the oxide. Dependent on the location of the trap with respect to the channel, the trap levels, and their barrier heights change. The closer the trap is located to the gate, the larger is the observed dependence of the capture time on the stress bias.

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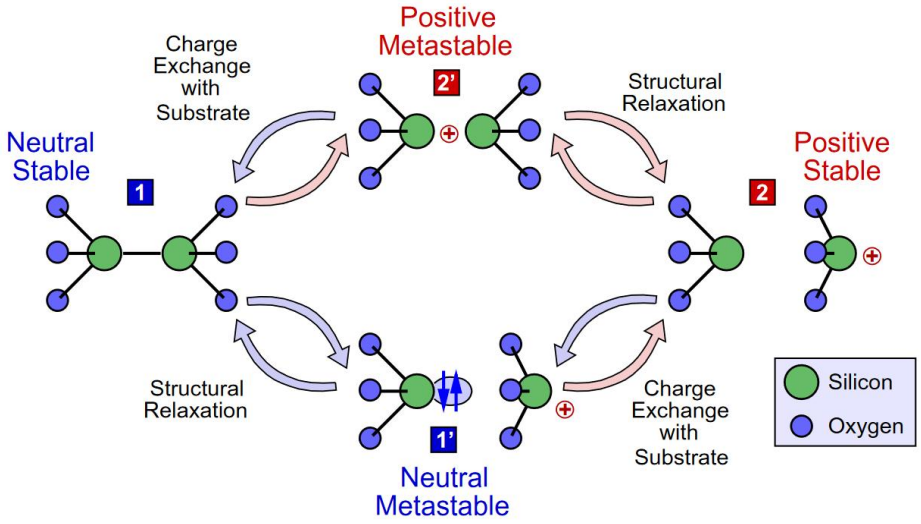

Figure 4.2: Schematic description of the four-state model: The four states of a switching trap exemplary shown for the E' center with its two stable states 1 and 2, and two meta-stable states $1'$ and $2'$. Initially, there is a neutral precursor (state 1). If a hole is captured, the Si-Si bond breaks and a positively charged E' center is created (state $2'$). From: [141]

Gate-Sided Hydrogen Release

The four-state NMP is limited to pre-existing oxide defects and couples the quasi-permanent component in stage two as a separate part of the two-stage model (see Section 4.3.2). Many studies indicated a mechanism for the quasi-permanent part coupled via hydrogen relocation, as hydrogen has been under discussion for a long time to be responsible for activating or creating defects or interface states under NBTI conditions [119, 130].

The gate-sided hydrogen release model has been developed based on long-time experiments (measurements of more than 8 months on a single device) and high-temperature studies [48, KWC3, 183]. The measurements revealed that, after bake at high temperatures (e.g. $T = 350°C$), additional defects are created. One possible mechanism leading to an increase in the quasi-permanent component according to the hydrogen release model is sketched in Fig. 4.3:

A hydrogen atom located at the gate site is trapped in a precursor state. If a gate potential is applied and the Fermi-level moves below the energy level of the trapped H^+, the hydrogen is neutralized. The neutralized hydrogen can now be released from the trapping site by passing a thermal barrier ($\approx 1.5\,eV$). Afterward, it diffuses through the oxide towards the channel, where it can occupy an empty H^+ trapping site (due to the amorphous structure of the SiO_2, these trapping sites are energetically above the channel Fermi-level and are available all over the oxide). As a consequence, an additional charge at the interface with very slow time constants is created and thus contributes to the quasi-permanent component.

The gate-sided hydrogen release model is based on the four-state NMP model extended by two mechanisms [48]:

1. The newly created defects form activated precursors due to additional thermally activated released hydrogen from a gate-sided hydrogen reservoir, which controls the total hydrogen concentration in the oxide. The hydrogen exchange between the different sites is modeled as a thermally activated hopping process with hopping rates.

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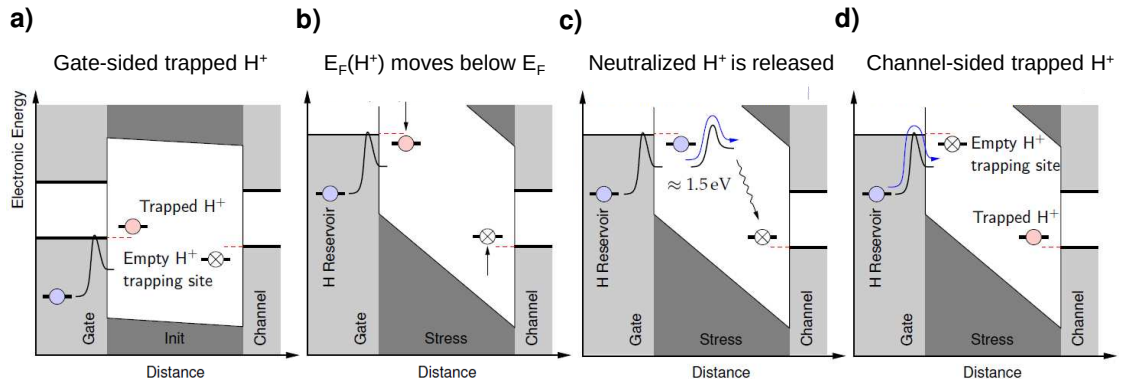

Figure 4.3: Schematic representation of the hydrogen release model with trapped H^+. **a)** Initially, there is a gate-sided trapped H^+, which is **b)** during stress below the Fermi-level and is **c)** neutralized and can be released by overcoming a thermal barrier and diffuses through the oxide and **d)** becomes trapped by a channel-sided precursor with its energy above the Fermi-level of the channel. Thus, at high temperatures additional H^+ can be released from the reservoir. From: [183]

2. The hydrogen is redistributed within the oxide: Hydrogen at a defect site can only be released in the neutral configuration (state 1 in the four-state NMP description) and can subsequently activate an energetically more favorable precursor.

The response of the system is determined by the thermal release of the trapped hydrogen which has to overcome barriers with widely distributed barrier heights. The process is reaction-limited. The gate-sided hydrogen release model is the most accurate model and able to describe all kinds of stress considering the complete stress history for each defect independently in a TCAD simulation. As such, it serves as a modeling benchmark.

4.4 Compact Models

The gate-sided hydrogen release model computes the electrical properties of the defects within the oxide requiring high computation power. Thus lifetime simulations of large circuits are too time-consuming. In this thesis, a compact model is developed and presented based on the capture and emission time map approach. The framework and the fundamentals of the capture and emission time maps are presented in the following. The extension of the model to fulfill all five requirements is presented in Chapter 6. Parallel to this work, two other compact models suitable for circuit simulations have been developed and are briefly presented: The defect sampling (DS) model by Giering *et al.* [52] and the compact-physics (comphy) model by Rzepa *et al.* [51].

4.4.1 The Capture and Emission Time Map

Key physics of BTI degradation can be captured with high accuracy through a more simplified model based on the gate-sided hydrogen release model: The capture and emission time map approach, which has been developed by Grasser in 2011. It is assumed that bias temperature instability can be understood in good approximation as the collective response of independent defects. TDDS studies reveal that each defect has a characteristic contribution to the overall threshold voltage shift as well as a capture and emission time constant [92]. These capture and emission time constants, or equivalently reaction rates, are widely distributed.

It has been shown by Grasser *et al.* that many of the experimentally observed features of BTI can be explained in a closed analytical form with bivariate Gaussian distributions describing capture and emission time maps of the defects [76]. The model can describe the long logarithmic-like recovery traces, the power-law time behavior, and the saturation for longer stress times as

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well as the differences and similarities between DC and digital AC stress. In this section, the fundamentals and approximations of the analytic capture and emission time map are described. Furthermore, the defect occupation probability after constant stress as well as digital AC stress is given.

From Individual Defects to Capture and Emission Time Maps

Charge capture and emission times of single defects are very sensitive to the applied bias and temperature. Independent of the physical model behind oxide and interface traps, they can in a good approximation be described with the same mathematical form of the two-state model (described in Section 3.3.1) with effective capture and emission times. This is an approximation of the four-state model of Section 4.3.2 (transitions between states 1 and 2′ in Fig. 4.2).

In the simple double-well model, the rates to overcome the barrier are [92, 141]

$$\tau_c = \tau_0 e^{\frac{E_c}{k_B T}} \text{ and } \tau_e = \tau_0 e^{\frac{E_e}{k_B T}}. \tag{4.9}$$

Proceeding from independent defects to defects of oxide and interface traps with widely distributed capture and emission time constants, so-called capture and emission time maps can be drawn: The number of defects contributing to the overall threshold voltage shift is obtained by summing up the contributions of all defects with a τ_c and τ_e combination weighted by the defect occupation probability O [92]:

$$\Delta V_{th}(t_{str}, t_{rec}) = \int_0^\infty \int_0^\infty O(\tau_c, \tau_e, t_{str}, t_{rec}) \cdot g(\tau_c, \tau_e) \, d\tau_e d\tau_c. \tag{4.10}$$

with g the density of defects with the dimension $\mathrm{V/s^2}$. O is the occupancy function depending on the device stress and recovery history. With $O = 0$ if the defect is uncharged and $O = 1$ is charged.

For constant stress, the ΔV_{th} is given by the sum of all defects charged until t_{str} and not yet discharged after t_{rec}.

Analytic Activation Energy Map Modeling

Capture and emission time maps can be extracted by numerical differentiation of a set of ΔV_{th} recovery curves via [92]:

$$g(\tau_c, \tau_e) \approx \frac{\partial^2 \Delta V_{th}(\tau_c, \tau_e)}{\partial \tau_c \partial \tau_e}. \tag{4.11}$$

The extracted CET map from experimental data is shown in Fig. 4.4. Although this approach is accurate for a single stress/recovery and temperature/voltage combination, it does not allow for lifetime extrapolation. The analytic CET map is a two-dimensional distribution which represents the contribution from distributed capture and emission time constants to the overall threshold voltage shift. The capture and emission time constants are reciprocally linked to first-order reactions for either charge trapping of defect creation as described in (4.9). An exemplary CET map is shown in Fig. 4.5.

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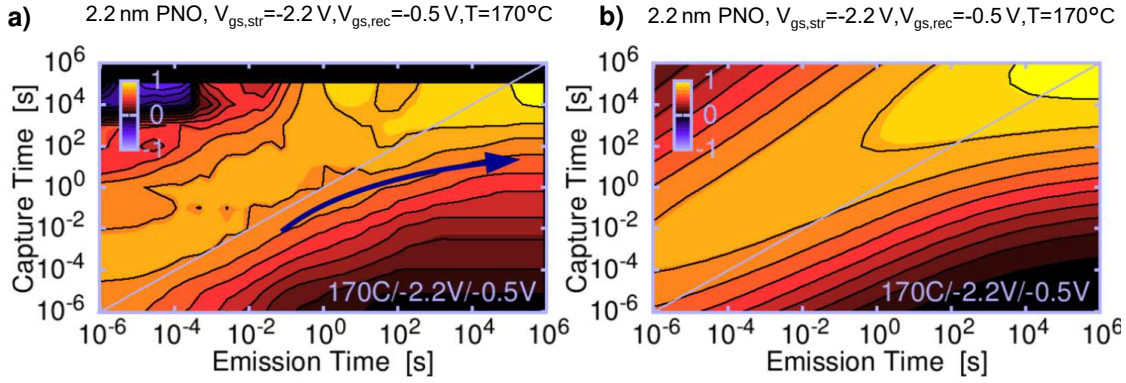

Figure 4.4: a) The CET map extracted from experimental data ($T = 170°C$, $V_{gs,str} = -2.2\,V$ and $V_{gs,rec} = -0.5\,V$) by numerically differentiation (logarithmic normalization). **b)** The analytic CET map fitted to the same MSM data containing all essential features. From: [76]

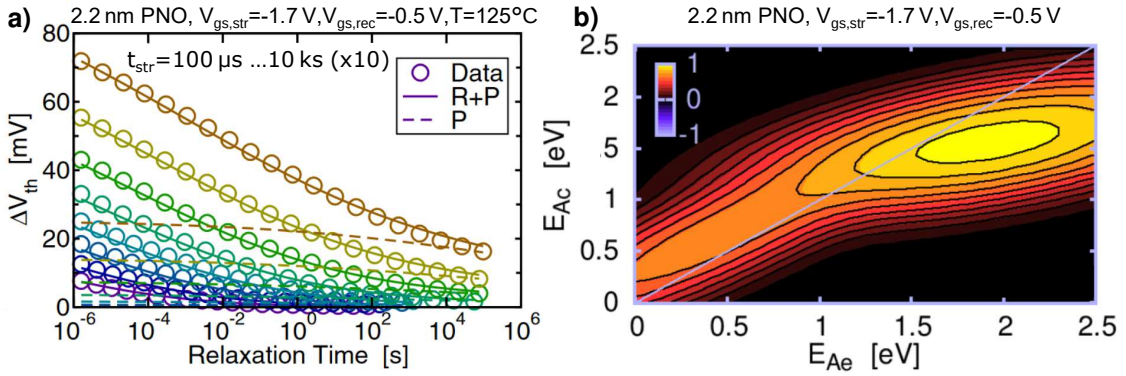

Figure 4.5: a) Comparison of the experimental recovery data (circles) at different stress times with the analytic model (lines) for a 2.2 nm PNO at $T = 125°C$. The solid lines are obtained from the activation energy map shown in **b)** with the dashed lines corresponding solely to the quasi-permanent component. From: [76]

The analytic model has the following properties [76]:

1. The BTI degradation is described by two contributions, the recoverable component R which dominates the recovery behavior, and the quasi-permanent component P, which typically does not recover within experimental time windows.

2. Gaussian distributions are used to model the capture and emission times because the power-law dependence is well captured by a Gaussian distribution as well as the slight saturation for long stress times [183].

3. Note that not the distribution of the capture and emission time constants themselves are modeled, but their corresponding activation energies. In Section 3.3.1, the properties of the temperature dependence are discussed. The capture and emission time constants have been found to be widely distributed following an Arrhenius equation [92, 94, 108–110]. The maps showing the capture and emission activation energies are therefore also called "activation energy maps". Thus, the CET maps are typically shown on logarithmic axes as the threshold voltage shift follows a power-law with stress time and shows a logarithmic recovery.

4. The characteristic temperature-independent time constant τ_0 is introduced. It has been shown that the time constants are uncorrelated with the depth of the defect in the oxide

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[184], which would otherwise determine the distribution of τ_0 via the Wentzel-Kramers-Brillouin (WKB) factor. Therefore, τ_0 is assumed to be not distributed and is a constant [145]. This results in a built-in temperature dependence - an activation energy map can be transformed with τ_0 into a capture-and-emission time map at any temperature: The capture and emission activation energies E_c and E_e are linked via the Arrhenius law (3.6) with $\tau_c(T)$ and $\tau_e(T)$.

5. The main model parameters are the mean values μ_c and μ_e of the capture and emission activation energies E_c and E_e, as well as the standard deviations σ_c and σ_e of the mean values, describing the position and width of the defect density distributions. As the emission times become larger with increasing capture times $E_e = E_c + \Delta E_e$, the mean of the emission times is described as $\mu_e = \mu_c + \mu_{\Delta e}$. As a consequence, R and P can be described as bivariate Gaussian distributions.

6. The amplitudes A_r, A_p give the maximum obtainable degradation if all defects are charged. The amplitudes strongly depend on the stress voltage as shown in Section 6.1.3.

The analytic model formulation by Grasser *et al.* for the charged trap density $g(E_c, E_e)$ for each component is given by [145]:

$$g(E_c, E_e) = \frac{A}{2\pi\sigma_c\sigma_{\Delta e}} \cdot \exp\Big(-\frac{(E_c-\mu_c)^2}{2{\sigma_c}^2} - \frac{(E_e-(E_c+\mu_{\Delta e}))^2}{2{\sigma_{\Delta e}}^2}\Big). \tag{4.12}$$

In the originally published model, the correlation coefficient is $\rho = \sigma_c/\sigma_e$ and is a consequence of the Ansatz for E_e and not a model parameter [145]. The total threshold voltage shift is then calculated following [76]:

$$\Delta V_{th}\left(t_{str}, t_{rec}\right) = \int_0^\infty \int_0^\infty O\left(E_c, E_e, t_{str}, t_{rec}\right) g\left(E_c, E_e\right) \, dE_e dE_c. \tag{4.13}$$

E_c, E_e are linked via the Arrhenius law (3.6) with τ_0 and T to t_{str}, t_{rec} and τ_c, τ_e. The analytic activation energy map is extracted by simultaneously optimizing the parameters of the analytic distribution in (4.12) to minimize the deviation from the ΔV_{th} measurements.

Occupation Probability

Whether a defect is charged or uncharged after the application of a stress or recovery bias depends on the stress history, the device has been exposed to. The occupation probability is the probability that the defect is either charged after the application of a stress bias or the defect is uncharged/neutral after the application of a recovery bias. The occupancy O after applying a DC stress or recovery bias for a stress time t_{str} and a recovery time t_{rec}, respectively, can be described by [76]

$$O(t_{str}, t_{rec}, \tau_c, \tau_e) = \left(1 - e^{-\frac{t_{str}}{\tau_c}}\right) e^{-\frac{t_{rec}}{\tau_e}}, \tag{4.14}$$

assuming that the defects have the occupancy $O(t_{str}, t_{rec}, \tau_c, \tau_e) = 0$ at time $t_{str} = 0$. For long stress times $t_{str} \gg \tau_c$, the occupancy is $O(t_{str}, t_{rec}, \tau_c, \tau_e) = 1$. In Fig. 4.6, the occupation probability maps for different DC stress cases are shown. In the following, the formula for the defect occupation probability of a digital AC stress pattern with one stress and one recovery pulse is derived. A charging pulse of length Δt_s is followed by a de-charging pulse Δt_r and the period time of the AC signal follows then as $\Delta T = \Delta t_s + \Delta t_r$.

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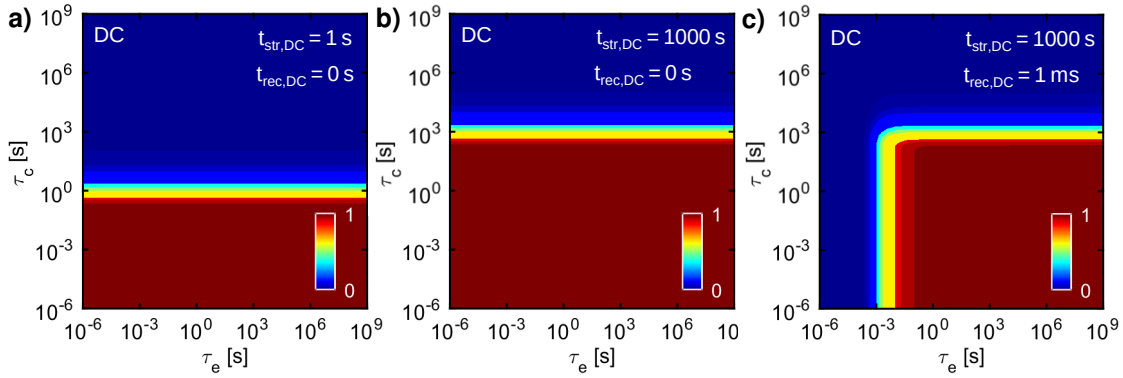

Figure 4.6: Defect occupation probability inside the CET map for DC stress with three different combinations of stress and recovery times. Occupation probability 1 corresponds to a charged defect and 0 to a neutral defect.

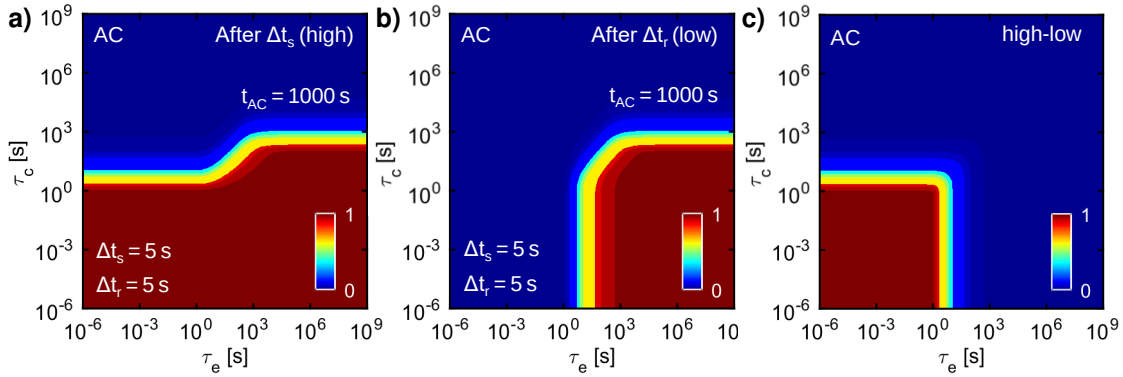

Figure 4.7: Defect occupation probability after digital AC stress with $t_{\mathrm{str}} = 10^3$ s $f = 0.1$ Hz **a)** after the end of the stress phase Δt_{s} and **b)** after the end of the recovery phase Δt_{r}. Occupation probability 1 corresponds to a charged defect and 0 to a neutral defect. **c)** Difference of the two cases shows which defects are constantly charged/uncharged during the AC stress.

After a charging pulse n (high phase H), the defect occupancy is

$$O_n(\Delta t_{\mathrm{s}}) = O_{\mathrm{H},n} = 1 - (1 - O_{\mathrm{L},n-1}) \cdot \mathrm{e}^{-\frac{\Delta t_{\mathrm{s}}}{\tau_{\mathrm{c}}}}. \tag{4.15}$$

After the following recovery pulse n (low phase L), the defect occupancy is

$$O_n(\Delta t_{\mathrm{r}}) = O_{\mathrm{L},n} = O_{\mathrm{H},n} \cdot \mathrm{e}^{-\frac{\Delta t_{\mathrm{r}}}{\tau_{\mathrm{e}}}}. \tag{4.16}$$

The abbreviations d and u for the time-independent factors are introduced for the up- and down-phases of the signal:

$$u = \mathrm{e}^{-\frac{\Delta t_{\mathrm{s}}}{\tau_{\mathrm{c}}}} \text{ and } d = \mathrm{e}^{-\frac{\Delta t_{\mathrm{r}}}{\tau_{\mathrm{e}}}} \tag{4.17}$$

and together with equations (4.15) and (4.16), a recursive equation can be given:

$$O_{\mathrm{L},n} = [1 - (1 - O_{\mathrm{L},n-1}) \cdot u]d \tag{4.18}$$

with $O_{\mathrm{L},0} = 0$. For $n = 1$,

$$O_{\mathrm{L},1} = d - ud \tag{4.19}$$

and for $n = 2$,

$$O_{\mathrm{L},2} = d - du + ud^2 - u^2d^2 = O_{\mathrm{L},1} + O_{\mathrm{L},1} \cdot ud \tag{4.20}$$

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is obtained. For each additional period, an additional term is added, the results after N periods of stress can be given as:

$$\begin{aligned} O_{\mathrm{L},N} &= \sum_{n=1}^{N} (d - ud) \cdot (ud)^{n-1} \\ &= (1 - ud^N) \cdot \frac{d - ud}{1 - ud} \end{aligned} \tag{4.21}$$

and for the end after the high pulse:

$$O_{\mathrm{H},N} = (1 - ud^N) \cdot \frac{1 - u}{1 - ud}. \tag{4.22}$$

The number of periods N are replaced by the AC stress time, which gives:

$$t_{\mathrm{AC}} = N \cdot \Delta T \tag{4.23}$$

and the AC charging time constant $\bar{\tau}$ is introduced as:

$$\frac{1}{\bar{\tau}} = \frac{\Delta t_{\mathrm{str}}}{\Delta T \cdot \tau_{\mathrm{c}}} + \frac{\Delta t_{\mathrm{rec}}}{\Delta T \cdot \tau_{\mathrm{e}}}. \tag{4.24}$$

The result for the occupancy after the recovery phase is obtained by inserting (4.23) and (4.24) in (4.21):

$$O_{\mathrm{L}}(t_{\mathrm{AC}}) = (1 - \mathrm{e}^{-\frac{t_{\mathrm{AC}}}{\bar{\tau}}}) \cdot \frac{d - ud}{1 - ud} \tag{4.25}$$

and equivalently for the stress phase:

$$O_{\mathrm{H}}(t_{\mathrm{AC}} - \Delta t_{\mathrm{r}}) = (1 - \mathrm{e}^{-\frac{t_{\mathrm{AC}}}{\bar{\tau}}}) \cdot \frac{1 - u}{1 - ud}. \tag{4.26}$$

In Fig. 4.7, the occupation probability maps for different AC stress cases are shown. It correctly covers degradation as well as recovery with a high accuracy and is able to simulate digital AC stress. However, the presented CET map model is not suitable for circuit simulations as it is in the presented form not suitable to simulate arbitrary stress stimuli (requirement 4 not fulfilled) and requires an extension which is developed within this thesis and presented and described in detail in Section 6.

4.4.2 Defect Sampling Model

The defect sampling model is based on the two-stage model described in Section 4.3.2, and employs a database with defect properties obtained from the TCAD analysis of experimental NBTI data. The TCAD-generated database samples the dependence of the capture and emission time constants on the stress voltage and temperature for e.g. $\sim 10^4$ defects. For the application for analog circuit simulations, the differential equation of the Markov model is efficiently solved for periodic stress patterns with a numerical solution [147, 185, 186]. For each defect, the differential equation governing the time evolution of the occupation probability w_k follows directly from (4.7) as

$$\dot{w}(t) = a(t)w(t) + b(t) \tag{4.27}$$

with $w(t_0) = w_0$ and

$$a(t) = -{\tau_{\mathrm{e}}}^{-1}(t) - {\tau_{\mathrm{c}}}^{-1}(t) \quad \text{and} \quad b(t) = -{\tau_{\mathrm{c}}}^{-1}(t) \tag{4.28}$$

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is solved using a numerically efficient algorithm [147]. The coefficients depend on the stress pattern $t \rightarrow V_{gs}(t)$ and are time-dependent. The model features a closed-form calculation of each defect and efficiently solves the differential equation, and is therefore well-suited for circuit simulations [KWJ4]. The model efficiently calculates stress patterns with nested periodicities on different time scales corresponding to, e.g., different IC power states, day-night cycles, and mission profile requirements [187].

4.4.3 Comphy

The compact-physics framework, short "Comphy", has been developed by TU Wien and imec and is a free open source software providing detailed physical oxide defect models [51]. The model is based on a description of the gate stack and channel properties as shown in Fig. 4.8.

The complex multi-state NMP model (see Section 4.3.2) is abstracted to an effective two-state model [140] for the recoverable component, and a simple double-well model is used to describe the quasi-permanent component [51]. The abstraction to a two-state model implies a loss in accuracy which affects the switching behavior of individual defects e.g. the frequency dependence (similar as for the CET and the defect-sampling approach).

The mean degradation is computed in a deterministic fashion and the variability by Monte Carlo sampling of individual defects [140]. Comphy features an AC mode to simulate the high-frequency long-term digital AC signals and can be applied for NBTI, PBTI, lifetime extrapolation as well as for gate stack engineering [188]. For arbitrary stress, a similar approach as for the defect-sampling model is used. The software is open source, but no implementation in a commercial circuit simulator has yet been presented.

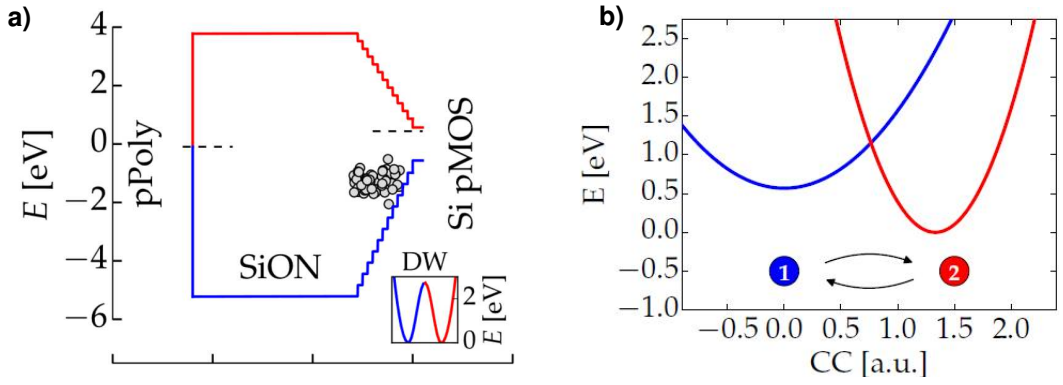

Figure 4.8: a) Comphy-calibrated band diagram of a pMOSFET at flat band conditions including the two-state NMP defects (circles). **inset)** Configuration coordinate diagram of the double-well mode for the quasi-permanent defects. From: [51]. **b)** Configuration coordinate diagram of a single defect described by the two-state NMP model within Comphy. From: [140]

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4.5 Discussion on the Suitability of the Models for Circuit Simulations

Empirical, physical as well as compact models for BTI have been described based on current literature. In the following, the suitability of the presented models for commercial circuit simulations is discussed. The requirements have been defined in Section 4.1, the properties of selected models are compared in Table 4.1.

The main advantage of empirical models is that the experimental and implementation effort as well as the computation time is low. As such requirements 4) and 5) are fulfilled. Digital stress patterns could be simulated with empirical models, but the model accuracy for analog stress signals is insufficient (requirements 1-3) not fulfilled). Empirical models are therefore not suitable for accurate circuit simulations.

Two physical models have been presented - the R-D model and the defect-centric gate-sided hydrogen release model. The R-D model is based on parameters contradictory to established literature on hydrogen in Si/SiO_2 systems [32, 172, 173], therefore this model is not considered for circuit simulations. The gate-sided hydrogen release model offers a fundamental physical simulation and is the most accurate model. Any $V_{gs}(t)$ pattern can be simulated, but the computation time depends on the stress time and is therefore too high for lifetime calculations on the circuit level.

Based on the gate-sided hydrogen release model, essential physics of BTI degradation can be captured with high accuracy through more simplified models: Three state-of-the-art compact models have been presented and their properties are compared in Table 4.1. The defect sampling (DS) model by Giering *et al.* and the compact-physics (comphy) model by Rzepa *et al.* fulfill the first four requirements. Both compact models are based on a defect database, which has to be generated from TCAD simulations. Nonetheless, the measurements required to generate the defect database are very time-consuming. Also, the implementation effort into a commercial circuit simulator is too high.

The presented CET map framework is promising for circuit simulations. A huge advantage is that the parameterization from the measurements can be standardized offering a fast adaption of the model for other technologies with an efficient integration into industrial circuit simulators. But, the model does not fulfill all requirements yet as it is restricted to DC or digital AC stress. Therefore, one goal of this thesis was to extend the model to fulfill all requirements and to demonstrate integration in a commercial circuit simulator. The results are presented in Chapter 6. In addition, to reduce the experimental effort, the TA-MSM technique is developed and presented in Section 5.2.2. The technique could be used for the parameterization of the other models, too.

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Table 4.1: Comparison of compact models: Defect sampling, Comphy, CET and this work to the TCAD reference (gate-sided hydrogen release model). In the simulation effort column, the example time corresponds to calculating 100 ks (or any desired lifetime) of arbitrary analog stress (such as sine stress) on a single-core hardware.

Model	base	defect states	number of parameters	experimental effort [time/FET]	simulation effort [time/FET]	feasible V_{gs} pattern/ stress times	NBTI variability	V_{ds} dep.	freq. dep.[a]	advantages	disadvantages
TCAD	10^4 indiv. defects	4	24	TDDS+ eMSM [1000h]	too high stress time dep.	any/ small	yes	yes	yes	fundamental physical simulation	stress time dep. simulation time
Defect sampling	10^4 indiv. defects	2	24 (via10^4 defects)	TDDS+ eMSM [1000h]	closed form for each defect [10 ms]	periodic nested periods/ any	yes	no	no	low comp. time/ variability/ nested periods	based on defect database
Comphy	10^4 indiv. defects	2	21	TDDS+ eMSM [1000h]	closed form for each defect [10 ms][b]	periodic nested periods/ any	yes	no	yes[c]	gate stack proccess optim./ low comp. time/ variability/ nested periods	based on defect database
CET	CET maps	2	12	eMSM [500h]	closed form for one V_{gs} [10 ms]	DC digital AC[d]	yes[e]	no	no	low comp. time/ fast para-meterization/ feasible	No arbitrary stress
This work	V_{gs} dep. AE maps	2	20	TA-MSM [50h]	closed form [10 ms]	periodic/ any	possible[f]	possible[g]	possible[h]	low comp. time fast para-meterization/ feasible	No 4 – *state* features, no gate-sided hydrogen release

[a] The frequency dependence is directly correlated with the number of defect states.
[b] Comphy applies the mathematical approach to calculate the response of the defects to an arbitrary stress pattern as the defect sampling model. Additionally an initial step is required to determine the time constants of the single defects
[c] An approximation of the frequency dependence is implemented.
[d] Only 2 voltages for stress and recovery possible: V_h and V_l of the digital AC stress
[e] The variability is a possible add-on to the CET map approach but has yet not been demonstrated
[f] Consideration of variability is no goal of this thesis, but a similar approach as for the defect sampling model could be implemented.
[g] Consideration of the V_{ds} dependence is no goal of this thesis, but implementation is a feasible add-on.
[h] The same approximation for the frequency dependence as employed for the Comphy model is a possible add-on for all 2-state models

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Part II

Bias temperature Instability in Si MOSFETs

Chapter 5

Measurement Setup and Experimental Techniques for Si MOSFETs

In this chapter, the measurement setup and the measurement techniques for the characterization of BTI of silicon-based MOSFETs are presented. First, the characterization measurement equipment used in this work is described. Second, the ultra-fast measurement equipment V_{th} measurement of logic silicon-based MOSFETs is introduced. Third, the devices under test are described and the measurement setup used to study BTI is presented. Furthermore, the TA-MSM technique to accelerate BTI via temperature is introduced (developed within this thesis). Fourth, the setup for application-relevant AC and analog stress measurements is presented. The chapter concludes with the description of ring oscillator circuit measurements.

5.1 Measurement Equipment

In this section, the two types of measurement equipment that have been used for the parameter extraction are presented - the standard industrial measurement equipment and the ultra-fast measurement equipment developed by Reisinger [58].

5.1.1 Standard Industrial Measurement Equipment

All initial $I_{\text{ds}}V_{\text{gs}}$-curve characterization measurements as well as the HCS, and circuit measurements were performed with standard lab equipment. It consists of a control PC with a LabVIEW measurement software, an HP-E5250A switching matrix, an HP-4155C analyzer, with four source measurement units (SMUs) and two voltage measure units.

All BTI measurements have been performed on package level and the setups are described in Section 5.2. The ring oscillator measurements have been performed on wafer level using an Ultracision 880e semi-automatic 200 mm probe station. The test module is contacted with a probe card with 25 copper-beryllium needles. The hot chuck of the probe station is controlled by a Temptronic ThermoChuck controller with maximum temperature $T = 150°\text{C}$.

5.1.2 Ultra-Fast Measurement Equipment

On the one hand, commercial instruments provide good accuracy and stability. On the other hand, the application of complex and fast stress and measure patterns is mostly prevented by the commercial firmware. Therefore, for accurate and precise timing of all applied voltages, a home-made instrument designed to fulfill all requirements for Si characterization is used. The ultra-fast

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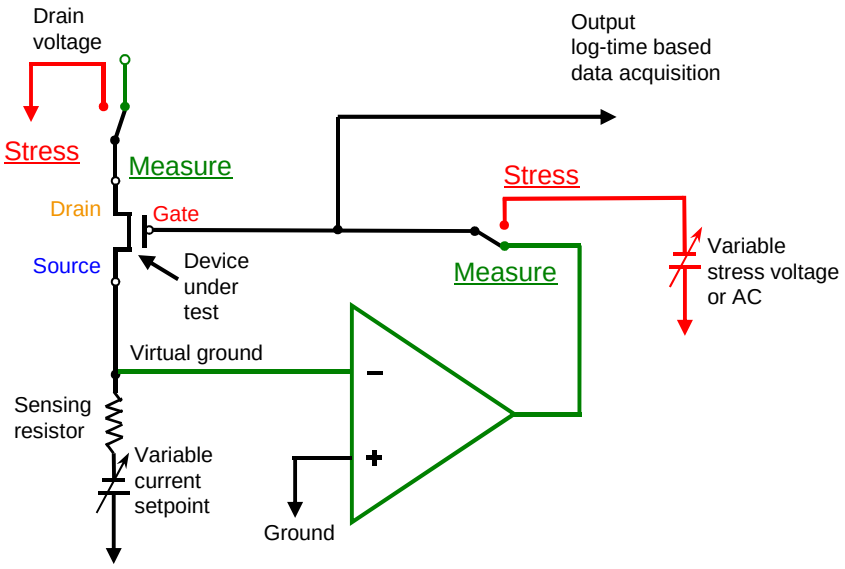

Figure 5.1: Ultra-fast measurement setup allowing to apply gate stress and to measure the threshold voltage. If the switch is positioned at "stress", the set stress voltage is applied to the gate of the device under test. If the switch is positioned at "measure", the amplifier in the feedback loop forces a constant current across source-drain. The achievable settling time of the gate voltage to V_{th} is $t_d = 1\,\mu s$. The setup is published in [58].

measurement equipment used throughout this work for Si-based MOSFETs BTI measurements has been proposed and developed by Reisinger in 2006 [58, 84].

The simplified setup diagram is shown in Fig. 5.1. A feedback loop is used to force a constant current across the source-drain of the device under test [58]. The operational amplifier minimizes the difference between the actual induced current and the variable current set-point (typically $I_0 \cdot w_{des}/l_{des}$) and applies the appropriate gate voltage to the device under test. The settled gate voltage V_{th} is recorded and the settling time after stress of the feedback loop is about 1 µs [84]. Thus a measurement delay between stress and V_{th} measurement of 1 µs is achieved.

5.2 Measurement Setup

In this section, the measurement setup used to study BTI of the silicon-based MOSFETs is presented and the Si devices under test are described. Within this thesis, a special measurement technique to accelerate BTI via temperature has been developed. The TA-MSM technique is an extension to the MSM technique. Since the TA-MSM technique requires special temperature control of the setup, the temperature dependency and measurement accuracy are studied in detail. For the verification of the developed model within this thesis, special AC stress measurement setups are needed. These application-relevant AC and analog stress measurement techniques are presented using an arbitrary waveform generator as well as ring oscillator circuits.

5.2.1 Devices Under Test

All measurements of silicon-based MOSFETs presented in this work were performed on a 130 nm power technology from Infineon Technologies AG [189]. The investigated device under test (DUT) are MOSFETs with a length $l_{des} = 120\,nm$, a width $w_{des} = 10\,\mu m$ and a 2.2 nm plasma nitrided gate oxide with 5 % nitrogen. The schematic cross section is shown in Fig. 5.2.

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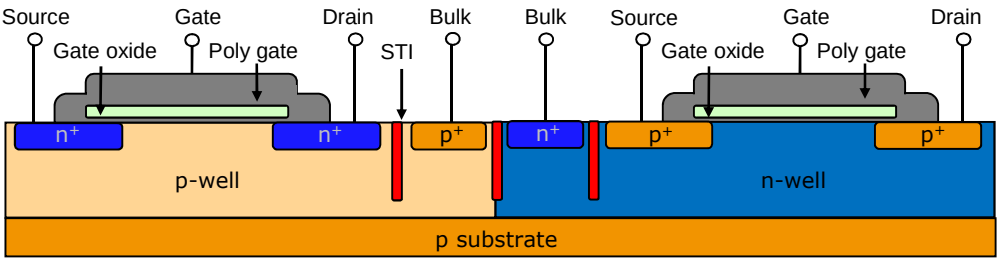

Figure 5.2: Schematic cross-section of the Si nMOSFET and pMOSFET with a SiON gate dielectric of the smart power technology under investigation.

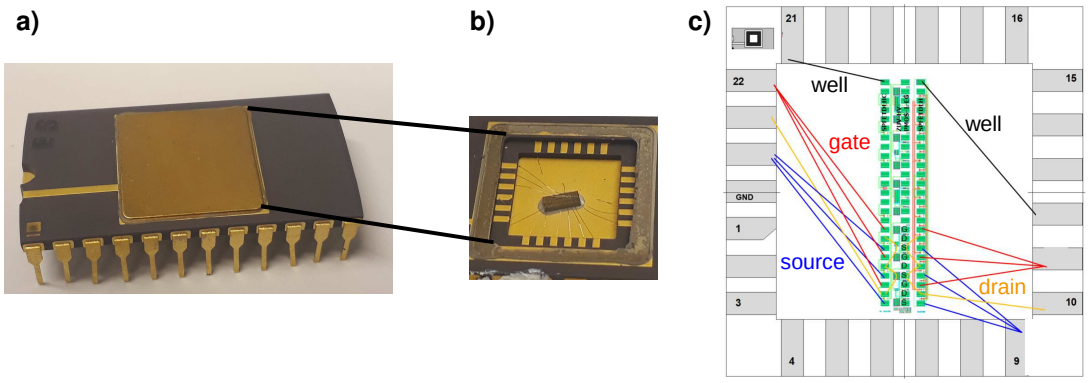

Figure 5.3: Sample and bonding information: **a)** Packaged sample for BTI measurements, **b)** Gold bond wires in package, **c)** Bond plan suitable for the TA-MSM measurements in the mini-oven.

For the BTI measurements, pMOSFETs are used, because negligible PBTI for nMOSFETs is observed for this technology. The test structures are positioned and bonded in C-Dip-24 packages as shown in Fig. 5.3 a-b). To reduce the noise, three pMOSFETs of the same type are connected together in parallel, meaning that the gates, sources, and drains of the three transistors are connected to one pin of the package (see bonding plan in Fig. 5.3 c).

5.2.2 Temperature Accelerated Measure Stress Measure Technique[1]

To enable MOSFETs lifetime extrapolation of up to 10 years, BTI is commonly accelerated via increased stress voltage and increased temperature [KWC2]. Acceleration of the degradation with stress voltage, as discussed in Section 3.3.1, decreases the capture time constants. Also, the number of active traps increases. As such degradation acceleration with the stress voltage does not correspond to an acceleration in time. On the contrary, degradation acceleration via temperature does not create new defects if the temperature is below $T = 250°C$ (compare discussion in Section 6.3). Therefore, temperature acceleration is the method of choice.

In this chapter, a new measurement technique, the TA-MSM technique, is presented. This measurement technique enables modeling of BTI without extrapolation. Capture and emission time constants at use temperatures ($T \leq 100°C$) of up to 10 years are determined [KWC2] as sketched in Fig. 5.4. The capture and emission time constants of BTI are widely distributed and the investigation of the physical mechanisms of BTI requires stress and recovery times over several decades in time [50, 190]. The shortest stress and the shortest recovery time as well

[1]The TA-MSM measurement technique has been introduced by the author of this thesis in [KWC2].

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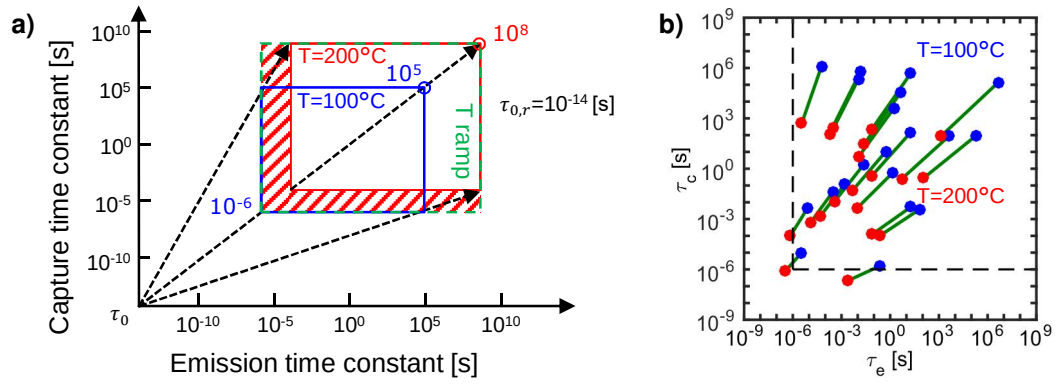

Figure 5.4: Arrhenius temperature activation: Schematic illustration of the experimental windows at different temperatures with a reference temperature of $T = 100°C$. All time constants are shown equivalent to $T_{ref} = 100°C$ and are calculated with $\tau_0 = 10^{-14}$ s. Experimental window with stress and recovery times up to 10^5 s at $T = 100°C$ (blue) and at $T = 200°C$ (red). The capture and emission time constants of the measurement window at $T = 200°C$ are shifted to up to equivalent 10 years at $T_{ref} = 100°C$. With a limiting measurement delay of $t_d = 1\,\mu s$, the shortest equivalent measurable emission time constant at $T = 200°C$ is $t_d(T_{ref} = 100°C) = 0.1$ ms. Therefore, the red dashed area indicates the capture and emission time constants that are not covered when measuring at $T = 200°C$. The new measurement technique overcomes this drawback and covers equivalent capture and emission time constants of 1 µs to up to 10 years (joint experimental windows of $T = 100°C$ and $T = 200°C$). **b)** Exemplary capture and emission time constants at $T = 100°C$ and corresponding decreased capture and emission time constants at $T = 200°C$ calculated with $\tau_0 = 10^{-14}$ s.

as the longest stress and the longest recovery time determine the experimental window. The experimental window is limited by the measurement time available and the measurement delay introduced by the measurement equipment (for all TA-MSM measurements, the measurement delay is $t_d \approx 1\,\mu s$). Commonly, for standard industrial applications, a lifetime of 10 years is required. In an industrial qualification measurement, BTI is accelerated via increased stress voltages. In addition, a time extrapolation is used, which is only suitable for worst-case lifetime estimation. The goal of the TA-MSM technique is to extend the experimental time window of degradation and recovery to more than 10 years without requiring voltage acceleration and time extrapolation.

The TA-MSM technique uses the fact that capture and emission time constant decrease with increasing temperature and shift into the experimental window as shown by Pobegen [90]. Thus, following the Arrhenius law Eq. 3.6, the change in defect time constant τ_1 to τ_2 when changing the temperature from T_1 to T_2 is:

$$\tau_2 = \tau_0 \left(\frac{\tau_1}{\tau_0}\right)^{\frac{T_1}{T_2}}; \quad \frac{\log(\tau_1/\tau_0)}{\log(\tau_2/\tau_0)} = \frac{T_2}{T_1}. \tag{5.1}$$

After the determination of τ_0, data recorded at a temperature T_1 can be calculated as a function of the time equivalent to a temperature, in the following referred to as temperature-time $\theta(T)$ [90]. To enlarge the equivalent measurement window in Fig. 5.4 a), simply increasing the temperature would accelerate both degradation and recovery. The experimental window in Fig. 5.4 would shift to longer capture as well as longer emission time constants. Thus, information about defects with short capture and emission time constants would be lost and would move out of the experimental window (e.g. shorter than 0.1 ms at $T = 100°C$, see dashed red area where the defects recover within the measurement delay). A schematic illustration for the temperature acceleration of the capture and emission time constants of the defects is given in Fig. 5.4 b).

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Experimental Setup

The electrical measurements were performed with the ultra-fast MSM technique as described in [58] and Section 5.1.2. To achieve an acceleration of the recovery and the ability to measure the capture and emission of defects with short emission times, a small electric oven has been constructed to perform temperature ramps. A cross-section and picture of the electric oven is shown in Fig. 5.5. The overall TA-MSM measurement setup is sketched in Fig. 5.6.

The packaged device is positioned between two aluminum half-shells within the thermal insulation of the oven. The pins of the package are contacted with gold needles. To prevent electrical shorts, the needles are placed in 1 mm thick glass tubes through a small cut-out of the housing of the oven. The heating of the oven is controlled via two resistive heaters located on the lower and upper aluminum half-shell. Cooling is performed with cold air provided by a Ranque-Hilsch vortex tube: Pressured air flows controlled by a valve inside the vortex tube, and separates the compressed air into a hot and cold stream [191]. In our measurement setup, the achieved cold stream has a temperature of about $T = 5°C$ and thereby provides faster cooling than what is achievable with air at room temperature. The oven contains a cut-out for the tube introducing the cold air in the oven, as well as a recess to channel the cold air through the oven to another cut-out where the then heated air escapes. The valve and the voltage of the resistive heaters is regulated by a proportional–integral–derivative (PID) controller and the temperature is measured by PT1000 temperature sensors. The computer simultaneously controls the measurement equipment and the controller to provide optimal synchronization of device stress and recovery with the device temperature.

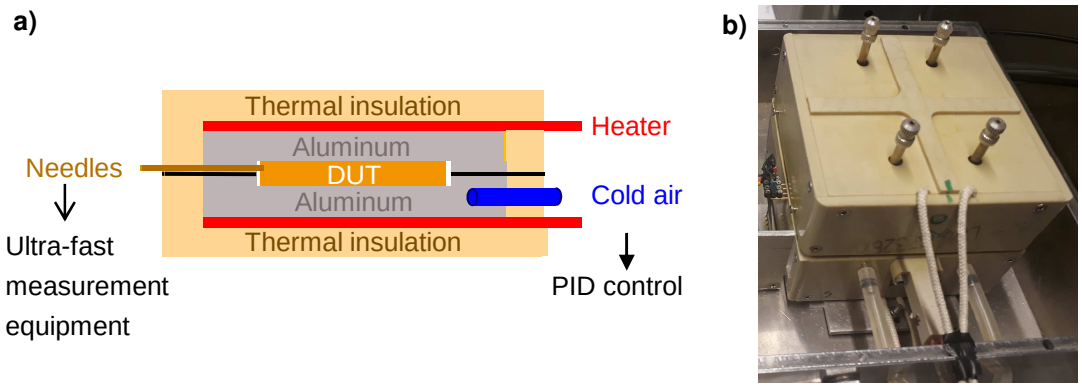

Figure 5.5: Cross-section and picture of the electric oven. The packaged DUT is positioned within two aluminum half-shells and contacted via needles placed within tiny glass tubes to prevent electrical contact with the aluminum half-shells. The DUT is heated via two resistive heaters and cooled down with cold air.

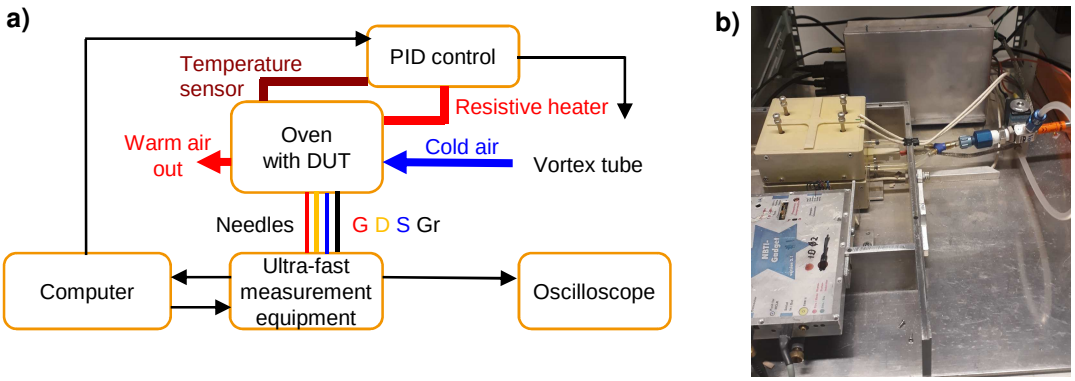

Figure 5.6: a) Schematic and **b)** picture of the TA-MSM measurement setup.

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Measurement scheme

The temperature-accelerated measurement scheme is illustrated in Fig. 5.7. It contains three different patterns (dependent on the stress time) and has been developed to extend the experimental time window of degradation and recovery of 1 µs to more than 10 years with the application of temperature ramps as presented in [KWC2]:

(a) For short stress times (below 1 ms), both the stress temperature T_{str} and the recovery temperature T_{rec} remain constant (e.g. at $T_{ref} = 100°C$, the reference temperature).

(b) For medium stress times (below 10 ks) $T_{rec} = T_{str}$. After 1 ks, T_{rec} is linearly increased by 100 K within 1 ks. Right before the next stress-recovery sequence, the sample is cooled down (not drawn) to the reference temperature.

(c) To reduce the total stress time, T_{str} is also increased. After stress, the temperature is decreased to the reference temperature while keeping the stress voltage applied to prevent recovery during cool-down. As soon as the reference temperature is reached, the same recovery temperature pattern is applied as described for the medium stress times.

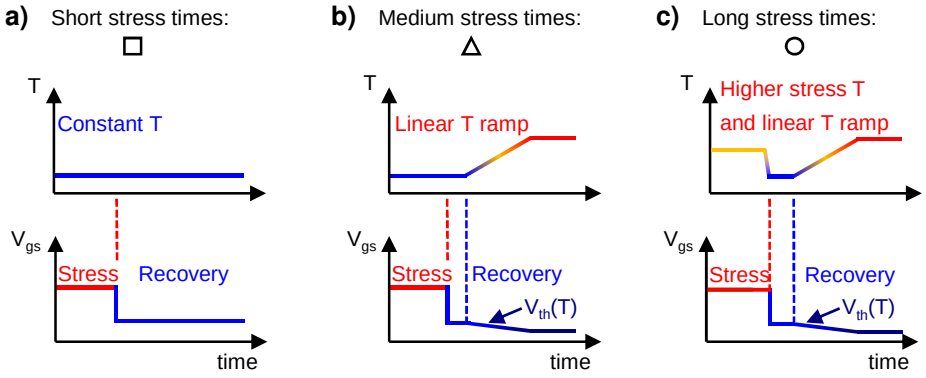

Figure 5.7: TA-MSM measurement scheme: **a) Short stress times:** Constant $T_{str} = T_{rec}$ **b) Medium stress times:** For the first 1 ks the T_{rec} = const and is subsequently linearly increased by 100 K within 1 ks. V_{th} is a function of temperature and decreases during the temperature ramp. Right before the next stress sequence, the sample is cooled down to T_{str}. **c) Long stress times:** Increased T_{str}. After stress, the temperature is decreased to T_{rec} while keeping the stress voltage applied. The measurement scheme for the recovery is the same as for medium stress times. During the up-ramps the V_{th} itself decreases with temperature following (5.2). In Section 5.2.2, the squares, triangles, and circles indicate, which measurement sequence has been applied.

Temperature Ramps

A major part of the accelerated recovery actually occurs during the temperature up-ramps after stress. The effect of the temperature ramp on single defects with five different emission activation energies E_e is illustrated in Fig. 5.8 a). In this example, charge emission of defects with $E_e \leq 1$ eV occurs before the temperature increases the defect state changes from 1 to 0 within seconds. These defects are not affected by the temperature ramp, whereas charge emission of defects with $E_e = 1$ eV and $E_e = 1.25$ eV is accelerated within the temperature ramp (see difference solid/dashed lines). Besides, defects with $E_e \geq 1.25$ eV recover only after keeping the temperature for a long time at $T = 200°C$.

The collective recovery of defects with distributed emission activation energies according to the activation energy map is simulated with and without the temperature ramp in Fig. 5.8 b). In this example, within the first 1 ks the ΔV_{th} decreased by 24 mV, due to recovery of defects with

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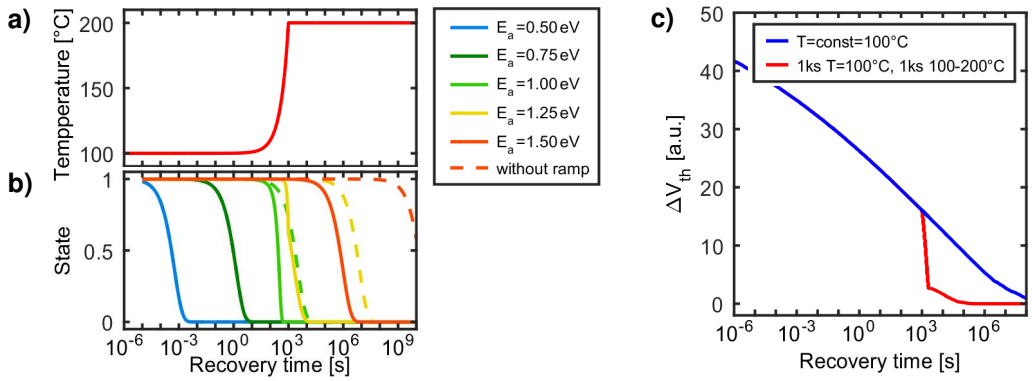

Figure 5.8: Effect of a temperature ramp on the recovery, exemplary calculation with $\tau_0 = 10^{-10}$ s. **a)** Linear temperature ramp within 1 ks from $T = 100 - 200°C$. **b)** Change of the charging state of 5 single defects with different emission activation energies with and without the temperature ramp (solid/dashed lines). Defects with emission activation energies below 1 eV are not affected by the temperature ramp, because charge emission already occurred before the significant temperature increase. Charge emission of defects with $E_e = 1$ eV and $E_e = 1.25$ eV is accelerated within the temperature ramp, whereas defects with $E_e \geq 1.25$ eV are uncharged by keeping the temperature constant at $T = 200°C$. **c)** Simulated collective defect behavior, recovery of V_{th} at $T = const = 100°C$ (blue). Red: After 1 ks, the temperature is linearly increased to $T = 200°C$ (TA-MSM scheme as shown in Fig. 5.7 b). During the temperature ramp, the recovery is accelerated by more than 4 decades in time.

emission time constants below 1 ks at $T = 100°C$. But, due to the broad distribution of emission time constants, the recovery of the remaining 18 mV takes more than 10^8 s without a temperature increase.

An acceleration of the recovery by more than four decades in time is achieved if the temperature is increased within 1 ks from $T = 100 - 200°C$ and afterward kept constant at $T = 200°C$ (as described in Fig. 5.7 b). Thus, already after less than 10^5 s, full recovery is observed.

Since V_{th} itself is a function of the temperature [192] it decreases during the up-ramps. To obtain the temperature dependence of the threshold voltage, the threshold voltage is measured for different constant temperatures after equilibrium is reached. As shown in Fig. 5.10 a), the temperature dependence of the threshold voltage approximately follows:

$$V_{th}(T) = -1.03\frac{\text{mV}}{\text{K}} \cdot T + 399.5\,\text{mV}. \tag{5.2}$$

The obtained value for the slope differs from device to device and varies in the range $-1 \pm 0.05\text{mV/K}$, which is in agreement with literature values for this oxide thickness and doping level [193]. Therefore, at first, a pre-stress temperature ramp is needed to calculate the difference between the reference and a recovery trace after stress. Such reference traces are shown in Fig. 5.9 for four consecutive ramps. The actual junction temperature and thus the measured threshold voltage of the transistor follows the preset temperature ramp because a good thermal conductivity between the oven and the packaged sample is achieved adding a heat-conductive paste.

The reproducibility of the temperature during the up-ramps is $\Delta T = \pm 0.1$ K, thus with (5.2) the accuracy of the ΔV_{th} due to temperature changes is a factor of 10 below the measurement resolution of $\Delta V = \pm 0.1$ mV. As seen in Fig. 5.9 c), the threshold voltage is stable after 100 s after the end of the ramp. Only an additional increase of 0.2 mV is observed with a proceeding number of temperature ramps. This is negligible compared to the overall threshold voltage shift during stress, but might be due to the additional creation of defects for high temperatures as discussed by Grasser in [183].

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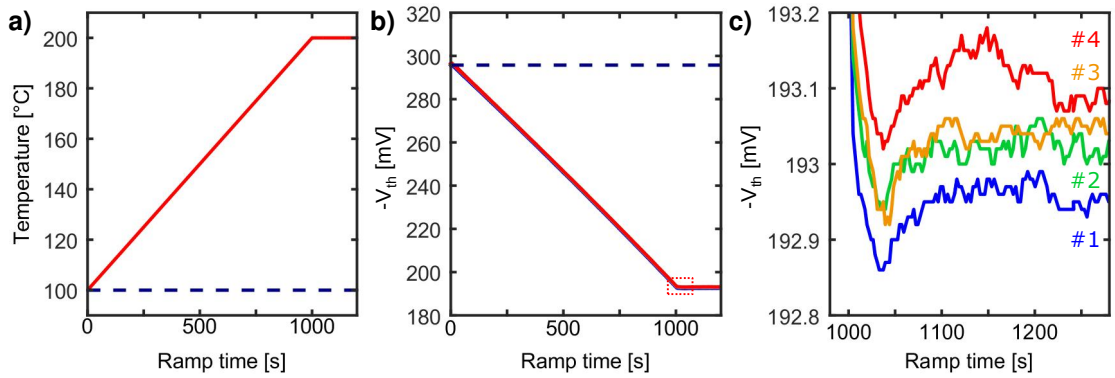

Figure 5.9: **a)** Measured mini-oven temperature during the temperature ramp. **b)** Dependence of the threshold voltage during the temperature ramp. Four reference temperature ramps are recorded before each stress measurement. The ΔV_{th} without the $V_{\mathrm{th},0}(T)$ is calculated by subtracting $V_{\mathrm{th},0}(T)$ from the after-stress V_{th}. **c)** Zoom in of b) to show the threshold voltage after the end of the ramp. The threshold voltage is stable 100 s after termination of the ramp and varies only by ±0.1 mV due to measurement accuracy and smaller temperature variations (±0.05 K). An increase of V_{th} by 0.2 mV with repetition of the temperature ramp is observed but is negligible compared with the overall threshold voltage shift.

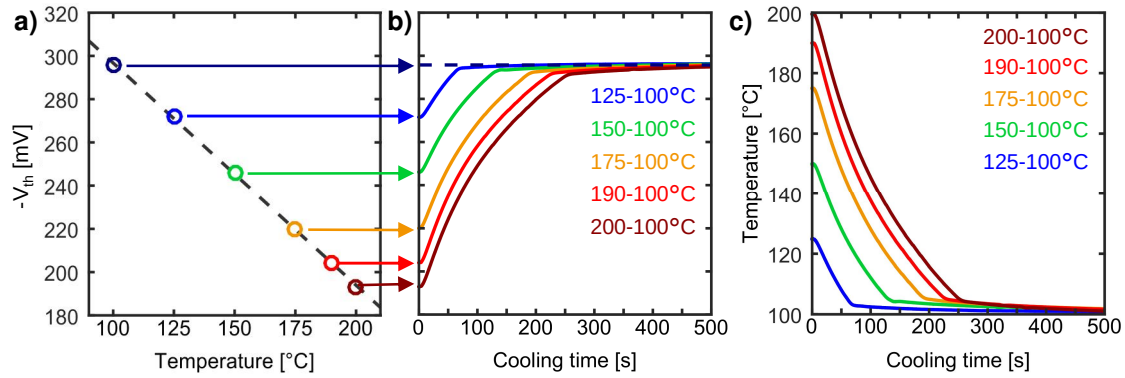

Figure 5.10: Cooling experiments: **a)** Extraction of the temperature dependence of the threshold voltage shift at different temperatures. **b)** Threshold voltage shift dependent on the cooling time with varied starting temperature. **c)** Temperature decrease during cooling with the vortex tube calculated with the temperature dependence extracted from a) and the measured threshold voltage shift in b).

To reduce the total required experimental time, all heating and cooling curves need to be known prior to the stress experiment:

- The exact junction temperature at any point in time during the measurement is needed for the calculations of the equivalent temperature-time $\Theta(T)$ during the ramp (see Fig. 5.9 a). The calculation of $\Theta_{\mathrm{rec}}(T_{\mathrm{ref}})$ requires the iterative consideration of the already passed recovery time and the additional recovery time within the next time/temperature step.
- The time to cool-down is required to set the time for the start of the next stress sequence. The stress temperature is reached after cool-down from $T = 200°\mathrm{C}$ after less than 500 s as shown in Fig. 5.10 c).
- As indicated in the measurement scheme Fig. 5.7 c), the stress voltage is kept applied during cool-down. For the stress temperatures used in Section 5.2.2, the threshold voltage during cooling as well as the calculated temperature are shown in Fig. 5.10 b-c). To calculate the correct additional stress time, the cooling curves are used and are taken into account for the setup of the stress and recovery sequences of the measurement scheme.

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In summary, not only the stress voltages and the timing of the recovery sequence has to be clearly defined and monitored, but also the temperature. The temperature dependence of the threshold voltage during the temperature ramps thus defines the recovery voltage.

5.2.3 Application-Relevant AC Stress

To proof the derived model and its predictions with realistic stress-scenarios, the degradation and recovery is studied by applying typical stress patterns of analog circuits. The applied stress schemes and the setups and product-relevant circuits are described in the following.

Measurements with an Arbitrary Waveform Generator

The idea of this measurement method is to drive single transistors in identical operation modes as during real circuit operation using a two-channel arbitrary waveform generator (AWG) Tabor PM8572A capable to provide the necessary current and voltages as sketched in Fig. 5.11. For this purpose, the voltage curves for the AWG are previously simulated using the Infineon SPICE circuit simulator. During stress, the applied stress voltages are monitored with a digital storage oscilloscope (DSO). A standard analyzer, a Keithley 2636B is used for device characterization with a measurement delay between the stress and the parameter extraction of about 2 ms. Any arbitrary transistor operation in the circuit can be simulated and measured using this setup and e.g. the applied stress signal can be varied in frequency and magnitude. The only requirement is a circuit simulation to obtain the desired stress-input signal.

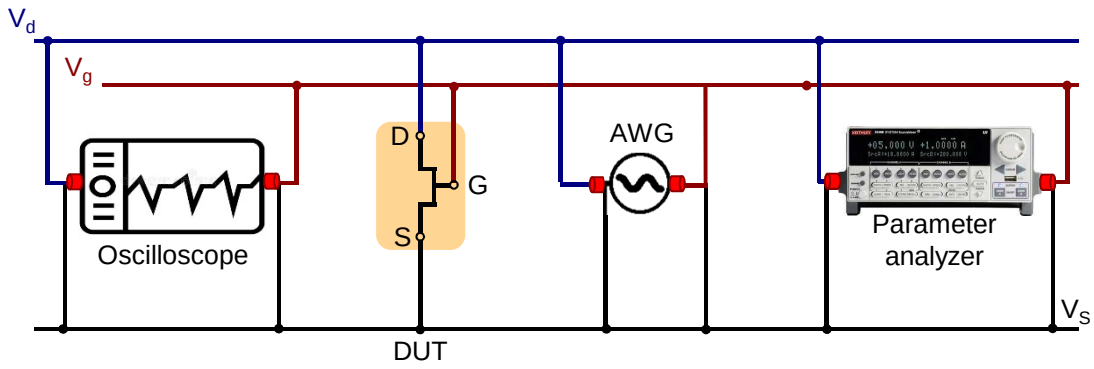

Figure 5.11: Arbitrary waveform setup: A two-channel arbitrary waveform generator applies previously simulated V_{ds} and V_{gs} patterns to the DUT. The stress can be interrupted to characterize the device with an analyzer. The applied stress voltages can be monitored with a DSO. Exemplary signals are shown in Fig. 7.20.

Ring Oscillator Circuit Measurements

For product relevant aging measurements, simple dedicated test circuits are often used. In particular, ring oscillators are frequently used to establish a correlation to product performance. The ring oscillator is placed between heater stripes to accelerate degradation and avoid the need for heating the chuck, which enables fast inline measurement using a process control monitor (PCM) as shown in Fig. 5.12 a). An example of the temperature ramp-up within a few hundred milliseconds and the stabilization phase is shown in 5.12 b). The PCM measurement equipment provides a spectrum analyzer for frequency degradation measurement and the frequency readout occurs during stress. After end of stress, switching to a lower V_{dd} increases the measurement time and requires optimization for NBTI recovery effects.

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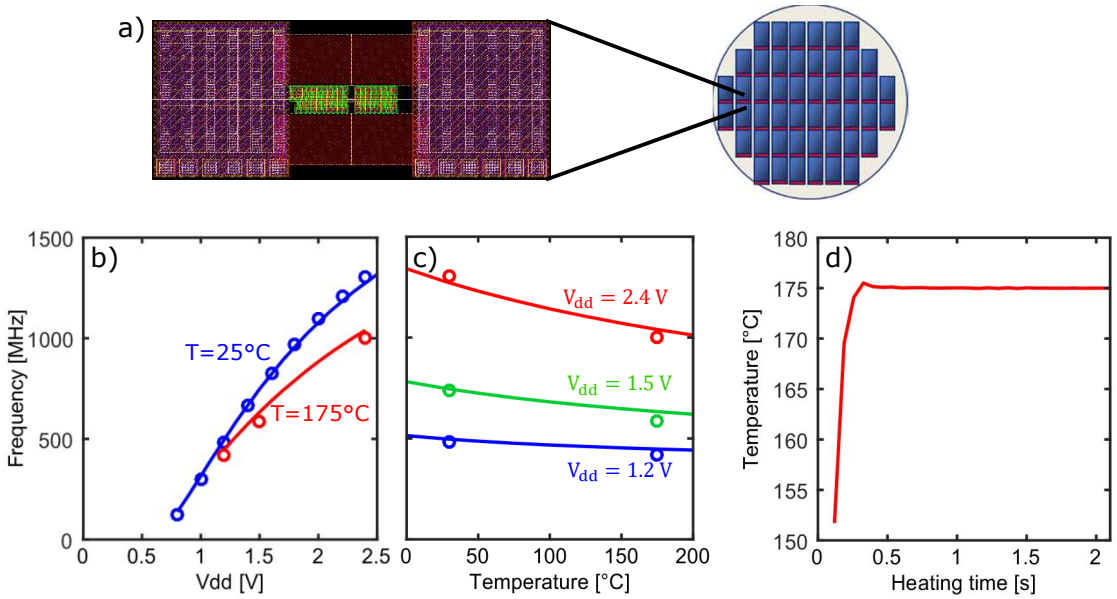

Figure 5.12: a) The ring oscillator circuit in between two poly heater stripes. The temperature sensor is located in the center of the gap. **b-c)** Measured and simulated ring oscillator properties (circles and lines, respectively): **b)** INV ring oscillator frequency dependent on the supply voltage for two different temperatures. **c)** Temperature dependence of the INV ring oscillation frequency at three different supply voltages. **d)** Measured temperature increase of the ring oscillator and subsequent temperature stabilization for the chuck temperature $T_{\mathrm{ref}} = 30°\mathrm{C}$ and $T_{\mathrm{str}} = 175°\mathrm{C}$.

The frequency shift due to aging of two different ring oscillators, a not OR logic gate (NOR) and an inverter logic gate (INV) ring oscillator is compared in Section 7.7.4, the schematic of the ring oscillator, the corresponding logic gates, and the time-dependent pFET stress voltage response to an applied V_{dd} are shown in Fig. 5.13.

The ring oscillator frequency is fixed by the device length and number of stages, but depends on the supply voltage and temperature as shown in Fig. 5.12 b-c). The measurement scheme for all ring oscillator measurements is the following:

1. Measurement of the ring oscillator frequency at $V_{\mathrm{dd}} = 1.5\,\mathrm{V}$ and $T_{\mathrm{ref}} = 30°\mathrm{C}$.
2. With the heating stripes the ring oscillators are heated up until the stress temperature is reached.
3. Measurement of the ring oscillator frequency at $V_{\mathrm{dd}} = 1.5\,\mathrm{V}$ and T_{str}.
4. In situ frequency measurement at stress: $V_{\mathrm{dd}} = V_{\mathrm{gs,str}}$ and $T = T_{\mathrm{str}}$.
5. Either recovery measurement at stress temperature with $V_{\mathrm{dd}} = 1.5\,\mathrm{V}$ and $T = T_{\mathrm{str}}$ or cool-down of the circuit within milliseconds and measurement of the frequency recovery at $T_{\mathrm{ref}} = 30°\mathrm{C}$.

Already during the first in situ frequency measurement (increase of V_{dd} to the stress voltage), the ring oscillator frequency decreases due to degradation. Therefore, measurements and simulation at $V_{\mathrm{dd}} = 1.5\,\mathrm{V}$ before and after stress are used to determine the zero hour frequency at stress conditions $f_0 = f(t = 0), V_{\mathrm{dd}} = V_{\mathrm{gs,str}}$. The initial frequency f_0 is then used as a reference for the in situ frequency read-outs. The measurement uncertainty for all ring oscillator frequency measurements is $\Delta f = \pm 0.1\,\mathrm{MHz}$. An advantage of the ring oscillators is that the measured ring oscillator frequency is directly correlated with the device degradation. An increase in V_{th} leads

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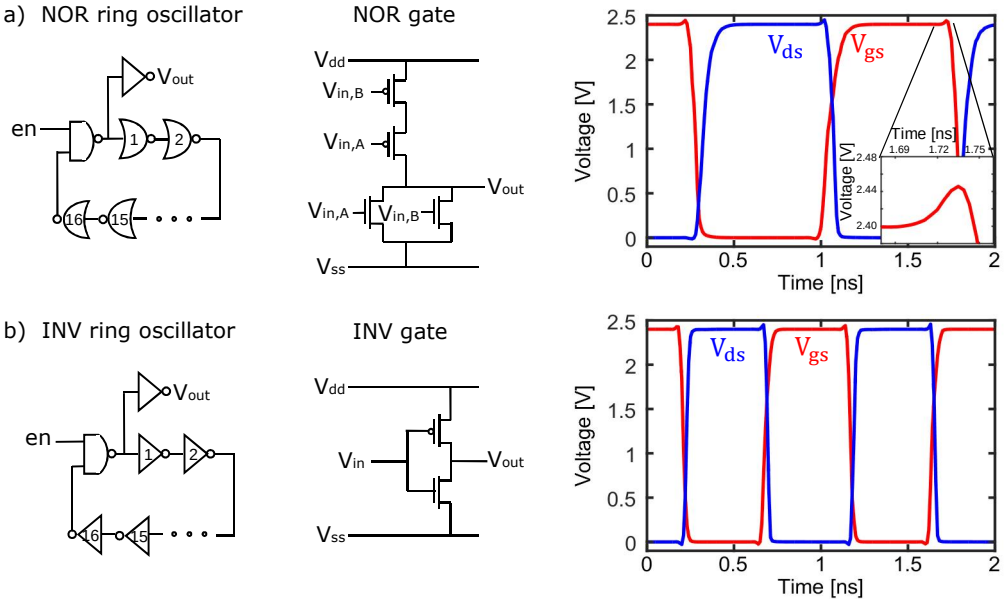

Figure 5.13: Sketch of the schematic (left) of the ring oscillator with 17 gates, the corresponding logic gate (middle) and plot (right) of the time-dependent pFET stress voltage response to an applied V_{dd} of **a)** a NOR ring oscillator **b)** an INV ring oscillator. The inset in the top-right plot shows a zoom-in of typically arising overshoots within the stress voltage response.

to a decreasing frequency. As such, the circuits provide a good framework for the validation of the aging models within the circuit simulator. Measurements and simulation are compared in Section 7.7.4.

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Chapter 6

Voltage-dependent activation energy maps

To enable MOSFETs lifetime extrapolation for up to 10 years, BTI is commonly accelerated via increased stress voltage and increased temperature. CET maps extracted from measurement data at constant temperatures are used to model the time dynamics responsible for the threshold voltage shift of BTI for DC as well as digital AC stress (compare Section 4.4.1). The goal of this thesis is the development of an analytic BTI model for arbitrary gate stress to fulfill all requirements for circuit simulations as outlined in Section 4.1. The first step towards this goal is the modification and extension of the analytic activation energy map model to include the stress-voltage dependence. The model is based on the analytic model by Grasser as described in Section 4.4.1 and [76]:

- The defect kinetics are described for each individual defect by a capture and emission time constant [141], where the time constants correspond to the reciprocal rates of the involved electrochemical reactions [194] (see Section 4.4.1).
- Instead of the calculation of discrete capture and emission time combinations for each defect as attempted in [94], an analytic formulation describing the defect density of the CET maps is used as described in Section 4.4.1 [76].
- A single CET map is valid for a given temperature, stress, and recovery voltage. To extract a single CET map, preferentially, very long recovery traces of more than 10^5 s are required as shown in [94] and presented in Section 6.1. Rather than extracting CET maps for different temperatures, a unified activation energy map representing CET maps is used for all temperatures. In Section 6.1.1, constant temperature measurements are used to demonstrate that the Arrhenius temperature activation is valid for a large number of defects and can be described by an activation energy map.

Constant temperature measurements are time-consuming and introduce an additional uncertainty due to variability. To reduce the experimental effort, the TA-MSM technique has been developed:

- Long recovery times are accelerated by the TA-MSM technique at constant stress voltage with linear temperature ramps [KWC2], reducing the measurement time of more than 300 hours (solely MSM) to less than 10 hours (TA-MSM). The TA-MSM technique is applied in Section 6.1.2 to extract the parameters of the activation energy maps with an extended experimental time window for degradation and recovery without requiring voltage acceleration and time extrapolation (see Section 5.2.2)
- The reduction of the experimental time with the TA-MSM technique enables performing several stress voltage-dependent measurements with an acceptable effort. A model for

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the stress-voltage dependence of BTI with voltage-dependent activation energy maps is demonstrated in Section 6.1.3 and [KWJ2].

The model validation and the application of the model to simulate standard qualification measurements, fast wafer-level reliability measurements as well as the degradation after AC and DC burn-in stress is presented in Section 6.2. The TA-MSM technique is not only beneficial to extract the model parameters but it is also a valuable tool for the study of the permanent component and the recently discovered reverse recovery effect (see Section 6.3). Benefits, limitations, and further improvements of the TA-MSM technique are discussed in Section 6.4.

6.1 Activation Energy Maps[1]

CET map modeling has been introduced by Reisinger [94] and Grasser [76, 145]. The CET map model assumes that BTI is the collective response of independent defects that exchange charges with the channel [76]. The charge exchange is thermally activated and the correlated activation energies can be described using two bivariate Gaussian distributions as shown in Section 4.4.1. However, it was found that the original model presented in [145] following (4.12) does not always produce reasonable results [195]. Therefore, in the following, the analytic model based on activation energy maps to describe the degradation and recovery behavior used in this work is introduced:

- The model is based on the defect-centric model (see Section 4.3.2) and follows the modeling approach of the Grasser analytic two-state model with capture and emission time maps described in Section 4.4.1.
- In contrast to the work of Pobegen *et al.*, the full set of extended MSM measurements with long recovery measurements as shown in Fig. 6.1 is used to optimize the model parameters. As such, the temperature dependence of degradation and recovery are simultaneously considered [111, 196]. Instead of capture and emission time constants, the model is formulated based on capture and emission activation energies as described in Section 4.4.1. Therefore, the temperature dependence of the defect time constants is implicitly included in the model. The effect of temperature on the capture and emission time constants is illustrated in Fig. 5.4.
- Previous publications have shown that BTI consists of a recoverable component R, dominating the recovery over usual experimental times of up to 100 ks [96, 164, 197]. Furthermore, a quasi-permanent component P has been observed with recovery times longer than typical experimental times ($\tau_e \geq 100$ ks) [93, 183, 198]. Thus, as described in Section 4.4.1, two bivariate Gaussian distributions are used, one for the recoverable and one for the quasi-permanent component [145].
- The different defect types R and P show the same temperature dependence but a different temperature-independent time constant τ_0 for each component in (3.6) is used: $\tau_{0,r}$ for the recoverable component and for the quasi-permanent component $\tau_{0,p}$.
- The correlation of the standard deviations is modeled as suggested in [195], with r the correlation parameter $0 \leq r \leq 1$ independent for each component. Thereby $r = 0$ denotes no correlation between the capture and emission energies, whereas $r = 1$ denotes correlation

[1] This section is based on a previous publication by the author of this thesis [KWC2].

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between the capture and emission energies. As in [145], the following relations apply:

$$\mu_e := r\mu_c + \mu_{\Delta e} \tag{6.1}$$

$$\sigma_e{}^2 := r^2\sigma_c{}^2 + \sigma_{\Delta e}^2 \tag{6.2}$$

$$\rho := r\frac{\sigma_c}{\sigma_e} \tag{6.3}$$

with ρ the correlation coefficient.

The modified analytic model formulation for the charged trap density $g(E_c, E_e)$ for each component R and P is then given by [145]:

$$g(E_c, E_e) = \frac{A}{2\pi\sigma_c\sigma_{\Delta e}} \cdot \exp\Big(-\frac{(E_c-\mu_c)^2}{2\sigma_c{}^2} - \frac{(E_e-(rE_c+\mu_{\Delta e}))^2}{2\sigma_{\Delta e}{}^2}\Big). \tag{6.4}$$

The 6 model parameters for each component are: The mean capture activation energy μ_c with its standard deviations σ_c, the additional mean activation energy $\mu_{\Delta e}$ with its standard deviations $\sigma_{\Delta e}$, the amplitude A and the temperature-independent time constant τ_0. In the course of this work, it has been found that $r = 1$ works well for the recoverable component and $r = 0$ for the quasi-permanent component, as such r is not considered a free model parameter. Thus, the activation energy map for one stress voltage consists of 12 parameters, which are extracted from measurements either at several constant temperatures or, as demonstrated in Section 6.1.2, by TA-MSM measurements by performing the following steps:

1. The defect occupation probability for each measurement point is calculated following (4.14) with consideration of the stress and recovery history.

2. The modeled $\Delta V_{th,model} = \Delta V_{th,r} + \Delta V_{th,p}$ is then calculated inserting (6.4) and (4.14) in (4.13) for each the recoverable and quasi-permanent component.

3. In a final step, an optimizer is used to jointly fit all model parameters to the experimental stress and recovery traces for all temperatures and voltages. As an optimizer, the non-linear *fminsearch* algorithm of Mathworks MATLAB®2015b is used, minimizing the least square S

$$S = \sum_{t_{str}}\sum_{t_{rec}} (\log(\Delta V_{th,model}(t_{str}, t_{rec})) - \log(\Delta V_{th,meas}(t_{str}, t_{rec})))^2. \tag{6.5}$$

   The threshold voltage shift increases exponentially with stress time, to ensure proper modeling for short as well as long capture and emission time constants, minimization of the least squares of the logarithm of ΔV_{th} has been chosen.

The model parameter extraction is demonstrated for 130 nm Si pMOSFETs as described in Section 5.2.1 with the ultra-fast measurement equipment described as Section 5.1.2. First, the threshold voltage shift after NBTI stress and recovery at three different temperatures is studied in Section 6.1.1. Second, to reduce measurement effort, the TA-MSM technique is applied for the extraction of the activation energy map parameters in Section 6.1.2 and the concept of equivalent times is introduced. Third, the stress voltage dependence of the activation energy maps is extracted from TA-MSM measurements with varied stress voltage. The voltage-dependent activation energy map is the basis of the circuit simulator compatible model presented in Section 7

6.1.1 Measurements at Constant Temperature

First, the threshold voltage shift ΔV_{th} and its recovery after different stress times is studied at three constant temperatures $T = 100°C$, $T = 150°C$, $T = 200°C$ as shown in Fig. 6.1 a-c).

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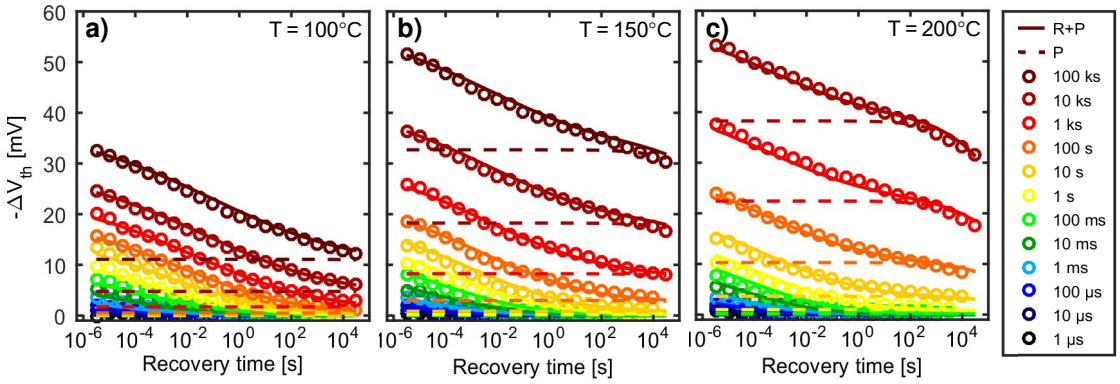

Figure 6.1: MSM sequences: Comparison of experimental data (circles) with the analytic model (lines) with $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$, $V_{\mathrm{gs,rec}}(T = 100°\mathrm{C}) = -0.3\,\mathrm{V}$ for stress times of 1 µs to 100 ks as denoted in the legend. **a)** $T = 100°\mathrm{C}$, **b)** $T = 150°\mathrm{C}$, **c)** $T = 200°\mathrm{C}$. For each temperature, a new sample is used. The activation energy map shown in Fig. 6.3 is used for the analytic model of all measurements. Solid lines correspond to the sum of the recoverable and quasi-permanent component, and the dashed lines to the contribution of only the quasi-permanent component. The comparison of the experimental data with the analytic model shows excellent agreement.

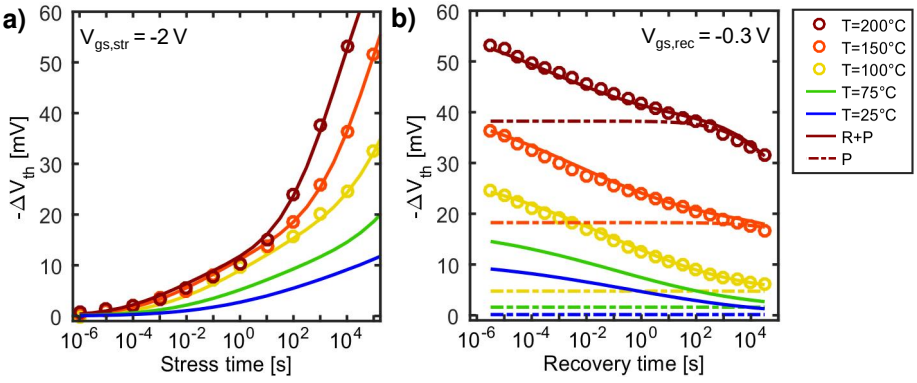

Figure 6.2: Temperature dependence: **a)** ΔV_{th} as a function of the stress time with $t_{\mathrm{d}} = 1\,\mu\mathrm{s}$ and **b)** ΔV_{th} after 10 ks stress with $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$. Measurements points (circles) are from Fig. 6.1. Simulations (lines) with the activation energy map (see Fig. 6.3) show that the temperature dependence is fully covered by the Arrhenius law with $\tau_{0,\mathrm{r}}$ and $\tau_{0,\mathrm{p}}$ given in Table 6.1. At $T = 200°\mathrm{C}$ also recovery of the quasi-permanent (dashed lines) component is observed.

Every stress is consecutively followed by a recovery phase in the range of 1 µs to 100 ks. During stress, no measurement data is obtained within the MSM scheme. For short stress times, the threshold voltage fully recovers to its pre-stress value. After longer stress times (dependent on the stress temperature), no full recovery is observed even for the longest recovery times of up to 100 ks.

The increased degradation after NBTI stress at higher temperatures is clearly visible - shorter stress times are required at higher temperatures to obtain the same threshold voltage shift as at low temperature. This indicates an acceleration of the capture time constants to shorter times when increasing the temperature. Furthermore, the recovery after the same stress time in Fig. 6.2 b) shows a slightly different slope for each temperature, already indicating that not only the capture time constants change with temperature, but also the emission time constants.

As a result, the comparison of the measurement data of the three temperatures with the analytic model of the activation energy maps shows excellent agreement for all temperatures, stress, and recovery times and is shown in Fig. 6.1 and Fig. 6.2.

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Table 6.1: Activation energy map parameters of Fig. 6.3 and Fig. 6.4. For the recoverable component $r = 1$, the mean activation energy is $\mu_{(e,0)} = 0.88\,\text{eV}$ according to (6.1) and $\sigma_e = 0.38\,\text{eV}$ according to (6.2). For the permanent component $r = 0$, thus $\mu_{(e,0)} = \mu_{(\Delta e,0)}$ and $\sigma_{\Delta e} = \sigma_e$.

	τ_0 [ns]	$\mu_{(c,0)}$ [eV]	σ_c [eV]	$\mu_{(\Delta e,0)}$ [eV]	$\sigma_{\Delta e}$ [eV]	A [mVeV^{-2}]	r
R	$5.5 \cdot 10^{-5}$	0.97	0.32	-0.08	0.22	28	1
P	0.57	1.27	0.17	1.57	0.21	82	0

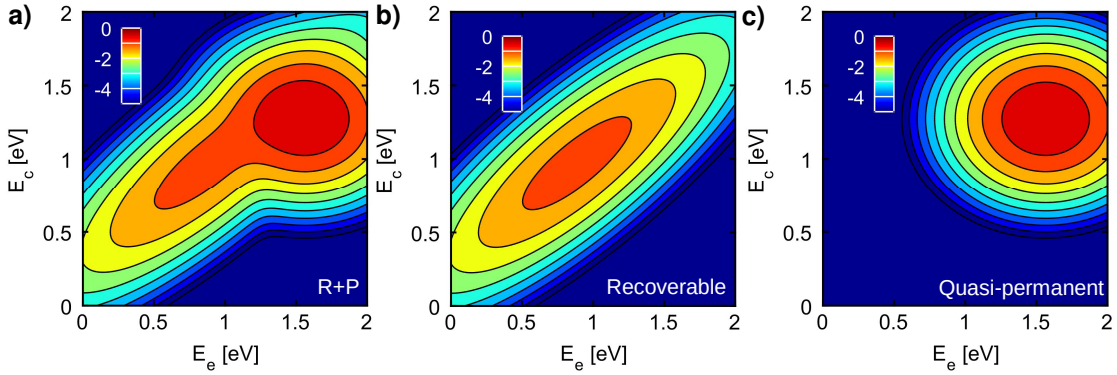

Figure 6.3: Activation energy map for a stress voltage of $V_{gs,str} = -2\,\text{V}$ and a recovery voltage of $V_{gs,rec} = -0.3\,\text{V}$, obtained from the measurements shown in Fig. 6.1. **a)** Sum of the recoverable and quasi-permanent component. **b)** Recoverable component. **c)** Quasi-permanent component. The parameters describing the activation energy map are listed in Table 6.1. The defect distribution and its contribution to the overall threshold voltage shift is shown on a logarithmic color scale, the density value z corresponds to a ΔV_{th} of $10^z\,\text{V/eV}^2$.

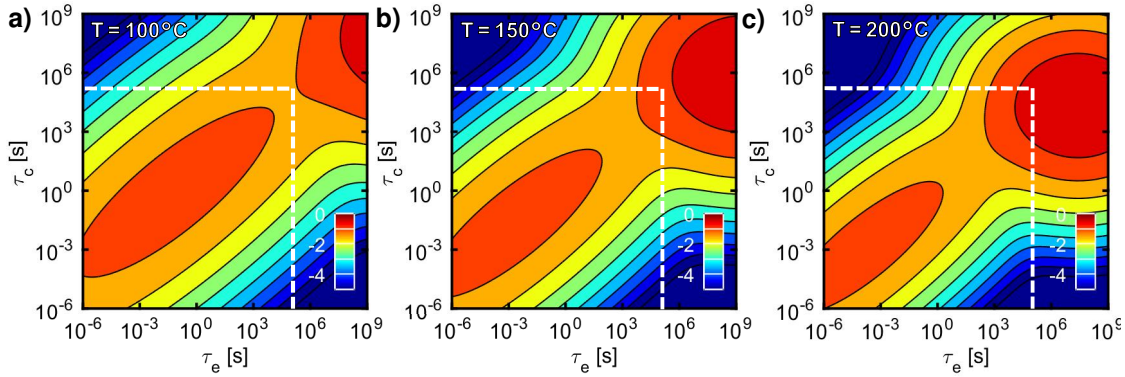

Figure 6.4: Temperature-dependent capture and emission time maps with $V_{gs,str} = -2\,\text{V}$, $V_{gs,rec} = -0.3\,\text{V}$ (equivalent to Fig. 6.3). **a)** T=100°C, **b)** T=150°C, **c)** T=200°C. The defect distribution and its contribution to the overall threshold voltage shift is shown on a logarithmic color scale, the density value z corresponds to a ΔV_{th} of $7 \cdot 10^z\,\text{mV/decade}^2$. The dashed squares indicate the experimental windows of the measurements shown in Fig. 6.1.

The resulting activation energy map shows in Fig. 6.3 a) the distribution of the capture and emission activation energies. The distribution of the quasi-permanent component, shown in Fig. 6.3 c), is located at high capture activation energies and increasing emission activation energies, whereas the recoverable defects, shown in Fig. 6.3 b), have smaller capture as well as smaller emission activation energies. Furthermore, the capture and emission activation energies of the recoverable component are correlated ($r = 1$), so that an increase in the capture activation energy directly results in an increase of the emission activation energy. In contrast, the capture

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and emission activation energies of the quasi-permanent component are uncorrelated ($r = 0$). In the following, r is fixed and not considered as a free model parameter.

Consequently, the temperature dependence of the capture and emission time constants is fully described by $\tau_{0,r} = 55\,\text{fs}$ for the recoverable and $\tau_{0,p} = 0.57\,\text{ns}$ for the quasi-permanent component. Error estimation for all parameters is given in Section 6.1.3. Following (3.6) with $\tau_{0,r}$ and $\tau_{0,p}$, for each temperature a CET map can be calculated from the activation energy map described by the parameters in Table 6.1. The corresponding capture and emission time maps at T=100/150/200°C are shown in Fig. 6.4 a)-c) with the dashed lines indicating the measurement windows of the MSM measurements of Fig. 6.1. Note that the capture and emission time constants of R and P show a different temperature dependence, therefore the two components always have to be considered independently.

The separation into a recoverable and quasi-permanent component necessitates long measurement times and also high temperatures. With increasing temperature, a strong increase especially of the quasi-permanent is observed in Fig. 6.2 a), which is in accordance with the increase of rates (reduction of capture time constants) with increasing temperature seen in Fig. 6.4a)-c). At room temperature, as seen in Fig. 6.2 b), no permanent degradation builds up, and even at $T = 200°\text{C}$, long recovery times are needed to observe a slight recovery of the quasi-permanent component [199]. For a quasi-permanent defect with an emission activation energy of $E_e = 1.6\,\text{eV}$, the emission time constant at $T = 200°\text{C}$ is 100 ks, which is equivalent to $\tau_e = 10^8\,\text{s}$ at $T = 100°\text{C}$.

To summarize, with the constant temperature measurements it has been demonstrated that the change of the defect time constants with temperature follows the Arrhenius law. Both stress and recovery can be modeled simultaneously using a single activation energy map with temperature-independent time constants $\tau_{0,r}$ and $\tau_{0,p}$ for the recoverable and quasi-permanent component. As such, any degradation and recovery at any temperature can be calculated using the activation energy map. The whole analytic model is solely based on measurement data without lifetime and voltage extrapolation, e.g. modeling of NBTI stress and recovery of more than 10 years at $T = 100°\text{C}$ is possible.

6.1.2 Temperature Acceleration with the TA-MSM Technique

Performing several measurements at constant temperature is time and test device consuming and introduces an additional uncertainty due to variability. To reduce the measurement time and improve the model accuracy, the TA-MSM technique has been developed by the author of this thesis as explained in Section 5.2.2. The measurement scheme is described in Fig. 5.7. For the following experiments, a base stress temperature of $T_{ref} = 100°\text{C}$ is used followed by a linear temperature ramp from $T = 100 - 200°\text{C}$. For stress times up to 10 ks, the stress temperature is $T_{ref} = T_{str} = 100°\text{C}$. For equivalent stress times higher than 10 ks, the stress temperature is increased to T_{str}=125/150/175/190°C as indicated in the legend in Fig. 6.5 and Fig. 6.6. The stress times and temperatures have been chosen based on the results shown in Fig. 6.1. $t_{str} = 32\,\text{ks}$ at $T_{str} = 190°\text{C}$ corresponds to $\Theta_{str}(T = 100°\text{C}) = 7 \cdot 10^7\,\text{s}$.

The ΔV_{th} versus recovery time measured by the TA-MSM technique is shown in Fig. 6.5. After 1 ks of recovery, the linear temperature ramp starts and the temperature is linearly increased from 100 – 200°C within 1 ks. Within the temperature ramp, an acceleration of four decades in recovery time is visible (highlighted area in Fig. 6.5 a). Without the temperature ramp, less than 1 mV would recover, whereas with the temperature ramp ΔV_{th} reduces for the longest stress time by 8 mV.

An important step for the analysis of the recovery induced by the temperature ramp is to calculate the equivalent recovery time $\Theta_{rec}(100°\text{C})$ with the obtained temperature-independent time constants $\tau_{0,r}$ and $\tau_{0,p}$ dependent on the real recovery time with varied temperature (see Section 5.2.2).

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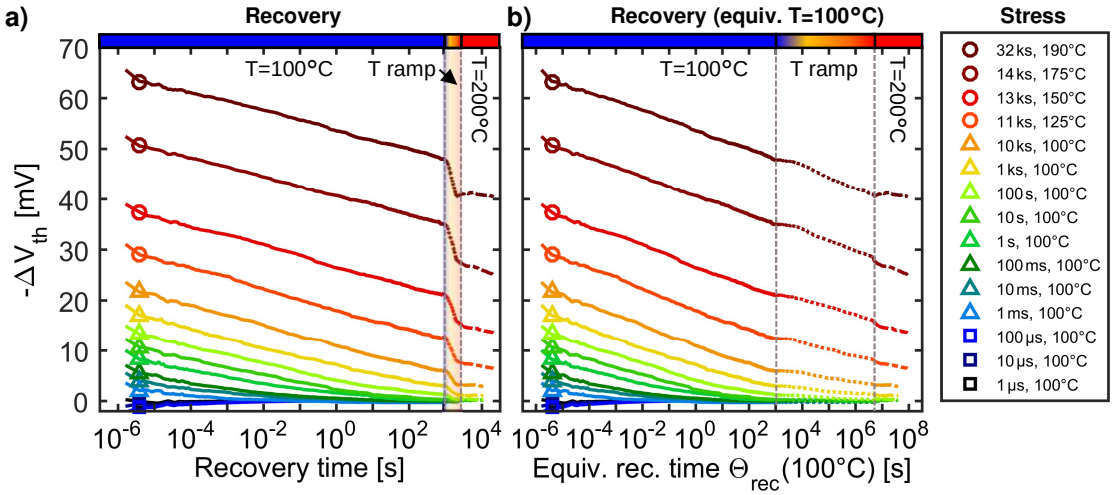

Figure 6.5: TA-MSM measurement with $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$, $T_{\mathrm{ref}} = 100°\mathrm{C}$ for **a)** real-time recovery and **b)** calculated equivalent recovery time at $T_1 = 100°\mathrm{C}$ using the Arrhenius law in (5.1) with $\tau_0 = \tau_{0,\mathrm{p}} = 0.57\,\mathrm{ns}$ and $T_2 = T_{\mathrm{meas}}$ for every change in temperature. The vertical grey dashed lines mark the start and end of the temperature ramp. By subtracting the reference from the measurement data, the ΔV_{th} is obtained (including the temperature ramp). The squares, triangles, and circles correspond to the measurement scheme shown in Fig. 5.7a-c), with the stress times and stress temperature denoted in the legend. A color bar at the top-axis highlights the temperature change during recovery, the exact temperature ramp is shown in Fig. 5.9 a). Measurements with stress times longer than 1 ms start with 1 ks recovery at $T = 100°\mathrm{C}$, followed by a linear temperature ramp within 1 ks from $100 - 200°\mathrm{C}$ and further recovery at 200°C. For stress times up to 10 ks, the stress temperature is $T = 100°\mathrm{C}$. In addition, the stress temperature is increased for stress times larger than 10 ks up to $T = 190°\mathrm{C}$ (see legend).

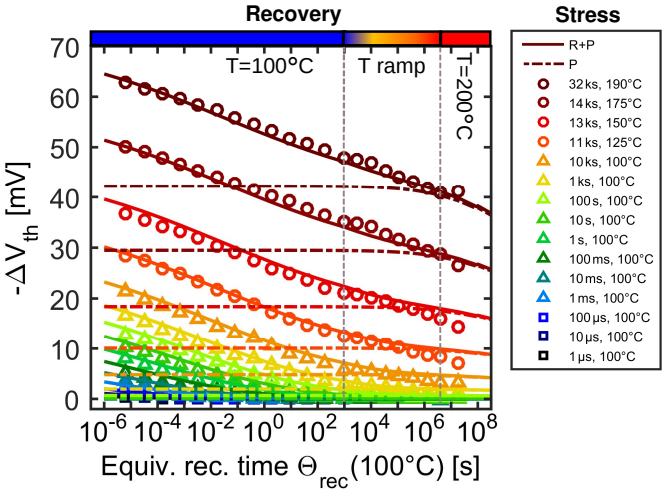

Figure 6.6: Comparison of the analytic model fit (lines) with the measurement data as shown in Fig. 6.5 b) with $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$, $T_{\mathrm{ref}} = 100°\mathrm{C}$. The stress times and increased stress temperatures are given in the legend. A color bar at the top-axis highlights the temperature change during recovery, the exact temperature ramp is shown in Fig. 5.9 a). The dashed lines correspond to the contribution of only the quasi-permanent component, whereas the solid lines correspond to the activation energy map model with the sum of the recoverable and quasi-permanent component. The analytic model fit is in excellent agreement with the measurement data for all stress and recovery times.

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A comparison of the ΔV_{th} recovery is shown in Fig. 6.5 with a) the real recovery time and b) the equivalent recovery time $\Theta_{\text{rec}}(100°\text{C})$. The acceleration of the recovery seen in Fig. 6.5 a) is stretched in time due to the temperature acceleration according to the Arrhenius law. As can be seen in Fig. 6.5 b), by considering this dependence, the recovery of ΔV_{th} is continuous without a change of slope.

The occupation probability included in the model following (4.14) has to consider all measurement conditions e.g. changes of stress temperature, increase of recovery temperature, and of course the stress and recovery history within the measurement sequence of the TA-MSM scheme. The comparison of the measurement results and the analytic model is shown in Fig. 6.6 and shows a very good agreement describing all stress and recovery times as well as the temperature dependencies of the measurements shown in Fig. 6.5. Furthermore, the model covers the extremely wide time window of up to 10 years in equivalent time $\Theta(T = 100°\text{C})$.

In addition to describing the accelerated data, the analytic model obviously also provides a good description for the MSM measurements at constant temperature shown in Fig. 6.1. Due to the linear temperature ramp, discrete temperatures are not the only ones included in the model. Furthermore, the continuous increase in temperature during the recovery increases the model accuracy (least square optimum) by a factor of two for all measurements compared to the model parameters obtained using only the measurements at constant temperature. The lines shown in Fig. 6.1 and the parameters given in Table 6.1 correspond to the more accurate parameters due to the TA-MSM measurements.

6.1.3 Stress Voltage Dependence of the Activation Energy Maps[2]

A circuit-simulator compatible BTI model has to consider the complete stress history of the device, therefore the model has to include for analog applications an accurate stress voltage dependence as well as a recovery voltage dependence. In this work, the stress voltage dependence of the model is included within the activation energy map formulation as three additional equations describing the stress voltage dependence of the parameters in Table 6.2. In the following, the model for the stress voltage is described whereas the recovery voltage dependence is included as a recovery voltage-dependent occupation probability map and is presented in Section 7.3.

TA-MSM measurements are performed at five different stress voltages on five different samples to obtain the stress voltage dependence of the activation energy map as shown in Fig. 6.7. In total, the measurement time is 50 hours, which is still a measurement time compatible with industrial measurements. The ΔV_{th} for each stress voltage is shown in dependence on the equivalent recovery time $\Theta_{\text{rec}}(T = 100°\text{C})$ in Fig. 6.7 a)-e) and the same measurement data is shown in Fig. 6.8 a)-e) on a logarithmic scale to highlight the accuracy of the model.

To discuss the influence of the gate stress voltage, the measurement data of Fig. 6.7 is first shown in Fig. 6.9 a) in dependence on the equivalent stress time $\Theta_{\text{str}}(T = 100°\text{C})$. Here, the higher equivalent stress time when increasing the stress temperature for $t_{\text{str}} \geq 10^4$ s is considered. Second, the dependence of ΔV_{th} on the equivalent recovery time $\Theta_{\text{rec}}(T = 100°\text{C})$ is shown in Fig. 6.9 b) after the same stress time. Here, the higher recovery temperature during the ramp is considered for $t_{\text{rec}} \geq 10^3$ s. Third, the ΔV_{th} after different stress times for the shortest measurement delay is shown in dependence on the stress voltage in Fig. 6.10 a). Fourth, the recovery of ΔV_{th} after the same ΔV_{th} is shown in Fig. 6.10 b).

[2]The main results presented in this section have been published by the author of this thesis in [KWJ2]

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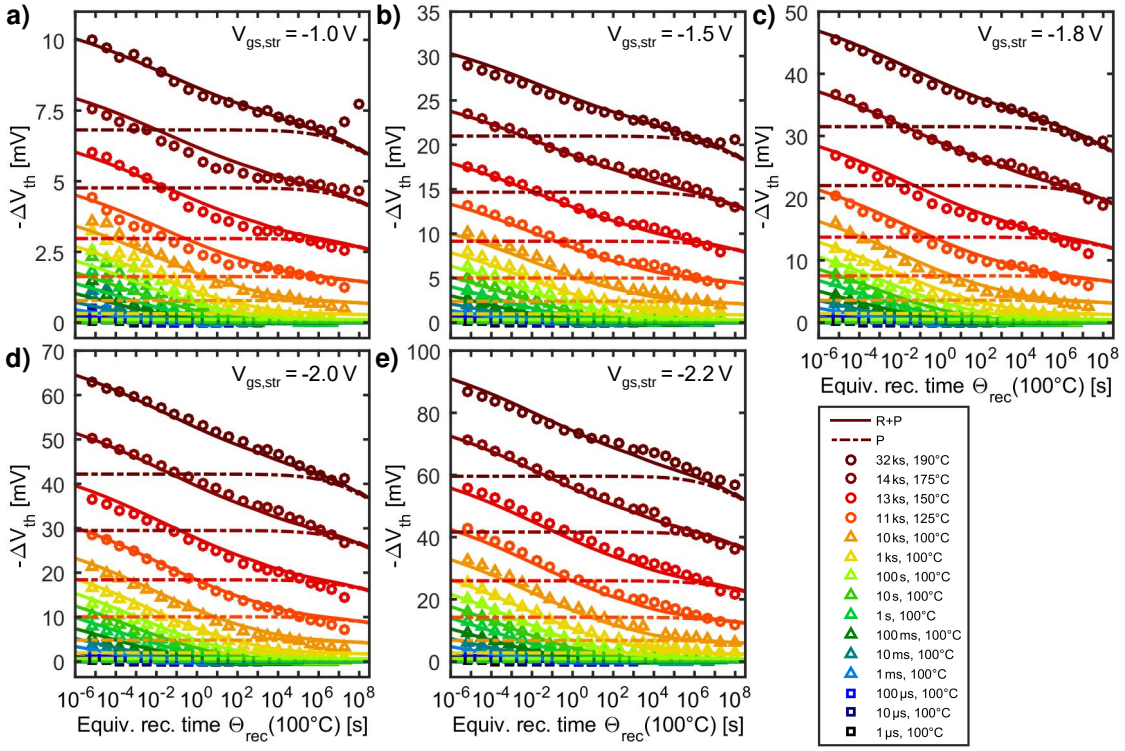

Figure 6.7: Stress voltage dependence of the TA-MSM measurements (linear scale): Comparison of the measurements with the voltage-dependent activation energy model (lines) for **a-e)** $V_{\mathrm{gs,str}} = [-1, -1.5, -1.8, -2, -2.2]$ V with $T_{\mathrm{ref}} = 100°\mathrm{C}$ and with $V_{\mathrm{gs,rec}}(T = 100°\mathrm{C}) = -0.3$ V. In the legend, the stress times and stress temperatures are denoted. For all measurements the same measurement scheme is used (see Section 6.1.1). The temperature ramps are shown in Fig. 6.6.

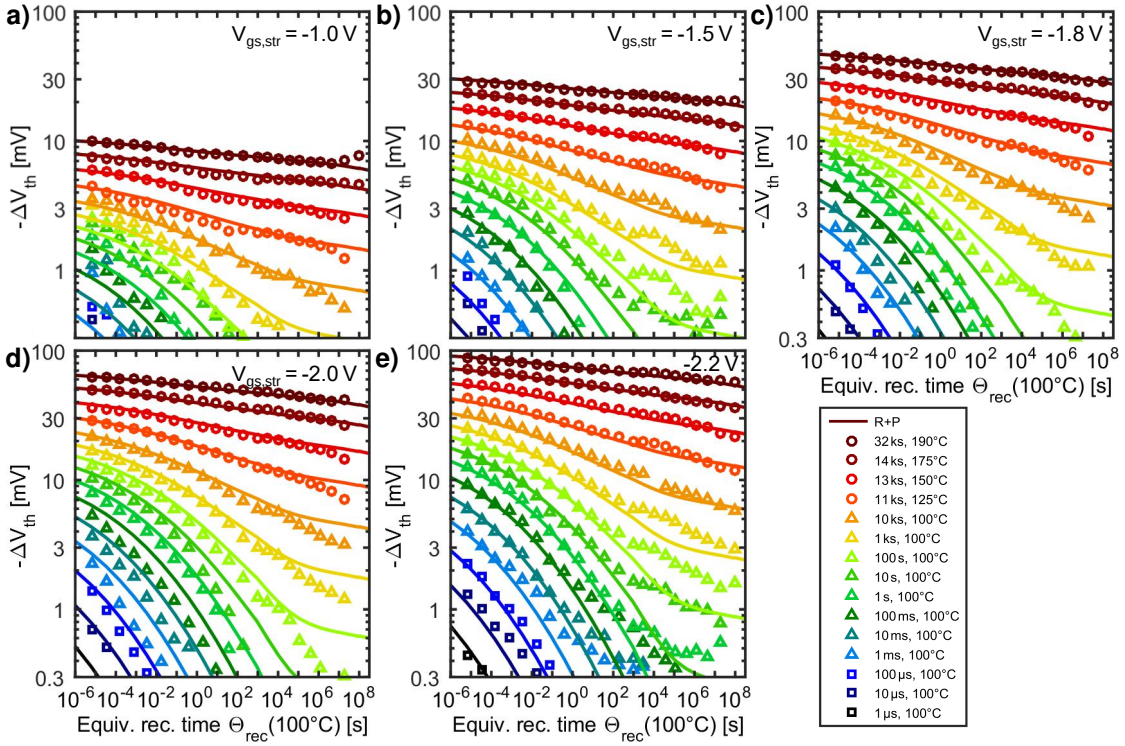

Figure 6.8: Same as Fig. 6.7 but on a logarithmic scale to highlight the agreement of measurement and simulation for the lower stress times with low ΔV_{th}. **a-e)** $V_{\mathrm{gs,str}} = [-1, -1.5, -1.8, -2, -2.2]$ V.

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An increase of the gate stress voltage leads to the following effects on the distribution of the capture and emission time constants:

- Performing a power-law fit (see (4.4) in Section 4.2) for $t_{str} \geq 10\,\text{ks}$ in Fig. 6.9 a) gives the same power-law exponent of $n = 0.12$ for all stress voltages. This already indicates that the relative distribution of the capture time constants $\geq 10\,\text{ks}$ does not change significantly, whereas for short stress times a parallel shift is not visible.

- No significant change in emission time constants can be observed. The slopes at the same ΔV_{th} level are roughly identical in Fig. 6.9 b).

- Obviously, ΔV_{th} increases with increasing stress voltage. The main effect is the strongly increasing number of active traps as seen in Fig. 6.10 a).

- Furthermore, to obtain the same amount of degradation, the required stress time increases with decreasing stress voltage. As a result, the emission time constants increase and an increasing number of quasi-permanent defects with longer capture and emission time constants contribute to the overall ΔV_{th} as seen in Fig. 6.10 b).

To model this voltage dependence, the analytic model equation for the activation energy map (6.4) is extended by:

- The increase of the active trap density with stress voltage is equivalent to an increase of the amplitude A of each component (A_r and A_p). Therefore, the increase of the amplitude is modeled empirically, following previous attempts by Grasser *et al.* [76]:

$$A = \left(\frac{V_{gs,str}}{V_0}\right)^m, \tag{6.6}$$

  with fitting parameters m and V_0. The obtained parameters for the amplitude from the measurements shown in Fig. 6.7 are $V_{(0,r)} = -4.77$, $V_{(0,r)} = -3.52$ and $m_r = 3.05$, $m_p = 2.78$.

- Previous TDDS studies on individual defects on Si [92] have shown that the mean capture activation energy μ_c of each distribution is expected to linearly decrease with increasing stress voltage (capture times decrease with increasing stress voltage as shown in Fig. 3.5). Thus, the linear decrease with increasing stress voltage of μ_c is modeled by:

$$\mu_c = \mu_{c,0} + kV_{gs,str}, \tag{6.7}$$

  where $\mu_{c,0}$ denotes the mean value of the activation energy constants for the charge capture at 0 V and k is the voltage acceleration constant.

- The emission times remain unaffected by the stress voltage ($\mu_e = \text{const}$) as seen in Fig. 6.9 b). Following (6.1) this translates with the voltage dependence of μ_c in (6.7) to:

$$\mu_{\Delta e} = \mu_{\Delta e,0} - kV_{gs,str}. \tag{6.8}$$

  The stress voltage dependence of the mean values μ_c of the capture activation energy of the recoverable is $k_r = 0.01\,\text{eV/V}$. No voltage dependence of the quasi-permanent component is observed ($k_p = 0\,\text{eV/V}$). Also, the stress voltage dependence is weak compared to the bias dependence of the individual traps (see Fig. 3.5 and Fig. 3.6). The reason for this is that with different gate bias the energetically available traps in the oxide change, too (see Fig. 7.1 and [200]). Thus the mean value in the model includes an overlap of both effects.

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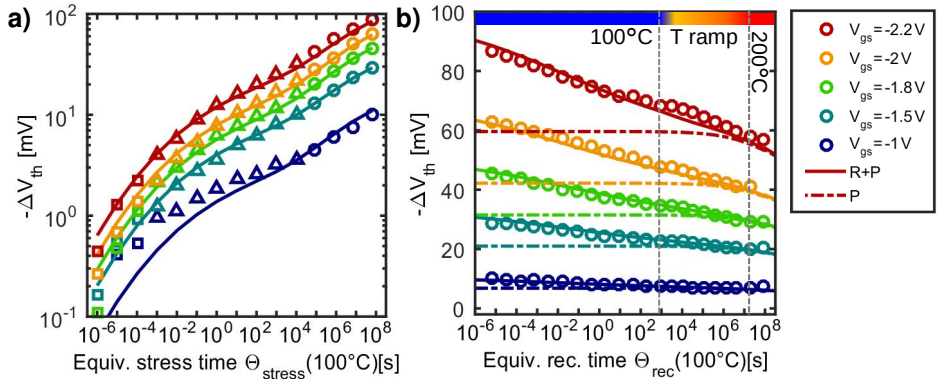

Figure 6.9: Stress voltage dependence of the TA-MSM measurements in comparison with the analytic model: **a)** Threshold voltage shift versus equivalent stress time with a recovery time of 1 µs (at $T = 100°C$) and **b)** Threshold voltage shift versus equivalent recovery time after $t_{str,equiv} = 10^8$ s for different stress voltages. The analytic model fit is shown as solid lines (quasi-permanent and recoverable component) with the same voltage-dependent activation energy map for all stress voltages and the parameters given in Table 6.2. The dashed lines correspond to the contribution of only the quasi-permanent component.

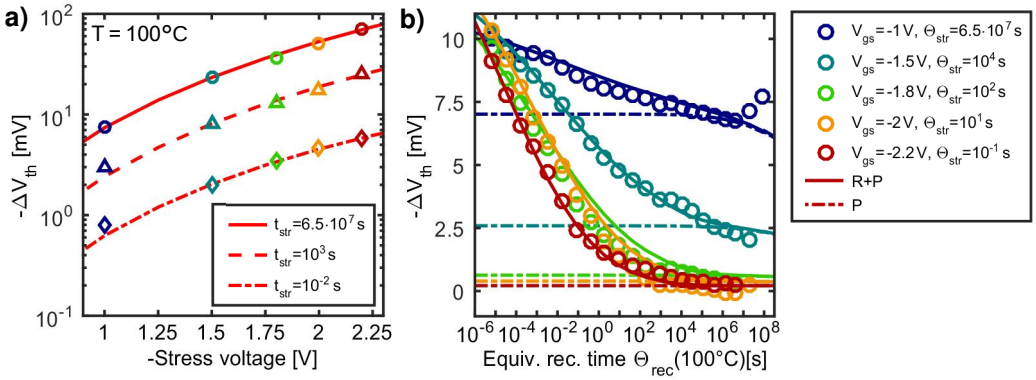

Figure 6.10: Voltage-dependent TA-MSM: Threshold voltage shift dependent on the stress voltage after different stress times and $t_{rec} = 1$ µs. The analytic model fit (quasi-permanent and recoverable component) for each stress time with the same voltage-dependent activation energy map for all stress voltages is shown as solid/dashed/dotted line, respectively. For $V_{gs,str} = -1$ V an increase of V_{th} for long recovery times is observed. This effect is discussed in Section 6.3.

The voltage-dependent activation energy map perfectly reproduces all dependencies of NBTI for the DC stress such as the stress voltage, stress time, recovery time, and temperature dependence. Measurement and simulation show a very good agreement for all stress conditions with a model error below 10 %. Deviations for $\Delta V_{th} \leq 1$ mV visible in Fig. 6.8 are mainly caused by the measurement accuracy of $\Delta V_{th} \leq \pm 0.5$ mV and do not impact the model accuracy for lifetime simulations. For the highest stress voltage ($V_{gs,str} = -2.2$ V) the maximum absolute deviation is 3.5 mV at a $\Delta V_{th} = 60$ mV. The resulting voltage dependence of the activation energy maps is shown for three exemplary voltages in Fig. 6.11. The most obvious feature is the increasing amplitude with increasing stress voltage for both components. In total, the voltage-dependent activation energy map consists of 16 parameters given in Table 6.2.

The relative deviation δ of the fit optimum ssq_{opt} (least square ssq minimization) for a slightly changed parameter is

$$\delta = \mathrm{ssq_{par}} / \mathrm{ssq_{opt}} - 1 \tag{6.9}$$

and the dependence on the varied parameter is shown in Fig. 6.12. In the following, the model accuracy dependent on the model parameters is discussed:

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Table 6.2: Voltage-dependent activation energy map parameters of Fig. 6.3 and Fig. 6.4. For the recoverable component $r = 1$, $\mu_{(e,0)} = 0.88\,\text{eV}$ according to (6.1) and $\sigma_e = 0.38\,\text{eV}$ according to (6.2). For the permanent component $r = 0$, $\mu_{(e,0)} = \mu_{(\Delta e,0)}$ and $\sigma_{\Delta e} = \sigma_e$.

	τ_0 [ns]	$\mu_{(c,0)}$ [eV]	σ_c [eV]	$\mu_{(\Delta e,0)}$ [eV]	$\sigma_{\Delta e}$ [eV]	V_0 [V]	m	k [eV/V]	r
R	5.5×10^{-5}	0.99	0.31	-0.11	0.22	-0.669	3.05	0.01	1
P	0.57	1.27	0.17	1.57	0.21	-0.407	2.78	0	0

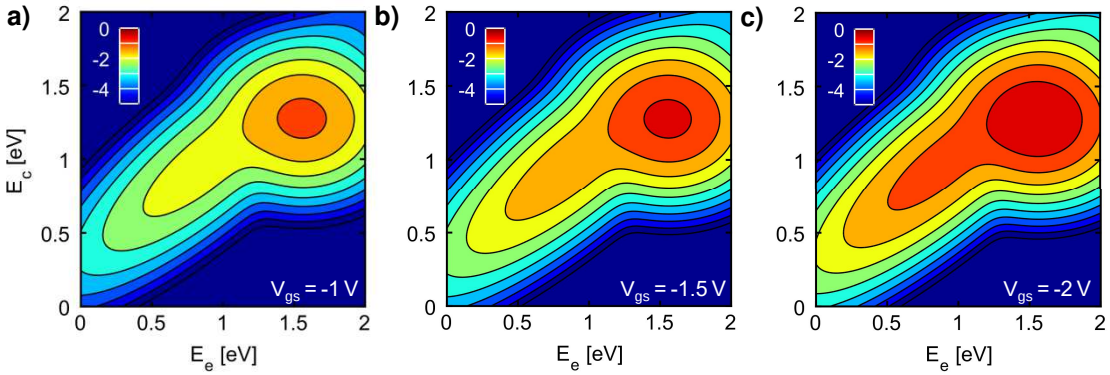

Figure 6.11: Activation energy maps for different stress voltages and a recovery voltage of $V_{gs,rec} = -0.3\,\text{V}$ obtained from the measurements shown in Fig. 6.7. **a)** $V_{gs,str} = -1\,\text{V}$, **b)** $V_{gs,str} = -1.5\,\text{V}$, **c)** $V_{gs,str} = -2\,\text{V}$ with the parameters given in Table 6.2. The defect distribution and its contribution to the overall threshold voltage shift is shown on a logarithmic color scale, the density value z corresponds to a ΔV_{th} of $10^z\,\text{V/eV}^2$.

- The parameters $\mu_{c0,r}$ as well as $\mu_{c0,p}$ are strongly correlated with $\tau_{0,r}$ and $\tau_{0,p}$ via (4.9), respectively. Furthermore, $\mu_{\Delta e0,r}$ and $\mu_{\Delta e0,p}$ are in the same manner correlated with $\tau_{0,r}$ and $\tau_{0,p}$. Due to the wide range of temperatures, stress, and recovery times, $\tau_{0,r}$ and $\tau_{0,p}$ are well-defined via the extended MSM measurements.

- Already small changes of the parameters $\tau_{0,r}$ and $\tau_{0,p}$ cause a significant loss in the model accuracy for a fixed $\mu_{c0,r}$ and $\mu_{c0,p}$ (black lines). However, optimization of all parameters for a fixed $\tau_{0,r}$ and $\tau_{0,p}$ and calculation of the relative fit deviation (black circles) shows that $\tau_{0,r}$ and $\tau_{0,p}$ can vary by one order of magnitude without a significant loss of model accuracy.

- Changes in the order of 10 % of $\sigma_{c,r}$, $\sigma_{c,p}$ and $\sigma_{\Delta e,r}$ cause a significant loss in the accuracy. But, $\sigma_{c,r}$, $\sigma_{c,p}$ and $\sigma_{\Delta e,r}$ only show a weak dependence on $\tau_{0,r}$ and $\tau_{0,p}$.

- The recovery of the quasi-permanent component is defined by $\mu_{(\Delta e,p)}$ and $\sigma_{\Delta e,p}$. The exact determination of these parameters requires very long measurement times at high temperatures. For the TA-MSM data, the accuracy is sufficient as the model covers equivalent recovery times of up to 10 years at $T = 100°\text{C}$. Extrapolation beyond these recovery times might include errors due to deviations in $\mu_{\Delta e,p}$ and $\sigma_{\Delta e,p}$.

- The stress voltage dependence is well-described via (6.6) by $V_{0,r}$, $V_{0,p}$, m_r, m_p with a high sensitivity of m_r and m_p. In addition to the stress voltage dependence of the amplitude, the stress voltage dependence of the capture time constants is described via (6.7) by k_r and k_p. $k_p = 0$ could be clearly determined.

- The optimum for the correlation parameter is $r_r = 1$ and $r_p = 0$ as model optimization with r as a free parameter resulted in $r_r = 1$ and $r_p = 0$. Thus, these parameters have been fixed and are no fit parameters. Nonetheless, the definition of $r_p = 0$ has to be further

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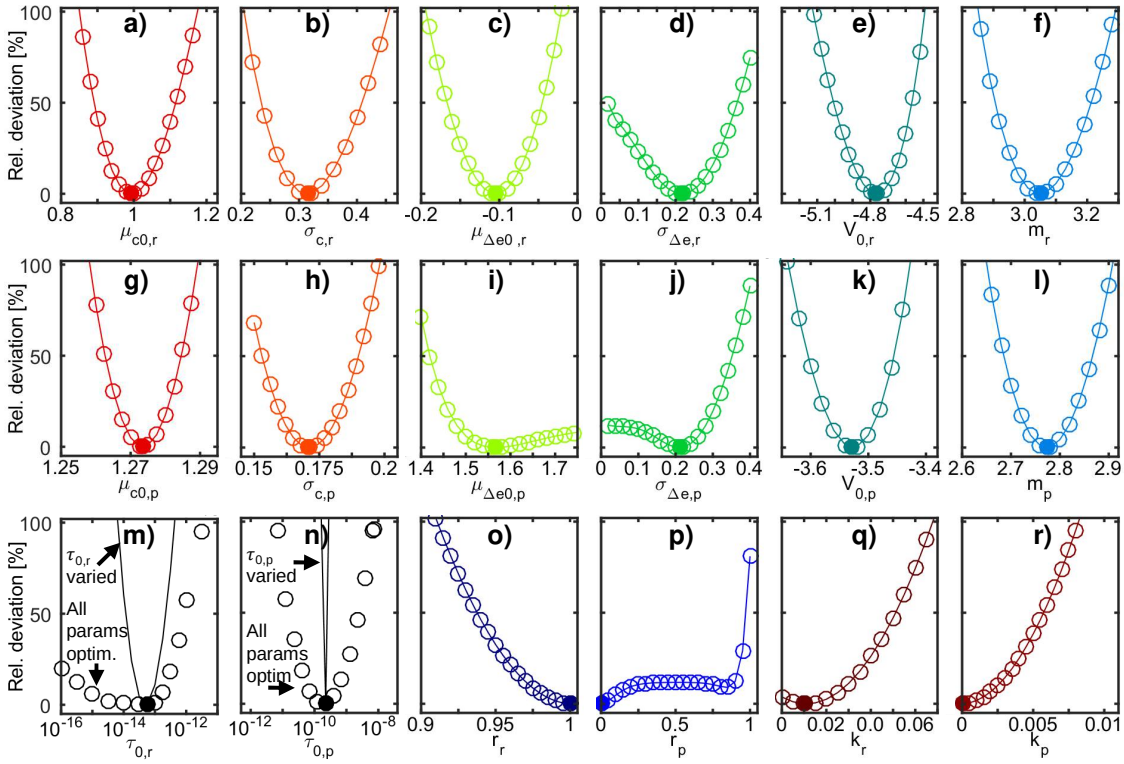

Figure 6.12: Relative fit deviation δ for the model parameters given in Table 6.2. All deviations (circles) have been determined by the variation of the model parameters and the log-based least square error is calculated (measurements and simulation shown in Fig. 6.8). 0% corresponds to the optimum fit as shown in Fig. 6.10 with the parameters given in Table 6.2. In addition, as a change in $\tau_{0,r}$ and $\tau_{0,p}$ causes huge changes in the model accuracy, the relative deviation for $\tau_{0,r}$ and $\tau_{0,p}$ shown in m) and n) has been also determined by varying $\tau_{0,r}$ or $\tau_{0,p}$ and optimizing all other parameters (circles).

evaluated as it would require longer stress and recovery measurements or higher stress and recovery temperatures for a better determination of the quasi-permanent component.

Please note that the parameters given in Table 6.2 are not universally valid. The model parameters have to be optimized for other technologies and depend on the oxide material, thickness, and processing. Measurements and simulations show a very good agreement over a wide range of stress voltages, temperatures, and stress and recovery times. For typical use voltages and temperatures the model accurate for up to 10 years of operation without extrapolation. The model is validated in Section 6.2.

6.2 Validation under DC Conditions

The voltage-dependent activation energy maps presented in Section 6.1.3 are the basis for the analytic BTI model. With the parameters of Table 6.2, the threshold voltage shift after any DC stress at different stress voltages, temperatures, and stress and recovery times can be calculated following (4.10) and (4.14). Nonetheless, the model accuracy and e.g. the suitability for voltage extrapolation has to be validated. The maximum stress voltage used to obtain the voltage-dependent activation energy maps is $V_{\mathrm{gs,str}} = -2.2\,\mathrm{V}$, to simulate higher voltages for e.g. burn-in tests it is also necessary to validate the model for voltages higher than the maximum stress voltage.

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6.2.1 DC Measurements under Varied Gate Bias and Temperature

Simulations for different stress voltages and temperatures are shown in Fig. 6.13 a) and b) without changing the parameters in Table 6.2. Measurements and simulation show a very good agreement, even for the highest stress voltage of $V_{gs,str} = -3.2\,V$ an accuracy below 10 % is achieved. Furthermore, the dependence of the degradation on temperature is studied at typical analog use conditions with $V_{gs} = -1.2\,V$ in Fig. 6.14. Even for stress times of 10^6 s, the ΔV_{th} at $T = 25°C$ is dominated by the recoverable component, whereas at $T = 125°C$. 90 % of the measured ΔV_{th} stem from the quasi-permanent component. In conclusion, the separation into the two components R and P is confirmed as well as the stronger temperature dependence of R than P with $\tau_{0,r} \ll \tau_{0,p}$.

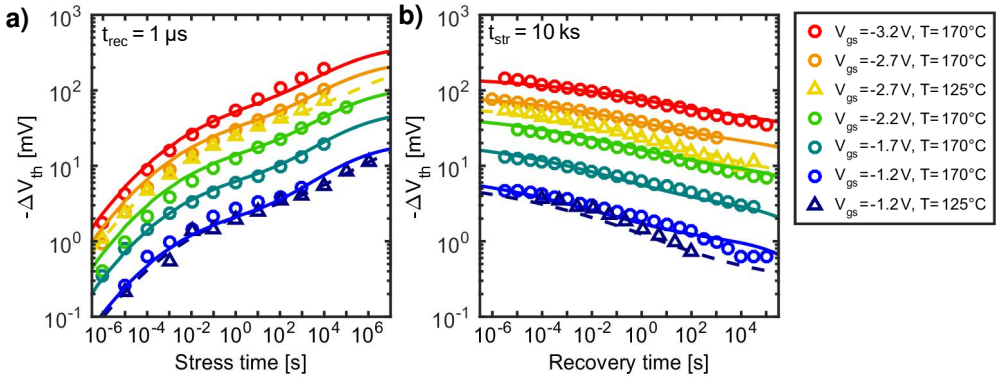

Figure 6.13: DC model validation: Comparison of the experimental data with the activation energy map model and the parameters given in Table 6.2 for different stress voltages $V_{gs,str} = [-1.2, -3.2]\,V$ and temperatures $T = [125, 170]°C$. Even though the model has been calibrated with measurements $V_{gs,str} = [-1, -2.2]\,V$, measurements and simulations for $V_{gs,str} = [-2.7, -3.2]\,V$ are in good agreement for all stress voltages and temperatures. (Data originally published in [51].

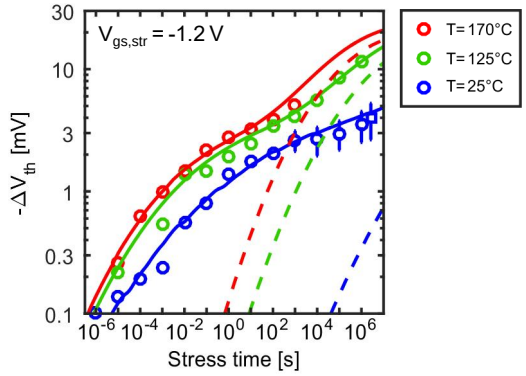

Figure 6.14: DC model validation at use conditions (real stress time): Comparison of the experimental data with the activation energy map model and the parameters given in Table 6.2 for the stress voltage $V_{gs} = -1.2\,V$ and temperatures $T = 25/125/170°C$. Even though the model has been calibrated only with temperature measurements from $T = 100 - 200°C$, measurements and simulations for $T = 25°C$ are in very good agreement. The ΔV_{th} at $T = 25°C$ is dominated for all stress times by the recoverable component and demonstrates the separation into the two components R and P with $\tau_{0,r}$ and $\tau_{0,p}$. Measurements by Hans Reisinger and Gerhard Rzepa.

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6.2.2 Industrial Application of the voltage-dependent activation energy maps

To understand and predict the threshold voltage shift of industrial stress tests such as burn-in tests and reliability monitoring tests, the voltage-dependent activation energy maps are very useful

Burn-in tests:
A burn-in test is a test to screen weak components that would otherwise fail during the qualified lifetime. For this, the components are stressed in an oven under high bias for up to 48 hours. Mostly several different tests are running in one oven, so that at end of stress the samples are disconnected from the stress, but remain in the oven and recover at high temperature ("practical" case). Ideally, the cool-down should occur in the oven with applied stress voltage. To prevent additional recovery after end of stress, the threshold voltage is measured at room temperature ("ideal" case). A comparison of the "ideal" and the "practical" case is shown in Fig. 6.15 a) for a typical burn-in stress condition. As a third case, an AC burn-in condition is shown with the "practical" recovery condition. For each case, a new sample is used.

- The "practical" case recovers significantly faster than the "ideal" case. After $t_{\mathrm{rec}} = 10^3$ s, the differences between the two cases amount to roughly 50 % ($\Delta V_{\mathrm{th}}(T_{\mathrm{rec}} = 30°\mathrm{C}) = 54\,\mathrm{mV}$ and $\Delta V_{\mathrm{th}}(T_{\mathrm{rec}} = 150°\mathrm{C}) = 38\,\mathrm{mV}$).
- A good verification of the temperature dependence is the calculation of the equivalent recovery temperature $\Theta_{\mathrm{rec}}(T = 30°\mathrm{C})$ as shown in Fig. 6.15 b). Since the recovery is dominated by the recovery of the recoverable component, the equivalent recovery time Θ_{rec} is calculated based on $\tau_{0,\mathrm{r}}$. Obviously, and as demonstrated in Fig. 6.15 b), the equivalent recovery of the two cases has to be the same due to the same amount of stress. With the same minimal measurement delay of $t_{\mathrm{d}} = 1\,\mu\mathrm{s}$, the shortest measured equivalent recovery time at $T = 150°\mathrm{C}$ is $\Theta_{\mathrm{rec}}(T = 30°\mathrm{C}) = 3\,\mathrm{ms}$.
- Burn-in tests can also be AC stress tests (with e.g. $V_{\mathrm{h}} = -2.2\,\mathrm{V}$, $V_{\mathrm{l}} = 0\,\mathrm{V}$ and $f = 100\,\mathrm{kHz}$). Consequently, there is already recovery during the high-temperature stress. Thus, the degradation and the following recovery after AC stress is significantly smaller in general than after DC stress and thus also less sensitive to the recovery temperature.

Measurements and simulations of the burn-in stress cases are in very good agreement and demonstrate the necessity of cool-down with applied bias and subsequent recovery measurement.

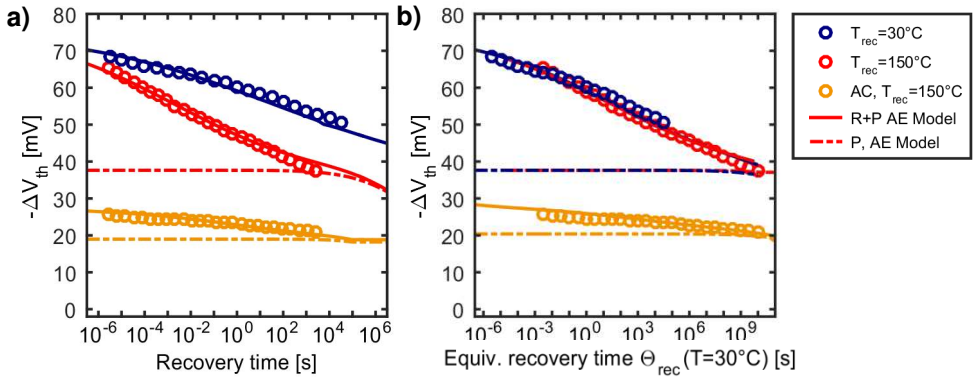

Figure 6.15: Measurements and simulation of the recovery of the threshold voltage shift after burn-in stress with $V_{\mathrm{gs,str}} = -2.2\,\mathrm{V}$ and $T_{\mathrm{str}} = 150°\mathrm{C}$. **a)** Recovery time and **b)** equivalent recovery time at $T = 100°\mathrm{C}$ for three different cases. Blue: The stress voltage is applied during cool-down and recovery at $T_{\mathrm{rec}} = 30°\mathrm{C}$. Red: $T_{\mathrm{str}} = T_{\mathrm{rec}} = 150°\mathrm{C}$. Orange: Recovery at $T_{\mathrm{rec}} = 150°\mathrm{C}$ after digital AC stress ($f = 100\,\mathrm{kHz}$, duty cycle=0.5, $V_{\mathrm{h}} = -2.2\,\mathrm{V}$, $V_{\mathrm{l}} = 0\,\mathrm{V}$). The solid (sum of quasi-permanent and recoverable component) and dashed (only quasi-permanent component) lines are simulated using the activation energy map.

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Fast Wafer Level Reliability tests (fWLR):
During fabrication, the MOSFETs are regularly tested concerning their reliability properties by fWLR monitoring stress tests. For this purpose, fWLR threshold voltage drift limits are needed to identify weak devices that would fail during the application before end-of-life (EOL) [201]. Since fWLR measurements need to be quickly performed, stress times are limited to less than ≈ 1 s. To obtain a measurable degradation, the temperature acceleration is therefore often higher than during standard qualification measurements [202]. Furthermore, standard measurement equipment with a measurement delay of $t_d = 1$ ms is used. In order to reduce the amount of recovery within the measurement delay, a commonly applied technique is the use of resistive heaters to be able to apply fast temperature changes to the device [88, 203]. The stress voltage is kept applied until the heater is switched off and the sample is cooled down to chuck temperature within seconds (see Section 2.5 and [85, 115]).

Until today, the standard lifetime models obtained from qualification measurements cannot be used to calculate these fWLR limits due to the lack of calibrated models considering different measurement times and stress/recovery temperatures of qualification and fWLR measurements. With the activation energy maps, it is possible to correlate these measurements and obtain the fWLR limits. The threshold voltage shift with stress time (same stress conditions) for three different measurement techniques with different measurement equipment, measurement delays, and measurement temperatures is compared in Fig. 6.16:

- With the resistive heater a recovery temperature $T_{rec} = 30°C$ is achieved with a measurement delay of $t_d = 10$ ms for the fWLR measurement with the Keithley 2636B.
- Qualification measurements are performed on wafer level with e.g. a measurement delay of $t_d = 1$ ms and $T_{str} = T_{rec} = 175°C$.
- The ultra-fast measurement equipment also used for the TA-MSM measurements has a measurement delay of $t_d = 1\,\mu s$.

The activation energy map model shows very good agreement with all three measurements. The fWLR measurement achieves the shortest effective measurement delay and therefore has the highest measured ΔV_{th}. A power-law fit to the last five measurement points as shown in Fig. 6.16 b) demonstrates the contradiction at EOL for the standard extrapolation technique using a power-law model such as (4.1). Different power-law exponents lead to different lifetimes.

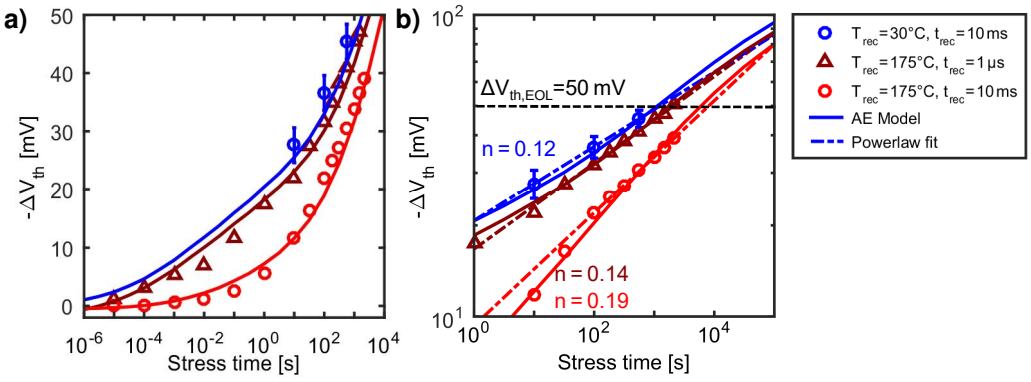

Figure 6.16: Comparison of three different measurement techniques after the same NBTI stress with $T_{str} = 175°C$, $V_{gs,str} = -2.2$ V. 1) fWLR Measurement with the resistive heater with $T_{rec} = 30°C$, $t_d = 10$ ms, 2) Qualification measurement at $T_{str} = T_{rec} = 175°C$ with $t_d = 10$ ms and 3) Measurements with the ultra-fast measurement technique at $T_{str} = T_{rec} = 175°C$ and $t_d = 2\,\mu s$. **a)** Linear y-scale. The solid lines are simulated using the activation energy map model. **b)** Logarithmic y-scale. The dashed lines correspond to power-law fits with the power-law exponent n.

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For a lifetime criterion of $\Delta V_{\text{th}} = 50\,\text{mV}$ as indicated in Fig. 6.16 b), the time until the criterion is reached varies by one order of magnitude dependent on the measurement technique.

6.3 Quasi-Permanent Component and Reverse Recovery Effect

When performing TA-MSM measurements, the temperatures for the base temperature and the temperature ramp have to be chosen to avoid post-stress degradation build-up as reported by Grasser *et al.* in [KWC3]. Similar degradation build-up during recovery measurements has also been reported in [98, 204, 205]. The basic mechanism is shown in Fig. 6.17 a) for $T_{\text{str}} = 200°\text{C}$. Regular recovery is observed for the first $\approx 1\,\text{ks}$, afterward the recovery turns around and a post-stress degradation builds up (further called "hump"). Typically no degradation is observed even for long stress times at $V_{\text{th}} = -0.3\,\text{V}$.

The post-stress degradation build-up increases with increasing stress time and starts to be visible after longer stress times e.g. $t_{\text{str}} = 1\,\text{ks}$. Furthermore, performing a bake step of one week at $T = 250°\text{C}$ and $V_{\text{gs}} = 0\,\text{V}$ before the start of the measurement (further called pre-bake) significantly reduces the post-stress degradation build-up as shown in Fig. 6.17 b). Instead of $\Delta V_{\text{th}} = 7\,\text{mV}$ (maximum BTI degradation before the post-stress degradation build-up at $t_{\text{str}} = 100\,\text{ks}$), the magnitude of the hump is only $\leq 2\,\text{mV}$ and not visible for $t_{\text{str}} \leq 100\,\text{ks}$. Another effect of the pre-bake is the increased contribution of the quasi-permanent component to the overall threshold voltage shift. The short-term recovery due to the recoverable component remains constant, but the quasi-permanent component increases from $\Delta V_{\text{th,p}} \approx 6.5\,\text{mV}$ to $\Delta V_{\text{th,p}} \approx 8\,\text{mV}$.

Grasser *et al.* have studied the annealing of the permanent component in [183]. Experimental results at $T = 250°\text{C}$ show an increase of defects with long capture and emission time constants. This increase saturates after ≈ 15 days at about 4 mV. This additional ΔV_{th} is temperature-dependent and drastically increases for $T = 350°\text{C}$. The additional ΔV_{th} at $T = 250°\text{C}$ and $T = 300°\text{C}$ is explained by a collection of normally distributed first-order processes [141], the additional drift at $T = 350°\text{C}$ is interpreted as the creation of additional defects [183].

The additional post-stress degradation build-up only decreases slowly as can be seen in Fig. 6.18 c). Grasser *et al.* have seen no influence of the $I_{\text{d}}V_{\text{g}}$ sweeps on the recovery of the additional post-stress degradation after 100 ks recovery [KWC3]. This already indicates that the charges contributing to the hump are due to either interface states with very long annealing times or fixed positive traps with time constants too large to react to $I_{\text{d}}V_{\text{g}}$ sweeps. Furthermore, comparing Fig. 6.18 a) and b), a clear temperature dependence of the post-stress degradation is identified. For $T = 150°\text{C}$ no reverse recovery is observed which can be explained by a narrow hydrogen-related defect band close to the valence band of Si, with a temperature and stress time-dependent difference between positively charged defects near the channel and the effective negative charge build-up near the gate due to an increasing and decreasing amount of hydrogen-related defects [KWC3].

To investigate the temperature-dependence of the post-stress degradation build-up, two different recovery measurements after 100 ks stress are compared in Fig. 6.18 b). The red curve shows the recovery and post-stress degradation build-up at constant temperature, whereas the temperature is linearly increased after 10 s within 500 s from $T = 200 - 250°\text{C}$. As can be seen in Fig. 6.18 b), the build-up is accelerated with increasing temperature. Assuming an Arrhenius-temperature activation for the individual processes contributing to recovery, a time-transformation is performed (as introduced for the TA-MSM and explained in Section 5.2.2) with a temperature-independent time constant $\tau_{0,\text{p}} = 0.57\,\text{ns}$ of the quasi-permanent component (see Table 6.2). As seen in Fig. 6.18 c), this leads to a very good agreement of the measurement with the temperature ramp and the measurement at constant temperature.

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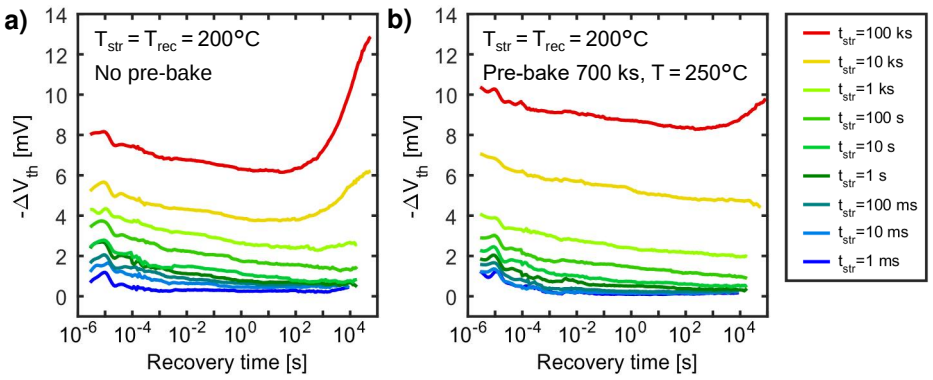

Figure 6.17: Post-stress degradation build-up at constant stress and recovery temperature of $T_{str} = T_{rec} = 200°C$ for two different samples for $V_{gs,str} = -1\,V$ and $V_{gs,rec} = -0.3\,V$. **a)** Without pre-bake and **b)** with pre-bake for 1 week at $T = 250°C$. The pre-bake significantly reduces the magnitude of the hump but causes an increase of the quasi-permanent component.

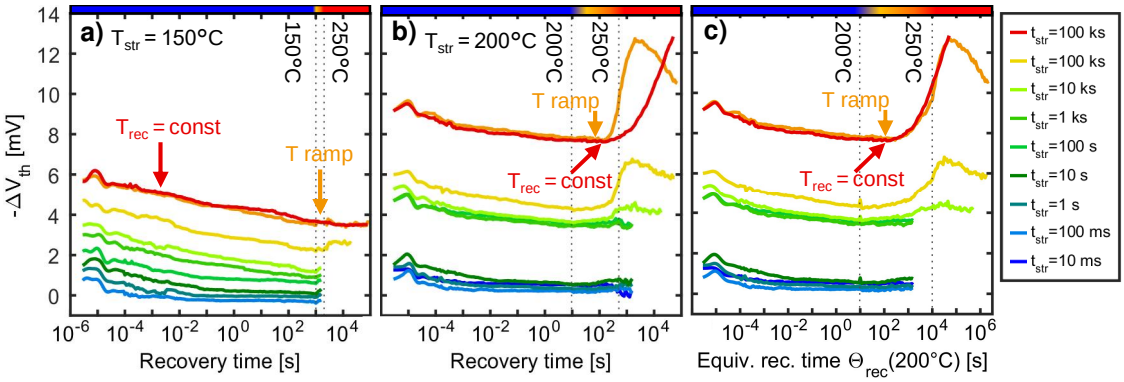

Figure 6.18: Temperature dependence of the post-stress degradation build-up and comparison of recovery measurements with and without temperature ramp (see temperature bar on top) for $V_{gs,str} = -1\,V$ and $V_{gs,rec} = -0.3\,V$. **a)** $T_{str} = 150°C$ and after 1 ks temperature ramp during recovery from $T = 150 - 250°C$. No humps observed within the measurement time, even with the temperature acceleration. **b)** $T_{str} = 200°C$ and after 10 s temperature ramps during recovery from $T = 200 - 250°C$. Post-stress degradation build-up with increasing stress times from 10 ks. **c)** Same measurement data as b) but with calculated equivalent recovery time $\Theta_{rec}(200°C)$. Measurement after 100 ks with and without recovery ramp show good agreement for the $\tau_{0,p} = 0.57$ ns as shown in Table 6.2. From this, a mean activation energy of $\approx 1.5 \pm 0.2$ eV is estimated.

Hence, the post-stress degradation build-up might be attributed to the same origin as the quasi-permanent defects: interface defects. This could be explained via the following scenario: During stress, interface states are created by the release of hydrogen via neutralization of trapped protons at the gate-side of the oxide. Since this process is quite slow, long stress times and high temperatures are required. After the release of the hydrogen, it quickly reacts with either passivated interface states or defects inside the oxide. However, in the gate-sided hydrogen release model [183] it is assumed that during stress hydrogen becomes trapped near the channel in a protonic configuration. During recovery, the protons are slowly released. Either these protons go back to the gate and a slow recovery of the quasi-permanent component is observed or a post-stress degradation builds-up due to depassivation of dangling bonds.

The reaction-limited process can only be seen on long time scales and is also accelerated by temperature. As estimated by Grasser *et al.*, the temperature dependence of the hump has an activation energy of $E_a \approx 1.8$ eV [KWC3]. The mean energy barrier for proton release in SiO_2 is $E_a \approx 1.7$ eV [206]. Considering an Arrhenius-like temperature activation and $\tau_{0,p}$, a mean

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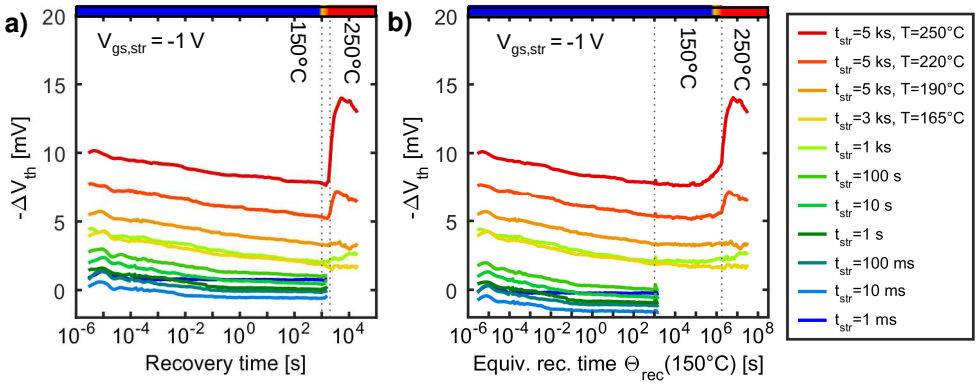

Figure 6.19: TA-MSM measurement with post-stress degradation build-up with stress temperatures up to $T_{str} = 250°C$ and a base temperature of $T = 150°C$ with temperature ramps after 1 ks from $T = 150 - 250°C$ (see temperature bar on top) for $V_{gs,str} = -1$ V. **a)** Original recovery time and **b)** equivalent recovery time $\Theta_{rec}(150°C)$. Post-stress degradation build-up can be observed starting from $T_{str} = 220°C$.

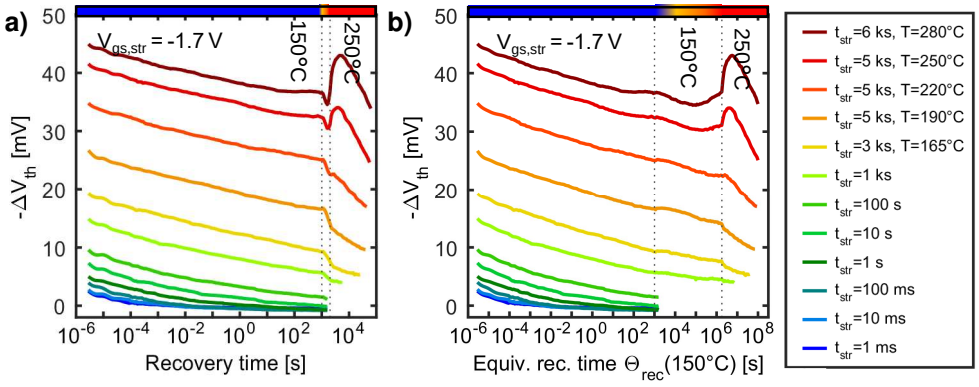

Figure 6.20: TA-MSM measurement with post-stress degradation build-up with stress temperatures up to $T_{str} = 250°C$ and a base temperature of $T = 150°C$ with temperature ramps after 1 ks from $T = 150 - 250°C$ (see temperature bar on top) for $V_{gs,str} = -1.7$ V. **a)** Original recovery time and **b)** equivalent recovery time $\Theta_{rec}(150°C)$. Post-stress degradation build-up can be observed starting from $T_{str} = 220°C$. The relative magnitude increases for lower stress voltages.

activation energy of 1.5 ± 0.2 eV is estimated from the measurements shown in Fig. 6.18 c).

To conclude, the temperature dependence of $\tau_{0,p}$ is consistent with the gate-sided hydrogen release model and with the findings shown in Fig. 6.18. Simulations in [KWC3] indicate that when the temperature is decreased below $T = 150°C$, the post-stress degradation is shifted to times longer than 10 years. As temperatures typically used in industrial applications are below $T = 150°C$, no post-stress degradation build-up should occur within the lifetime of the devices.

However, the post-stress degradation build-up interferes with the TA-MSM technique due to high-temperature acceleration and thus limits the maximum usable temperature for the experiments. TA-MSM measurements shown in Fig. 6.19 and Fig. 6.20 include stress temperatures up to $T_{str} = 280°C$ and we can clearly see humps for both stress voltages starting for stress temperatures higher than $T_{str} = 220°C$ for $V_{gs,str} = -1$ V and $T_{str} = 250°C$ for $V_{gs,str} = -1.7$ V. It is assumed that for $V_{gs,str} = -1.7$ V, the hump is solely blurred due to the accelerated recovery at $T = 250°C$ as voltage-dependent measurements shown in [KWC3] indicate a voltage-independent occurrence of the hump, but the relative height of the hump is higher for lower stress voltages (e.g. for $V_{gs,str} = -1$ V the $\Delta V_{th,hump} = 5$ mV, whereas the degradation directly after stress amounts to $\Delta V_{th,hump} = 10$ mV.

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To be clear, the humps are not a peculiarity of the technology under investigation, the same investigations have been performed in three different laboratories for different technologies by Grasser *et al.* [KWC3]. The effect shows a strong process dependence, but post-stress degradation clearly occurs in all technologies under stress conditions of no voltage acceleration and long stress and recovery times at high temperatures.

6.4 Benefits, Limitations, and Further Improvements of the TA-MSM Technique

Compared to constant temperature MSM measurements, the TA-MSM technique offers improved model accuracy due to its consideration of several stress and recovery temperatures. Furthermore, with the TA-MSM technique, only one measurement per stress and recovery voltage has to be performed. This speeds up the measurement time by at least a factor of 10 compared to the time required for the same experimental window with eMSM measurements at a minimum of three constant temperatures. Furthermore, only one sample is required per stress/recovery voltage condition. This decreases the influence of device-to-device variability for the model and additionally enables to study variability at the end-of-life by acquiring statistics for the same measurement condition.

A fundamental requirement of the TA-MSM technique is stable control of the temperature. In addition, it is necessary to record a reference prior to any stress experiment. An improvement to the shown measurement technique would be the reduction of the measurement base temperature to room temperature or even lower temperature (requires an active cooling system). This would further reduce the measurable capture and emission activation energy without the necessity for a faster measurement equipment. At e.g. room temperature, a recovery time $t_\mathrm{d} = 1\mu\mathrm{s}$ corresponds to $\Theta_\mathrm{rec}(100°\mathrm{C}) = 3 \cdot 10^{-8}\,\mathrm{s}$.

Furthermore, another impact of the measurement technique on the measured ΔV_th is the reduction of $V_\mathrm{th}(T)$ during the temperature ramp. Due to the constant current measurement, the threshold voltage is extracted at a different operating point when increasing the temperature, which translates into a lower measured threshold voltage and thus a lower recovery voltage (compare Section 2.1.1). As such, the recovery after stress is additionally accelerated. For the temperature ramp between $T = 100°\mathrm{C}$ and $T = 200°\mathrm{C}$, the change of the threshold voltage with temperature is $\Delta V_\mathrm{th}(\Delta T) = 0.1\,\mathrm{V}$ (see Fig. 5.9 b). The recovery voltage dependence is included in the model via the occupation probability maps as presented and discussed in Section 7.

Also, under certain circumstances (high stress temperatures, low stress voltages) an additional degradation can build up during recovery, consistent with a gate-sided hydrogen release mechanism as discussed in Section 4.3.2 and Section 6.3. To avoid this additional degradation build-up for the extraction of the activation energy map parameters, stress temperatures have been carefully chosen and have been restricted for the TA-MSM measurements to $T_\mathrm{str} = 190°\mathrm{C}$. Nonetheless, also the measurement in Fig. 6.7 a) with $V_\mathrm{gs} = -1\,\mathrm{V}$ shows a post-stress degradation build-up of $\approx 1\,\mathrm{mV}$ for long recovery times which is not taken into account in the model.

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Chapter 7

A Compact BTI Model for Arbitrary Gate Stress[1]

Until today, there is no commercially available circuit-compatible model considering BTI including recovery for silicon-based MOSFETs. Primary, the goal set for this thesis has been to develop a suitable model compatible with aging simulators which fulfills all requirements discussed in Chapter 4.1: Sufficient accuracy, consideration of stress history, different defect types, low simulation effort, acceptable experimental and low implementation effort. In this chapter, an efficient compact model to analytically calculate the threshold voltage shift induced by NBTI after an arbitrary gate bias stress, fully meeting all five requirements stated above, is presented.

The model has to reproduce all features of NBTI presented in Chapter 3: The stress-voltage dependence, long-term recovery, temperature dependence, recovery during AC stress as well as degradation and recovery during analog stress. The intended accuracy of the model (agreement between model and experimentally observed ΔV_{th}) has to be better than 10%, which is sufficient for all industrial applications as $\delta \geq 10\%$ due to sample-to-sample, lot-to-lot and wafer-to-wafer variation [207, 208]. Current BTI models used within aging simulators [154, 155, 158] neglect recovery and thus mostly overestimate the total degradation by roughly a factor of 2.

The voltage-dependent activation energy map presented in Section 6.1.3 is only valid for digital stress with $V_{\text{gs,str}} = V_{\text{h}}$ and $V_{\text{gs,rec}} = V_{\text{l}} = V_{\text{th}}$ (measurement condition), which is of no use for a circuit simulator [KWJ2]. An extension to the voltage-dependent activation energy map model for any arbitrary stress pattern requires consideration of the full stress history of the defects as e.g. at higher gate voltages different defects become accessible which have not been active before and as such have a different "history".

To include arbitrary voltage stress in the model, the following steps have to be performed and are discussed in detail in this chapter:

1. The main problem arising for arbitrary stress patterns is the challenge of how to simplify the mathematical calculation. In this work, the stress pattern is discretized by using N_{V} voltage classes and the arbitrary stress pattern is approximated by a digital AC pattern per voltage class. The division of the defects into voltage classes and the discretization scheme are described in detail in Section 7.1.

2. In the next step, the discretization of the arbitrary stress signal into digital AC pattern per voltage class necessitates the introduction of transformed stress times as well as transformed recovery times considering the voltage acceleration for stress and recovery. The voltage dependence of the capture time constants is introduced in Section 7.2 and the voltage dependence of the emission time constants is introduced in Section 7.3.

[1] This chapter is based on a publication of the author of this thesis [KWJ3].

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3. Each voltage class contributes a ΔV_{th} to the overall threshold voltage shift and has a different distribution of capture and emission activation energies dependent on the class voltage. This is included in the model and described in Section 7.4 via differential activation energy maps calculated using the voltage-dependent model derived in Section 6.1.3.

4. Furthermore, the defect occupation probability after digital AC stress can be easily calculated as described in Section 4.4.1 [162]. However, the resulting digital AC stress patterns from arbitrary stress can have up to n sequentially following charging/discharging pulses and thus require a more complex calculation, which is still numerically solvable, but calculation time depends on the number of pulses n (see Fig. 7.10. Therefore, the necessary extension of (4.25) for a mathematically efficient solution of n pulses is derived in Section 7.5.

5. In the last step, the implementation of the effects discussed in points 1-4) into the model is described in Section 7.6. The overall threshold voltage shift after arbitrary gate stress is then calculated as the sum of all contributions to the threshold voltage shift of the voltage classes.

In this chapter, an accurate and efficient model to consider arbitrary voltage gate stress is derived. Validation of the model, including a comparison of model and measurement after analog AC stress as well as the application to circuit simulations with the example of two different ring oscillators presented in Section 7.7. Section 7.8 concludes the chapter with a summary of the model properties and approximations made during the development of the model.

7.1 Voltage Classes

The defect occupation probability after DC and digital AC stress can be calculated following (4.14) and (4.25). For arbitrary stress patterns, one possibility is to calculate the threshold voltage shift iteratively for each point in $V_{\text{gs}}(t)$ by calculating the occupancy in a stepwise manner according to (4.17). This is computationally very intensive and thus impracticable for the use in a circuit simulator for lifetime simulations. The problem is solved by the following four approximations:

1. N_{V} voltage classes with corresponding class voltages $V_{\text{bin},i}$ ($i \in \mathbb{N} | \, 1 \leq i \leq v$) are introduced. The occupation probability is calculated for each voltage class. Obviously, a too small number of voltage classes introduces errors while too many increase the computational effort without significantly improving the accuracy as discussed in Section 7.8.

2. Per voltage class, the stress pattern $V_{\text{gs}}(t)$ is approximated by a digital AC pattern.

3. For high model accuracy and consideration of the decrease and increase of the capture and emission time constants with applied gate voltage, it is mandatory to calculate a transformed stress time for $V_{\text{gs}}(t) \geq V_{\text{bin},i}$ as well as a transformed recovery time for $V_{\text{gs}}(t) \leq V_{\text{bin},i}$.

4. A periodic $V_{\text{gs}}(t)$ pattern is required for lifetime models. However, any analog circuit has a repetitive pattern within a dedicated mode, therefore this requirement should always be fulfilled. Furthermore, applications can feature multiple periodicities on different time scales e.g. day-night cycles, power-down modes, and different mission profiles.

As an example, three voltage classes within the energy bands of a pMOS are illustrated in Fig. 7.1. Only when a certain threshold value of the stress voltage (the class voltage $V_{\text{bin},i}$) is reached, the defects of the voltage class N_i can be charged within a finite stress time. In Fig. 7.1 three cases are illustrated:

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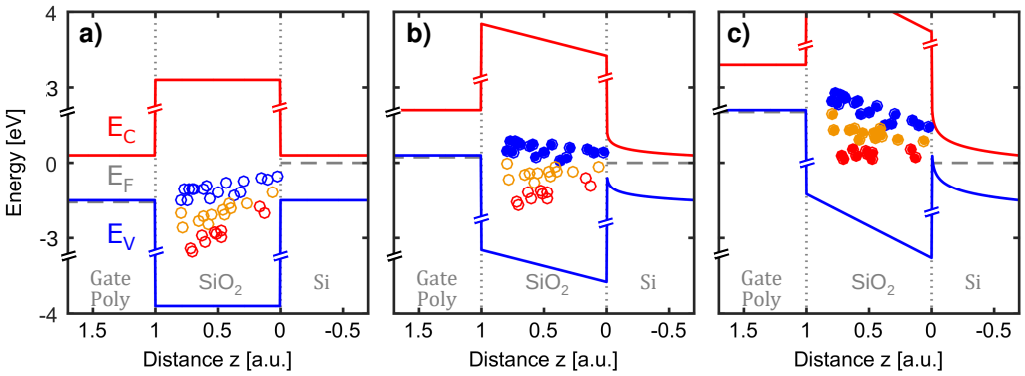

Figure 7.1: Exemplary schematic of three voltage classes within the energy band of a pMOS: **a)** Without applied stress voltage. All defects remain uncharged. **b)** $V_{\mathrm{gs,str}} = \mathrm{V_{gs,blue}}$, all defects are shifted with the applied stress voltage. The blue defects are located below the channel level but above the gate fermi level with a finite capture time. **c)** Increased stress voltage $V_{\mathrm{gs,str}} = \mathrm{V_{gs,red}}$, all defects are further shifted. Blue, orange and red defects are located below the Fermi level and will be charged within a finite capture time. The capture times for the blue and orange defects are reduced (see (7.2)).

- No stress voltage is applied (flat-band condition) as shown in Fig. 7.1 a). All defects within the oxide and the interface are located above the Fermi level E_{F} and cannot be charged.
- The stress threshold voltage is increased to the stress threshold voltage of the blue defects $V_{\mathrm{gs}} = V_{\mathrm{gs,blue}}$ as shown in Fig. 7.1 b). All defects are shifted with V_{gs} to lower energies and the blue defects are now located below the Fermi level and have a finite capture time constant τ_{c}. The capture time constant τ_{c} of the blue defects depends then on the type and location of the defect within the oxide.
- The stress voltage is further increased to the stress threshold voltage of the red defects $V_{\mathrm{gs}} = V_{\mathrm{gs,red}}$ as shown in Fig. 7.1 c). The defects further shift to lower energies and the blue, orange, and red defects are located below E_{F}. As a result, the capture time constants τ_{c} of all defects are finite and the capture time constants τ_{c} of the blue and orange defects are reduced compared to stress at their stress threshold voltages.

The class voltages $V_{\mathrm{bin},i}$ are used to approximate the $V_{\mathrm{gs}}(t)$ pattern by digital AC patterns with n stress and recovery pulses dependent on the $V_{\mathrm{gs}}(t)$ pattern. An exemplary discretization of the stress pattern is shown in Fig. 7.2 a):

- For each voltage class, the digital AC pattern is different as shown in Fig. 7.2 b) and c).
- If the stress voltage is higher than the threshold stress voltage of each voltage class ($V_{\mathrm{gs}}(t) \geq V_{\mathrm{bin},i}$), the capture time constants of the defects within this voltage class decrease. Equivalently, this can be translated into a longer stress time $t_{\mathrm{s,trans}}$ at the class voltage as shown in Fig. 7.2 d) and e).
- The emission time constants are also recovery voltage-dependent as explained in Section 3.3.1. Thus, if $V_{\mathrm{gs}}(t) \leq V_{\mathrm{bin},i}$, a transformed recovery time $t_{\mathrm{r,trans}}$ is calculated.

The modeling of the translation into a digital AC pattern with $t_{\mathrm{s,trans}}$ and $t_{\mathrm{r,trans}}$ is described in Section 7.2 and Section 7.3.

7.2 Voltage-Dependent Capture Time Constants

The experimental separation of the contributions of each voltage class to the overall ΔV_{th} is challenging because e.g. an equivalent DC stress required to charge the red defects in Fig. 7.1 c)

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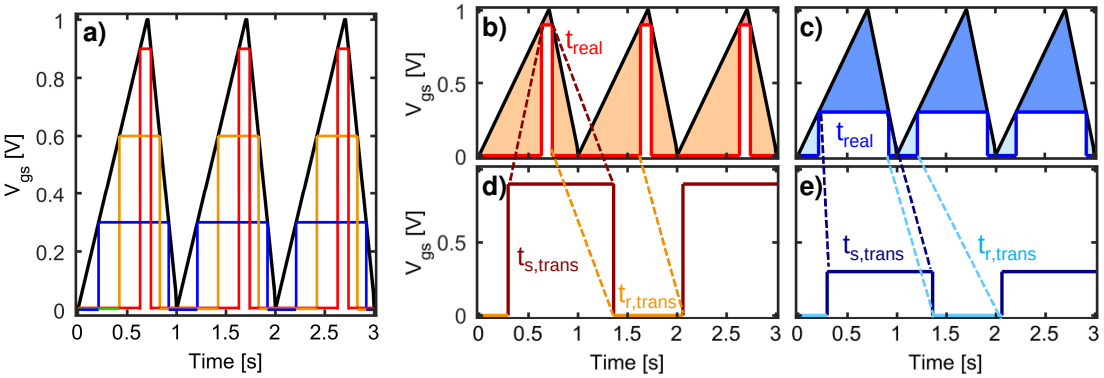

Figure 7.2: Exemplary discretization of a sawtooth V_{gs} stress pattern. **a)** Stress pattern for three voltage classes (blue, orange, red) and the discretization of the pattern. **b)** and **c)** Discretization for the red and blue defects. If the stress voltage is higher than the class voltage (dark red and dark blue shaded area in b) and c), the effective stress time is increased according to (7.3). For recovery voltages lower/higher than the initial threshold voltage (light red and light blue shaded area in b) and c), the effective recovery time is accelerated/decelerated according to (7.4). **d)** and **e)** The digital approximation of the stress pattern with the effective stress and recovery times of the blue and red defects in b) and c).

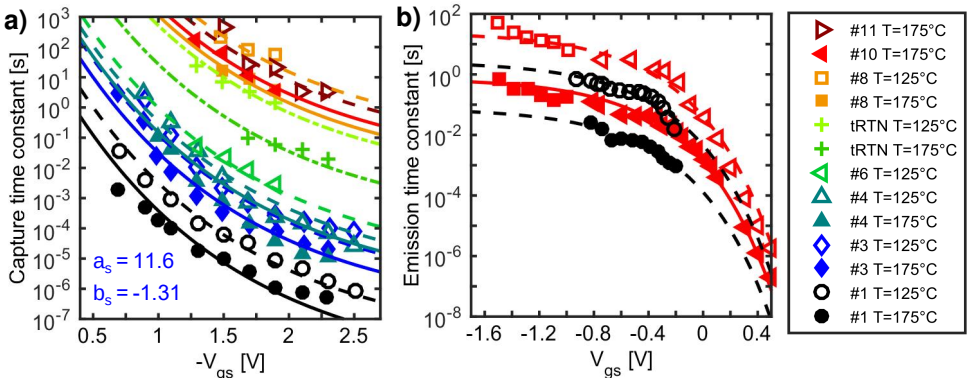

Figure 7.3: Voltage and temperature dependence of the capture and emission time constants, measurement data of selected defects from [92] and [107]. **a)** A strong stress voltage dependence of the capture time constants is observed. Lines correspond to a double exponential fit following (7.1). **b)** The dependence of the emission time constants on the recovery voltage is shown for two defects measured in the linear and saturation regime.

($V_{gs,str} = V_{gs,red}$) also includes the threshold voltage shift introduced by the blue, orange, and red defects. Nonetheless, TDDS data on small-area MOSFETs with only a small number of defects can be used to study the individual capture and emission time constants of each defect as shown in Fig. 3.5 and Fig. 3.6.

Extracted capture and emission time constants from TDDS measurements of 11 defects are shown in Fig. 7.3 a) and b) as presented in [92] and [107]. As discussed in Section 6.1.1, the extracted capture time constants show a clear Arrhenius temperature dependence. Furthermore, a non-linear dependence of $\log_{10}(\tau_c)$ with the applied stress bias is observed. For the analytic model, a common fit of the data shown in Fig. 7.3 a) is performed with a different offset per defect. The offset is irrelevant for the model because all times are calculated relatively. The dependence of the capture time constants with applied stress bias V_{gs} is obtained as:

$$\log_{10}(\tau_c) = a_s \cdot e^{-\frac{V_{gs}}{b_s}} \tag{7.1}$$

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with $a_s = 11.6$ and $b_s = -1.31\ \mathrm{V}^{-1}$. Thus, for a certain defect with a threshold stress voltage of $V_{\mathrm{bin},i}$, the stress voltage $V_{\mathrm{gs,str}}$ is higher than $V_{\mathrm{bin},i}$ according to (7.1), the stress time required to charge this defect is reduced (reduced capture time constant).

The reduction of the capture time constants can be translated in a transformed stress time as illustrated in Fig. 7.2 via

$$\frac{t_{\mathrm{s,trans}}}{t_{\mathrm{s,real}}} = \frac{\tau_{\mathrm{c}}(V_{\mathrm{gs}})}{\tau_{\mathrm{c}}(V_{\mathrm{bin},i})} \tag{7.2}$$

Thus, the transformed stress time $t_{\mathrm{s,trans}}$ is calculated for each voltage class $V_{\mathrm{bin},i}$ by inserting (7.1) in (7.2):

$$t_{\mathrm{s,trans}}(i) = t_{\mathrm{s,real}} \cdot 10^{a_s\left(\exp\left(-\frac{V_{\mathrm{gs}}(t)}{b_s}\right)-\exp\left(-\frac{V_{\mathrm{bin},i}}{b_s}\right)\right)}. \tag{7.3}$$

The transformed stress times are used for the calculation of the defect occupancy maps in Section 7.5. The model implementation is described in Section 7.6.

7.3 Voltage-Dependent Emission Time Constants

Conventional TDDS measurements and pulsed TDDS measurements reveal a dependence of the emission time constants on the recovery voltage $V_{\mathrm{gs,rec}}$ for switching traps [92] and [107], whereas also bias-independent τ_{e} have been observed for defects being in a neutral meta-stable state without switching possibility to the stable state $(1')$ associated with fixed oxide traps (see explanation in Section 3.3.1 and Section 4.3.2). As shown in Fig. 7.3 b), an exponential dependence of the emission time constants on the recovery voltage $V_{\mathrm{gs,rec}}$ is observed for the switching traps. Due to the different dependence on the recovery voltage of single defects, the acceleration obtained from TDDS measurements is not used in the derived model.

Thus, the recovery voltage dependence after the same amount of degradation has been studied on large-area devices with many defects as shown in Fig. 7.4 for two stress times. The measurements in Fig. 7.4 show the following effects:

- An increase of the recovery voltage $V_{\mathrm{gs,rec}} \leq V_{\mathrm{th}}$ leads to an acceleration of the recovery as can be seen in Fig. 7.4 a) and b), whereas a decrease in the recovery voltage for $V_{\mathrm{th}} \leq V_{\mathrm{gs,rec}} \leq V_{\mathrm{gs,str}}$ leads to a deceleration of the recovery.
- If the recovery time is longer than the stress time, a further increase in the ΔV_{th} is observed (see $t_{\mathrm{str}} = 1\,\mathrm{s}$ and $V_{\mathrm{gs,rec}} \geq -1.5$ in Fig. 7.4 a). The time from reversal of the recovery to degradation depends on the applied recovery voltage with respect to the initial stress voltage and stress time.
- For long stress times, multiplication of the recovery time with an acceleration factor as shown in Fig. 7.5 a) leads to a universal recovery curve [56, 209].
- The extracted acceleration factor in dependence on the recovery voltage is shown in Fig. 7.5 b) and spans more than 8 orders of magnitude.

Based on these findings, the recovery voltage dependence is modeled as:

$$t_{\mathrm{r,trans}} = t_{\mathrm{r,real}} \cdot \underbrace{a_{\mathrm{r}} b_{\mathrm{r}}^{V_{\mathrm{gs}}}}_{a_{\mathrm{tr}}}. \tag{7.4}$$

The parameters $a_{\mathrm{r}} = 28.3$ and $b_{\mathrm{r}} = 800$ are determined by a fit of (7.4) to the extracted acceleration factor (black dashed line in Fig. 7.5 b)).

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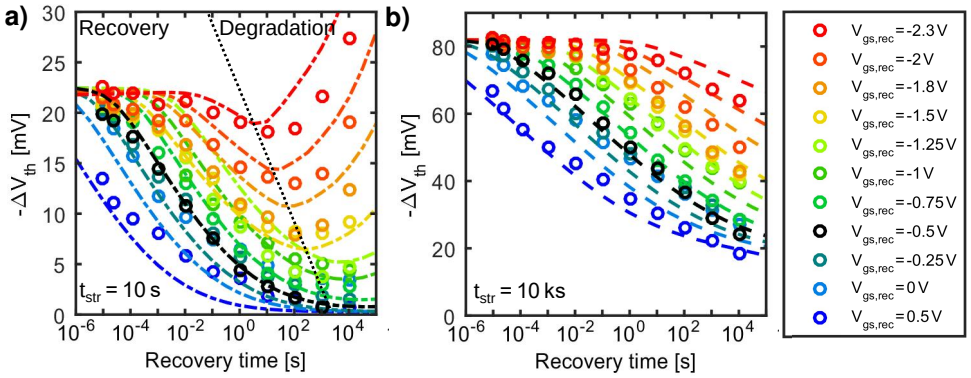

Figure 7.4: Measured threshold voltage recovery dependent on the recovery voltage in comparison with the activation energy map model including the recovery voltage dependence. Stress conditions for all measurements: $T = 125°\mathrm{C}$ and $V_{\mathrm{gs,str}} = -2.8\,\mathrm{V}$ for two different stress times **a)** $t_{\mathrm{str}} = 1\,\mathrm{s}$ and **b)** $t_{\mathrm{str}} = 10\,\mathrm{ks}$ (measurement data from Gunnar Rott , partly published in [KWJ3]). The recovery voltages range from $V_{\mathrm{gs,rec}} = -2.3\,\mathrm{V}$ to $V_{\mathrm{gs,rec}} = +0.5\,\mathrm{V}$. Dashed lines correspond to the simulated threshold voltage shift obtained with (7.4). Measurements and model are in good agreement.

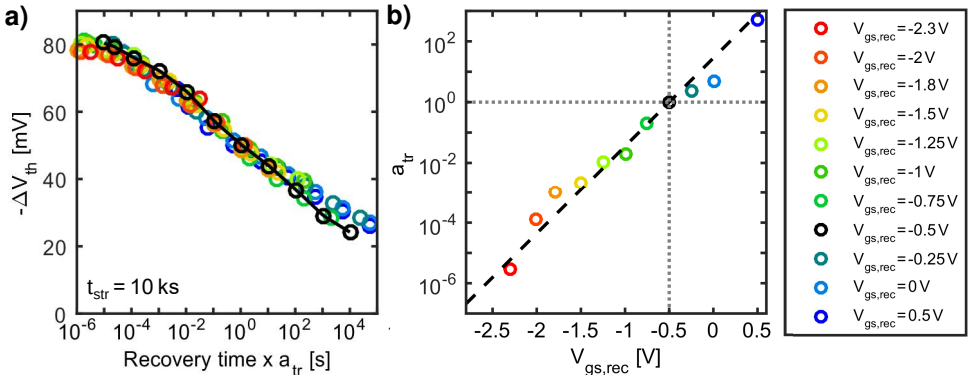

Figure 7.5: Recovery time dependence with recovery voltage: Multiplication of the recovery time with the acceleration factor $\alpha(V_{\mathrm{gs,rec}})$ leads to a universal recovery curve. **a)** Recovery after the same amount of degradation for different recovery voltages (same data as shown in Fig. 7.4 b)) considering the recovery time acceleration with an acceleration factor α. **b)** Extracted acceleration factor in dependence of the recovery voltage. The color of the recovery voltage in b) corresponds to the same color in a).

As there are many defects of different voltage classes that contribute to the overall threshold voltage shift, (7.4) can therefore only represent the cumulative defect behavior of all voltage classes N_{V}. Nonetheless, the implementation of this recovery voltage dependence for all voltage classes reproduces the recovery measurements of Fig. 7.4 very well.

The model also predicts the degradation reversal if the recovery time is significantly longer than the preceding stress time as it is just an onset of stress at this recovery voltage. In addition, good agreement is achieved for all recovery voltages. The contribution of each voltage class N_i to the overall threshold shift for the measurements in Fig. 7.4 is shown for an exemplary set of 11 voltage classes in Fig. 7.6 for three different recovery voltages with $V_{\mathrm{gs,str}} = -2.8\,\mathrm{V}$. Dependent on the recovery voltage, either all defects show recovery ($V_{\mathrm{gs,rec}} = 0\,\mathrm{V}$) or only defects with $V_i \geq V_{\mathrm{gs,rec}}$ recover. For recovery times larger than the stress time of $t_{\mathrm{str}} = 10\,\mathrm{ks}$, additional degradation is observed for $V_{\mathrm{gs,rec}} = 2.3\,\mathrm{V}$.

Due to the non-uniformly distributed class voltages, the highest contribution to the overall ΔV_{th} stems from $V_{\mathrm{bin}} = -2.8\,\mathrm{V}$, whereas barely any contribution stems from $V_{\mathrm{bin}} \geq -0.5\,\mathrm{V}$. Obviously, the highest model accuracy is obtained for $N_{\mathrm{V}} \to \infty$ as discussed in Section 7.8.

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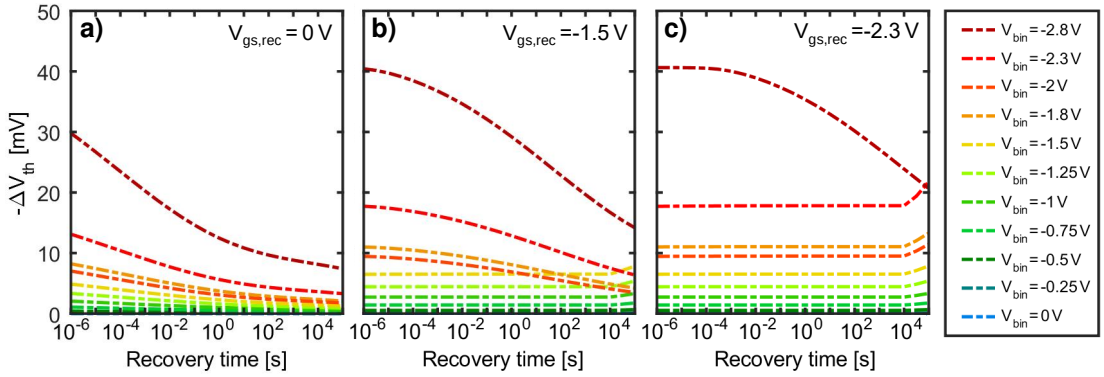

Figure 7.6: Contribution of each voltage class to the overall threshold voltage shift for three different recovery voltages and $t_{str} = 10\,\text{ks}$ as shown in Fig. 7.4 b). **a)** For $V_{gs,rec} = 0\,\text{V}$ all voltage classes show recovery. **b)** For $V_{gs,rec} = -1.5\,\text{V}$ all voltage classes with $-1.5\,\text{V} < V_{bin}$ show recovery. **c)** For $V_{gs,rec} = -2.3\,\text{V}$ only recovery is observed for the highest class voltage $V_{bin} = -2.8\,\text{V}$. All lower voltage classes result in increasing ΔV_{th} with increasing recovery time.

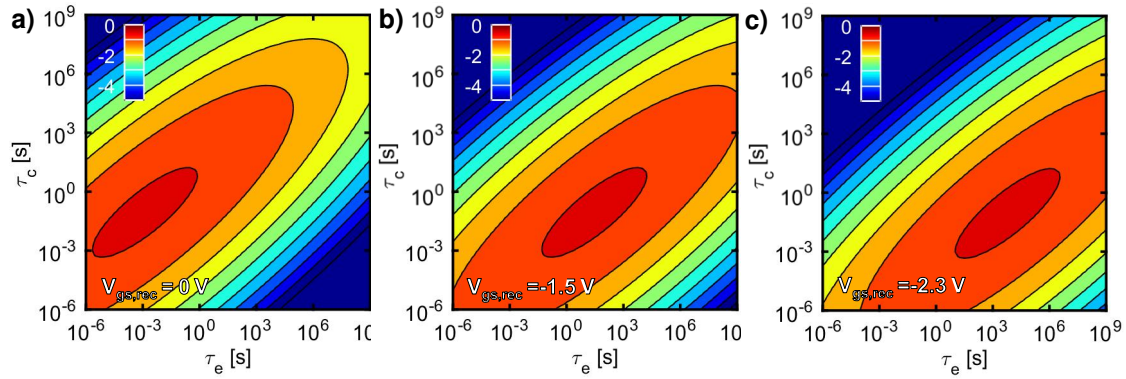

Figure 7.7: Recovery voltage dependence of the recoverable component of the capture and emission time maps at $T = 125°\text{C}$ and $V_{gs,str} = -2.8\,\text{V}$ for three different recovery voltages: **a)** $V_{gs,rec} = 0\,\text{V}$, **b)** $V_{gs,rec} = -1.5\,\text{V}$, **c)** $V_{gs,rec} = -2.3\,\text{V}$ following (7.4) with the parameters given in Table 7.1. The defect distribution and its contribution to the overall threshold voltage shift is shown in a logarithmic color scale, the density value z corresponds to a ΔV_{th} of $10^{\mathbf{z}}\,\text{V/eV}^2$.

For a finite number of voltage classes a smart binning of the voltage classes has to be chosen to obtain a high model accuracy. The voltage classes are implemented in the model as follows: the highest voltage class is the maximum stress voltage $V_{bin,max} = \max(V_{gs,str})$. Furthermore, the voltage classes are distributed on a logarithmic scale with decreasing voltage steps towards $V_{bin,max}$.

The effect of the recovery voltage on the activation energy map is illustrated in Fig. 7.7 for the recoverable component[2]. Decreasing the recovery voltage shifts the emission time constants to higher time constants and thus causes a deceleration of the recovery. Vice versa, increasing the recovery voltage even to positive voltages decreases the emission time constants and accelerates the recovery.

[2]The recovery voltage-dependent measurements shown in Fig. 7.4 only allow a conclusion on the behavior of the recoverable component as the recovery time at $V_{gs,rec}$ is too short to observe recovery of the quasi-permanent component. Nonetheless, rectangular AC measurements and simulations shown in Fig. 7.15 demonstrate that the quasi-permanent component also shows a recovery voltage dependence.

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7.4 Differential Activation Energy Maps

In the presented model, the overall threshold voltage shift consists of the contributions to the threshold voltage shift of all voltage classes N_V. The activation energy maps as presented in Section 6.1 correspond to the sum of all defects N_i with voltage class $V_{bin} \leq V_{gs,str}$. To model ΔV_{th} after arbitrary stress, the contributions from the voltage classes have to be separated. Thus, differential activation energy maps $g_{diff}(E_c, E_e)$ corresponding to the defect density of each voltage class are introduced.

The differential activation energy map consists of the defects additionally contributing to the threshold voltage shift when changing the stress voltage from V_i to V_{i+1}. For the quasi-permanent component, as the mean capture energy is stress voltage-independent ($k_p = 0$), the differential energy maps is the difference in the amplitudes:

$$g_{diff,p}(E_c, E_e) = g(V_{i+1}) - g(V_i) = A_p(V_{i+1}) - A_p(V_i). \tag{7.5}$$

Since $k_r \neq 0$, the capture activation energies of the recoverable component are voltage-dependent, thus $g(V_{i+1})$ is calculated following (4.13) and the differential activation energy map of the recoverable component is

$$g_{diff,r}(E_c, E_e) = g(V_{i+1}) - g(V_i, \Delta E_c). \tag{7.6}$$

The capture activation energies exhibit an additional shift ΔE_c for the lower voltage class due to $V_{i+1} > V_i$ (as discussed in Section 7.2). This has to be considered via:

$$\Delta E_c = k_B T \log\left(\frac{\tau_{c,real(V_i)}}{\tau_{c,trans(V_{i+1},V_i)}}\right) \tag{7.7}$$

In Fig. 7.8 exemplary differential activation energy maps are shown for $V_1 = 2\,V$ and $V_2 = 2.1\,V$. Due to the subtraction in (7.6), the shift of the capture activation energies ΔE for the recoverable component leads to a positive and negative contribution of the recoverable component R to the differential energy map. In fact, the negative contribution is negligible and only visible due to the logarithmic color scale. The capture activation energies of the quasi-permanent component remain unaffected as $k_p = 0$ and $\Delta E_c = 0$.

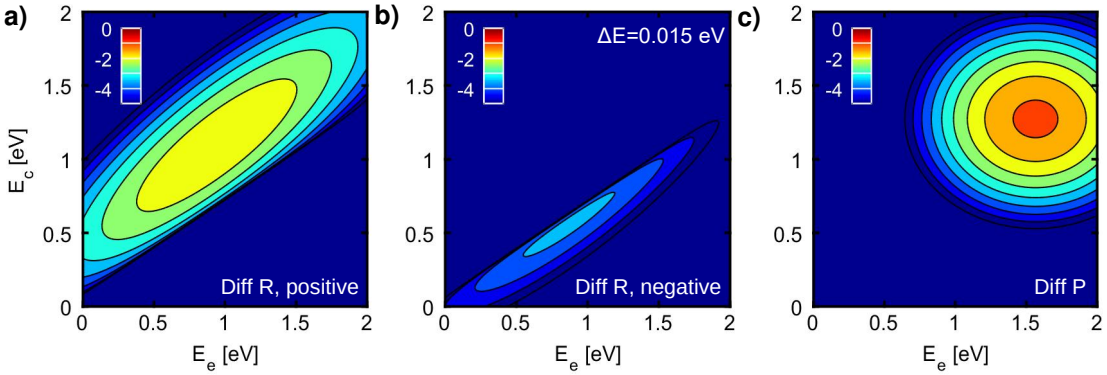

Figure 7.8: Differential activation energy maps obtained with the parameters presented in Table 6.2 following (7.6), showing the contribution of defects getting activated when changing the stress voltage from $V_{gs,str} = -2$ to $V_{gs,str} = -2.1$. All maps are shown on a logarithmic color scale, the density value z corresponds to a ΔV_{th} of $10^z\,V/eV^2$. **a)** Recoverable component (positive contribution), **b)** recoverable component (negative contribution) and **c)** quasi-permanent component.

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7.5 Occupation Probability Maps

The discretization of any $V_{gs}(t)$ pattern leads to arbitrarily complicated digital AC patterns with j stress and j recovery pulses within one period (see example in Fig. 7.2). Nonetheless, a periodic $V_{gs}(t)$ pattern is assumed. Even for analog circuits, this is always fulfilled at least for a certain circuit operation mode. In Section 4.4.1, the calculation of the defect occupancy O is discussed as being analogous to the response of an RC-element to an AC stress time t_{AC}. The equations for constant stress and recovery are based on the occupancy after DC stress following (4.14) and are derived starting from the occupancy after digital AC stress with $j = 1$ stress and recovery pulses according to (4.25).

In this chapter, the defect occupancy O of a digital AC pattern with j stress and recovery pulses within one period is derived. First, the case of $j = 2$ stress and recovery pulses is calculated. Second, the equations are generalized for j stress and j recovery pulses with the occupancy after n periods of stress with interruption after the high pulse O_n^{Hi} ($i \in \mathbb{N} | \, 1 \leq i \leq j$) and the occupancy with interruption after the low pulse O_n^{Li} ($i \in \mathbb{N} | \, 1 \leq i \leq j$). For $j = 2$, the response to the first charging pulse $\Delta t_{s,1}$ (high phase H) is named O_n^{H1} following (7.8) and the response after the first recovery pulse $\Delta t_{r,1}$ (low phase l) is named O_n^{L1} following (7.9). The occupancy after the second charging pulse $\Delta t_{s,2}$ is named O_n^{H2} following (7.10) and the occupancy after the second recovery pulse $\Delta t_{s,2}$ is named O_n^{L2} following (7.11):

$$O_n(\Delta t_{s,1}) = O_n^{H1} = 1 - (1 - O_{n-1}^{L2}) \cdot e^{-\frac{\Delta t_{s,1}}{\tau_c}} \tag{7.8}$$

$$O_n(\Delta t_{r,1}) = O_n^{L1} = O_n^{H1} \cdot e^{-\frac{\Delta t_{r,1}}{\tau_e}} \tag{7.9}$$

$$O_n(\Delta t_{s,2}) = O_n^{H2} = 1 - (1 - O_n^{L1}) \cdot e^{-\frac{\Delta t_{s,2}}{\tau_c}} \tag{7.10}$$

$$O_n(\Delta t_{r,2}) = O_n^{L2} = O_n^{H2} \cdot e^{-\frac{\Delta t_{r,2}}{\tau_e}} \tag{7.11}$$

with $O_0^{L2} = 0$.

The abbreviations $d_1, ...d_j$ and $u_1, ...u_j$ for the time-independent factors are introduced for the up- and down-phases of the signal:

$$u_j = e^{-\frac{\Delta t_{s,j}}{\tau_c}} \text{ and } d_j = e^{-\frac{\Delta t_{r,j}}{\tau_e}}. \tag{7.12}$$

Using equations (7.8), (7.9), (7.10), (7.11) a recursive equation for O_n^{L2} can be given:

$$\begin{aligned} O_n^{L2} &= (1 - (1 - (1 - (1 - O_{n-1}^{L2}) \cdot u_1) \cdot d_1) \cdot u_2) \cdot d_2 \\ &= d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2 + O_{n-1}^{L2} \cdot u_1 d_1 u_2 d_2. \end{aligned} \tag{7.13}$$

For $n = 1$, we obtain:

$$O_1^{L2} = d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2, \tag{7.14}$$

and for $n = 2$, we obtain:

$$O_2^{L2} = O_1^{L2} + O_1^{L2} \cdot u_1 d_1 u_2 d_2. \tag{7.15}$$

For each additional period, one term is added to (7.15). The result after N periods can be a given by a sum formula:

$$\begin{aligned} O_N^{L2} &= \sum_{n=1}^{N} (d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2) \cdot (u_1 d_1 u_2 d_2)^{n-1} \\ &= (1 - (u_1 d_1 u_2 d_2)^N) \cdot \frac{d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2}{1 - u_1 d_1 u_2 d_2} \end{aligned} \tag{7.16}$$

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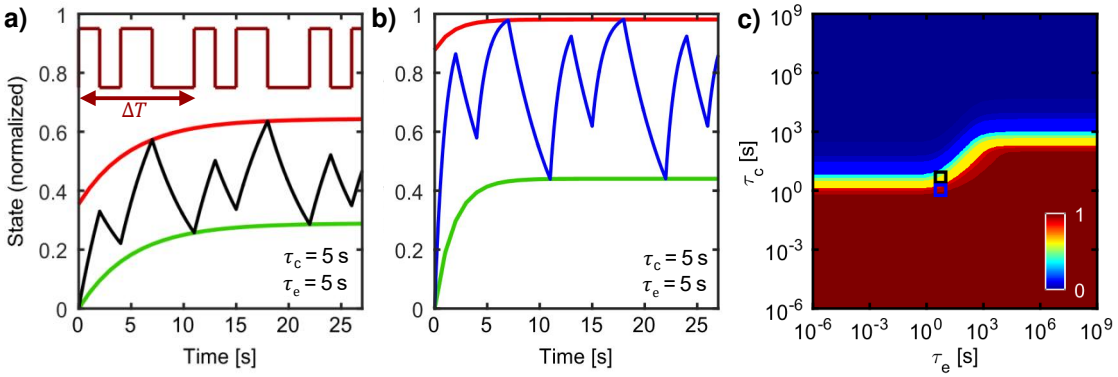

Figure 7.9: Defect occupancy for a pulse pattern with $j = 2$. **a)** $\tau_c = \tau_e = 5\,\mathrm{s}$ and **b)** $\tau_c = 1\,\mathrm{s}$, $\tau_e = 5\,\mathrm{s}$. **c)** Occupancy map dependent on the capture and emission times, after the second high pulse. The squares mark the positions of the capture and emission times of a) and b).

The period ΔT is given by:

$$\Delta T = \Delta t_{\mathrm{s,tot}} + \Delta t_{\mathrm{r,tot}} \tag{7.17}$$

with

$$\Delta t_{\mathrm{s,tot}} = \sum_{i=1}^{j} \Delta t_{\mathrm{s,i}} \text{ and } \Delta t_{\mathrm{r,tot}} = \sum_{i=1}^{j} \Delta t_{\mathrm{r,i}}. \tag{7.18}$$

The number of periods N is replaced by the AC stress time

$$t_{\mathrm{AC}} = N \cdot \Delta T \tag{7.19}$$

and the AC charging time constant $\bar{\tau}$ is introduced as

$$\frac{1}{\bar{\tau}} = \frac{\Delta t_{\mathrm{s,tot}}}{\Delta T \cdot \tau_c} + \frac{\Delta t_{\mathrm{r,tot}}}{\Delta T \cdot \tau_e}. \tag{7.20}$$

Inserting (7.19) and (7.20) in (7.16) gives the envelope function after the last recovery pulse in dependence of the AC stress time

$$O^{\mathrm{L2}}(t_{\mathrm{AC}}) = (1 - \mathrm{e}^{-\frac{t_{\mathrm{AC}}}{\bar{\tau}}}) \cdot \frac{d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2}{1 - u_1 d_1 u_2 d_2}. \tag{7.21}$$

The occupation probability maps after the end of the first or second stress phase can be calculated using the set of equations (7.8), (7.9), (7.10) and (7.11). For the end of the second stress pulse we obtain

$$O^{\mathrm{H2}}(t_{\mathrm{AC}} - \Delta t_{\mathrm{r,2}}) = (1 - \mathrm{e}^{-\frac{t_{\mathrm{AC}}}{\bar{\tau}}}) \cdot \frac{1 - u_2 + d_1 u_2 - u_1 d_1 u_2}{1 - u_1 d_1 u_2 d_2}. \tag{7.22}$$

An example of the charging and discharging dynamics within a pulse pattern with $j = 2$ is shown in Fig. 7.9 a-b) for different combinations of τ_c and τ_e. The complete occupation probability map after the second charging pulse is shown in Fig. 7.9 c) for all combinations of τ_c and τ_e.

For stress times much longer than the charging time constant $\bar{\tau}$, $O_{\mathrm{H}}(t_{\mathrm{AC}})$ and $O_{\mathrm{L}}(t_{\mathrm{AC}})$ saturate

$$O^{\mathrm{L2}}(t_{\mathrm{AC}} \to \infty) = \frac{d_2 - u_2 d_2 + d_1 u_2 d_2 - u_1 d_1 u_2 d_2}{1 - u_1 d_1 u_2 d_2} \tag{7.23}$$

$$O^{\mathrm{H2}}(t_{\mathrm{AC}} \to \infty) = \frac{1 - u_2 + d_1 u_2 - u_1 d_1 u_2}{1 - u_1 d_1 u_2 d_2}. \tag{7.24}$$

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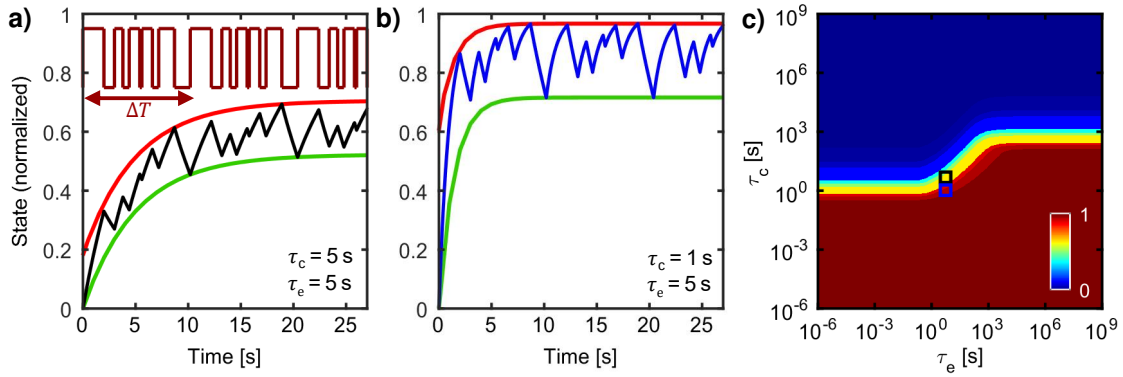

Figure 7.10: Defect occupancy for a pulse pattern with $j = 5$. **a)** $\tau_c = \tau_e = 5\,s$ and **b)** $\tau_c = 1\,s$, $\tau_e = 5\,s$. The black and blue lines are recursively calculated for each point in time of the stress pattern. The red and green lines are calculated following (7.22) and (7.21). **c)** Occupancy map dependent on the capture and emission times, after the second high pulse. The black and blue squares mark the positions of the capture and emission times of a) and b), respectively.

Analogously to $j = 2$, for j periodically following stress and recovery pulses, the occupancy after the ith stress and recovery pulse is derived

$$\begin{aligned} O_N^{\mathrm{L}j} &= \sum_{n=1}^{N} (d_j - u_j d_j + d_{j-1}u_j d_j - u_{j-1}d_{j-1}u_j d_j + \ldots - u_1 d_1 \ldots u_{j-1}d_{j-1}u_j d_j) \cdot (u_1 d_1 \ldots u_j d_j)^{n-1} \\ &= (1 - (u_1 d_1 \ldots u_j d_j)^N) \cdot \frac{d_j - u_j d_j + d_{j-1}u_j d_j - u_{j-1}d_{j-1}u_j d_j + \ldots - u_1 d_1 \ldots u_{j-1}d_{j-1}u_j d_j}{1 - u_1 d_1 \ldots u_j d_j} \end{aligned} \tag{7.25}$$

Inserting (7.19) and (7.20) in (7.25) gives the envelope function after the last recovery pulse in dependence of the AC stress time:

$$\begin{aligned} O^{\mathrm{L}j}(t_{\mathrm{AC}}) &= \left(1 - \mathrm{e}^{\frac{-t_{\mathrm{AC}}}{\tau}}\right) \cdot \frac{d_j - u_j d_j + d_{j-1}u_j d_j - u_{j-1}d_{j-1}u_j d_j + \ldots - u_1 d_1 \ldots u_{j-1}d_{j-1}u_j d_j}{1 - u_1 d_1 \ldots u_j d_j} \\ &= \left(1 - \mathrm{e}^{\frac{-t_{\mathrm{AC}}}{\tau}}\right) \cdot \left(d_j + \sum_{i=0}^{j-1} \left(\prod_{k=0}^{i} u_{j-k}d_{j-k}\right)(d_{j-k-1} - 1)\right) \cdot \left(1 - \prod_{i=1}^{j} u_i d_i\right)^{-1} \end{aligned} \tag{7.26}$$

The occupancy after the end of any V_{h} and V_{l} pulse within the pattern is recursively calculated. E.g. for the last high pulse:

$$\begin{aligned} O^{\mathrm{H}j}(t_{\mathrm{AC}}) &= \left(1 - \mathrm{e}^{\frac{-t_{\mathrm{AC}}}{\tau}}\right) \cdot \frac{1 - u_j + d_{j-1}u_j - u_{j-1}d_{j-1}u_j + \ldots - u_1 d_1 \ldots u_{j-1}d_{j-1}u_j}{1 - u_1 d_1 \ldots u_j d_j} \\ &= \left(1 - \mathrm{e}^{-\frac{t_{\mathrm{AC}}}{\tau}}\right) \cdot \left(1 + \frac{1}{d_j} \cdot \sum_{i=0}^{j-1} \left(\prod_{k=0}^{i} u_{j-k}d_{j-k}\right)(d_{j-i-1} - 1)\right) \cdot \left(1 - \prod_{i=1}^{j} u_i d_i\right)^{-1}. \end{aligned} \tag{7.27}$$

Similar to the example with $j = 2$, the charging and discharging dynamics within a pulse pattern with $j = 5$ are shown in Fig. 7.10, calculated following (7.26) and (7.27). The complete occupation probability map is shown in Fig. 7.9 c). Furthermore, it can be deduced that if $O(\tau_c, \tau_n) = 1$, then $O(\tau_c, \tau_{n+1}) = 1$ as well as if $O(\tau_{c,n}, \tau_e) = 0$, then $O(\tau_{c,n+1}, \tau_e) = 0$. In addition, with (7.26) and (7.27) for $\tau_c \gg t_{\mathrm{AC}}$, it follows for all τ_e $O = 0$ as well if $\tau_c \ll \min(\Delta t_{s,i})$, it follows for $\tau_e \gg t_{\mathrm{rec}}$ $O = 1$. With these simplifications, the calculations can be accelerated by at least a factor of two dependent on the stress/recovery pattern.

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7.6 Implementation within the Model

There are two possibilities to integrate the stress and recovery voltage dependence of the capture and emission time constants in the model: Either by integrating the dependence into the calculation of the differential activation energy maps as shown for the recovery voltages in Fig. 7.7, or by integrating it into the calculation of the occupation probability maps. As sketched in Fig. 7.2 b-e), the latter has been chosen and a stress time transformation following (7.3) and a recovery time transformation following (7.4) is introduced dependent on the stress and recovery voltages of the $V_{\mathrm{gs}}(t)$ for each voltage class but only for the recoverable component. Covering these dependencies in the occupation probability maps has several advantages:

- For constant stress and following recovery, the recovery voltage dependence can easily be considered within the activation energy map of the recoverable component as shown in Fig. 7.7. With decreasing recovery voltage the emission time constants shift to larger values, whereas for $V_{\mathrm{gs,rec}} = 0\,\mathrm{V}$ decreased emission time constants are observed. For more complicated stress patterns, the shift of the emission time constants as well as the capture time constants cannot be easily calculated.

- The separation of the $V_{\mathrm{gs}}(t)$ pattern from the activation energy maps simplifies the calculation, because the effect of the $V_{\mathrm{gs}}(t)$ pattern can be separately calculated within the occupation probability maps and no effect on the differential activation energy maps have to be considered.

- The inclusion of the stress and recovery voltage dependence of each voltage class via (7.3) and (7.4) only affects the digital stress pattern. Then, as shown in the next section, the calculation of occupation probability maps with n pulses has a straight-forward solution.

- In applications, stress patterns can also feature multiple periodicities on different time scales e.g. day-night cycles, power-down modes, and different mission profiles with different temperatures. The history of the device is considered within the occupation probability maps and as such, multiple periodicities with different circuit operation modes are also covered within one simulation.

The four parameters needed to describe the transformed stress and recovery times following (7.3) and (7.4) are shown in Table 7.1.

Table 7.1: Parameters for the transformed stress and recovery times as described by (7.3) and (7.4).

Stress voltage dependence	
a_{s}	11.6
b_{s}	−1.31

Recovery voltage dependence	
a_{r}	28.3
b_{r}	800

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7.7 Model Validation

A good model accuracy of constant stress/recovery sequences and digital AC stress is the basis for a model developed to simulate arbitrary stress patterns. The activation energy map model is able to reproduce and explain all important typical characteristics of DC NBTI covering the stress voltage as well as the temperature dependence (see Section 6.2). In this chapter, the model is first validated against measurements after applying an accumulation pulse. This experiment is a good demonstration of the separation into a recoverable and quasi-permanent components as well as the recovery voltage dependence. Secondly, measurements and simulations of rectangular AC stress are presented (duty cycle, frequency, and low level dependence). Thirdly, measurements and simulation of analog AC stress like sawtooth-, sine- and triangular-shaped stress patterns are compared. Finally and most importantly, measurements and circuit simulations of NOR and INV ring oscillators are presented. All following simulations are based on the parameters presented in Table 6.2 and Table 7.1.

7.7.1 Accumulation Pulse

MSM measurements with a pulse into accumulation and with varied pulse length as shown in Fig. 7.11 provide a separation into recoverable and quasi-permanent component. The recoverable defects are emptied during the accumulation pulse. Further recovery at $V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$ after the accelerated recovery phase does not establish before the effective recovery time of the accumulation pulse. This leads to a plateau as seen in Fig. 7.11 c). The length of the plateau depends on the duration of the accumulation pulse. Measurements and simulations are in good agreement for both stress times and all applied recovery pulse times with respect to small deviations due to sample-sample variation in the experiment.

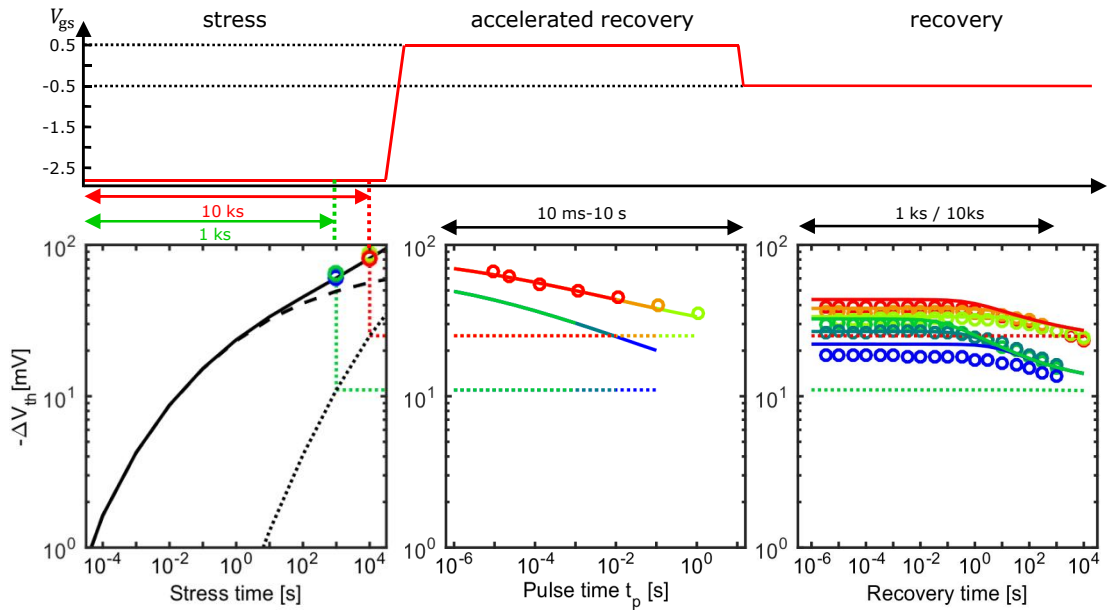

Figure 7.11: Recovery after an accumulation pulse **a)** Stress phase with $T = 125°\mathrm{C}$ and $V_{\mathrm{gs,str}} = -2.8\,\mathrm{V}$ of up to 10 ks. **b)** ΔV_{th} after an accumulation pulse of $V_{\mathrm{gs,rec}} = 0.5\,\mathrm{V}$ with varied pulse length (10^{-2} – 10^{2} s). **c)** Following recovery after the accumulation pulse with $V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$. Measurement data from [199], a comparison with Comphy can be found in [210, p.79].

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7.7.2 Rectangular AC Stress

To simulate rectangular AC signals as shown in Section 7.5, the defect occupation probability is calculated for the two discrete levels V_l and V_h based on (4.25). In the following, the influence of the frequency, duty cycle, as well as the low level V_l is discussed and the performance of the model is evaluated.

Dependence on the Frequency

To explore the limits of the derived modeling approach, the measured degradation after digital AC stress with varied frequency is compared to the simulation in Fig. 7.12. Within the last stress period before the measurement charges are trapped, as such the frequency dependence is dominated by this effect. For example, a duty cycle of $dc = 0.5$ within the stress period $t_\mathrm{str} = 1/2f$, before the measurement of ΔV_th, leads to charging of all defects with a capture time constant smaller than $\approx 1/2f$. The contribution of these defects to ΔV_th is $\approx 10\,\mathrm{mV}$ for the example shown in Fig. 7.12. This contribution recovers fast and is only measurable due to the short measurement delay of $t_\mathrm{d} = 1\mu\mathrm{s}$. For frequencies below 10 kHz, the dependence on the frequency is well reproduced by the model. Due to the measurement delay of $t_\mathrm{d} = 1\mu\mathrm{s}$ during the calibration of the activation energy maps, the simulated ΔV_th is constant when increasing the frequency above 10 kHz. For frequencies higher than 10 kHz, the frequency dependence of the meta-stable states as discussed in [182] and Section 4.3.2 has to be taken into account. Still, the overestimation for $f = 2\,\mathrm{MHz}$ is less than 20%.

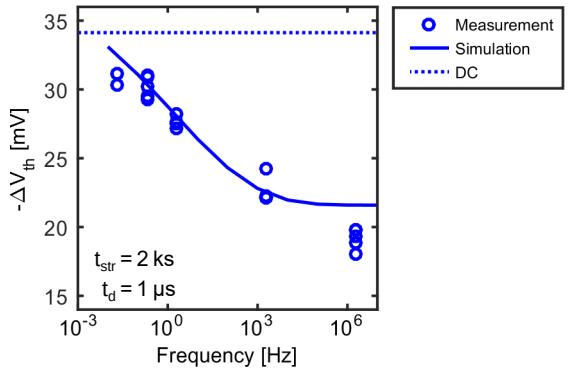

Figure 7.12: Frequency dependence of digital AC stress with $V_\mathrm{h} = -2.2\,\mathrm{V}$, $V_\mathrm{l} = 0\,\mathrm{V}$, $T = 170°\mathrm{C}$, $dc = 0.5$, $t_\mathrm{str} = 2\,\mathrm{ks}$ and $t_\mathrm{d} = 1\,\mu\mathrm{s}$. The DC degradation is shown as a reference with the same net stress time $t_\mathrm{str} = 1\,\mathrm{ks}$. The activation energy map model with the two-state approximation reproduces the frequency dependence up to 10 kHz very well. Due to the measurement delay of $t_\mathrm{d} = 1\mu\mathrm{s}$, the simulated ΔV_th is constant when increasing the frequency above 10 kHz. For higher frequencies, meta-stable states have to be taken into account [182]. Measurement data provided by Karina Rott. A comparison with Comphy can be found in [210, p.101].

Dependence on the Duty Cycle

A well-known and often reported characteristic of NBTI is the duty cycle dependence of the AC-ΔV_th showing the shape like a lying "S" with sharp rises between $dc = 0 \leq 10\%$ and $90 \leq dc = \leq 100\%$ [56, 162, 182]. The duty cycle dependence is shown in Fig. 7.13 a) for measurements with $V_\mathrm{l} = 0\,\mathrm{V}$. The "S-shape" is well reproduced. A comparison with $V_\mathrm{l} = -0.5\,\mathrm{V}$ is shown (as published in [162]), even though $V_\mathrm{l} = 0\,\mathrm{V}$ is the actual V_l of the measurement. Simulations with $V_\mathrm{l} = -0.5\,\mathrm{V}$ show a higher degradation compared to $V_\mathrm{l} = 0\,\mathrm{V}$, as the lower V_l leads to accelerated recovery within the AC stress.

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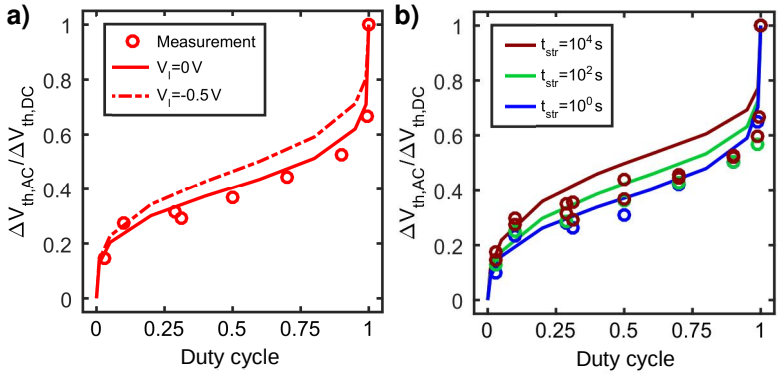

Figure 7.13: Duty cycle dependence: Experimental data from [162]. The solid and dashed lines show the simulations with $V_\mathrm{l} = 0$ V and $V_\mathrm{l} = -0.5$ V, respectively. **a)** Experimental and simulated duty cycle dependence of ΔV_th with $T = 175°\mathrm{C}$ and $V_\mathrm{h} = -2.7$ V, $f = 100\,\mathrm{kHz}$, $t_\mathrm{str} = 10\,\mathrm{s}$ and a recovery time of $t_\mathrm{d} = 1\mu\mathrm{s}$. **b)** Simulated and measured duty cycle dependence as a function of the stress time, same stress conditions as a).

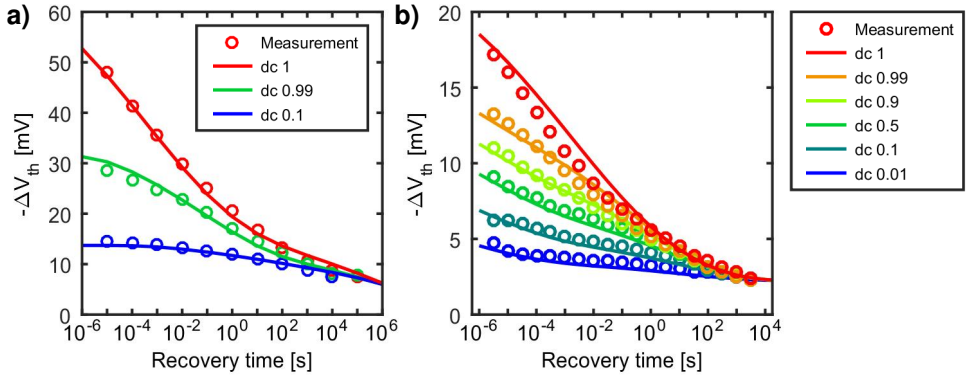

Figure 7.14: Measured and simulated recovery in dependence of the duty cycle with all measurements having the same accumulated stress time. **a)** Recovery after accumulated stress of $t_\mathrm{net} = 100\,\mathrm{s}$ and duty cycle $dc = 1/0.99/0.1$ ($t_\mathrm{AC} = 100/101/1000\,\mathrm{s}$, respectively), with $T = 175°\mathrm{C}$ and $V_\mathrm{h} = -2.7\,\mathrm{V}$, $V_\mathrm{l} = 0\,\mathrm{V}$, $f = 100\,\mathrm{kHz}$. **b)** Recovery after accumulated stress of $t_\mathrm{net} = 10\,\mathrm{s}$ for the duty cycle $dc = 1/0.99/0.9/0.5/0.1/0.01$ ($t_\mathrm{AC} = 10/10.1/11/20/100/1000\,\mathrm{s}$, respectively) with $T = 150°\mathrm{C}$ and $V_\mathrm{h} = -2.2\,\mathrm{V}$, $V_\mathrm{l} = 0\,\mathrm{V}$, $f = 2\,\mathrm{kHz}$. Simulations and measurements are in good agreement. Measurements provided by Hans Reisinger and Karina Rott.

Furthermore, a varied stress time, as shown in Fig. 7.13 b), influences the ratio between the recoverable and quasi-permanent component and as such, the relative contribution of recovery during the AC stress (higher relative ΔV_th for longer stress times). For long stress times with a frequency of 100 kHz, the duty cycle dependence cannot be reproduced perfectly, as meta-stable states have not been taken into account in the model [182].

The recovery after different duty cycles with the same net stress times is shown in Fig. 7.14 for two different stress conditions (different high level, frequency, and stress temperatures). As all measurements are performed with the same net stress time, all recovery traces have to merge at a well-defined point in time, dependent on their duty cycle and the net recovery time they have seen within the AC stress. The merging point of the recovery traces depends on V_l, due to the low level-dependent acceleration of the recovery time. Even though no meta-stable states have been taken into account for the model, simulations are in good agreement with the measurements shown in Fig. 7.14 a) due to the short net stress time and a smaller error for the duty cycles close to the edges (0.1 and 0.99, compare Fig. 7.13 b). Because of the lower frequency of 2 kHz, very good agreement over the whole range of the duty cycles is achieved in Fig. 7.14 b).

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Dependence on the Low Level

Variation of the low level strongly influences the recovery within the AC stress. For $V_l \geq V_{th}$, the recovery is decelerated, effectively resulting in a duty cycle increase and a higher ΔV_{th}. Vice versa, for $V_l \leq V_{th}$, the recovery is accelerated, effectively resulting in a duty cycle decrease and a lower ΔV_{th}. The measurements with varied recovery voltage shown in Fig. 7.4 and Fig. 7.11 are only suitable to determine the recovery voltage dependence of the recoverable component, as the time with applied recovery voltage was not sufficient to observe a recovery of the quasi-permanent component.

Rectangular AC measurements with varied low level as presented in Fig. 7.15 provide further insight on the recovery voltage dependence of the quasi-permanent component as the effective duty cycle is influencing the occupation probability of the recoverable as well as the quasi-permanent component (compare occupation probability maps in Fig. 4.7 and Fig. 7.15 d)). Fig. 7.15 a) shows the threshold voltage shift over stress time. The recovery following directly after end of stress is shown in Fig. 7.15 b). Increasing V_l results in longer effective emission time constants within the AC stress. After stress ΔV_{th} is decreased with no recovery, due to an already reduced recoverable component within the AC stress. In Fig. 7.15 c), ΔV_{th} after 10^5 s stress is shown in dependence on the low level for two different cases: 1) Both the recoverable as well as the quasi-permanent component are modeled recovery voltage-dependent or 2) only

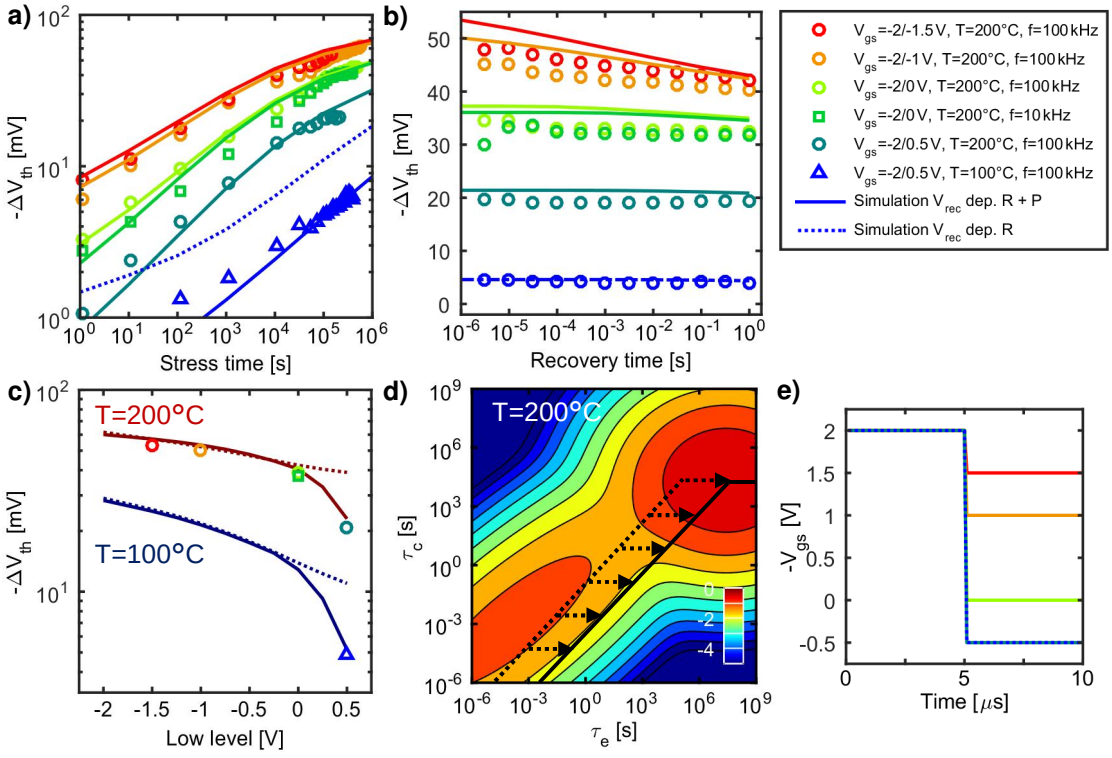

Figure 7.15: Rectangular AC stress with varied low level V_l for two temperatures and two frequencies with $V_h = -2$ V and duty cycle $dc = 0.5$. The stress is interrupted after the end of V_l. The legend denotes the applied V_h, V_l, temperature, and frequency. **a)** ΔV_{th} with stress time and **b)** recovery after $t_{str} = 10^5$ s. **c)** V_l dependence of the ΔV_{th} after $t_{str} = 10^5$ s. **d)** Capture and emission time map for $T = 200°C$. Comparison of the defect occupancy if the recovery voltage dependence is included/not included in the model (solid lines/dashed lines) with $V_l = +0.5$ V. Defects with longer emission times than the dashed/solid lines are occupied after $t_{str} = 10^5$ s rectangular AC stress at $V_l = 0.5$ V. **e)** Stress pattern for the low level combinations at $f = 100$ kHz. Good agreement between the model and measurements is achieved for all stress conditions if the recovery voltage dependence of the recoverable and quasi-permanent component is considered (solid lines).

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the recoverable component is considered to be recovery voltage-dependent. The effect on the defect occupancy of these two cases is illustrated in the CET map in Fig. 7.15 d). As seen in Fig. 7.15 c), to explain the decrease of ΔV_{th} with $V_{\mathrm{l}} = +0.5\,\mathrm{V}$, the recovery voltage dependence of the quasi-permanent component has to be considered within the model, too. Nonetheless, the exact recovery voltage dependence of the quasi-permanent component remains speculative but is considered in this model to be the same as for the recoverable component (see (7.4) with the parameters in Table 7.1). With this approach, good agreement is achieved for all V_{l}, temperature, and frequency combinations.

7.7.3 Analog AC Stress

The model accuracy for arbitrary waveform patterns is best demonstrated with MSM measurements on single transistors. A circuit includes many different transistors which may be in different states of degradation, as such the dependence on the stress pattern and the following recovery can be overshadowed. In this section, MSM measurements with different analog stress patterns are studied. First, the influence of the stress pattern on the degradation is discussed for arbitrary waveform patterns. Second, the measured ΔV_{th} after applying a triangular signal with different low levels at two frequencies and two temperatures is compared to the simulations. Third, measurements and simulations of "real" circuit stress patterns applied to single transistors are presented. For all the following simulations, $N_{\mathrm{V}} = 20$ is used. The simulation accuracy dependence on the number of voltage classes is discussed in Section 7.8.

Sine, Sawtooth, and Triangular Stress

In this section, MSM experiments using different analog $V_{\mathrm{gs}}(t)$ patterns are presented and simulated. To compare the ΔV_{th} for different analog signals a sine stress pattern is chosen, as typical for analog applications. Also, a sawtooth stress pattern is chosen as a special case aiming for the biggest differences compared to the already discussed rectangular case. The recovery after four different stress times is compared to the simulation in Fig. 7.16.

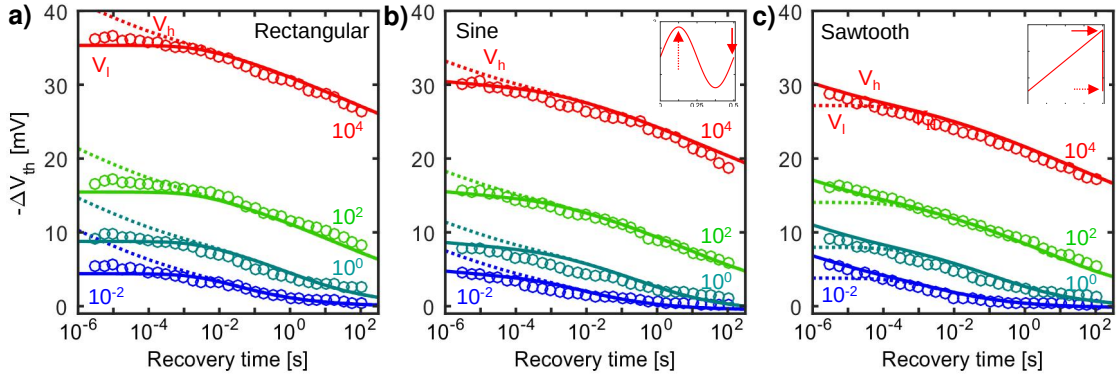

Figure 7.16: The analog-stress MSM experiments: periodical application of **a)** digital AC, **b)** sine and **c)** sawtooth with oscillation of the stress voltage between the values $V_{\mathrm{l}} \leq V_{\mathrm{h}}$ with $V_{\mathrm{l}} = -0.5\,\mathrm{V}$ and $V_{\mathrm{h}} = -2.8\,V$. Shown are the MSM ΔV_{th} recovery curves after four stress times $10^{-2}, 10^{0}, 10^{2}$ and $10^{4}\,\mathrm{s}$ at $T = 125°\mathrm{C}$ and $f = 2\,\mathrm{kHz}$. Measurement data from Gunnar Rott as published in [52]. The measured ΔV_{th} also depends on the point of interruption of the analog stress pattern, which unfortunately has not been considered by the experimentalist. Therefore, solid lines correspond to the actual interruption chosen in the experiment (as indicated by the solid red arrows in Fig. 7.16). In addition, the dotted lines indicate in Fig. 7.16 a) and b) the interruption at the maximum of the $V_{\mathrm{gs}}(t)$ pattern. For the sawtooth in 7.16 c), the maximum of the $V_{\mathrm{gs}}(t)$ pattern has been chosen in the experiment, therefore interruption at the minimum of the $V_{\mathrm{gs}}(t)$ pattern is shown as dashed lines.

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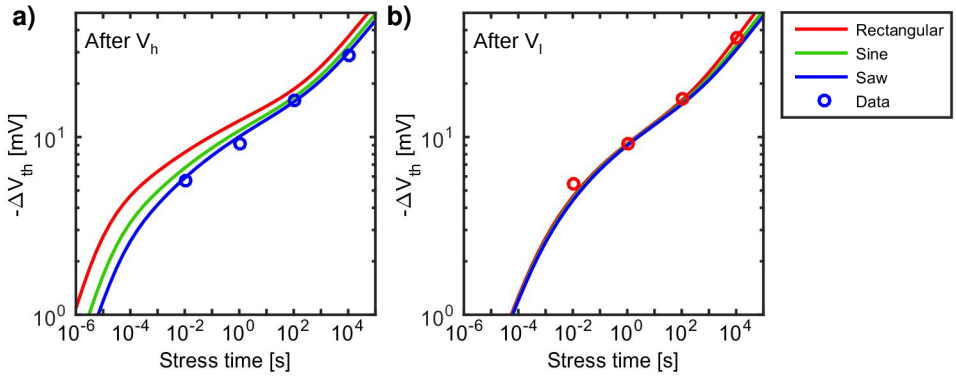

Figure 7.17: Degradation with stress time for different analog stress patterns after interruption of the stress at **a)** V_h and **b)** V_l with $V_\mathrm{l} = -0.5\,\mathrm{V}$ and $V_\mathrm{h} = -2.8\,V$, $T = 125°\mathrm{C}$ and $f = 2\,\mathrm{kHz}$. Where available, measurement points of Fig. 7.16 are shown as circles in the corresponding color of the applied stress. A 20% higher degradation is observed for the rectangular pattern compared to the sawtooth.

As the measured ΔV_th also depends on the point of interruption of the analog stress pattern, simulations for the interruption after end of V_l and V_h are compared. As expected, due to the same amount of stress and only different read-out conditions, both simulated cases merge after $\approx 0.1\,\mathrm{ms}$ recovery time. The deviation between measurements and simulation for all stress and recovery times is less than 5 %. Furthermore, the comparison of the ΔV_th in dependence on the stress time for all three signals shown in Fig. 7.17 reveals a 20% higher degradation for the digital AC pattern compared to the ΔV_th after sawtooth stress (lowest degradation of the three cases).

Nevertheless, the main differences can be seen after the end of V_h, due to the short-term influences of the pattern on ΔV_th. For the same duty cycle, the rectangular stress has the longest time period at V_h, whereas the pattern with the shortest time at V_h is the sawtooth stress. The threshold voltage shift ΔV_th after an interruption at V_l is shown in Fig. 7.17 b). Here, only differences for long stress times are visible. Giering *et al.* presented simulations to the same set of measurement data using the defect sampling model and compared the simulation with TCAD simulations of the NMP four-state model (models presented in Section 4.4.2 and Section 4.3.2, respectively). A comparison of the three models can be found in [KWJ4]. All three models achieve good accuracy between measurement and simulation with a deviation of less than 5 %.

The simulated ΔV_th during the first five stress periods as shown in Fig. 7.18 reveals the variation of V_th within one stress period for a rectangular and a sine stress pattern with $f = 2\,\mathrm{kHz}$. To simulate the occupancy change within one stress period, the occupancy has to be calculated point by point of the $V_\mathrm{gs}(t)$ pattern following (4.16) and (4.17) (as shown in Fig. 7.10). In addition, the simulation is compared to TCAD simulations using a defect database as presented in [52] and in Section 4.4.2. The agreement between both simulation methods is good, there are only small deviations due to differences in the model parametrization [KWJ4]. Nonetheless, the step-by-step calculation of ΔV_th is computation time-intensive and depends on the simulated stress time. Therefore, the simplified calculation of the occupancy map is introduced for stress interruption at the end of V_h and V_l following equations (7.26) and (7.27). For lifetime simulations, the consideration of the details in $\Delta V_\mathrm{th}(t)$ is not necessary. It is sufficient to simulate the difference between V_h and V_l at EOL.

For analog circuits, a correct consideration of the low level is essential as e.g. comparators are sensitive to a varied low level. The biggest differences in ΔV_th have been observed for a varied low level (see Fig. 7.15). Therefore, ΔV_th of an analog triangular stress pattern is studied with a varied low level in dependence on the stress and recovery time as shown in Fig. 7.19 a) and Fig. 7.19 b) with the applied triangular stress pattern shown in Fig. 7.19 c).

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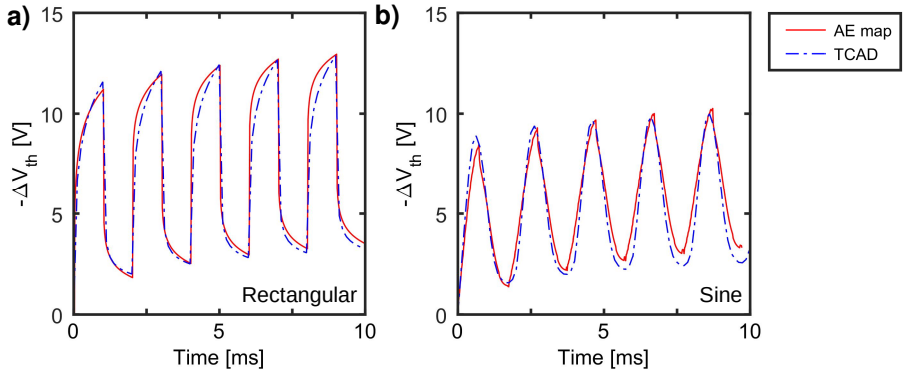

Figure 7.18: Simulated ΔV_{th} during application of **a)** rectangular stress and **b)** sine stress with a frequency of $f = 2\,\mathrm{kHz}$ and $V_{\mathrm{h}} = -2.8\,\mathrm{V}$ and $V_{\mathrm{h}} = 0\,\mathrm{V}$ at $T = 125°\mathrm{C}$. The blue dashed lines correspond to TCAD simulations as presented in [52]. The red solid lines are simulations with the activation energy map and $N_{\mathrm{V}} = 50$.

The frequency of 5 kHz has been chosen to guarantee that the stress voltage pattern shown in Fig. 7.19 c) is always applied to the gate. The lowest degradation is measured for $V_{\mathrm{l}} = +0.5\,\mathrm{V}$ as for Fig. 7.15. Due to the recovery within the stress pattern, the degradation is dominated by the quasi-permanent component. Only a slight decrease from the DC stress (reduction of about 10 mV is seen for $V_{\mathrm{l}} = -1\,\mathrm{V}$. Here, within the low phase for $V_{\mathrm{l}} = -1\,\mathrm{V}$, only about 5 mV of the degradation recovers within the measurement time. For $V_{\mathrm{l}} = 0\,\mathrm{V}$ less than 3 mV recover within the first 100 s, whereas for $V_{\mathrm{l}} = 0.5\,\mathrm{V}$ less than 1 mV of recovery is observed. A frequency reduction from 5 kHz to 500 Hz results in an even smaller recoverable component, due to the interruption at the end of the low phase and hence longer recovery before measurement. After a recovery time of 1 ms, both stress conditions show identical ΔV_{th}. Increasing the temperature to $T = 200°\mathrm{C}$ increases the relative contribution of the quasi-permanent component and results in a three times higher degradation after 100 ks stress.

All simulations are in good agreement with the measurement and are a good verification of the introduced $V_{\mathrm{gs,rec}}$ dependence of the recoverable and quasi-permanent component.

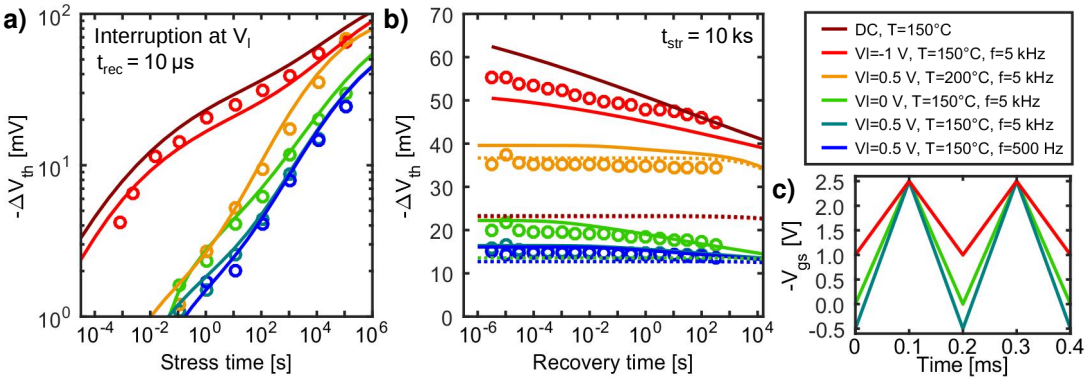

Figure 7.19: Triangular AC stress. The legend denotes the different low levels V_{l}, temperature T and frequency f with $V_{\mathrm{h}} = -2.5\,\mathrm{V}$. Circles correspond to measurement data, lines to the simulation with the model. **a)** ΔV_{th} with stress time, **b)** recovery of ΔV_{th} after $t_{\mathrm{str}} = 10\,\mathrm{ks}$. The dark red line shows a simulation for DC stress at $V_{\mathrm{gs}} = -2.5\,\mathrm{V}$. **c)** $V_{\mathrm{gs}}(t)$ for three different low levels $V_{\mathrm{l}} = -1, 0, +0.5\,\mathrm{V}$ with $f = 5\,\mathrm{kHz}$.

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Real Circuit Stress Patterns

As a next step, the degradation of application-relevant stress is studied. Simulated circuit stress patterns are applied to the single transistors with the measurement setup described in Section 5.2.3. The simulated sub-circuit is illustrated in Fig. 7.20 a) and the simulated V_{gs} signal of the pMOS within the seventh inverter shown in Fig. 7.20 b) is applied to single transistors using an AWG.

To study the influence of different supply voltages V_{dd}, the $V_{gs}(t)$ stress pattern as shown in Fig. 7.20 s) is multiplied by a factor such that the plateau of the input signal lies at $V_{gs} = -2.7/-2.3/1.9$ V as shown in Fig. 7.20 b). This stress signal is then applied to the single transistor. The induced threshold voltage shift with stress time is shown in Fig. 7.20 c). Even for long stress times up to 10^6 s very good agreement between simulation and measurement is observed for all three conditions ($N_V = 20$). A rectangular approximation of the input signal ($N_V = 2$) as indicated with the dashed lines shown in Fig. 7.20 b) overestimates the total degradation by $+35\%$.

The arbitrary waveform setup has proven to be a good tool to evaluate the models for circuit simulations with real application-relevant stress signals. In this case, solely the impact of BTI is studied. In the future, this setup can also be used to vary the relation of HCS and BTI by applying the output signal in Fig. 7.20 a) to V_{ds} and varying the stress voltage, stress temperature, frequency, fan-out, or the length of the n-channel and p-channel transistors [KWC1, KWJ1, KWC7].

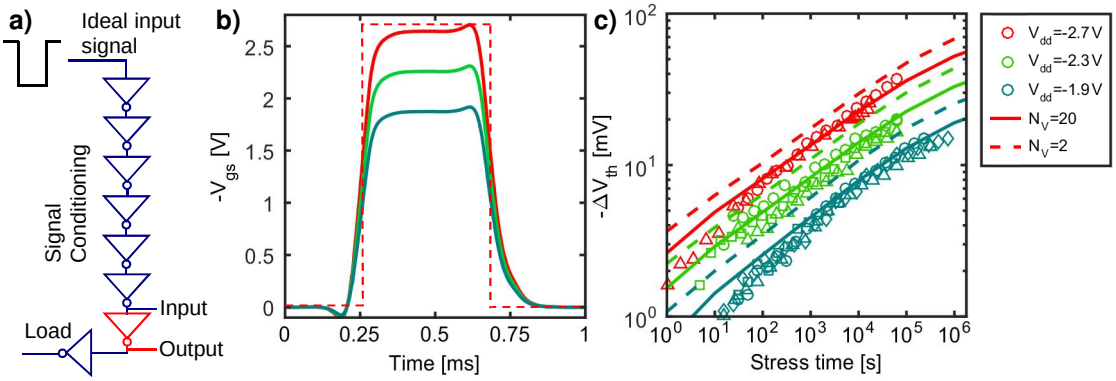

Figure 7.20: a) Simulated sub-circuit, the input pattern of the seventh inverter is used as stress signal. **b)** Applied V_{gs} stress patterns with different magnitudes (multiplication of the input signal by a factor such that the plateau of the stress signal lies at $-2.7/-2.3/-1,9$ V ($V_{ds,str} = V_{ds,meas} = -0.1$ V, $T = 150°$C). The dashed lines indicate a rectangular approximation of the stress signal taking the overshoots into account. **c)** Threshold voltage shift with stress time for the three stress patterns. For all three signals, good agreement between measurement and simulation is achieved with $N_V = 20$. The rectangular approximation (dashed lines), as shown in b), overestimates the actual degradation by $+35\%$. Measurements provided by Christian Schlünder and Fabian Pröbster with some of the data published in [KWC7].

7.7.4 Circuits

The modeling approach presented here has been implemented within the Infineon in-house SPICE circuit simulator and first measurements and simulations have been performed to demonstrate the applicability of the model for circuit simulations.

Implementation of the Model in the Circuit Simulator

The circuit aging simulation, as currently implemented within the Infineon in-house circuit-simulation framework, is sketched in Fig. 7.21 [KWJ1]. First, the investigated circuit is simulated without any aging. For each transistor, all internal voltages are recorded and written to an output

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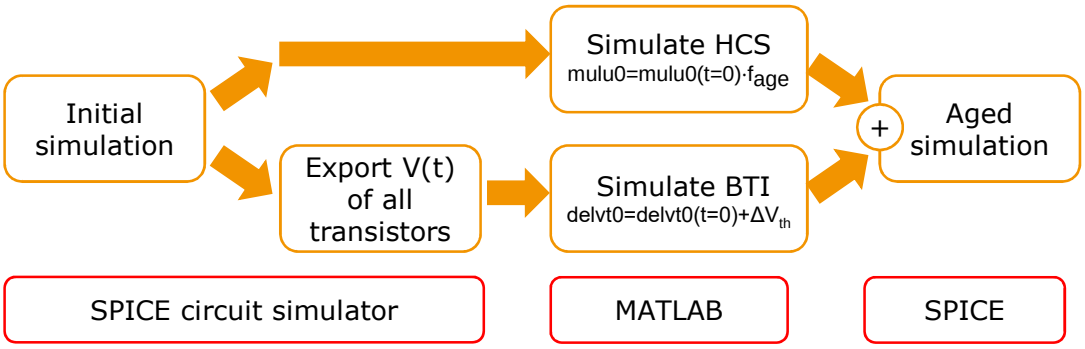

Figure 7.21: Schematic of the circuit aging simulation flow implemented in the INFINEON in-house circuit simulator. The HCS model is integrated into the SPICE circuit simulator via assertions following (4.6). The model calculates the relative decrease f_{age} of $I_{\text{d,lin}}$. The aged parameter *mulu0* in the circuit simulation is calculated based on the initial BSIM parameter for the mobility $mulu(t = 0)$. The BTI simulation is performed separately in MATLAB with the model presented in Section 7. A shift in V_{th} is considered by the BSIM parameter *delvt0*.

file. The standard SPICE simulation has non-uniform distributed time intervals dependent on internal currents and voltages. For the output file, a voltage discretization is used to reduce the file size.

The BTI simulation is performed separately, a shift in V_{th} is considered by the BSIM parameter *delvt*0. For each transistor, based on the SPICE simulation, the BTI induced degradation is calculated with MATLAB with the model presented in Section 7. The BSIM parameter *delvt*0 for each transistor is written to an alteration file which introduces the model parameter changes for the following SPICE simulation.

HCS is empirically modeled considering a mobility degradation dependent on the temperature, length, drain, and gate voltage of each transistor following (4.6) as described in Section 4.2. To model HCS degradation, only the BSIM parameter *mulu*0 is altered and the calculation is integrated into the circuit simulator. Solely considering *mulu*0 reflects the degradation of the operating point with the highest degradation, but the simulation is currently improved to consider several operating points and thus more than one BSIM parameter has to be altered during aging.

Finally, the circuit is simulated again with the adapted (aged) transistor model parameters. Due to the closed-form of the model, the computational effort is stress time- and frequency-independent. Calculation of ΔV_{th} after 10 years for 1000 transistors with MATHWORKS MATLAB ®2015b takes $\ll 10\,\text{s}$ for a discretization with $N_{\text{V}} = 20$ on an Intel®Core i5 4300M 2.60 GHz. As a comparison, the zero-hour SPICE simulation in this example takes 60 s.

As designers want to compare the circuit function at zero hours with the circuit after a specific operating time, two SPICE simulations are needed. As such, the additional computation time for the aging calculation does not significantly affect the overall simulation time.

Several circuit operating modes exist for most circuits. For HCS different modes can be simulated subsequently. The BTI defect sampling model as presented by GIERING *et al.* in [KWJ4] offers an efficient solution for such patterns without significantly affecting the simulation time (see Section 4.4.2). Several operating modes can also be simulated with the activation energy map model. The occupation probability map after stress within the application mode *A* can be used as input for the application mode *B* and so on. In such a manner, the degradation can be calculated for subsequent modes. For example, day/night cycles with two different operation modes would be *ABAB*. Though, for lifetime calculations the computation time can significantly increase e.g. for day/night cycles this would mean $2 \cdot 365 * 10$ calculation steps. As a consequence,

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this increases the simulation time per transistor for the model to several seconds. Another simple possibility would be the calculation of the occupancy for several modes following (7.26). Nonetheless, this also increases the computation time, because (7.26) extends to $n \to \infty$.

Ring Oscillator Measurements and Simulation

The ring oscillator frequency is easy to measure and in direct correlation to the device degradation. Ring oscillators with different gates, e.g. INV, NOR, or NAND gates are differently impacted by the device stress. For example, the NOR ring oscillator is more sensitive to NBTI, whereas the NAND ring oscillator is more sensitive to HCS. In contrast, INV ring oscillators are sensitive to both degradation mechanisms. One possibility to separate the degradation mechanisms would be the use of different lengths, e.g. long gate length suppresses hot carrier degradation.

Circuit aging simulations are further presented and the ring oscillator frequency decrease for a NOR and INV ring oscillator are compared at different stress conditions. The measurement setup and the circuit design is presented in Section 5.2.3. All ring oscillator measurements have been performed with the purpose to test the suitability for fWLR monitoring by Rolf Vollertsen as partly published in [4] and [KWJ4]. Unfortunately, the longest stress times are 100 s and 1 ks, dependent on the stress condition. To observe a measurable change in the ring oscillator frequency, the circuits are stressed at elevated temperatures and increased V_{dd}. For one stress condition, the ring oscillator stress patterns of the NOR and INV are shown in Fig. 5.13. For each type of ring oscillator, ten fresh chips are measured per stress condition and all measured frequency changes are shown in Fig. 7.22 and Fig. 7.23 for the NOR and INV ring oscillator, respectively.

The highest simulated single transistor threshold voltage shift within the INV and NOR ring oscillator is very similar e.g. $\Delta V_{\mathrm{th,INV}} = 31\,\mathrm{mV}$ and $\Delta V_{\mathrm{th,NOR}} = 33\,\mathrm{mV}$ for the stress condition $V_{\mathrm{dd}} = 2.4\,\mathrm{V}$ and $T = 175°\mathrm{C}$. Due to the design of the two ring oscillators with the number and design of the aged transistors, the oscillation frequency is differently influenced by the aging of the single transistors: As shown in Fig. 5.13, the NOR gate contains two stacked PMOS and two NMOS, whereas the INV gate consists only of one PMOS and one NMOS as shown in Fig. 5.13. The measured frequency decrease of the INV ring oscillator is clearly lower than that of the NOR ring oscillator for all stress times and stress conditions.

To compare the models and the influence of the degradation on the frequency shift, the contributions of the single models are:

1. HCS (empirical model following (4.6)).
2. BTI considering recovery with the activation energy model.
3. Sum of HCS and BTI considering recovery with the activation energy model.
4. Sum of HCS and BTI without consideration of recovery. The model without consideration of recovery is obtained by the voltage-dependent activation energy map model with a shift of the emission activation energies of $\mu_{\Delta \mathrm{e}} + 3\,\mathrm{eV}$ such that the emission time constants are far outside of the experimental window.

Unsurprisingly, the contributions from BTI and HCS vary depending on the stress condition:

- Comparing the two temperatures $T = 175°\mathrm{C}$ and $T = 125°\mathrm{C}$, the contribution of BTI decreases with decreasing temperature, whereas due to the negative effective activation energy of HCS of the NMOS, the contribution of HCS to the overall frequency shift is slightly increased.

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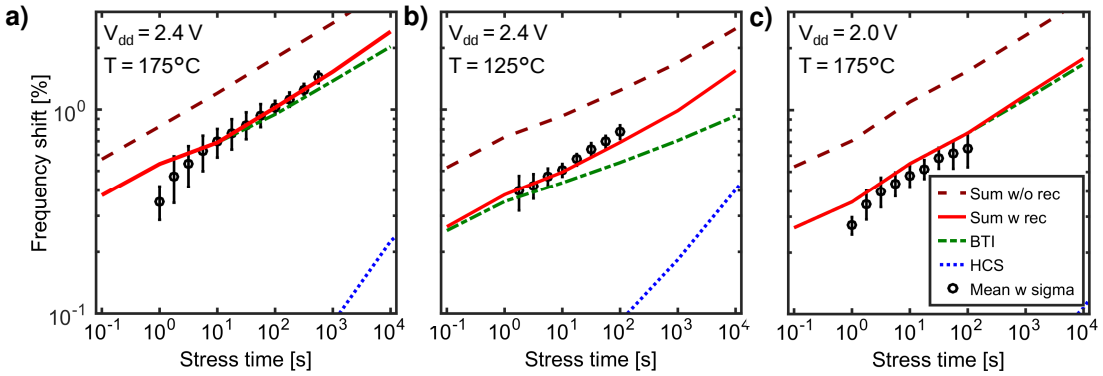

Figure 7.22: Measured (mean and 1 sigma of ten chips) and simulated frequency shift of the NOR ring oscillator at different stress conditions. **a)** $T = 175°C$, $V_{dd} = 2.4\,V$, **b)** $T = 125°C$, $V_{dd} = 2.4\,V$, **c)** $T = 175°C$, $V_{dd} = 2\,V$. Measurement data provided by Rolf Vollertsen.

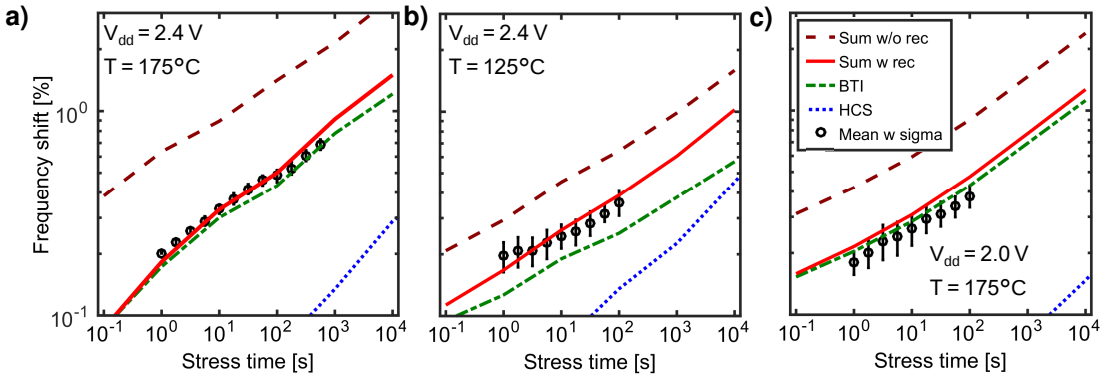

Figure 7.23: Measured (mean and 1 sigma of ten chips) and simulated frequency shift of the INV ring oscillator at different stress conditions. **a)** $T = 175°C$, $V_{dd} = 2.4\,V$, **b)** $T = 125°C$, $V_{dd} = 2.4\,V$, **c)** $T = 175°C$, $V_{dd} = 2\,V$. Measurement data provided by Rolf Vollertsen.

- In contrast, comparing the supply voltages $V_{dd} = 2.4\,V$ and $V_{dd} = 2\,V$, HCS is almost negligible for both ring oscillators for $V_{dd} = 2\,V$ due to the strong voltage dependence of HCS on V_{ds}.

The highest degradation is observed for $V_{dd} = 2.4\,V$ and $T = 175°C$. After $t_{str} = 1\,ks$, the NOR and INV ring oscillator frequency decreased by $1.65 \pm 0.05\,\%$ and $0.79 \pm 0.03\,\%$ (average and standard deviation of all eight measured chips respectively). It has to be noted that the aged transistor parameters have a different influence on the overall frequency shift depending on the operation condition of the ring oscillator. This results in a frequency shift of $3.8 \pm 0.2\,\%$ and $2.2 \pm 0.1\,\%$ for the NOR and INV ring oscillator comparing the measurements before and after stress at use conditions with $V_{dd} = 1.5\,V$ and $T = 175°C$.

For all stress and measurement conditions, good agreement between simulation and measurements is achieved when considering HCS and BTI with recovery. A comparison of the Giering defect sampling model (see Section 4.4.2) and the developed model is presented in [KWJ4]. The differences between the two models are small: The NBTI induced frequency shift of the model developed in this thesis lies slightly above the defect sampling model for the INV and for the NOR ring oscillator, but both models show a very similar dependence on the stress time.

Neither the BTI model presented in this thesis and the model presented by Giering do consider high-frequency effects [211]. Furthermore, the contributions of HCS and BTI are considered independently. The first findings indicate that the actual degradation is less than the addition of the single effects [212, 213]. A further unknown parameter decreasing the measured frequency shift is the delay introduced during frequency measurement. Nonetheless, the dependence on

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stress time as well as the magnitude is perfectly covered for all stress conditions and shows the applicability of single transistor aging models for circuit aging simulations. By contrast, the empirical model disregarding BTI recovery overestimates the frequency shift by a factor of two for both ring oscillators which has an enormous impact on the lifetime. This demonstrates the necessity for an accurate recovery model. Hence, the BTI model accounting for recovery strongly improves the accuracy of circuit aging simulations.

7.8 Model Approximations, Limitations, and Evaluation

The presented model has proven to be an accurate and efficient model for the threshold voltage shift after arbitrary analog BTI stress and is well-suited to be used in a circuit simulator. Benefits, approximations, and limitations of the model are discussed in this section. In the end, the requirements defined in Section 4.1 are discussed.

Benefits:

- The experimental effort required to ensure accurate model calibration could be drastically reduced, due to the TA-MSM measurement technique. An activation energy map can be recorded within a relatively short measurement time of 10 hours per stress voltage, that is a reduction by a factor of 10 compared to constant MSM measurements.
- No time-consuming TDDS measurements are required. Nonetheless, for different technologies $V_{\mathrm{gs}}(\tau_{\mathrm{c}})$ might change and additional TDDS investigations could become necessary.
- A closed-form description of the activation energy map is used. The whole model consists of 20 parameters, 8 parameters for the recoverable and 8 parameters for the quasi-permanent component listed in Table 6.2 including the temperature and voltage dependence as well as 4 parameters for the consideration of stress and recovery time acceleration and deceleration listed in Table 7.1.
- The discretization of the stress signal into N_{V} digital stress patterns with n pulses enables calculation of any arbitrary periodical stress signal.
- Due to the closed form of the activation energy maps and the numerically efficient calculation of the occupation probability maps following (7.26), the simulation effort is stress time-independent such that lifetime studies (several years of operating time) can be simulated as fast and accurately as short stress times. The simulation time for 1000 transistors with MATHWORKS MATLAB ®2015b takes $\ll 10\,\mathrm{s}$ for a discretization with $N_{\mathrm{V}} = 20$ on an Intel®Core i5 4300M 2.60 GHz and 61×61 bins of the activation energy map.
- Nested periodic stress patterns for different operation modes such as day/night cycles can be iteratively calculated. Numerically efficient solutions can be derived from (7.26).

Approximations:

- The collective defect behavior is modeled, no single defects were studied.
- The two-state model is employed. No meta-stable states as for the four-state NMP model are considered (compare Section 4.3.2). Differences are mainly in the high-frequency dependence as shown in Fig. 7.12 [182, 211]. Nonetheless, the mean degradation of ΔV_{th} at BTI conditions is captured by the two-state NMP model.

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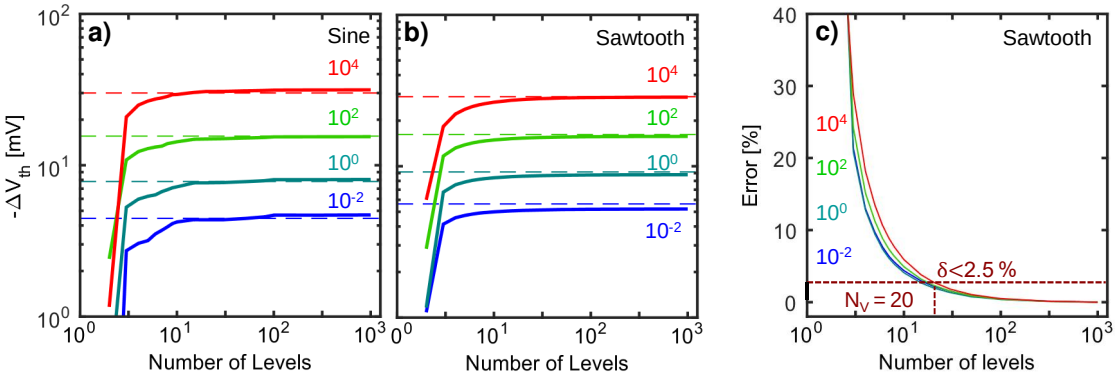

Figure 7.24: Simulation accuracy dependent on the number of voltage classes N_V (solid lines): **a)** sine and **b)** sawtooth. Measurement data with $t_d = 1\mu s$ for 4 different stress times as in Fig. 7.16 is shown as dashed lines. **c)** Error due to the discretization dependent on the number of voltage classes relative to the "ideal" case of $N_V = 1000$. $N_V = 20$ is used for the simulations as a good compromise between accuracy ($\delta \leq 2.5\%$) and simulation time.

- The stress and recovery acceleration factors are individual defect properties (see (7.3) and (7.4)). Nonetheless, for this model, the mean values are used. When considering e.g. stress at $V_{gs,str} = -2.8$ V and $V_{gs,rec} = -2.3$ V, only defects activated for $V_{gs,str} \leq -2.3$ V recover. This is considered in the model. Experimentally, this separation is not possible when studying large devices as seen in Fig. 7.4. This error is included in the extraction of the recovery acceleration factor (see (7.4)). However, this effect is only relevant for recovery voltages very close to the stress voltage due to the strong stress voltage dependence. E.g. for $V_{gs,str} = -2.8$ V and $V_{gs,rec} = -2$ V, more than 95 % of the defects show recovery.

- Previously, it was assumed that only R shows a dependence on $V_{gs,rec}$ as discussed in Section 7.7.2. No recovery of P was observed in Fig. 7.4 and Fig. 7.11, due to insufficient long application of the recovery pulse. However, modeling of the low level dependence shown in Fig. 7.15 for $V_l = +0.5$ V was not possible without including a recovery voltage dependence of P. Nonetheless, the exact recovery voltage dependence of P is unknown. For simplicity, the same dependence is assumed for R and P in this model. For the circuit simulations, no impact of positive voltages is assumed as application conditions do not contain positive V_{gs} for the pMOS.

- The stress signal is discretized into N_V voltage classes. Assuming $N_V = \infty$, maximum accuracy would be achieved resulting in $t_{sim} = \infty$. Simulations have shown that e.g. $N_V = 20$ already reduces the deviation δ from the "ideal" case to $\delta \leq 2.5\%$ (see Fig. 7.24). This deviation is negligible, as sample-to-sample, wafer-to-wafer, and lot-to-lot variation are on the order of $\delta \geq 10\%$ [207, 208].

Limitations:

- Since the model only considers the mean occupancy, it does not include RTN.

- For numerical efficiency, the occupation probability maps are calculated using envelope functions (see (7.26)). To calculate $\Delta V_{th}(t)$ in between V_h and V_l, a slower, iterative calculation of the defect occupation probability with $V_{gs}(t)$ has to be used (see Fig. 7.18).

- The V_{ds} dependence is not yet included in the model but is a possible and feasible add-on unless you have HCD.

- No variability is included but this would be a possible and feasible add-on.

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Evaluation of the requirements:

The goal was to develop a suitable model for use within an aging simulator which fulfills all five requirements introduced in Section 4.1.

1. Very good modeling accuracy is achieved: A wide range of measurements and simulations with accuracy $\delta \leq 5\%$ (for $N_V = 20$) have been presented covering rectangular AC stress patterns, analog stress patterns and circuit simulations.

2. The complete stress history is considered. All changes in stress and recovery voltage as well as temperature are included in the model. Furthermore, different application modes can be simulated.

3. The defects are separated into voltage classes and the occupancy of these defects is considered depending on their previous stress history.

4. The model is described in closed form and is numerically efficient with a stress time independent simulation time. The additional computation time for the circuit aging simulation is significantly lower than the simulation time for the circuit without aging.

5. Implementation into the SPICE circuit simulator has been demonstrated. The experimental effort is significantly reduced due to the introduction of the TA-MSM technique, which is suitable for model extraction in general).

Therefore, all requirements for circuit simulations are fulfilled. The aging model has been successfully implemented in the INFINEON in-house SPICE circuit simulator.

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Part III

Bias Temperature Instability in SiC MOSFETs

Chapter 8

Properties and Reliability of SiC MOSFETs

Silicon carbide (SiC) is a wide-bandgap semiconductor and a IV/IV compound. SiC-based MOSFETs promise superior performance for power devices as discussed in the following chapter. The applications of SiC MOSFETs are very different to the Si devices in logic integrated circuits presented in the first part of this thesis: SiC MOSFETs are used in e.g. motor drives, inverters, converters, switch-mode power supplies, induction heating systems, and photovoltaics. All these applications require high power densities and blocking voltages beyond 600 V.

Up to today, for these applications, Si device technologies such as super junction MOSFETs are currently used. However, to reduce system costs and improve performance by increasing e.g. the power density, some of these applications will be served in the near future by either hybrid or full SiC solutions. As of today, SiC MOSFETs perform far below their theoretical limits e.g. the channel mobility is lower than expected. For all new technologies, the reliability of the devices has to be ensured for the full product lifetime. Therefore it is important to understand the effects influencing the reliability, to analyze the differences compared to Si devices and to evaluate the impact and relevance of these effects for the application.

8.1 History and Challenges of SiC MOSFETs[1]

SiC has been used for a century as an abrasive and as a ceramic material due to its exceptional hardness. The electronic advantages have been known for a long time. The first application in power electronics as a voltage-dependent resistor in lightning arrestors was in 1930 (first patent from McFarlin [214]). Infineon released the first commercial SiC Schottky diodes in 2001 [215], but it was not until 2008 that SemiSouth Laboratories introduced the first commercial 1200 V JFET. In 2011, Cree presented the first 1200 V SiC MOSFET [216].

The commercialization of SiC MOSFETs was slowed down by point-defects at the SiC/SiO_2 interface and extrinsic defects within the gate oxide bulk. Currently available MOSFETs still have a channel mobility much lower than the SiC bulk mobility and a much higher extrinsic gate oxide defect density than Si MOSFETs. However, during recent years, channel properties have significantly improved and SiC MOSFETs have a competitive $R_{\mathrm{ds,on}} \times A_{\mathrm{act}}$ (*on* resistance times active area). Furthermore, gate oxide extrinsics have been reduced by applying efficient electrical screening measures [38]. What remains a challenge is the much more difficult and expensive crystal growth process compared to Si, but also these costs are constantly decreasing (see Section 8.2.3, [217, 218]).

[1] This chapter is based on a previous publication of the author of this thesis [KWJ6].

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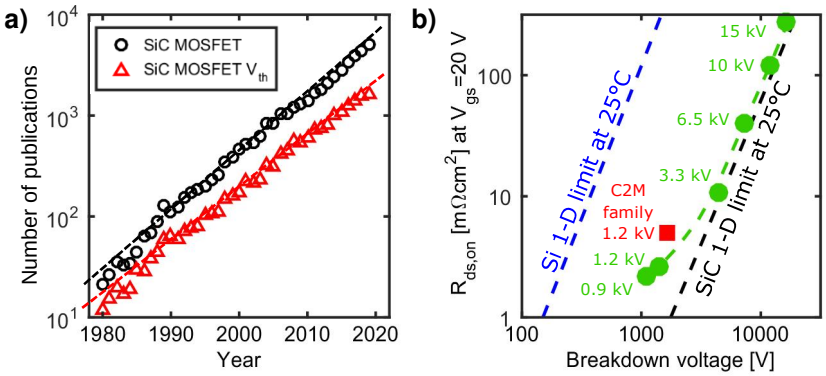

Figure 8.1: a) Number of publications on Silicon Carbide MOSFETs and their threshold voltage. Source: google scholar [34]. **b)** Specific *on* resistance ($R_{\text{on,sp}}$) of next-generation SiC MOSFETs measured at a gate bias of 20 V at $T = 25°\text{C}$ as a function of breakdown voltage. Adapted from [222].

There certainly is a growing interest in SiC MOSFET devices which is for instance reflected by the number of publications which is continuously doubling every 5 years according to google scholar, with no sign of saturation (see Fig. 8.1 a). The reduction in system cost has the potential to compensate for the higher cost of the SiC raw material [219]. Therefore, the actual SiC market grows at a rate of 40% per year [220], with more and more manufacturers entering the market (such as Wolfspeed, Rohm, Infineon, ST, Littlefuse, Fuji, Mitsubishi, Toshiba, Renesas, and others) [221].

8.2 Properties of SiC MOSFETs

In this section, the material and electrical properties of SiC MOSFETs are described. Furthermore, two different layouts are presented and the fabrication of the devices is outlined.

8.2.1 Material and Electrical Properties

Silicon carbide is a compound semiconductor consisting of 50 % silicon and 50 % carbon atoms and can grow in a wide range of crystal structures (*polytypes*). The polytype is characterized by its Si-C stacking sequence and each polytype has different electrical, optical, thermal, and mechanical properties. Fig. 8.2 shows the stacking sequences of the most common SiC polytypes 3C-SiC, 2H-SiC, 4H-SiC, and 6H-SiC. C stands for cubic and H for hexagonal. The 4H-SiC polytype is the polytype receiving the most attention for device applications. Single-crystal 4H-SiC wafers of 4, 6, and 8 inches diameter are available commercially. The abbreviation "SiC" refers to 4H-SiC in this work, since all devices investigated in this thesis are based on the 4H-SiC polytype unless otherwise stated.

The main advantage compared to gallium arsenide (GaAs) and Si-based MOSFETs is that SiC MOSFETs offer operation at a higher temperature, higher frequency, and higher power density due to its high breakdown field, its high thermal conductivity, and its wide bandgap as shown in Table 8.1. In principle, the bandgap of SiC would allow operation as a semiconductor up to temperatures of 1000°C, while Si becomes intrinsic above roughly 400°C [223]. However, for the operation at these high temperatures, a proper package is required. In addition, the saturation drift velocity of the electrons is more than twice as high as for Si and GaAs, which is highly beneficial for high-frequency operation. Furthermore, the breakdown voltage of a MOSFET is limited by the epilayer thickness and the doping as well as the breakdown field of the semiconductor. The breakdown field for SiC is approximately one order of magnitude higher than for

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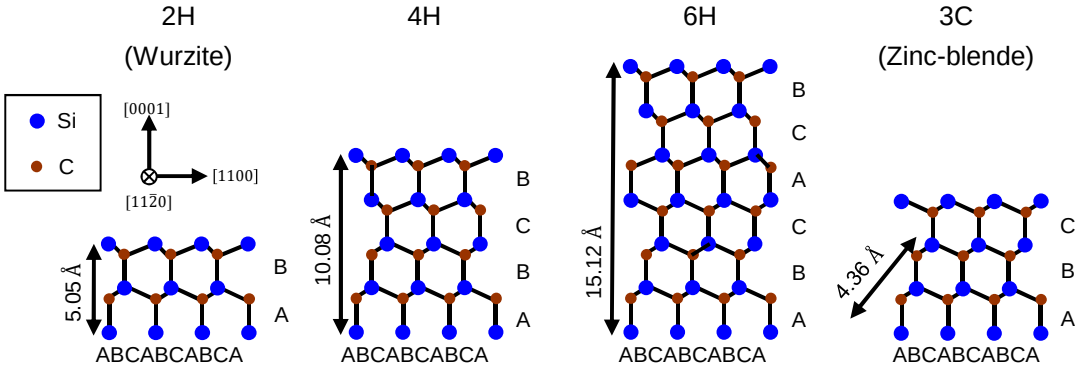

Figure 8.2: Stacking sequences of the most common SiC polytypes (viewed from the $[11\bar{2}0]$ direction). Adapted from [225].

Table 8.1: Comparison of material properties for Si, 4H-SiC, GaN and GaAs [224, 226, 227]

Properties	Si	4H-SiC	GaN	GaAs
Crystal structure	Diamond	Hexagonal	Hexagonal	Zincblende
Energy Gap [eV]	1.12	3.26	3.5	1.43
Electron Mobility $[\mathrm{cm}^2/\mathrm{Vs}]$	1400	900	1250	8500
Hole Mobility $[\mathrm{cm}^2/\mathrm{Vs}]$	600	100	200	400
Breakdown Field $[\mathrm{V}/\mathrm{cm}^2 \cdot 10^6]$	0.3	3	3	0.4
Thermal Conductivity $[\mathrm{W}/\mathrm{cm}^\circ\mathrm{C}]$	1.5	4.9	1.3	0.5
Saturation Drift Velocity $[\mathrm{cm}/\mathrm{s}]$	1	2.7	2.7	2.0

Si and GaAs. To increase the breakdown voltage for a given device, the thickness of the drift zone has to be increased and its doping has to be reduced. Consequently, for SiC MOSFETs, a much thinner layer of 4H-SiC can withstand a given voltage as compared to e.g. Si. Vice versa, the same layer thickness can withstand higher voltages. A thicker layer leads to an undesired increase in the specific $R_{\mathrm{ds,on}}$ (product $R_{\mathrm{ds,on}}$ times active area) as shown in Fig. 8.1). To reach a certain target $R_{\mathrm{ds,on}}$, one has to increase the size of the MOSFET, which on the other hand increases capacitances with the square of the breakdown voltage [224]. Vice versa, the specific $R_{\mathrm{ds,on}}$ of the MOSFET improves with the square of the semiconductors breakdown field and the higher allowed doping level in the drift zone further improves $R_{\mathrm{ds,on}}$. Due to these effects, the potential for high voltage applications with SiC MOSFETs is far above 1200 V.

From an application point of view, the advantages of a SiC MOSFET are lower capacitances, which improve dynamic losses and allows a lower $R_{\mathrm{ds,on}}$, which in turn reduces static losses, improves the efficiency and/or allows a higher switching speed [228]. Especially for applications such as switching converters, size is reduced due to smaller heat-sinks and a smaller size of inductors and capacitors is achieved. Gallium nitride (GaN) has comparable or even better material properties. But one important advantage of SiC is that it possesses a native oxide, SiO_2, which is the same as for Si MOSFETs and thus in principle allows production using the same manufacturing lines.

To discuss the electrical differences between a Si and a SiC MOSFET, their $I_{\mathrm{ds}}V_{\mathrm{gs}}$-curves are shown in Fig. 8.3. The total $R_{\mathrm{ds,on}}$ of the MOSFET is a sum of channel, JFET, drift-zone and substrate resistances, whereas the relative contributions of the components are different between SiC and Si MOSFETs. $R_{\mathrm{ds,on}}$ of the Si MOSFET at high V_{gs} is dominated by the resistance of the drift zone. Due to the low transconductance of the Si MOSFET at high gate voltages, the dependence of $R_{\mathrm{ds,on}}$ on a degradation ΔV_{th} vanishes. In contrast, the $R_{\mathrm{ds,on}}$ of the SiC MOSFET is dominated

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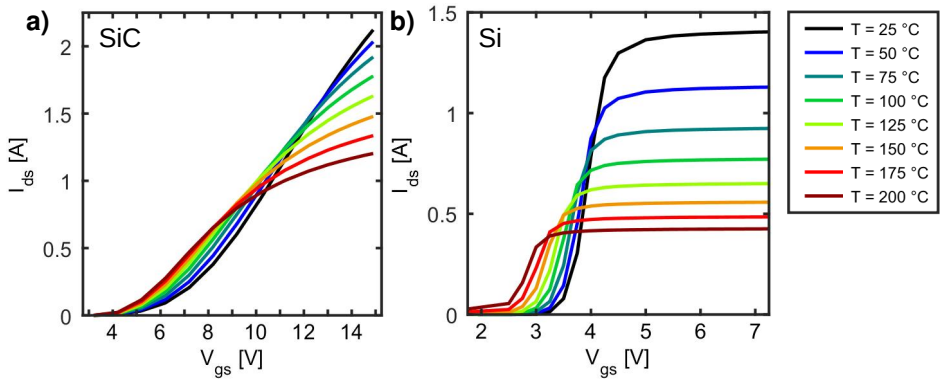

Figure 8.3: Comparison of **a)** SiC and **b)** Si MOSFETs $I_{ds}V_{gs}$-curves in dependence on the temperature with $V_{ds} = 1$ V.

by the channel resistance, especially for voltage classes below 1.2 kV as seen in Fig. 8.1 b). Furthermore, the $R_{ds,on}$ of the SiC MOSFET at low temperature is directly proportional to the gate overdrive $(V_{gs} - V_{th})$.

8.2.2 Layout of SiC MOSFETs

Especially for voltage classes below 1200 V, about 50 % of the total *on* resistance in SiC MOSFETs originates from the channel resistance due to a higher interface trap density and a very low drift layer resistance. Therefore, the die size has to be increased, which significantly increases the chip costs due to the expensive raw material. A decrease in the channel resistance is very important and can for instance be achieved by using a crystal-plane with higher mobility and shrinking the pitch size. Currently available commercial SiC MOSFETs are mostly lateral, but there are also trench devices under development and already in the market [224, 229]. The cross-sections of the two layouts are shown in Fig. 8.4 and Fig. 8.5.

The DMOS inversion channel (red arrows) forms on the (0001) crystal plane (Si-face). A smaller pitch size is achieved with the trench design where the inversion channel forms along with the *c*-axis of the 4H-SiC crystal plane (*a*-face), which is advantageous due to the higher mobility.

Trench devices require a highly doped p region to shield the insulator from the high electric fields in the off-state of the device due to the high drain potential. The advantages of trench MOSFETs, such as lower chip size for the same $R_{ds,on}$, are described in detail in [38, 224, 230].

The number of interface traps depends strongly on the fabrication and on the inversion layer crystal plane, which is different for trench and planar MOSFETs as will be discussed in Section 8.2.3 and Section 10.3.3.

8.2.3 Device Fabrication

The fabrication of SiC MOSFETs brings along serious challenges. While for Si it is possible to pull a single crystal from molten Si with a seed crystal in the Czochralski process, this is not possible for SiC and different processes have to be used. For commercial wafers, bulk crystals are usually grown along with the $[0001]$ direction by seeded sublimation (physical vapor transport (PVT)). Today, 150 mm wafers are produced with this method. While for Si typical growth rates of the crystal in the growth direction are some mm/min, for SiC they are at the most a few mm/hour [235]. The complicated growth technique, together with the slow growth rate and a length of the boules of roughly 30 – 50 mm leads are the main reasons for the high costs of about $1000 for one 150 mm SiC substrate wafer (in 2015, [236]). In order to reach the full potential

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of SiC MOSFETs the crystal quality and therefore the growth methods will have to be further improved.

Different from silicon wafers, silicon carbide wafers are sliced off-angle from the cylindrical boules to enable polytype preservation during the following homoepitaxial growth process. The 4H-SiC (0001)-wafer is usually tilted 4° toward the [11$\bar{2}$0] or [0001] direction [237]. Growing a homoepitaxial layer on top of the sublimation-grown wafer is necessary to further improve the crystalline quality of the substrate. The most commonly used technique for SiC is the chemical vapor deposition (CVD) process in a hot-wall reactor [238]. Typical temperatures for hot wall CVD are in the range of 1500 – 1650°C, high-temperature CVD reaches temperatures up to 2300°C [239]. The polytype control is achieved by a step-controlled epitaxy process [240–242], where due to the off-axis cut angle only a single possible bond configuration remains. The off-axis cut causes an increased roughness of the surface of the SiC/SiO_2 interface since all step edges are also transferred to the surface. This might result in a decreased mobility for the surface of the inversion channel, which can be avoided using trench devices.

The doping of SiC substrates and epitaxial layers is mostly realized during growth by adding precursors containing the doping atoms, e.g. n-type doping is achieved by adding nitrogen (N) to the sublimation atmosphere, while aluminum (Al) is used for p-type doping of SiC [241, 243]. While for silicon, the dopants are driven into the selected area by diffusion, ion implantation has to be used for SiC due to the low diffusion constants of the dopants [244]. A serious disadvantage results from the fact that the dopants predominantly reside at interstitial sites after the implantation and the implantation creates damage in the crystal lattice. Therefore, high temperature anneals of about 1700°C are required to move the dopants to the desired lattice sites and to heal the damage in the crystal [245]. However, even after the anneals point defects can remain in the crystal and influence the performance of the device [246].

In addition, an insulating gate oxide is needed to manufacture SiC MOSFETs. SiC is the only wide-bandgap semiconductor with a native oxide which happens to be the same as that for silicon, SiO_2. A particularly useful property of SiO_2 is that it can be grown by thermal oxidation. However, the mobility at the interface is even for commercially available MOSFETs one order of magnitude below the theoretical bulk value of $\mu_{\text{int}} \approx 1000\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ [247, 248]. Studies suggest that the low mobility is due to a high density of interface traps D_{it} [247]. Nonetheless, the fabrication process of Si MOSFETs has been optimized over the years and requires a hydrogen post oxidation anneal (POA) for the interface passivation. For Si MOSFETs, typical trap densities are in the range of 10^9 – $10^{10}\,\text{eV}^{-1}\text{cm}^{-2}$ [2, 249]. For SiC MOSFETs, however, the hydrogen anneal is not as effective [247, 250–252]. Although other passivation gases are used for SiC MOSFETs e.g. nitric oxide (NO) [253–255] or nitrous oxide (N_2O) [38], typical trap

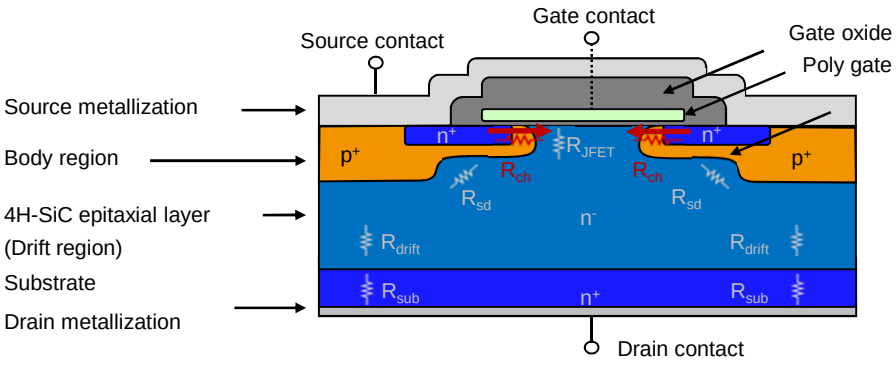

Figure 8.4: Schematic cross-section of a SiC MOSFET. Adapted from: [231].

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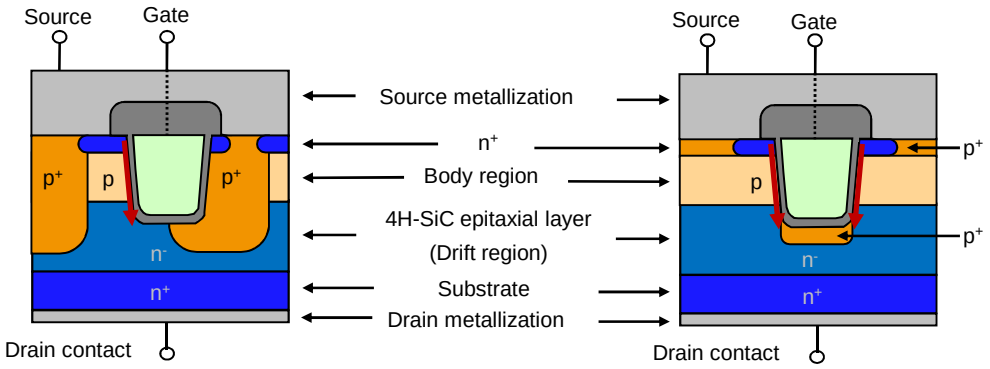

Figure 8.5: Schematic cross-section of two typical power SiC MOSFET trench layouts: **a)** a-face: The inversion channel forms on the $(11\bar{2}0)$ crystal plane [232, 233] and **b)** various crystal planes [234].

densities are in the range of $10^{11} - 10^{12}\,\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ [256–258] and thus two orders of magnitude higher than for Si MOSFETs. Furthermore, combining NO anneals with H (or ammonia (NH_3) results in higher mobility but also increases reliability issues [59, 259, 260]. Research with alternative processes e.g. passivation using phosphor (P) [261] is ongoing. Further discussion on the high density of interface traps is given in Section 8.4.

8.3 Reliability of SiC MOSFETs[2]

For silicon carbide MOSFETs, the reliability tests on wafer level and for packaged products reported are the same as the ones typically applied to Si power MOSFETs and IGBTs e.g. power cycle tests, temperature cycle tests, temperature humidity storage (forward and reverse bias), high- and low-temperature storage, positive and negative high temperature bias, high temperature reverse bias [262, 263] as well as short circuit robustness tests [264, 265]. There are some reports about special reliability issues regarding the degradation of the body diode [63, 266] and soft error rates, which are similar to Si devices. Furthermore, a well-known degradation mechanism in MOSFETs is the degradation due to channel hot carriers. For SiC, so far there are less than a handful of reports [267, 268] without any conclusive results.

For a long time, a serious problem of SiC MOSFETs has been the gate oxide quality [38] causing threshold voltage instabilities. A typical distinction is between intrinsic and extrinsic threshold voltage instabilities. Whereas extrinsic threshold voltage instabilities are mostly due to ionic contamination, the intrinsic threshold voltage instabilities are linked to the physical properties of the oxide and the interface [38]. Extrinsic threshold voltage instabilities can be reduced during device processing for example by preventing mobile ions from entering the gate oxide (as is well established for Si MOSFET technologies) [38]. It has been demonstrated by the application of smart screening techniques that the extrinsic failure rates of SiC MOSFETs can be reduced to the same low failure rate as Si MOSFETs or IGBTs. A detailed discussion on the extrinsic gate oxide reliability of SiC MOS structures can be found in [269].

Recently, several studies on the intrinsic threshold instabilities due to BTI on SiC MOSFETs have been performed, showing an increased bias temperature instability compared to Si MOSFETs [38, 59, 61, 66, 67, 77, 79, 253, 254, 268, 270–279]. Thereby, three observations have been made:

[2]This chapter is based on a previous publication of the author of this thesis [KWJ6].

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- SiC MOSFETs show a pronounced difference between the up- and down-sweep of the $I_{ds}V_{gs}$-curves [277, 280]. This hysteresis depends on the selected low and high biases for the sweeps and the sweep time (see also the investigations in this work in Section 2.1.2). It has been argued that interface traps in the range of $10^{11} - 10^{12}$ defects/eVcm^2 are the root cause of this hysteresis [38, 277]. The effect is known for Si MOSFETs but is negligible as Si MOSFETs show a lower density of interface traps and the narrow bandgap causes a fast disappearance of the effect [24]. Devices with the MOS channel on a vertical crystal plane of 4H-SiC (e.g. the a-face of the $(11\bar{2}1)$ plane) show a larger hysteresis effect than devices with the MOS channel at the planar crystal plane of 4H-SiC (e.g. the Si-face of the (0001) plane) [256].

- Negative gate stress results in hole capture leading to a reduction in the threshold voltage (negative ΔV_{th}). This effect is accelerated with increased negative gate voltage. This is a short-term effect and has the same origin as the hysteresis, the interface traps. No long-term threshold voltage shifts due to negative gate voltages have been observed [38].

- Positive gate stress results in electron capture leading to undesirable positive V_{th} shifts. This effect is accelerated with increasing gate voltage. If the threshold voltage is significantly increased, the overdrive ($V_{ov} = V_{gs,use} - V_{th}$) is reduced, which degrades the channel resistance. As the channel resistance of SiC MOSFETs amounts to $\approx 50\%$ of the $R_{ds,on}$, contrary to Si MOSFETs, the $R_{ds,on}$ of SiC MOSFETs is very sensitive to a reduction in the gate voltage overdrive [38].

- Recovery after positive as well as negative gate bias stress occurs when the stress is removed. This recovery is accelerated when the voltage is switched into the direction opposite to the stress voltage.

Measurement methods to separate the fast and slow recovering components of BTI e.g. using preconditioning techniques [38, 77] have been proposed for lifetime extraction. To understand the origin and in order to model these threshold voltage shifts, these measurement techniques are ill-suited (a discussion on BTI measurement techniques is given in Section 9.2). Furthermore, no model is available describing the timing dynamics after constant stress and the following recovery as well as switching dynamics or hysteresis effects. The physics and the microscopic origin of the defects are still under debate [38, 67, 275, 281]. A discussion on the nature of the traps is given in the following section.

8.4 Nature of the Traps and Differences to Si MOSFETs

In the following, a brief overview of the literature on the physical nature of the traps is given and it is discussed why the hysteresis is a feature so strongly observed on SiC-based MOSFETs. There are clear differences of SiC MOSFETs to Si-based devices:

- SiC-based MOSFETs show a much larger interface trap density D_{it} than Si-based MOSFETs. In Si MOSFETs, the silicon dangling bonds have been identified as the main interface defect type (P_b centers) [127, 251]. Carbon dangling bond-like defects have been observed for SiC MOSFETs and are often referred to as P_{bC} centers [282–286].

- The ΔV_{th} of the hysteresis is directly related to the number of trapped charges N_{it} at the interface. As SiC MOSFETs have a bandgap three times larger compared to Si (compare Table 8.1 [287]) and assuming a uniform trap distribution and $\Delta E_G = E_G$, this implies:

$$\Delta V_{th} = q\frac{N_{it}}{C_{ox}} = \frac{Q_{it}}{C_{ox}} = q\frac{D_{it}\Delta E_G t_{ox}}{\varepsilon_0 \varepsilon_r^{SiO_2}} \tag{8.1}$$

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with the elementary charge q, the oxide capacitance C_{ox}, the vacuum permittivity ϵ_0, the relative permittivity of SiO_2 $\epsilon_r^{SiO_2}$, the oxide thickness t_{ox} and Q_{it} the total number of interface charges are given by

$$Q_{it} = qN_{it} = qD_{it}\Delta E_G \tag{8.2}$$

with the density of interface traps D_{it} within the energetic window ΔE_G. For Si MOSFETs, the estimation of a maximum hysteresis is 3 – 35 mV, whereas for SiC MOSFETs the expected hysteresis is in the range of 1 – 10 V, which has been confirmed for various manufacturers as discussed in Section 10.3.3.

In the following, several studies and measurement techniques to figure out the physical nature of the traps are presented and discussed. For unknown effects, ion contamination is often suggested as the reason. For the change in ΔV_{th} due to positive as well as negative bias, ion contamination can however be excluded due to the following reasons. First, the capture and emission time constants extracted from the measurements presented in Section 10.1 and Section 10.2 are too short to be related to any ion movement. Second, at low temperatures, ion movement should be suppressed, but NBTI is also observed at low-temperature measurements at e.g. $T = -60°C$ [277]. Third, typical ion contamination is caused by sodium Na^+ as well as Potassium K^+ [274].

Some publications [288, 289] try to attribute defects to oxide trap energy levels or depth in the gate oxide and tunneling processes simply based on the $\Delta V_{th}(t_{str}, t_{rec})$. However, RTN and TDDS (see e.g. [25, 184, 290] and Section 2.6) studies on individual defects of Si MOSFETs have shown the defects with long capture and emission time constants (defects attributed to the more permanent component) are not necessarily located deeply in the oxide. Furthermore, elastic tunneling models [50, 291] have been shown to be inconsistent [141] due to too short tunneling time constants for slow traps in NBTI in Si MOSFETs. SiC MOSFETs generally have a larger gate oxide thickness (several tens of nanometers), which would be large enough to explain the longer time constants. However, all time constants are thermally activated [KWC5], which is also clear evidence against elastic tunneling and rather supports a thermally activated structural relaxation process for SiC MOSFETs like for NBTI in Si MOSFETs [141].

Furthermore, a classic characterization technique is charge pumping [292–294], which has been also applied to SiC MOSFETs [256, 259, 295]. In these studies, short-term threshold variations have been attributed to interface trapped charge and long-term effects to border traps [38, 259, 296]. Interface trapped charges are often defined as point defects at the semiconductor-dielectric interface, which are located energetically within the semiconductor bandgap and are often related to dangling bond-like centers [297]. Whereas border traps are described as traps within the SiO_2 close to the semiconductor-dielectric interface and are often linked to oxygen vacancies [250, 298], hydroxyl E' centers or silicon-oxygen bonds [299]. An NMP based model has been presented for the up-sweep of the $I_{ds}V_{gs}$ curves by Tyaginov *et al.* modeling the temperature dependence by mainly considering pre-existing border traps [300]. In addition, Schleich *et al.* have implemented an NMP-based model in the 1D simulator Comphy [51] to investigate positive BTI.

Differences in the hysteresis of devices with vertical crystal planes of a 4H-SiC (e.g. the a-face) and planar devices of 4H-SiC (e.g. Si-face) were reported in [277] and also in this work in Section 10.3.3. Vertical devices show better channel mobility, and the larger hysteresis in these devices has been attributed to a lower density of interface states D_{it} close to the conduction band (reduction of electron trapping at gate voltages higher than the threshold voltage) and a higher D_{it} around mid-gap (increase of charge trapping in the sub-threshold regime of the MOSFET) [38, 256, 277].

A few studies are using ESR or electrically detected magnetic resonance (EDMR) to identify the relevant defects at the SiC/SiO_2 interface in SiC devices [128, 288, 301–303]. Gruber *et al.* correlate the dominant hyperfine EDMR spectrum at the SiC/SiO_2 interface of planar devices

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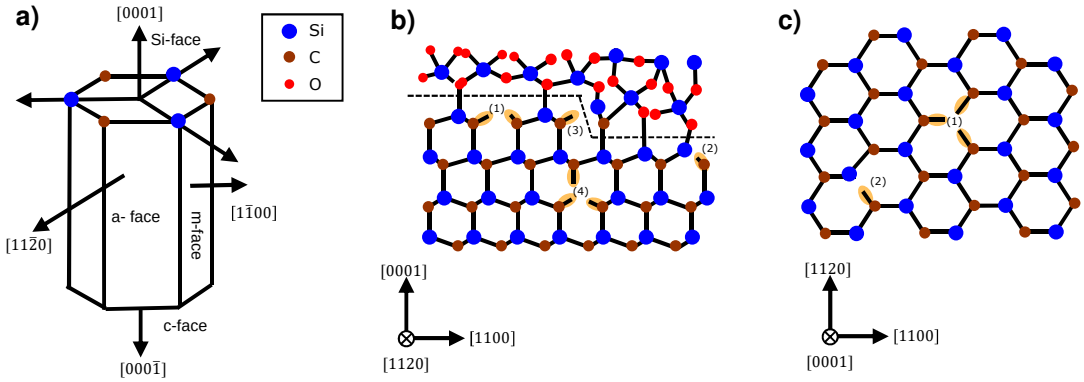

Figure 8.6: a) Location of the planes for SiC MOSFETs. Schematic example with ball and stick-models of different P_{bC} centers at the Si-face for different views **b)** along the $[1120]$ direction and **c)** along the $[0001]$ direction with (1) interfacial silicon vacancy V_{Si}, (2) P_{bC} center due to relaxation, (3) P_{bC} center at an edge, bulk silicon vacancy V_{Si}. After: [225]

(Si-face) with DFT calculations by Cottom *et al.* to carbon dangling bonds P_{bC} [217, 303–305]. Furthermore, on trench SiC MOSFETs (a-face), Gruber *et al.* have recently observed an increase in the EDMR spectra related to an increased carbon density at the surface of the a-face (more carbon dangling bonds) [225, 306]. Gruber illustrates in [225] a schematic of different examples of P_{bC} centers at the Si-face SiC/SiO_2 interface as shown in Fig. 8.6 for interfacial and bulk Si vacancies (possible to exist in several planes), P_{bC} due to relaxation and P_{bC} at an edge. As the trench interface consists of an off-axis cut (see Fig. 8.5), there are many corners and edges as illustrated in Fig. 8.6 b) case (3).

Although the studies presented here have contributed significantly to the understanding of the nature of these defects, they are not in complete agreement with the microscopic defect structure and succeed only partially in finding a direct correlation between resonance spectra and performance-limiting defects and threshold voltage instabilities, respectively.

As for Si MOSFETs, from large area devices with many defects contributing to the measured ΔV_{th}, it is difficult to distinguish between the different defect types and their properties e.g. their activation energies [162]. Therefore, at the moment SiC defect models and classifications – though they might be plausible in some cases – remain speculative and are not sufficiently backed by evidence. Further EDMR/ESR investigations and electrical spectroscopy on individual defects [141] could be the key to unraveling the physical nature of the defects responsible for the positive as well as the negative ΔV_{th}. Once the defects are identified, they could help our understanding of how to avoid the remaining defects by e.g. post-oxidation-anneal, and thus help to reduce short- as well as long-term threshold voltage instabilities.

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Chapter 9

Measurement Setup and Applied Experimental Techniques for SiC MOSFETs

Measuring the threshold voltage shift in SiC introduces several experimental challenges. In this chapter, the measurement setup and measurement techniques for the characterization of BTI of SiC MOSFETs applied in this work are presented. First, the devices under test are described. Second, the requirements for accurate measurements of the SiC threshold voltage instabilities are discussed, based on the measurement techniques presented in Chapter 2. Third, we describe the measurement setup to fulfill the derived requirements. Fourth, the AC measurement technique, which has been developed within this thesis to analyze the threshold voltage shift during an AC stress is introduced. Finally, an on-the-fly technique for the extraction of $\Delta R_{\mathrm{ds,on}}$ within typical application stress patterns is presented.

9.1 Devices Under Test

The in-depth analysis of threshold voltage shifts induced by positive and negative gate bias was performed on Infineon 4H-SiC n-doped MOSFETs test structures with a trench design. A schematic cross section of the devices is shown in Fig. 8.5 b) where the channel forms on a $(11\bar{2}0)$ crystal plane (a-face). All devices were fabricated with a SiO_2 dielectric (deposited with CVD) and a POA in NO atmosphere.

For comparison, lateral and trench SiC MOSFETs of other manufacturers are studied, too. The investigated devices from other manufacturers were commercially available MOSFETs from 5 different manufacturers (Rohm Gen 1 and Gen 2, Cree Gen 2 and Gen 3, ST Gen 1 and Gen 2, Littlefuse, On Semi). They are randomly labeled T for the trench SiC MOSFETs and D for the lateral MOSFETs to maintain anonymity. All investigated devices were packaged.

9.2 Measurement Considerations for SiC MOSFETs[1]

Already a short-time application of a positive or negative gate voltage introduces a significant threshold voltage shift in SiC MOSFETS. As such measurements of the threshold voltage are strongly influenced by the measurement scheme. Also, a dominant part of threshold shifts and instabilities in SiC is due to fast components [KWC4, 59, 66]. Furthermore, a large, fast recovering threshold hysteresis has been reported for SiC a decade ago [66] and still exists for the most

[1] This chapter is based on a previous publication of the author of this thesis [KWJ6].

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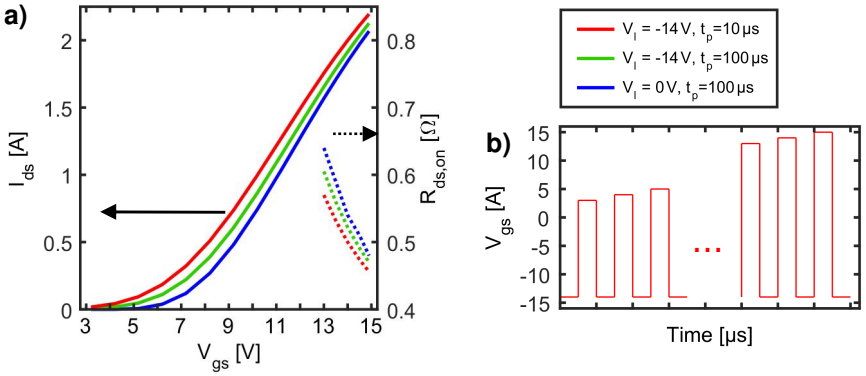

Figure 9.1: a) Dependence of I_{ds} and $R_{ds,on}$ on the negative pulse voltage V_l and on the pulse length, $V_{ds} = 1\,V$ at $T = 25°C$. **b)** Illustration of the measurement sequence.

advanced generations of SiC MOSFETs. Thus these fast components cannot be neglected and have to be considered when choosing the measurement routine.

For Si power MOSFETs, $I_{ds}V_{gs}$-curves in the regime of high V_{gs} and high currents are measured in pulsed mode to avoid self-heating of the MOSFET by pulsing V_{gs} or V_{ds} with a high current only flowing for a sub-milliseconds time. For a Si MOSFET, any threshold hysteresis is below the resolution limit [24].

In contrast, the threshold voltage hysteresis of SiC MOSFETs (see Fig. 2.2) is significant and exists for all SiC technologies. Without proper consideration of all measurement parameters of the $I_{ds}V_{gs}$-curves, the hysteresis affects reproducibility and comparability of measured parameters as e.g. $R_{ds,on}$ and V_{th}. The influence of the measurement settings is shown in Fig. 9.1 for two pulsed $I_{ds}V_{gs}$-curves recorded with a short (10 µs) and a long pulse length (100 µs) as well as two different base levels. Due to the V_{th}-hysteresis, the drain current decreases during the pulse, thus the drain current averaged over the pulse length is significantly higher for the short pulse. Furthermore, to avoid self-heating, the MOSFET is kept in a state of low I_{ds} at $V_{gs} = V_{base}$ for a time much longer than the pulse length. As a consequence of the hysteresis, the measured current and $R_{ds,on}$ is significantly lower for the negative pulse base. A detailed discussion on the reproducibility of measurements of SiC MOSFET device parameters is given in [KWJ9]. There are numerous reports which compare measured values of ΔV_{th}, power-law coefficients of ΔV_{th} versus stress time, dependence on the measurement delay of the instrument[78] or sweep rates [279] and many more (e.g. [38, 78–80, 97, 278]).

Considering the phenomena discussed in Section 9.2, the requirements to correctly study these effects in SiC MOSFETs are:

1. Complete consideration of the function $V_{gs}(t)$ and additionally the temperature from the start to the actual determination of V_{th}.

2. The measurement delay (time between end of stress and V_{th} determination) has to be as short as possible. Typical switching frequencies are around 50 kHz, which correspond to switching periods on the order of 10 µs. Thus fast measurement techniques require a measurement delay below 10 µs when assessments of short-term stress are desired.

3. In order to predict and simulate threshold voltage shifts, for example from long negative DC stress and bipolar AC stress, the measurement should be able to provide the data required to extract CET (or activation energy) maps [KWC5], which means extended stress and recovery sequences with stress and recovery times of 10^{-6} to at least 10^5 s.

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9.3 Measurement Setup

To perform SiC application-relevant stress, such as pulsed bipolar AC measurements, a requirement is to terminate the stress sequence at a predefined position. For SiC, this requires an arbitrary pulse generator with e.g. 25 V output, the capability to drive an nF-capacitive load and obviously, synchronization with the device's current measurement system. The microcontroller used in this home-build equipment allows, especially for repetitive sequences, a timing exactly reproducible within 10 ns [KWC5]. Fig. 9.2 shows the specialized SiC test-setup. Besides, the setup contains two (for high and low current) source measuring units (not shown) to measure I_{ds} or I_{gs}. The setup supports the following possibilities:

- Stress at a constant voltage and measurement of V_{th} with a measurement delay of 1 µs with drain currents of up to 5 mA.
- Stress with a bipolar AC stress signal with a maximum amplitude of ±40 V and interruption of the stress with an accuracy of 10 ns within the AC signal as well as the measurement of the V_{th} recovery with the same delay as for the DC measurement.
- Application of bipolar AC stress and measurements of the $R_{ds,on}$ during the application of the stress.

Temperature control is achieved using a mini-oven with a similar setup as shown in Fig. 5.5, but designed for TO-247 packages.

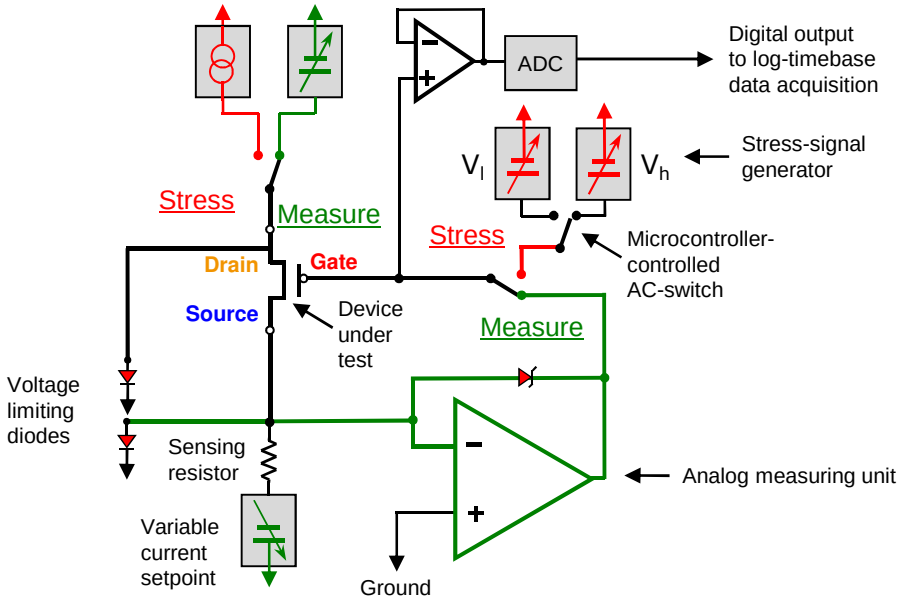

Figure 9.2: Simplified SiC measurement setup: The setup consists of two main components:
1) A stress-signal generator, consisting of digital-analog converter generating V_h and V_l and analog switches driven by the pulse width modulation unit of a microcontroller.
2) An analog measuring unit, consisting of analog switches and an operational amplifier in a feedback loop to control V_{gs} in a way to make I_{ds} constant. As presented in [KWC5].

9.3.1 AC Measurement Setup[2]

Measurements of V_{th} under real application conditions as shown in Fig. 9.3 with a time resolution below the AC switching period are very important to correctly obtain the threshold voltage

[2]The measurement setup has been developed within this PhD research and was first presented in [KWC4].

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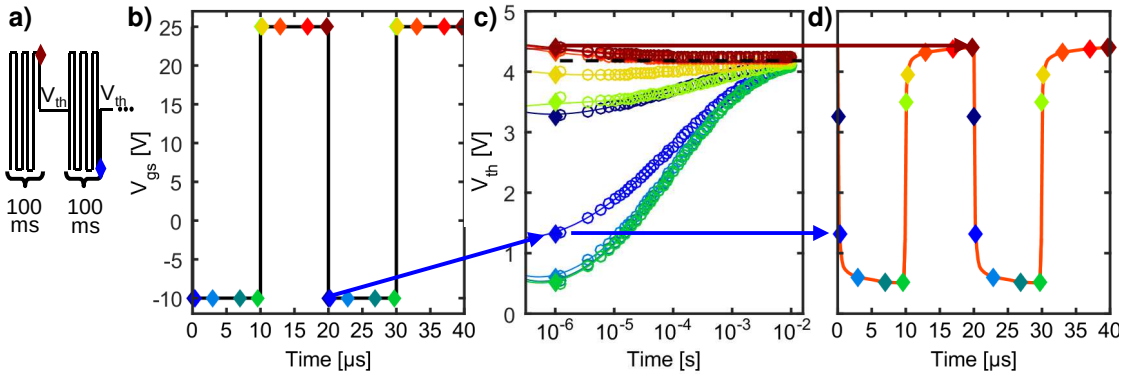

Figure 9.3: Explanation of the SiC AC measurement technique, example with real data ($T = 175°C$, $V_h = 25\,V$, $V_l = -10\,V$, $f = 50\,kHz$): **a)** The AC stress is interrupted at different points in time of the AC stress. Directly after interrupting the stress, the threshold voltage is measured from 1 µs to 10 ms recovery time. Between each measurement point, another AC stress of 100 ms is applied to restore the pre-measurement trap occupation state. **b)** An example 50 kHz bipolar AC signal is shown with different points of interruption as described for a). **c)** Recovery traces after each interruption of the AC signal with the plotted time, the recovery time under $V_{gs} = V_{th}$. **d)** The first measurement points ($t_d = 1\,\mu s$) are shown with the corresponding timing position during the AC signal.

shift within the application and not only a hysteresis within an $I_{ds}V_{gs}$-curve sweep. A real-time analysis of the V_{th} behavior under AC stress has to overcome the following problems:

- For application-relevant investigations, the frequency should be in the range of 50 kHz.
- The measurement delay should be as short as possible and significantly shorter than the period time.
- For an analysis of how V_{th} changes during the switching, the AC signal has to be interrupted at several points.
- The applied AC gate signal V_h and V_l should cover the upper and lower specifications of the data sheet.

The shortest possible measurement delay with our setup is $t_d = 1\,\mu s$, therefore already within the measurement, V_{th} recovers, and the trap occupation state caused by the bipolar AC signal is disrupted. Therefore, to measure the behavior of V_{th} in real-time during the AC stress, the following steps are performed:

1. The AC gate stress is interrupted at different positions in time during the AC signal (see diamonds Fig. 9.3 b).
2. A V_{th} recovery trace (1 µs up to 10 ms) back to the initial V_{th} is recorded for each interruption of the AC gate signal (see Fig. 9.3 c).
3. In-between each interruption, the pre-measurement trap occupation state has to be restored (see Fig. 9.3 a). It has to be ensured that the intermediate stress is long enough to fully restore the trap occupation state and is short enough that only the traps with short capture and emission times are activated. In the following experiments, an intermediate stress time of $t_{AC} = 100\,ms$ to restore the history has been chosen. With this condition, barely any slowly recovering components are activated, and thus applying another AC stress does therefore not increase the long-term V_{th}.
4. The actually measured hysteresis can thus be shown as e.g. a function of the AC period with the threshold voltage extracted at the shortest possible delay (here 1 µs) with respect to

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the timing of the interruption of the gate stress. Note that the major part of the hysteresis is only detected if the gate is switched from inversion to accumulation as shown in Fig. 9.3 d).

To our knowledge, measurements of V_{th} under real application conditions with a time resolution below the AC switching period have to our knowledge only been reported by the author of this thesis [KWC4, KWJ5, KWC5, KWJ6].

9.3.2 Dynamic *on* Resistance

To study the impact of ΔV_{th} on $R_{ds,on}$ during application conditions (bipolar AC stress with V_h and V_l voltages), we perform recovery-free on-the-fly measurements of the drain-source *on* resistance with a specified V_{gs} applied to bias the device to the "on" state. The measurement setup for on-the-fly dynamic $R_{ds,on}$ measurement shown in Fig. 9.4 is an extension of the measurement setup presented in Fig. 9.2.

The $R_{ds,on}$ during an AC gate signal is measured on-the-fly by forcing a constant current ($\lessapprox 1$ A) across source-drain and measuring the corresponding voltage drop V_{ds} during the V_{gs}-"on"-phase. A two-stage differential amplifier (green in Fig. 9.4) is used. In order to avoid under/overshoots in the pulse response of the constant current source, a passive source has been chosen. Most important for fast settling times is that all amplifier inputs/outputs have voltage limiting circuits (represented by diodes in red) to prevent amplifier saturation. All switches are fast solid-state analog switches with matching *on* resistance.

For a MOSFET with an $R_{ds,on}$ of 100 mΩ, the input voltage V_{ds} of the amplifier varies between 15 V and 10 mV during off- and on-phase, respectively. The post-amplifier with gain = 10 adapts the output voltage to the 1 mV-sensitivity of a DSO. Both stages of the differential amplifier use fast operational amplifiers with a gain-bandwidth-product of 200 MHz and a slew rate of 10^3 V/µs.

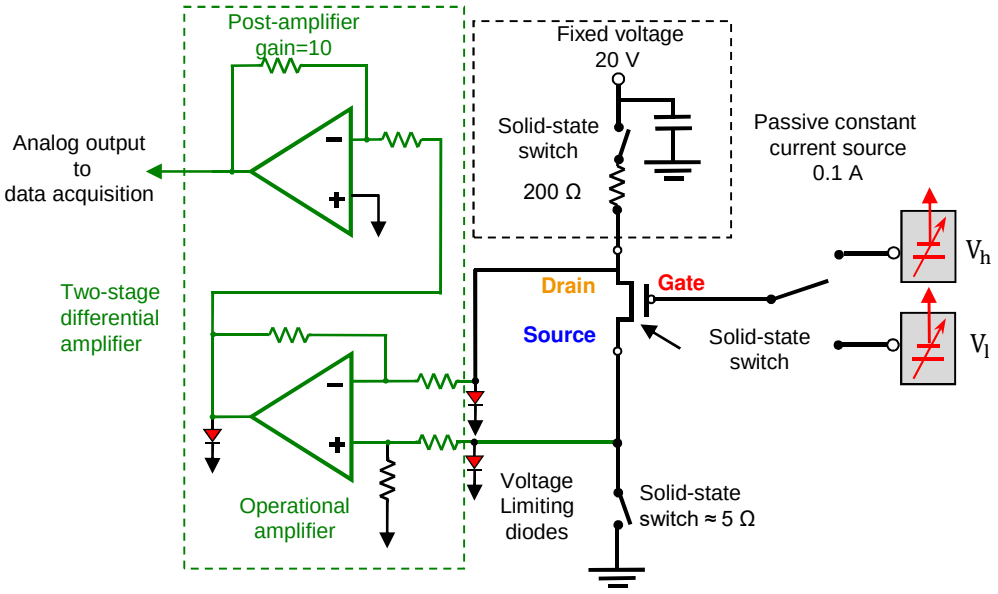

Figure 9.4: Measurement setup for on-the-fly dynamic $R_{ds,on}$ measurement: The setup is an extension of the measurement setup presented in Fig. 9.2. It consists of two additional components: 1) A passive constant current source of 0.1 A to the drain in order to avoid under/overshoots in the pulse response of the constant current source and 2) a two-stage differential amplifier with two fast operational amplifiers with a gain-bandwidth-product of 200 MHz and a slew rate of 10^3 V/µs. Clipping diodes (red) at the amplifier-inputs are required to prevent the amplifier from running into saturation. The post-amplifier with gain = 10 adapts the output voltage to the 1 mV-sensitivity of a DSO.

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Chapter 10

Modeling the Bias Temperature Instability in SiC MOSFETs

Among the challenges regarding reliability and performance issues, bias temperature instabilities (BTI) are arguably among the most important [61, 128, 307] and are in general not linked to macroscopic defects or impurities [38]. SiC-based devices can experience increased threshold voltage shifts when the gate is subjected to use voltages as their silicon-based counterparts, a problem that could severely limit the performance and range of applications for the technology. Regarding intrinsic threshold voltage instabilities, which have been extensively studied for Si devices, there are two major differences: The wider bandgap of SiC and the SiC/SiO_2 interface compared to the Si/SiO_2 interface. The interface differences are not only due to the different bandgap and the narrower band offsets to the dielectric but also a result of vacancies and carbon-related point defects, which only exist in SiC [247, 282, 288]. Different interface properties thus also cause different threshold voltage instabilities with different dependencies on e.g. temperature and voltage than the previously presented Si-MOSFETs.

Although many studies on threshold voltage instability for SiC MOSFETs exist, they do not provide a profound model of the effects and are mostly performed with measurement delays which are too long and devices that are not ready for application yet [38, 67, 253, 270–276, 278].

In this chapter, new features and peculiarities of threshold voltage variations of SiC MOSFETs are studied in detail and short-term as well as long-term modeling of application-relevant AC stress is demonstrated. As the devices are subjected to positive as well as negative gate voltages during the typical application, threshold voltage instabilities of both polarities have to be investigated.

First, in Section 10.1, the differences and similarities in the effects of constant positive DC gate stress regarding temperature, stress, and recovery voltage dependence are discussed. Furthermore, it is shown that these dependencies can be modeled with the activation energy maps for the recoverable and quasi-permanent component as shown for silicon-based MOSFETs in Chapter 6. In Section 10.1.6, PBTI of trench and planar SiC MOSFETs of different manufacturers are compared. Second, the dependence of the threshold voltage shift due to negative gate bias is studied in Section 10.2. SiC devices show fast recovering negative threshold voltage shifts due to NBTI. It is shown that these shifts are fully recoverable and can be modeled with an activation energy map only containing a recoverable component. Third, in Section 10.3, the properties of the hysteresis visible in $I_d V_g$-curves as well as during typical application of an AC voltage are discussed. In addition, the relevance of the hysteresis for the *on* resistance is demonstrated and discussed. A manufacturer comparison will also be presented in this section. In a final step in Section 10.4, the derived models for PBTI and NBTI are applied to simulate application-relevant AC stress.

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10.1 Positive Bias Temperature Instability[1]

With the commercial introduction of SiC power MOSFETs comes the requirement to determine the reliability of these devices. Especially studies on the stability of the device threshold voltage are required [61]. In this section, the focus lies on the threshold voltage instabilities due to positive gate bias stress. An increase in negatively charged traps (electron trapping in the oxide or in the interface) results in a positive shift of the threshold voltage [78]. To analyze the physical nature of the defects responsible for the positive ΔV_{th} (as well as the negative ΔV_{th} under negative gate bias), spectroscopy on individual defects like for NBTI in Si devices is required [92]. Presently, such measurements are not yet available, thus the author of this thesis refrains from speculations on the physical origin of these effects, but a literature overview about ongoing discussions of the nature of the traps has been given in Section 8.4.

For Si MOSFETs, threshold voltage shifts due to BTI can be well-understood as the collective response of an ensemble of independent defects [76]. To determine whether this is also true for SiC MOSFETs, the kinetics of charge capture and emission applying the MSM scheme as described in Section 2.2 are studied on SiC trench nMOSFETs using the ultra-fast measurement setup described in Section 9.3. The samples are described in detail in Section 9.1. Each MSM measurement consists of stress times covering 12 decades in time ranging from 100 ns to 200 ks and recovery times after each stress period from 1 µs to 100 ks. To enable lifetime simulations, a model describing the stress and recovery of PBTI of SiC MOSFETs is required. A description of the charge capture and emission kinetics of SiC MOSFETs is provided by the activation energy maps as shown for Si in Section 6.1.

10.1.1 Temperature Dependence

For Si MOSFETs the threshold voltage shift increases with rising temperature (as discussed in Section 6.1.1). The threshold voltage shift in dependence on the stress time for Si and SiC MOSFETs with the same oxide thickness t_{ox} and the same E_{ox} is compared in Fig. 10.1 a) for two different temperatures.

Si MOSFETs generally show a lower ΔV_{th} due to a lower trap density compared to SiC. In addition, SiC MOSFETs show a higher, but fast recovering ΔV_{th} with a peculiarity that is only visible at short measurement delays: The measured ΔV_{th} at lower temperatures is higher than at high temperatures. Recent reports have observed the same temperature dependency as for Si MOSFETs for PBTI of SiC MOSFETs [59, 61, 78]. Therefore, the measurements presented in Fig. 10.1 a) provided surprising results for the temperature dependence. Thus two questions arise:

1. Why is a higher threshold voltage shift observed for the lower temperatures and is this in contradiction with thermal activation as described by the Arrhenius law?

2. Why do other studies on SiC threshold voltage shifts not show this temperature dependence?

In the following, the contradiction of the thermal activation in 1) is resolved by applying the concept of activation energy maps to SiC MOSFETs. Thus, the kinetics of charge capture and emission are modeled consistently with previous work on Si MOSFETs. The capture and emission activation energies are described by two bivariate Gaussian distributions [76, 272]: One distribution for the defects having short capture and emission times and one distribution for the charged defects having emission times mostly permanent in typical experimental time windows from capture and emission times 1 µs to 100 ks. Furthermore, temperature activation

[1] This chapter is based on a previous publication of the author of this thesis [KWJ5] and [KWC5].

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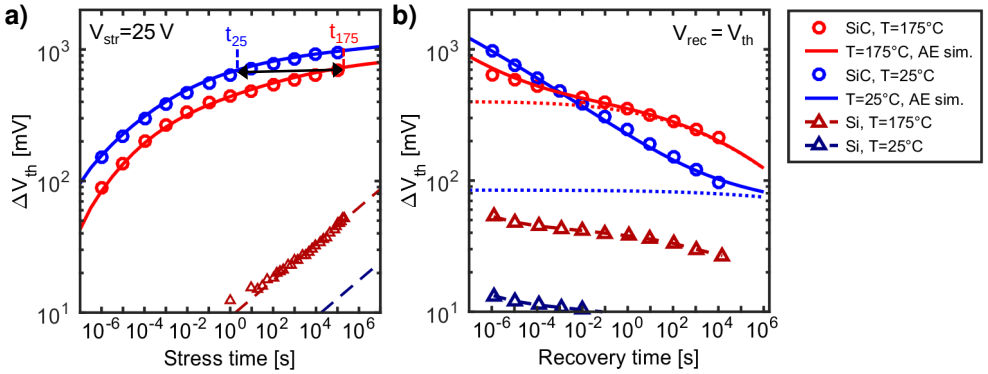

Figure 10.1: Comparison of SiC and Si MOSFETs with the same t_{ox} and the same E_{ox} during positive gate bias stress of $V_{gs,str} = 25\,V$ at $T = 25°C$ and $T = 175°C$. **a)** Dependence on the stress time for a measurement delay of $t_d = 1\mu s$: SiC shows higher ΔV_{th} with a reversed temperature dependence compared to Si. The ΔV_{th} at $T = 25°C$ is larger than at $T = 175°C$. **b)** Recovery after 200 ks stress. The slope of the V_{th} recovery at $T = 25°C$ is higher than at $T = 175°C$. A crossing of the measured ΔV_{th} is observed at around $t_d = 5\,ms$. The solid blue and red lines in both figures a) and b) show the simulations for each temperature obtained by the analytic activation energy map shown in Fig. 10.3 with the parameters given in Table 10.1. The dotted lines in b) correspond to simulations of solely the quasi-permanent component, which is for a delay of $t_d = 1\,\mu s$ at $T = 25°C \approx 10$ times and at $T = 175°C \approx 2$ times lower than the recoverable component.

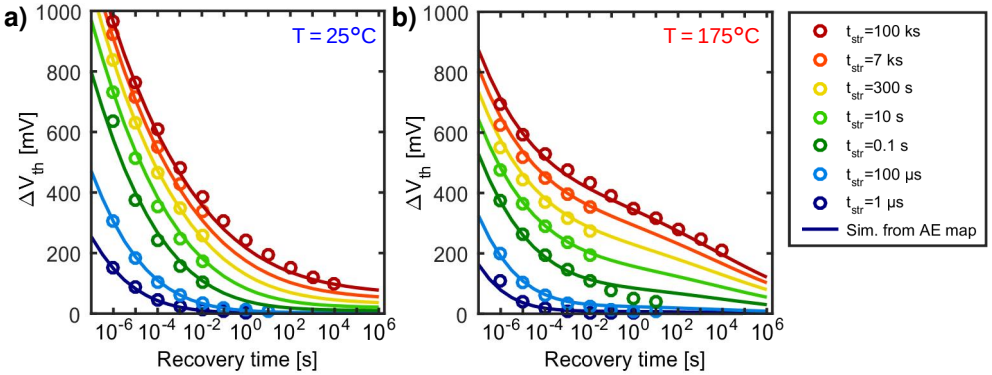

Figure 10.2: Recovery after positive DC stress of $V_{gs,str} = 25\,V$ at **a)** $T = 25°C$ and **b)** $T = 175°C$. The recovery for all stress times at $T = 25°C$ occurs faster than at $T = 175°C$. The solid lines in both figures show the simulations for each temperature obtained by the analytic activation energy map shown in Fig. 10.3.

of the individual capture and emission time constants is modeled according to the Arrhenius equation in (3.6) [90].

As a result from fits to the measurement data with all recovery measurements of stress times from 100 ns up to 200 ks at $T = 25°C$ and $T = 175°C$ as shown in Fig. 10.2, the activation energy map is obtained and $\tau_{0,r} = \tau_{0,p} = 6 \times 10^{-15}$ s is determined. The parameters for the activation energy maps shown in Fig. 10.4 are given in Table 10.1 and the solid lines in Fig. 10.1 and Fig. 10.2 correspond to calculations with the activation energy map shown in Fig. 10.3 a). Besides, the recoverable and the quasi-permanent component are shown separately in Fig. 10.4 b) and Fig. 10.4 c). To highlight the contributing defects, the measurement windows of the measurements are indicated in Fig. 10.3 a) with the blue ($T = 25°C$) and red ($T = 175°C$) rectangles. For a stress time of 200 ks and a measurement delay of 1µs, the charged trap occupation probability map as shown in Fig. 10.3 b) provides the explanation for the higher measured ΔV_{th} at $T = 25°C$ than at $T = 175°C$:

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Table 10.1: Activation energy map parameters for PBTI for Fig. 10.4, Fig. 10.5 and Fig. 10.9. For the recoverable component $r = 1$, the mean activation energy is $\mu_{(e,0)} = -0.67\,\text{eV}$ according to (6.1) and $\sigma_e = 0.59\,\text{eV}$ according to (6.2). For the permanent component $r = 0$, $\mu_{(e,0)} = \mu_{(\Delta e,0)}$ and $\sigma_{\Delta e} = \sigma_e$. The recoverable component has a mean negative emission activation energy which can be explained by the fact that these defects are difficult to detect (measurement delay too long). Thus, extrapolation towards short time constants of fitted data in the measurement window with a Gaussian distribution is spurious.

	τ_0 [fs]	μ_c [eV]	σ_c [eV]	$\mu_{\Delta e}$ [eV]	$\sigma_{\Delta e}$ [eV]	m	k [eV/V]	r
R	6	-0.47	0.55	-0.2	0.2	1.45	0.001	1
P	6	1.54	0.36	1.64	0.36	0.023	0	0

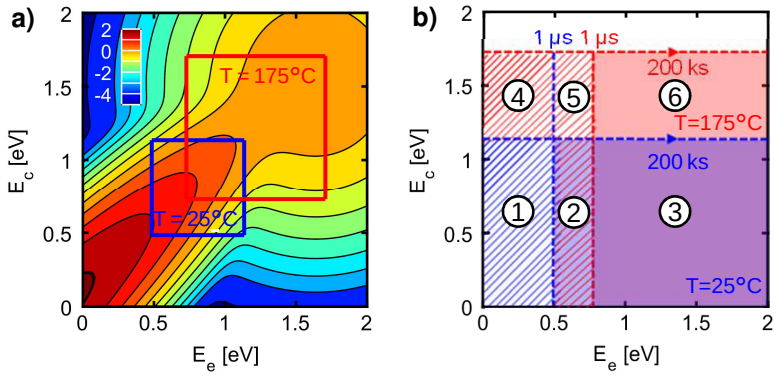

Figure 10.3: a) Analytic activation energy map obtained with stress and recovery data as shown in Fig. 10.2 with recovery traces for stress-times from 1 µs up to 200 ks at $V_{gs,str} = 25$ V. The chargeable trap density g is shown in dependence of the capture and emission activation energies with the defect distribution and its contribution to the overall threshold voltage shift shown on a logarithmic color scale. Thus, the density value z corresponds to a ΔV_{th} of 10^z V/eV^2. The measurement range from 1 µs to 200 ks is marked in blue for $T = 25°C$ and in red for $T = 175°C$. **b)** Charge trap occupancy map shown for the DC stress at $T = 25°C$ and $T = 175°C$. The blue and red filled rectangle mark the traps that are occupied for a stress time of 200 ks and a measurement delay of 1 µs. The blue and red patterned areas indicate the region of the activation energy map that is out of the measurement range at $T = 25°C$ and $T = 175°C$, respectively.

- After 200 ks stress, the trap centers within the area 1-3) at $T = 25°C$ and within area 1-6) at $T = 175°C$ are charged. Even though at $T = 175°C$, also defects with higher activation capture energies are activated, the measured threshold voltage shift is lower for short recovery times.
- With a measurement delay of 1µs, defects within area 1) at $T = 25°C$ and within area 1), 2), 4) and 5) at $T = 175°C$ are already recovered within the measurement delay. This is due to the acceleration of recovery with high temperature such that a huge amount of defects recovers already within the measurement delay as indicated with the dashed area in Fig. 10.3 b).
- A higher defect density within area 2) than within area 6) in Fig. 10.3 a) is observed. Therefore, the measured ΔV_{th} at $T = 25°C$ is higher than at $T = 175°C$ for short recovery times.
- Defects within area 6) have longer emission times, whereas defects within area 2) quickly recover as seen in Fig. 10.1 b). The recovery at a lower temperatures occurs a lot faster than at higher temperatures. Thus, after 5 ms recovery time, a crossing of the measured ΔV_{th} is observed.

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Thus, conventional measurements with typical measurement delays $t_d \leq 100\,\text{ms}$ for this reason do not resolve the higher threshold voltage shifts at lower temperature. Furthermore, conventional extraction of activation energies leads to a non-physical dependence of conventional extracted activation energies on the measurement delay. This effect is discussed in Section 11. Despite performing measurements with measurement delays of 1 µs at different temperatures (and also at room temperature) on Si MOSFETs (see Fig. 6.14), such a crossing or higher ΔV_{th} at lower temperatures has not been observed for Si MOSFETs. The reason is a different distribution of the defect density (see Fig. 6.11). For Si MOSFETs the defect density in the CET map increases from short to long capture time constants τ_c [76, 111]. For SiC by contrast, as seen in Fig. 10.4 b), the density of the recoverable component increases towards shorter time constants. From the activation energy maps shown in Fig. 10.4, the following conclusions can be drawn:

- The seemingly paradoxical temperature dependence of ΔV_{th} on the recovery time can be fully understood and described with the PBTI activation energy maps as shown in Fig. 10.4. Measurements of higher threshold voltage shifts at lower temperatures compared to high temperatures are not in contradiction with the Arrhenius law. On the contrary, dependencies of the individual traps are simply the result of differently distributed capture and emission energies of the recoverable and quasi-permanent defects in SiC MOSFETs compared to Si MOSFETs.

- Charge capture and emission of the individual traps is of course thermally activated, thus ΔV_{th} increases with temperature. From the fits with the activation energy map model, the temperature-independent time constant $\tau_{0,r} = \tau_{0,p} = 10^{-15}\,\text{s}$ is obtained.

- Due to thermal activation, emission time constants of traps around 1µs at $T = 25°\text{C}$ decrease with increasing temperature and become shorter than the measurement delay at $T = 175°\text{C}$. The fast onset of ΔV_{th} after short stress times is due to the many defects with short capture time constants (compare Fig. 10.1 a) for $t_{str} \leq 1\,\text{ms}$). Since the traps with short capture time constants ($\tau_c \leq 1\,\text{ms}$) have also short emission time constants ($\tau_e \ll 1\,\text{ms}$), ΔV_{th} vanishes as quickly as it appears within milliseconds (see Fig. 10.1 b). This explains why previous reports on threshold voltage instabilities did not mention a reverse temperature dependence: The used measurement delays were longer than the time of the crossing point ($t_d \geq 1\,\text{ms}$), thus measured threshold voltage shifts at lower temperatures were lower than at higher temperatures.

- The quasi-permanent component is less sensitive to the measurement delay and as such, the contribution to the overall ΔV_{th} is also for the shortest measurement delay in Fig. 10.1 a factor of four higher at $T = 175°\text{C}$ than at $T = 25°\text{C}$.

- Same as for Si MOSFETs, the correlation between the capture and emission activation energies for the charged trap density of the recoverable defects described by (4.13) is $r = 1$, whereas the correlation of the more permanent defects (with capture times bigger than e.g. 10 s at $T = 175°\text{C}$) is $r = 0$.

- All emission time constants of the recoverable component are shorter than their corresponding capture time constants (see Fig. 10.5 a) and b)). Therefore, the remaining ΔV_{th} after a measurement delay $t_d \leq 1\,\text{ms}$ is less at high temperatures than at low temperatures.

Please note, the increased defect density below $E_e = 0.5\,\text{eV}$ ($t_d = 1\,\mu\text{s}$ at $T = 25°\text{C}$) with a negative mean emission activation energy μ_e of the recoverable component is an artifact and is explained by the fact that these defects are difficult to detect in threshold voltage measurements. The measurement delay of $t_d = 1\mu\text{s}$ is not sufficiently small to fully capture the distribution of the recoverable component towards $E_e = 0\,\text{eV}$. Consequently, the extrapolation towards short

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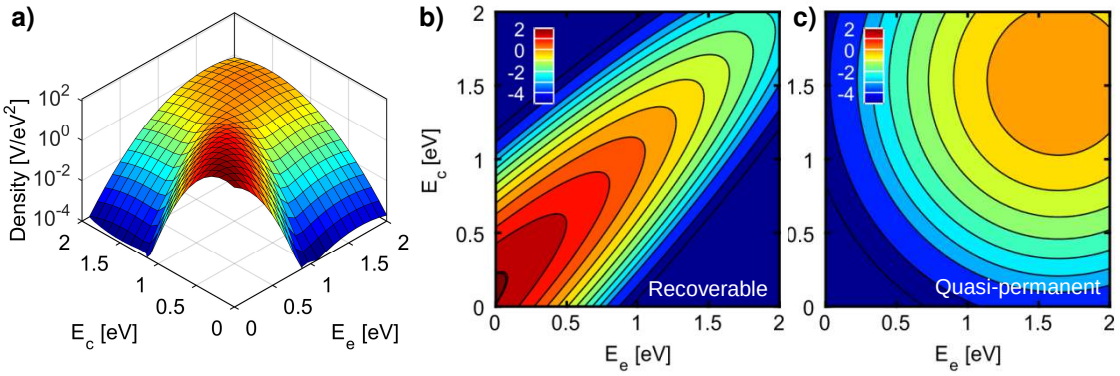

Figure 10.4: Analytic activation energy map as shown in Fig. 10.3 for $V_{\mathrm{gs,str}} = 25$ V. **a)** Recoverable and quasi-permanent component, same as the 2D-plot in Fig. 10.3. **b)** Solely the recoverable component and **c)** solely the quasi-permanent component. The defect distribution and its contribution to the overall threshold voltage shift is shown on a logarithmic color scale, the density value z corresponds to a ΔV_{th} of 10^z V/eV^2.

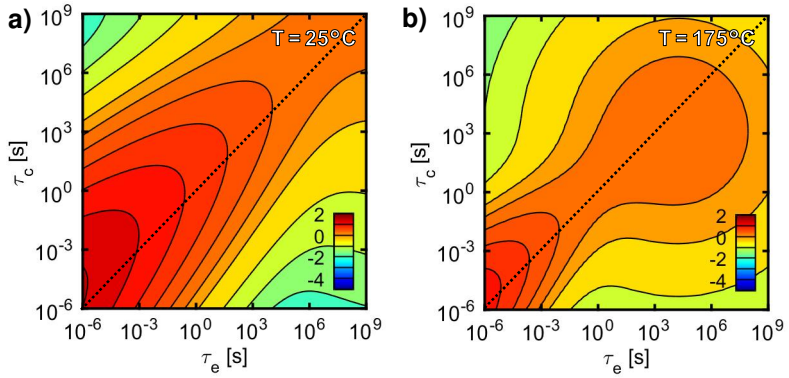

Figure 10.5: Temperature dependence of the PBTI capture and emission time maps. Instead of the capture and emission activation energies in Fig. 10.3), the defect density g is shown as a function of the capture and emission time constants at **a)** $T = 25$°C and **b)** $T = 175$°C. Both maps are shown on a logarithmic color scale as in Fig. 10.3, z corresponds to a ΔV_{th} of 7×10^z mV/decade^2. At $T = 25$°C, barely any defects of the quasi-permanent component contribute within the lifetime to ΔV_{th}, whereas at $T = 175$°C, the capture and emission time map is dominated for $\tau_{\mathrm{c}} \geq 1$ s by the quasi-permanent component.

time constants of fitted data in the measurement window with a Gaussian distribution is spurious. Nevertheless, the results are completely in accordance with measurement data for $t_{\mathrm{d}} \geq 1\,\mu$s. Measurements with shorter measurement delays and/or lower temperatures would be required to fully determine the distribution of the recoverable component.

10.1.2 Validation: Different Recovery Temperatures

To demonstrate the validity of the PBTI activation energy map model and the temperature dependence, the recovery of ΔV_{th} after the same stress time and voltage is compared for three different conditions: 1) $T_{\mathrm{str}} = T_{\mathrm{rec}} = 25$°C, 2) $T_{\mathrm{str}} = T_{\mathrm{rec}} = 175$°C with 3) $T_{\mathrm{str}} = 175$°C and $T_{\mathrm{rec}} = 25$°C as shown in Fig. 10.6 b). To measure the recovery at $T = 25$°C after the high-temperature stress at $T_{\mathrm{str}} = 175$°C, the sample is cooled down with bias applied, such that during the cool-down, ΔV_{th} does not recover [91]. The simulated ΔV_{th} for this measurement is obtained by the activation energy map shown in Fig. 10.3 with the parameters given in Table 10.1. An additional requirement for the calculation of the occupancy map is that the different recovery temperatures have to be taken into account. To further illustrate this effect, the

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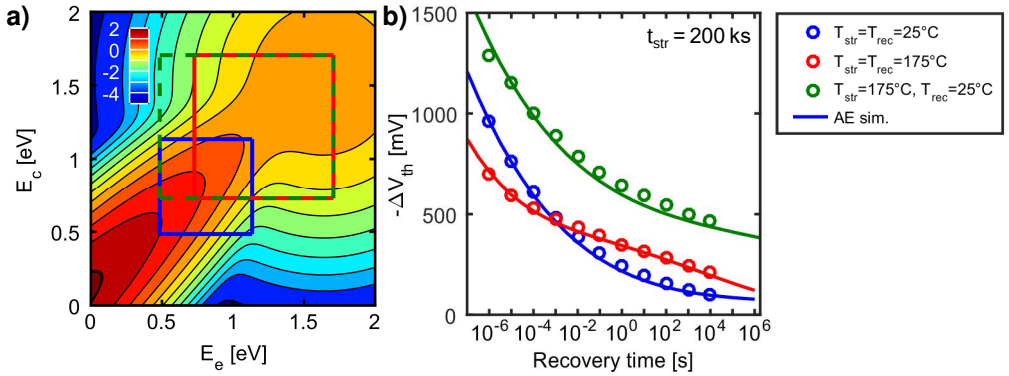

Figure 10.6: a) Activation energy map as shown in Fig. 10.3 with the measurement windows for $T_{str} = T_{rec} = 25°C$ (blue square), $T_{str} = T_{rec} = 175°C$ (red square) and $T_{str} = 175°C$ and $T_{rec} = 25°C$ (green square). The map is shown on a logarithmic color scale as in Fig. 10.3. z corresponds to a ΔV_{th} of 10^z V/eV^2. **b)** ΔV_{th} recovery traces after $t_{str} = 200$ ks at $T_{str} = T_{rec} = 25°C$ (blue) and $T_{str} = T_{rec} = 175°C$ (red) in comparison with $T_{str} = 175°C$ and $T_{rec} = 25°C$ (green). Symbols are experimental data. The solid lines are simulations obtained by the analytic activation energy map shown in a) and Fig. 10.3 with the parameters given in Table 10.1.

measurement windows of each recovery measurement is indicated in Fig. 10.6 a). After 200 ks stress at $T = 25°C$, barely any charged traps of the quasi-permanent component contribute to ΔV_{th} whereas at $T = 175°C$ more of the quasi-permanent components contribute to the overall threshold voltage shift (see also Fig. 10.5). The measurement condition 3) with the recovery at $T = 25°C$ clearly shows the highest ΔV_{th}. The recovery is dominated by the discharge of defects of the recoverable component. For $T_{rec} = 175°C$, these defects are already recovered within the measurement delay, whereas for $T_{rec} = 25°C$ after stress condition 1) and 3), recovery mainly differs by an offset in the quasi-permanent component. After 10 ks recovery at $T_{rec} = 25°C$, a saturation of the recovery is observed. To reach the same ΔV_{th} as after 10 ks high-temperature recovery, much longer recovery time at room temperature is necessary.

In conclusion, the recovery measurements at high temperatures are misleading and information about the short time constants is lost. In fact, as is also the case and well-known for Si MOSFETs, the threshold voltage shift after high-temperature stress is higher than for room temperature stress. To avoid loss of information and provide comparability of different stress temperatures, ΔV_{th} after high-temperature stress should also be measured at room temperature or even cryogenic temperatures with a measurement delay as short as possible [91]. For lifetime extrapolation, capture and emission time maps should be used in order to properly consider the recovery.

This work demonstrates the first model which accurately describes and explains the temperature dependence of PBTI including recovery effects. With this model, the differences between the recovery at $T = 175°C$ and $T = 25°C$ can be fully attributed to the temperature acceleration of the recovery at high temperatures.

10.1.3 Gate Stress Voltage Dependence

To provide a complete modeling approach for ΔV_{th} after DC as well as after long-term AC stress, the activation energy map has to be extended to include also the stress voltage dependence [94]. The stress and recovery time dependence of ΔV_{th} at four different stress voltages is compared in Fig. 10.7 and a power-law-like dependence for long stress times is observed. The power-law exponent is $n = 0.035 \pm 0.03$ and independent of the stress voltage (extracted from the last five measurement points in Fig. 10.7 a) following (4.1)).

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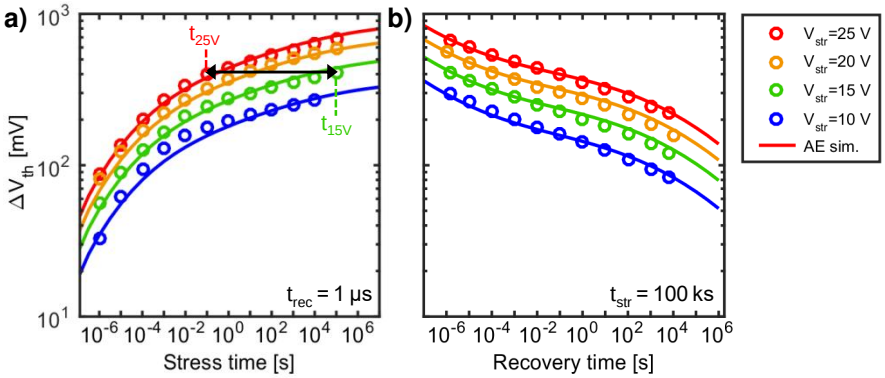

Figure 10.7: a) Comparison of ΔV_{th} as a function of stress time for four different voltages with $t_{\text{d}} = 1\,\mu\text{s}$ and $T = 175°\text{C}$. **b)** Comparison of the recovery after 100 ks stress time. The solid lines show the simulations for each voltage obtained by the voltage-dependent analytic activation energy map as shown in Fig. 10.9. Good agreement between measurement and simulations is achieved with the parameters given in Table 10.1.

The measured ΔV_{th} at a fixed stress/recovery time increases linearly with the stress voltage as shown in Fig. 10.8 a). Also, the emission time constants seem to be unaffected by the stress voltage, as ΔV_{th} in all recovery measurements shown in Fig. 10.7 b) decreases in the same manner for each stress voltage, solely linearly shifted in amplitude by the stress voltage.

To model the voltage dependence of PBTI of the SiC MOSFETs, the model for the activation energy map discussed in Section 4.4.1 is extended:

- The threshold voltage shift linearly increases with stress voltage as shown in Fig. 10.7a). Therefore, the amplitudes of each component (A_{r} and A_{p}) (equivalent to the number of active traps) are modeled to linearly increase with stress voltage $V_{\text{gs,str}}$ and slope m:

$$A = m \cdot V_{\text{gs}}. \tag{10.1}$$

- Previous studies on individual defects of Si MOSFETs [92] have shown that the mean value μ_{c} of each distribution linearly decreases with increasing stress voltage (capture times decrease with increasing stress voltage). From the measurements in Fig. 10.7, a strong increase of μ_{c} when increasing the stress voltage is not expected, nonetheless following the previous results on Si MOSFETs, the linear decrease of μ_{c} with increasing stress voltage is modeled by:

$$\mu_{\text{c}} = \mu_{\text{c,0}} - kV_{\text{gs}} \tag{10.2}$$

  with $\mu_{\text{c,0}}$ the mean value of the activation energy constants for the charge capture at 0 V and k the voltage acceleration constant.

- According to the NMP model, the emission times remain unaffected by the stress voltage. Due to the relation of the capture and emission energies in (4.13) and (10.2), the mean value $\mu_{\Delta\text{e}}$ of the activation energy constants for the charge capture at 0 V is increased accordingly:

$$\mu_{\Delta\text{e}} = \mu_{\Delta\text{e,0}} + kV_{\text{gs}} \tag{10.3}$$

The effect of an increased stress voltage on the activation energy map is shown in Fig. 10.9. The modeling results calculated with the voltage-dependent activation energy map for each voltage are shown as lines in Fig. 10.7 and Fig. 10.8. Model and measurement are in perfect agreement.

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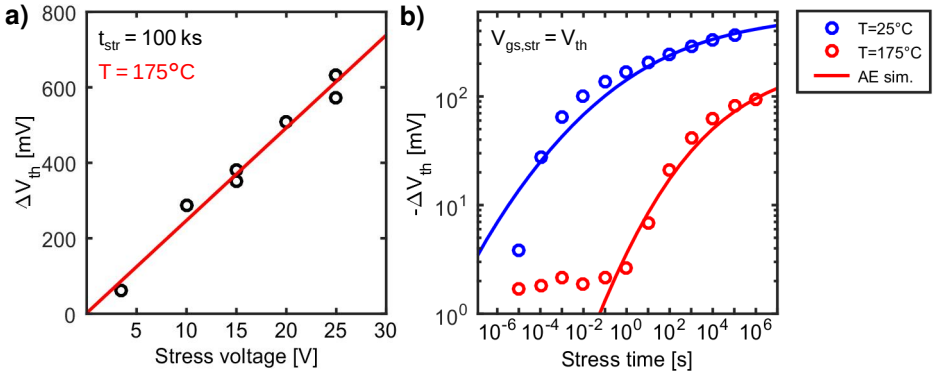

Figure 10.8: **a)** SiC PBTI threshold voltage shift in dependence on the stress voltage for a stress time of $t_{str} = 100\,\text{ks}$ and a recovery time of $t_d = 1\mu\text{s}$ with $T = 175°\text{C}$. The circles correspond to the measurement points whereas the red solid line corresponds to the simulation by the voltage-dependent activation energy map as shown in Fig. 10.9 with the parameters given in Table 10.1. **b)** The threshold voltage shift solely induced by measurement of the threshold voltage such that $V_{gs,str} = V_{th}$ at $T = 25°\text{C}$ and $T = 175°\text{C}$. Due to the extraction of the threshold voltage at the same drain current for both temperatures ($I_{ds} = 2\,\text{mA}$), the stress voltage is different for each temperature with $V_{gs,str} \approx 4.3\,\text{V}$ at $T = 175°\text{C}$ and $V_{gs,str} \approx 5.1\,\text{V}$ at $T = 25°\text{C}$.

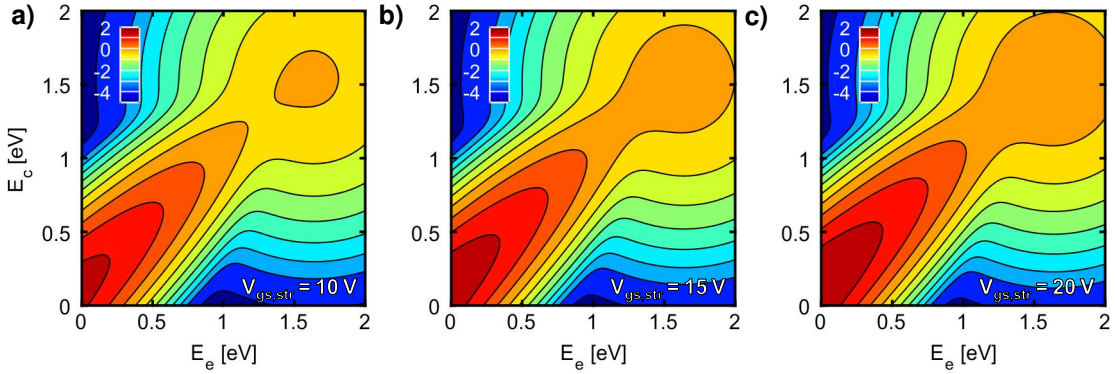

Figure 10.9: Voltage-dependent analytic activation energy map for SiC as shown in Fig. 10.3 for **a)** $V_{gs,str} = 10\,\text{V}$, **b)** $V_{gs,str} = 15\,\text{V}$ and **c)** $V_{gs,str} = 25\,\text{V}$. All maps are shown on a logarithmic color scale as in Fig. 10.3, z corresponds to a ΔV_{th} of $10^z\,\text{V/eV}^2$.

The obtained parameters for the voltage-dependent activation energy maps are given in Table 10.1. Similar to Si MOSFETs [76], a stronger voltage dependence of the amplitude and mean values is observed for the recoverable component than for the quasi-permanent component ($k_r = 0.001\,\text{V/eV}$ and $k_p = 0\,\text{V/eV}$).

The following differences and similarities for the voltage dependence to Si MOSFETs are observed:

- For Si MOSFETs, the number of active traps increases following (6.6) with roughly V_{gs}^4 instead of a linear dependence on the stress voltage as observed here for SiC MOSFETs.
- Stress voltage-independent mean emission time constants have also been observed for Si as discussed in [76] and Section 6.1.3. The strong bias dependence of the individual traps does not directly translate into the distribution of time constants and the reason for this is that with different gate bias, the energetically available traps in the oxide also change [200].

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- For Si MOSFETs, due to $\Delta V_{\text{th}} \propto {V_{\text{gs}}}^4$, applying V_{th} for a long time does not cause any significant threshold voltage shift. As seen in Fig. 10.8 b), already applying V_{th} ($V_{\text{gs,str}} = V_{\text{th}}$ for $t_{\text{str}} = 100\,\text{ks}$) increases the threshold voltage of the SiC MOSFETs by more than 100 mV. Thus, extreme caution is required when setting up measurements to not affect the measurement due to unwanted threshold voltage instabilities. To ensure the comparability of the measurements and enable modeling, the same device preconditioning should be applied before any new sample can be stressed and measured. One possibility is the preconditioning technique proposed by Rescher *et al.* (see Section 2.3 and [79]).

Commonly used lifetime models, whether they are applied to for Si or SiC MOSFETs, are based on a power-law following (4.4). In these simple models, the decrease of the lifetime at accelerated stress conditions compared to use conditions is often considered with a voltage acceleration factor and the extracted voltage acceleration factor a_{v} is defined as

$$a_{\text{v}} = \frac{t_{V_1}}{t_{V_2}}, \tag{10.4}$$

with t_{V_1}, the stress time needed to reach a certain $\Delta V_{\text{th,lim}}$ during application of a gate stress voltage V_1. And t_{V_2}, the stress time to reach $\Delta V_{\text{th,lim}}$ at V_2 (as indicated by the arrows in Fig. 10.10 b) with $V_1 = 15\,\text{V}$ and $V_2 = 25\,\text{V}$). Dependent on the measurement delay, the extracted voltage acceleration factor shown in Fig. 10.10 a) differs by four orders of magnitude.

In conclusion, the parameters required for lifetime predictions, e.g. stress time dependence, activation energy, and voltage acceleration factor depend strongly on the measurement delay and measurement technique (e.g. preconditioning). The simple standard empirical modeling approaches are therefore not recommended.

Furthermore, lifetime estimation according to the JEDEC [308] procedure allows a measurement delay of 48 hours. This is inappropriate for SiC MOSFETs because of the strong recovery dependence and the negligence of the fast recovering components. With the use of PBTI CET maps, all parameters needed for lifetime predictions are provided and the measurement delay is considered in the model. Furthermore, the maps can be used for the simulation of AC stress as shown in Section 10.4.

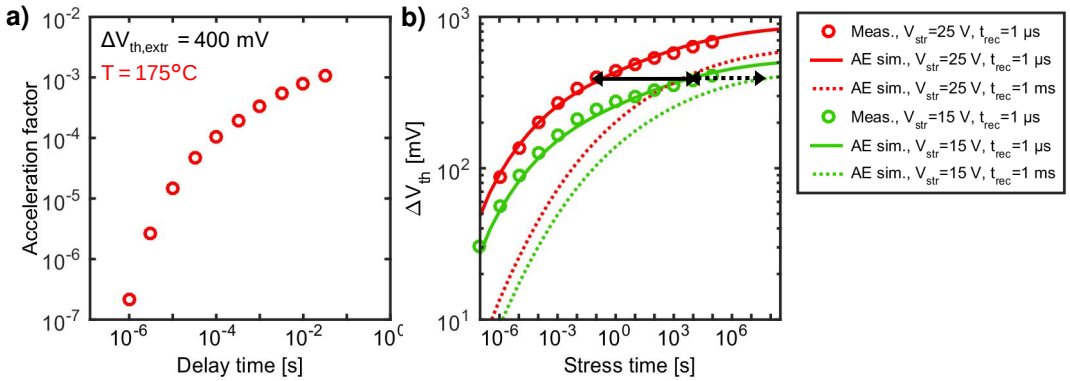

Figure 10.10: a) Voltage acceleration factor taken at $\Delta V_{\text{th}} = 400\,\text{mV}$ between 15/25 V as a function of the recovery time. With this approach, the extraction of lifetime models for SiC MOSFETs is hampered by different voltage acceleration factors depending on the measurement delay. **b)** Stress time dependence of ΔV_{th} for two different recovery times. Arrows indicate the extraction of the voltage acceleration factor.

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10.1.4 Recovery Voltage Dependence

In addition to the stress voltage dependence of the capture time constants, there is also a dependence of the emission time constants on the recovery voltage. In particular, it is necessary to study the time-constants with recovery voltage for negative as well as positive stress to provide a model for bipolar AC stress with variable voltage levels. When switching from positive to negative gate voltage, the accelerated recovery of the positive ΔV_{th} with decreased recovery voltage has to be considered. The dependence of the measured V_{th} recovery after a recovery pulse V_p with different pulse times t_p is shown for two different recovery voltages in Fig. 10.11. All recovery traces at $V_{gs,rec} = V_{th}$ merge at a certain point in time because the recovery pulse V_p causes an acceleration of the recovery. Negative recovery pulses lead to a drastic short-term reduction of V_{th} due to NBTI (compare Section 10.2.3).

Full recovery after NBTI occurs within less than a second, therefore the positive ΔV_{th} due to PBTI can still be extracted from Fig. 10.11 b). The time t_p it takes for V_{th} to recover back to its initial value after positive stress dependent on the recovery voltage is shown in Fig. 10.12 for two stress times for $T = 25°C$ and $T = 175°C$. Applying e.g. $V_p = -5\,V$ after positive stress accelerates the recovery back to the initial V_{th} by more than 8 orders of magnitude in time compared to applying $V_p = 5\,V$ during recovery (dependent on the temperature and positive bias stress time). These properties have to be considered when performing simulations with the activation energy map by correcting the occupation probability map by the corresponding de- or accelerated recovery times as has been discussed in detail in Section 7.6.

10.1.5 Influence of the Preconditioning Pulse

To remove the recoverable component from the measurement and obtain a mostly measurement delay-independent threshold voltage shift, the preconditioning technique has been proposed by Rescher *et al.* [38, 77] and has been summarized in Section 2.3. In Fig. 10.13, the measurement results of the preconditioning technique are compared to the measurement results with a measurement delay of $t_d = 1\mu s$ without the preconditioning.

Preconditioning is performed by applying $V_{gs} = -15\,V$ for 1 s before every readout. As can be seen in Fig. 10.13, the measured ΔV_{th} with preconditioning is $\approx 25\%$ of the measured ΔV_{th} with a delay of $t_d = 1\mu s$. As intended with the preconditioning, the measured ΔV_{th} consists of only a contribution of the quasi-permanent component.

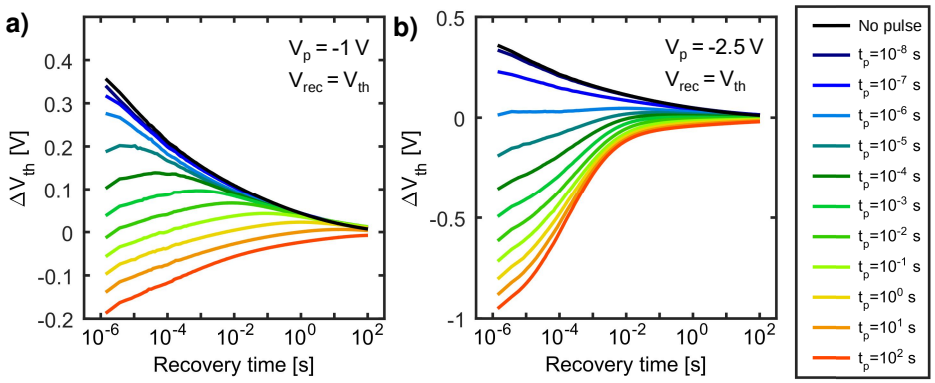

Figure 10.11: Recovery at $V_{gs,rec} = V_{th}$ from positive stress ($V_{gs,str} = 25\,V$, $t_{str} = 1\,s$) at $T = 175°C$ after applying a recovery pulse with different pulse times t_p with a recovery voltage of **a)** $V_p = -1\,V$ and **b)** $V_p = -2.5\,V$. The black line shows the recovery without the recovery pulse at $V_{gs,rec} = V_{th}$. All recovery curves merge at a defined point in time as a decreased recovery voltage results in an acceleration of the recovery.

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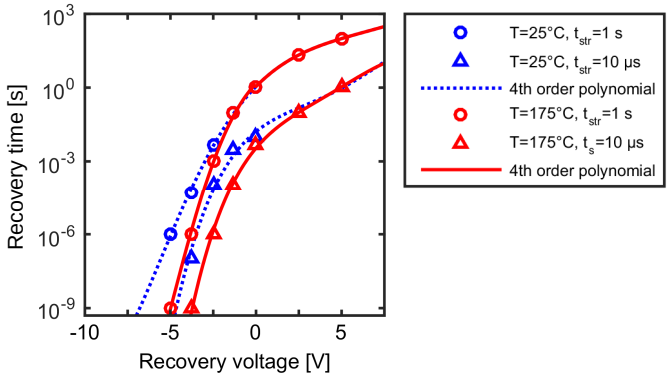

Figure 10.12: Recovery from positive stress ($V_{\mathrm{gs,str}} = 25\,\mathrm{V}$, $t_{\mathrm{str}} = 10\,\mu\mathrm{s}$ (rectangles) and $t_{\mathrm{str}} = 1\,\mathrm{s}$ (circles)) at $T = 25°\mathrm{C}$ and $T = 175°\mathrm{C}$. Shown is the required time at $V_{\mathrm{gs,rec}}$ to recover V_{th} back to its initial value (compare example in Fig. 10.11). The required time decreases drastically with decreasing recovery voltage. The recovery voltage dependence is empirically modeled by a 4th order polynomial for each temperature (dashed and dotted lines).

The simulations of the quasi-permanent component with a measurement delay of 1 s, which corresponds to the length of the preconditioning pulse, is a factor of two higher than the measurement results obtained with preconditioning. This already indicates that not only the recoverable component shows recovery acceleration by the preconditioning pulse of $V_{\mathrm{gs}} = -15\,\mathrm{V}$, but also the quasi-permanent component shows accelerated recovery for $V_{\mathrm{gs,rec}} = -15\,\mathrm{V}$ compared to $V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$. Measurements as shown in Fig. 10.12 with longer stress times are required to also obtain the recovery voltage dependence of the quasi-permanent component. Simulations with a delay of 100 ks ($V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$) show good agreement with the measurement data, which would correspond to an acceleration of the recovery by five decades in time by applying $V_{\mathrm{gs,rec}} = -15\,\mathrm{V}$ instead of $V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$. For industrial measurements, with a low timing resolution and undefined waiting time before the measurement, the preconditioning technique is recommended. Nonetheless, for physical investigations fast threshold voltage measurements are the method of choice.

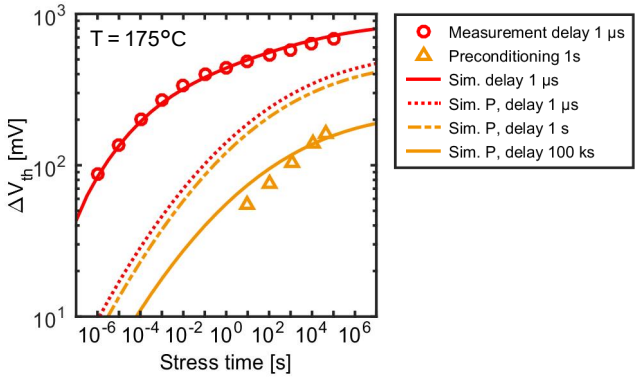

Figure 10.13: Comparison of ΔV_{th} with the fast MSM measurement technique and a measurement delay of $t_{\mathrm{d}} = 1\mu\mathrm{s}$ (circles) and the preconditioning technique (triangles) as presented in Section 2.3 with $V_{\mathrm{gs}} = 25\,\mathrm{V}$ at $T = 175°\mathrm{C}$. Preconditioning is performed with $V_{\mathrm{gs}} = -15\,\mathrm{V}$ for 1 s before every readout. Simulations obtained by the PBTI activation energy map (see Fig. 10.5) are shown as lines. The solid red line corresponds to the simulation with the recoverable and quasi-permanent component with $t_{\mathrm{d}} = 1\mu\mathrm{s}$, the dotted red line shows solely the corresponding quasi-permanent component. The orange lines correspond to simulations of only the quasi-permanent component with different measurement delays ($t_{\mathrm{d}} = 1\,\mathrm{s}$ and $t_{\mathrm{d}} = 100\,\mathrm{ks}$) as the recoverable component is fully discharged due to $V_{\mathrm{gs}} = -15\,\mathrm{V}$ for 1 s. Preconditioned measurements provided by Gerald Rescher [79].

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10.1.6 Manufacturer Comparison

In this section, commercially available SiC MOSFETs of three different manufacturers are compared regarding their threshold voltage shift under positive bias temperature stress. The purpose of this comparison is not to discuss and compare different oxide qualities. Rather, the goal of this study is to demonstrate that the observed temperature dependence of the threshold voltage shift (see Section 10.1.1) is not a unique feature of the studied trench MOSFETs, but a fundamental property of the SiC/SiO_2-system. The devices are labeled T2 (T=trench), D1 and D2 (D=lateral) to maintain manufacturer anonymity. All devices were stressed and measured with the same MSM scheme as presented in Section 2.2 using the setup described in Section 9.3 with $V_{ds} = 0.1\,V$ and $I_{ds,meas} = 2\,mA$ at $T_{str} = 25°C$ and $T_{str} = 175°C$. The stress voltage of $V_{gs,str} = 25\,V$ was chosen in such a way that the applied bias is within the maximum allowed gate bias specified in the datasheets.

A similar dependence of the measured ΔV_{th} on the stress time is observed for all three devices as shown in Fig. 10.14 a-c) for $T = 25°C$ and $T = 175°C$. The measured threshold voltage shift at $T = 25°C$ is for all devices higher than at $T = 175°C$ (with a recovery time of $t_d = 1\,\mu s$) which has also been observed for the previously investigated trench MOSFET. Furthermore, a pronounced recoverable component is observed for all devices (fast increase of ΔV_{th} for short stress times with $t_{str} \leq 100\,ms$). A comparison of the recovery of the threshold voltage shift per nanometer oxide thickness in Fig. 10.14 d-f) reveals the crossing of the recovery traces for all devices. Since the crossing point of the recovery traces occurs faster than $t_d = 100\,ms$, measurement techniques with long measurement delays as in [59, 61, 78] could not reveal this feature of the positive bias temperature instability for SiC devices.

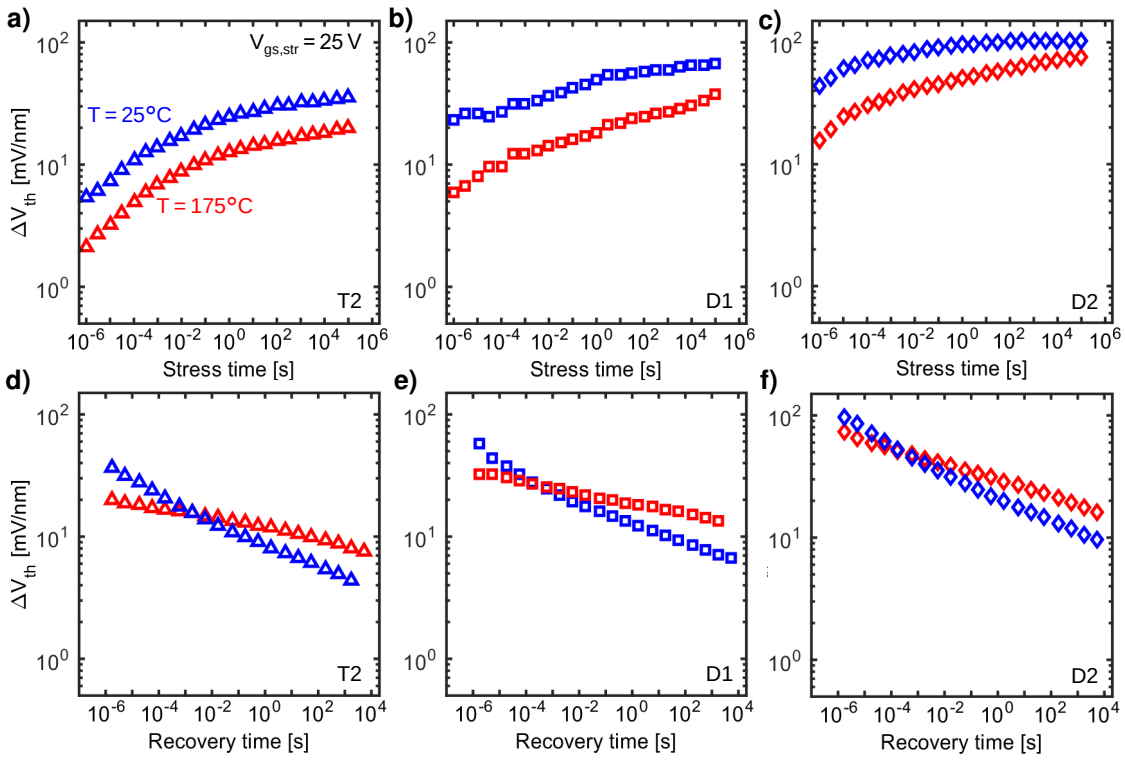

Figure 10.14: SiC PBTI manufacturer comparison: **a-c)** stress at $V_{gs,str} = 25\,V$ and following **d-f)** recovery of the threshold voltage shift per nanometer oxide thickness at $T = 25°C$ and $T = 175°C$ for the devices T2, D1 and D2. The stress time dependence is shown with a measurement delay of $t_{rec} = 1\,\mu s$ while the recovery is shown for $t_{str} = 100\,ks$.

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Although devices from different manufacturers differ in the absolute values of the threshold voltage shift, the oxide thickness, and oxide properties, the similar dependencies of all devices indicate that the observed threshold voltage shifts discussed in Section 10.1 are a fundamental property of the SiC/SiO_2-interface independent of the device architecture (trench or lateral) and are not related to e.g. device processing, mobile ion contamination, or chip-package interaction.

Overall it can be concluded that even though the measured threshold voltage shifts for SiC devices are higher than for their silicon counterparts, fundamental differences are the distribution of the capture and emission time constants and the higher number of traps with capture as well as emission time constants below 1 s. This is likely a consequence of the different energetic positions of the 4H – SiC conduction and valence band edges [273]. The main contribution to the threshold voltage shift at $T = 25°C$ of all SiC MOSFETs under test does not originate from permanent damage of the interface. Threshold voltage shifts at $T = 25°C$ are nearly fully recoverable within typical measurement times of $t_{rec} = 100\,ks$.

10.2 Negative Bias Temperature Instability (NBTI)

To prevent unintentional turn-on due to noise, SiC MOSFETs are typically turned off with negative applied gate voltages, and thus switching is performed with bipolar (negative as well as positive) AC voltages. Therefore, it is of particular importance to also analyze and model the threshold voltage after negative gate bias stress. Application of a negative gate voltage results in a decrease of the threshold voltage leading to a five orders of magnitude increase in the leakage current [61] (source-drain current at $V_{gs} = 0\,V$). This effect can be directly seen when comparing up- and down-sweeps of $I_{ds}V_{gs}$-curves with negative starting voltages [59–61]. The observed sub-threshold voltage hysteresis and its dependence on the starting voltage of the $I_{ds}V_{gs}$-sweep can be well-explained by the shift of the threshold voltage towards smaller threshold voltages by increasing the negative voltage [60, 277] (see Section 10.3). Despite the straight-forward measurement, any extraction of the threshold voltage shift within an $I_{ds}V_{gs}$-sweep is influenced by the sweep rate. The sweep is usually quite slow and in the range of $\approx 100\,ms$ (compare Section 2.1.2). Furthermore, due to the longer measurement delay (compared to $t_d = 1\,\mu s$), the negative ΔV_{th} has already partially recovered when the up-sweep reaches $V_{gs} = V_{th}$. Thus the hysteresis is only visible in the sub-threshold regime and ΔV_{th}^{hyst} depends on the sub-threshold current chosen for the extraction. To fully characterize and model all dependencies of NBTI for SiC MOSFETs, recording $I_{ds}V_{gs}$-sweeps is not the measurement technique of choice.

The advanced measurement technique applied in this work (presented in Section 9.3) provides information on the time-dynamics determined by the capture and emission time constants after NBTI stress and recovery. In this section, the threshold voltage shift after negative stress is studied and modeled in dependence of the temperature, stress, and recovery voltage. The derived model is then applied in Section 10.3.1 to simulate the threshold voltage hysteresis in $I_{ds}V_{gs}$-sweeps.

10.2.1 Temperature Dependence

Under negative gate bias, a large and very fast negative ΔV_{th} is observed (e.g. up to 4 V ΔV_{th} within seconds of NBTI stress). A typical voltage used for turn-off is $V_{gs} = -5\,V$ as shown in Fig. 10.15 a) which causes a reduction of V_{th} by about 3 V. This reduction in the threshold voltage is not permanent for all temperatures, in fact, full recovery is observed within milliseconds to seconds as seen in Fig. 10.15 b). Even for short stress times, the threshold voltage shift is observed and it already saturates after $t_{str} = 100\,s$ at $T = 175°C$. To study and model the distribution of the time constants for capture and emission of the defects, the same concept as for the PBTI activation energy maps is applied to the negative gate bias MSM measurements.

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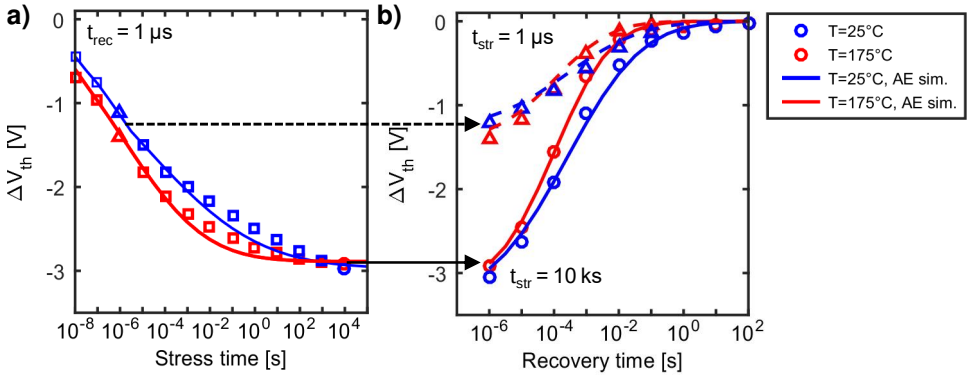

Figure 10.15: Threshold voltage shift after negative stress and its recovery at $V_{gs,str} = -5\,V$, $V_{gs,rec} = V_{th}$ for two temperatures ($T_{str} = T_{rec} = 25°C$ and $T_{str} = T_{rec} = 175°C$). **a)** Saturation of V_{th} is observed after $t_{str} = 100\,ks$ at $T = 175°C$. At $T = 25°C$, the time to saturation is significantly longer (symbols correspond to the measurement data with a measurement delay of 1 µs). **b)** Recovery towards the initial V_{th} at $V_{gs,rec} = V_{th}$ for $t_{str} = 1\,\mu s$ (triangles) and $t_{str} = 10\,ks$ (circles). Solid and dashed lines are simulations obtained by the NBTI CET maps shown in Fig. 10.17 for each temperature.

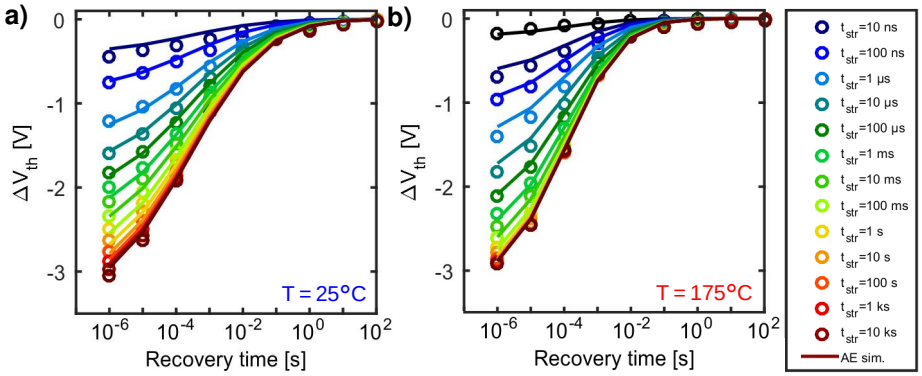

Figure 10.16: Threshold voltage shift and its recovery for all stress and recovery times used for the extraction of the activation energy maps in Fig. 10.17 with $V_{gs,str} = -5\,V$ and $V_{gs,rec} = V_{th}$ at **a)** $T = 25°C$ and **b)** $T = 175°C$.

A typical data set with MSM measurements for stress times from $t_{str} = 100\,ns$ up to $t_{str} = 100\,ks$ and recovery times until full recovery ($t_{rec} = 1\mu s$ up to $t_{rec} \sim 100\,ks$) is shown in Fig. 10.16 and the activation energy map parameters in Table 10.2 are obtained from the fit to the shown MSM data (calculation of the threshold voltage shift for each stress/recovery time and optimizing the parameters of the activation energy map). The corresponding maps are shown in Fig. 10.17.

Contrary to PBTI, the distribution of the traps does not contain traps having long capture and emission time constants. These results are fully consistent with the observations of full recovery and saturation of the ΔV_{th} for long stress times. Therefore, the activation energy map in Fig. 10.16 solely contains a recoverable component and as such, the number of parameters describing the distributions is reduced by a factor of 2 (no permanent component). Furthermore, the density of traps with small capture and emission time constants is higher than for PBTI and correlates with the 3 V ΔV_{th} observed after only $t_{str} = 100\,s$ stress at $T = 175°C$. Additionally, the capture and emission time constants in Fig. 10.17 are narrowly distributed and show a wider distribution of the capture time constants than the emission time constants.

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Table 10.2: NBTI Activation energy map parameters with $V_{gs,rec} = V_{th}$ and $V_{gs,rec} = \text{const} = 5\,V$ obtained with the measurements shown in Fig. 10.17. Contrary to PBTI, NBTI activation energy map consist solely of a recoverable component with correlation parameter $r = 0$.

	τ_0 [µs]	μ_c [eV]	σ_c [eV]	$\mu_{\Delta e}$ [eV]	$\sigma_{\Delta e}$ [eV]	A_0 [V]	r
R ($V_{gs,rec} = V_{th}$)	10	0.001	0.235	0.1	0.1	3.14	0
R ($V_{gs,rec} = \text{const}$)	2	-0.01	0.28	0.12	0.15	3.05	0

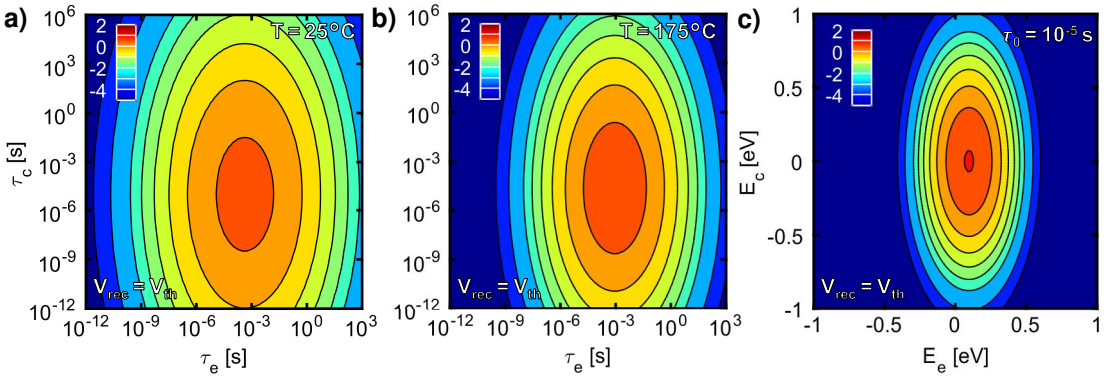

Figure 10.17: NBTI capture and emission time maps ($V_{gs,str} = -5\,V$, $V_{gs,rec} = V_{th}$) at **a)** $T = 25°C$ and **b)** $T = 175°C$ and the activation energy map in **c)** obtained by a common fit for both temperatures to the measurement data shown in Fig. 10.16 with recovery traces for stress times from $t_{str} = 100\,ns$ up to $t_{str} = 100\,ks$. All maps are shown on a logarithmic color scale, z corresponds to a ΔV_{th} of 20×10^z mV/decade^2 for the CET maps and to a ΔV_{th} of 10^z V/eV^2 for the activation energy map in c).

The temperature dependence is slight, but shows some interesting effects:

- The difference in temperature is mainly visible in a longer stress time to saturation t_{sat} ($T = 25°C$: $t_{sat} \approx 10\,ks$; $T = 175°C$: $t_{sat} \approx 100\,s$). Due to the logarithmic color scale, it becomes apparent that the distribution of the capture and emission time constants at $T = 25°C$ is broader than at $T = 175°C$, which explains the longer time to saturation.
- For stress times longer than $t_{str} = 10\,ks$ in Fig. 10.16, the measured V_{th} is lower at $T = 25°C$ due to slower recovery at $T = 25°C$ than at $T = 175°C$. Furthermore, due to the same reason, a crossing of the ΔV_{th} recovery is observed for the short stress times (e.g. at $t_d = 1\,\mu s$ in Fig. 10.15 a).

As for PBTI, these temperature dependencies can be explained with the Arrhenius temperature acceleration: The activation energies for charge capture and charge emission are below 100 meV with $\tau_0 = 10^{-5}$ s as shown in Fig. 10.17 c). Negative emission energies as seen in Fig. 10.17 c) are unphysical and are artifacts of the Gaussian distribution used for the fit. Furthermore, the value for $\tau_0 = 10^{-5}$ s might be influenced by the limitations of the measurement delay of $t_d = 1\,\mu s$. For further investigations, measurements with shorter delays and/or lower temperatures are required. Nonetheless, the negative activation energies do not influence the simulations, due to the correct consideration of the measurement delay of $t_d = 1\,\mu s$.

10.2.2 Recovery Voltage Dependence

A complete model of SiC threshold voltage instabilities should also include the NBTI recovery voltage dependence as during switching operations there is recovery of either PBTI at negative recovery voltages or recovery of NBTI at positive voltages. A constant current is forced to measure the threshold voltage and as such, during the NBTI measurements, the recovery voltage

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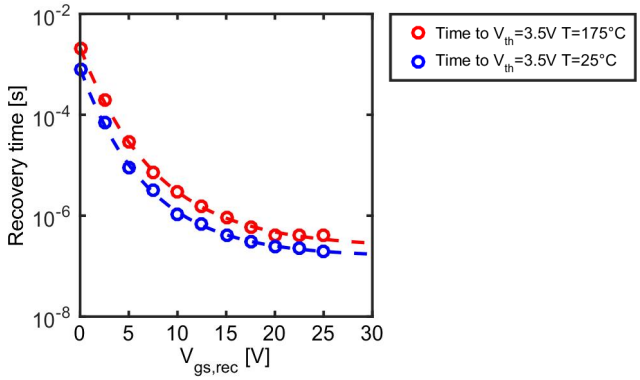

Figure 10.18: Recovery from negative stress ($V_{\mathrm{gs,str}} = -10\,\mathrm{V}$, $t_{\mathrm{str}} = 10\,\mathrm{ms}$) at $T = 25°\mathrm{C}$ and $T = 175°\mathrm{C}$. Shown is the required time at $V_{\mathrm{gs,rec}}$ to recover V_{th} back to a value of 3.5 V. The required time decreases exponentially with increasing recovery voltage (dashed lines), the charge emission at operation voltage occurs within 100 ns after switching to a positive V_{gs}.

is not constant but is equal to the measured recovering V_{th}. As this V_{th} varies already for stress with $V_{\mathrm{gs}} = -5\,\mathrm{V}$ by 3 V, the recovery voltage dependence should first be extracted from separate measurements and then be considered in the extraction of the activation energy maps to obtain the activation energy maps for a constant recovery voltage. As discussed for PBTI in Section 10.1.4, the recovery voltage dependence is integrated within the calculation of the occupation probability map. The time required of V_{th} to recover back to the initial V_{th} after NBTI stress of $V_{\mathrm{gs}} = -10\,\mathrm{V}$ is shown as a function of the recovery voltage in Fig. 10.18. The recovery time depends exponentially on the gate voltage during recovery and is empirically modeled as:

$$t_{\mathrm{rec,trans}} = a_{\mathrm{rec}} \cdot \exp^{b_{\mathrm{rec}} V_{\mathrm{gs,rec}}} \tag{10.5}$$

For switching applications, the recovery of NBTI with positive voltages above 15 V is the most relevant as it occurs within typical applications. Important for the application is that in the first 100 ns after switching from negative to positive voltages most of the negative ΔV_{th} disappears, and the negative ΔV_{th} actually helps to switch the MOSFET faster into the on-state than without this ΔV_{th}. To obtain the activation energy maps at a constant recovery voltage, the recovery voltage dependence of V_{th} has to be included in the model as shown in Fig. 10.19.

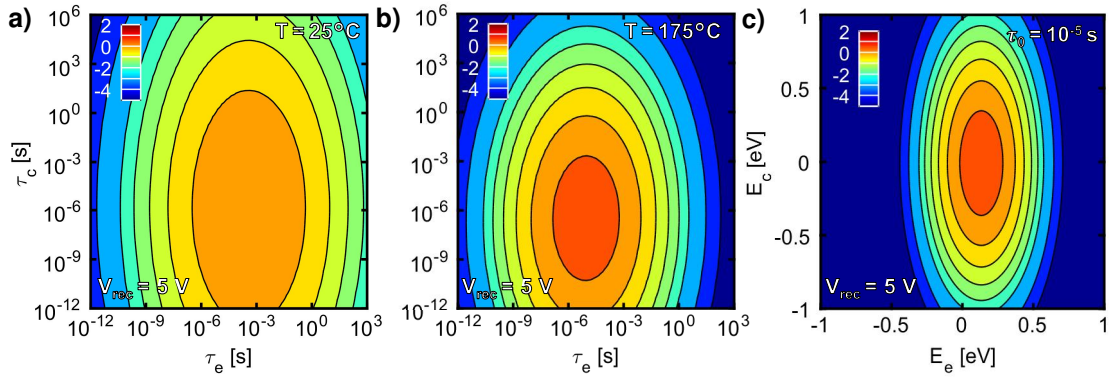

Figure 10.19: NBTI capture and emission time maps at a constant recovery voltage $V_{\mathrm{gs,rec}} = 5\,\mathrm{V}$ (same stress voltage as Fig. 10.17 of $V_{\mathrm{gs,str}} = -5\,\mathrm{V}$,) at **a)** $T = 25°\mathrm{C}$ and **b)** $T = 175°\mathrm{C}$ and the activation energy map in **c)** obtained by a common fit for both temperatures to the measurement data shown in Fig. 10.16 considering the recovery voltage dependence during the measurement via (10.5) (see Fig. 10.18). All maps are shown on a logarithmic color scale, z corresponds to a ΔV_{th} of 20×10^z mV/decade^2 for the CET maps and to a ΔV_{th} of 10^z V/eV^2 for the activation energy map.

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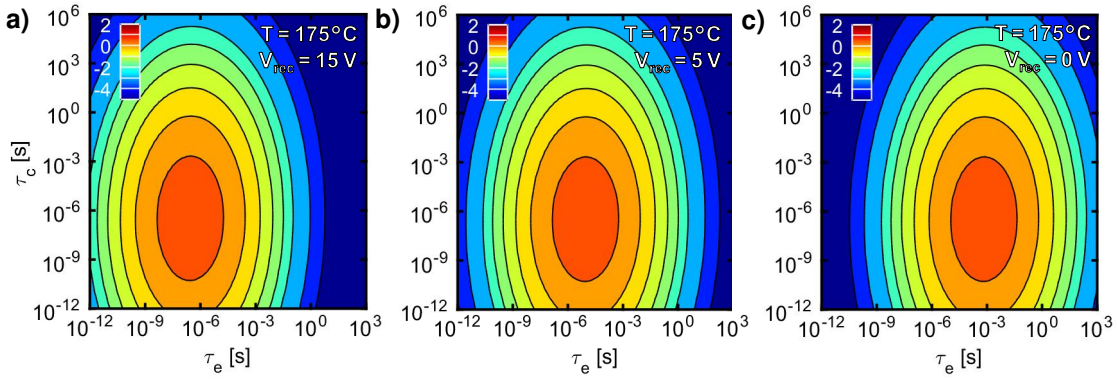

Figure 10.20: NBTI capture and emission time maps for different constant recovery voltages ($V_{\mathrm{gs,str}} = -5\,\mathrm{V}$, $T = 175°\mathrm{C}$). **a)** $V_{\mathrm{gs,rec}} = 15\,\mathrm{V}$, **b)** $V_{\mathrm{gs,rec}} = 5\,\mathrm{V}$ and **c)** $V_{\mathrm{gs,rec}} = 0\,\mathrm{V}$ (see Fig. 10.18). All maps are shown on a logarithmic color scale, z corresponds to a ΔV_{th} of 20×10^{z} mV/decade^2 for the CET maps.

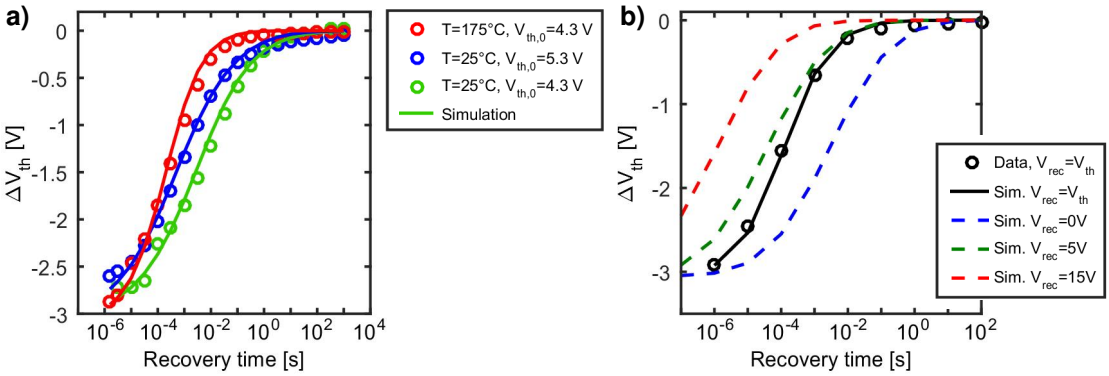

Figure 10.21: SiC NBTI recovery at different recovery voltages with $V_{\mathrm{gs,str}} = -5\,\mathrm{V}$. **a)** Measurement of the threshold voltage at different current set-points (recovery voltage of $V_{\mathrm{gs,rec}} = V_{\mathrm{th}} = 5.3\,\mathrm{V}$ and $V_{\mathrm{gs,rec}} = V_{\mathrm{th}} = 4.3\,\mathrm{V}$). A decreased recovery voltage leads to a deceleration of the recovery by roughly one decade in time. **b)** Comparison of different constant recovery voltages to the actual measurement recovery voltage V_{th}.

Thus, the parameters of the activation energy maps have to be calculated considering the recovery acceleration/deceleration of the measured V_{th} with respect to a constant recovery voltage. For the maps in Fig. 10.19, $V_{\mathrm{rec,ref}} = 5\,\mathrm{V}$ has been chosen, which is close to the threshold voltage before stress at room temperature. In the next step, the calculation is included for each stress/recovery time in the occupancy map (same approach as for the Si MOSFETs demonstrated in Section 7.3). The maps at constant recovery voltage of $V_{\mathrm{gs,rec}} = 5\,\mathrm{V}$ show a broader distribution of the emission time constants than at $V_{\mathrm{gs,rec}} = V_{\mathrm{th}}$ in Fig. 10.17. Directly after NBTI stress, the measured V_{th} is below 5 V, which effectively decelerates the recovery, for $V_{\mathrm{gs,rec}} = \mathrm{const} = 5\,\mathrm{V}$, this results in a broader distribution. Furthermore, the improved model takes into account that the pre-stress threshold voltage at $T = 25°\mathrm{C}$ is $\approx 800\,\mathrm{mV}$ higher than at $T = 175°\mathrm{C}$. Thus, the extracted τ_0 also deviates from the previously extracted value (compare parameters in Table 10.2). As the model improvement only affects the emission activation energies, μ_{c} and σ_{c} are not affected.

To demonstrate the effect of the recovery voltage on the capture and emission time maps, the maps are shown for three constant recovery voltages in Fig. 10.20. Increasing the recovery voltage decreases the emission time constants according to (10.5) based on the measurements shown in Fig. 10.18. The recovery voltage dependence of NBTI is validated with measurements at a different current setpoint such that the extracted V_{th} is reduced by 1 V. As such, the recovery voltage

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itself is also reduced by 1 V. As a result, the reduced recovery voltage in Fig. 10.21 a) leads to a deceleration of the recovery by roughly one decade in time. Measurements and simulation show very good agreement. Furthermore, measurements at different temperatures with the same recovery voltage show that the differences in temperature are further increased which is consistent with the reduced τ_0 (compare parameters in Table 10.2). The influence of the recovery voltage on the time to full recovery is shown in Fig. 10.21 b) in comparison with the actual measurement recovery voltage V_{th}. With the inclusion of the recovery voltage dependence, considering the applied measurement technique, any ΔV_{th} after NBTI stress can be simulated.

10.2.3 Gate Stress Voltage Dependence

In the following, the stress voltage dependence of NBTI is studied and modeled. The ΔV_{th} with stress time for different stress voltages is shown in Fig. 10.22 and the dependence on the recovery time is shown in Fig. 10.23. The following effects are observed:

- At $T = 175°\text{C}$ for stress voltages below $V_{\text{gs,str}} = -10\,\text{V}$, the threshold voltage shift saturates already after stress times below 10 ms. Furthermore, the maximum induced threshold voltage shift strongly depends on the stress voltage as shown in Fig. 10.24 b). For stress voltages above $V_{\text{gs,str}} = -5\,\text{V}$, the saturation is not observed within stress times below 100 s.
- The temperature difference has been discussed in detail for $V_{\text{gs,str}} = -5\,\text{V}$ in Section 10.2.2 e.g. a longer time to saturation is observed for $T = 25°\text{C}$ compared to $T = 175°\text{C}$. For $V_{\text{gs,str}} = -2.5\,\text{V}$, no saturation is observed for $T = 25°\text{C}$ within $t_{\text{str}} = 100\,\text{s}$, whereas at $T = 175°\text{C}$ the saturated ΔV_{th} is reached.
- Due to the faster recovery at $T = 175°\text{C}$, the saturated threshold voltage shift with $t_{\text{d}} = 1\,\mu\text{s}$ is for all stress voltages lower for $T = 175°\text{C}$ than for $T = 25°\text{C}$.
- The time until full recovery is observed is independent of the stress voltage and roughly one order of magnitude larger at $T = 25°\text{C}$ than at $T = 175°\text{C}$.

To include the stress voltage dependence in the activation energy map model, first, the activation energy map parameters are optimized independently for each stress voltage and the following dependencies are observed:

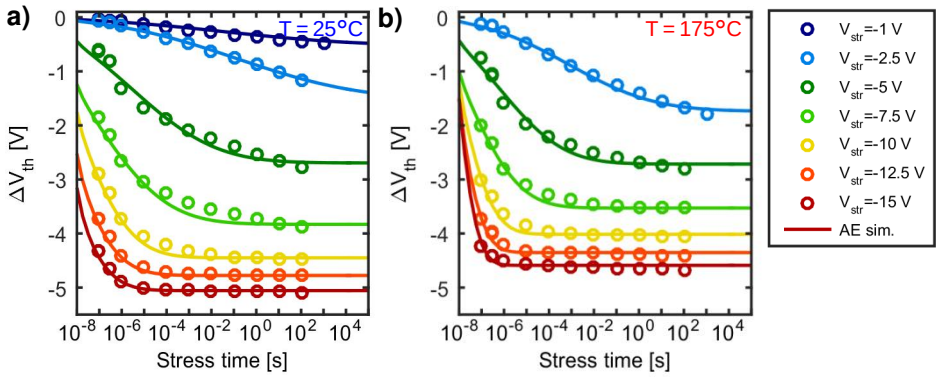

Figure 10.22: Threshold voltage shift with stress time for different stress voltages with $t_{\text{rec}} = 1\,\mu\text{s}$ at **a)** $T = 25°\text{C}$ and **b)** $T = 175°\text{C}$. Circles are measurement data, lines correspond to simulations with the voltage-dependent activation energy map for NBTI (parameters: Table 10.3).

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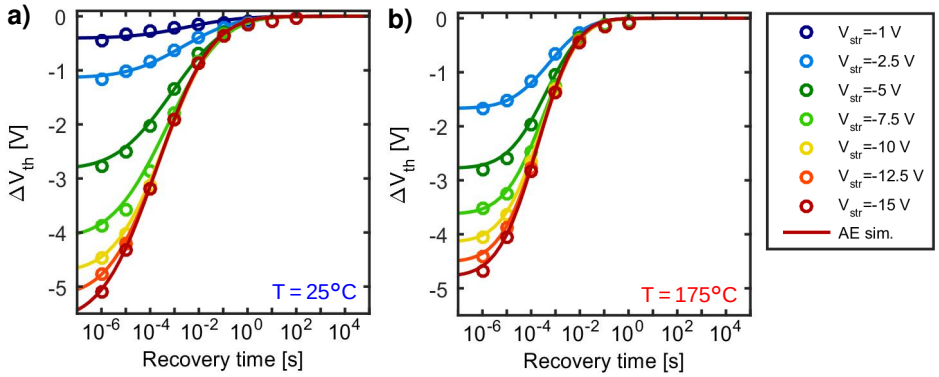

Figure 10.23: Recovery after NBTI stress dependent on the stress voltage with $t_{str} = 100\,s$ at **a)** $T = 25°C$ and **b)** $T = 175°C$. Circles are measurement data, lines correspond to simulations with the voltage-dependent activation energy map for NBTI (parameters: Table 10.3).

- The mean capture energy μ_c decreases with increasing stress voltage $|V_{gs,str}|$. A linear dependence is observed as shown in Fig. 10.25 a):

$$\mu_c = \mu_{c,0} + k_c \cdot V_{gs,str}. \tag{10.6}$$

  However, the standard deviation σ_c is unaffected by the stress voltage.

- Only a slight decrease for increasing stress voltages is observed for the mean value of the emission activation energy $\mu_{\Delta e}$. A linear dependence on the stress voltage as shown in Fig. 10.25 b) has been found:

$$\mu_{\Delta e} = \mu_{\Delta e,0} + k_e \cdot V_{gs,str}. \tag{10.7}$$

  However, the standard deviation σ_e is unaffected by the stress voltage.

- The active number of traps increases with increasing stress voltage $|V_{gs,str}|$ with a saturation towards $V_{gs,str} = -15\,V$. This dependence is implemented via:

$$A = a_0 \cdot (1 - e^{a_1 \cdot V_{gs,str}}). \tag{10.8}$$

- Individually extracting the temperature-independent time constant τ_0 for each stress voltage results in a τ_0 in the range of $10^{-6}\,s$ to $10^{-5}\,s$ (from $V_{gs,str} = -2.5\,V$ to $V_{gs,str} = -15\,V$). Nonetheless, obtaining good model parameters for all temperatures and stress times would require longer measurements for the stress voltages $-5 \leq V_{gs,str} \leq 0\,V$ as they are not yet in saturation for stress times $t_{str} \leq 1\,ks$. In addition, it would require shorter stress times for the stress voltages $-15 \leq V_{gs,str} \leq -5\,V$, as the decrease in V_{th} occurs with time constants $\tau_c \ll 1\mu s$. Thus, with the current measurement data, the temperature dependence of the stress voltage seems to be slight, therefore for the NBTI model, a constant τ_0 has been used for all stress voltages.

Naturally, the recovery voltage dependence during the measurement $V_{gs,rec} = V_{th}$ has to be considered also for the extraction of the stress voltage dependence. The derived dependencies as well as the individual fit parameters are shown in Fig. 10.25 and Fig. 10.24. The effect of the stress voltage on the capture and emission time maps is shown exemplarily in Fig. 10.26 a)-c) and the obtained parameters are given in Table 10.3.

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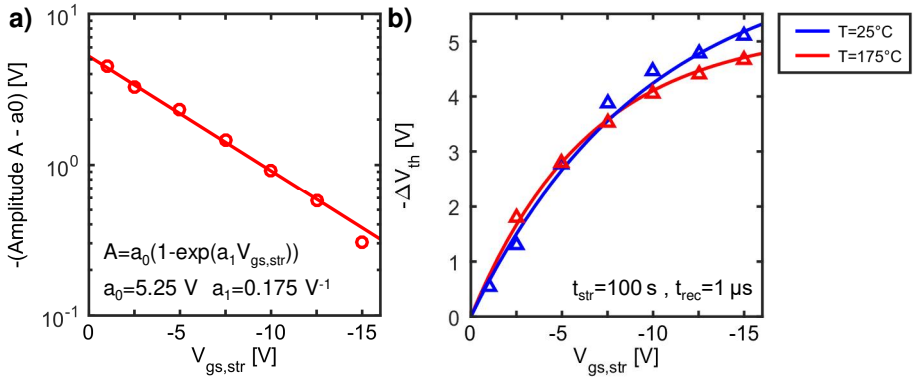

Figure 10.24: **a)** Voltage dependence of the defect density (amplitude in (4.13)) for SiC NBTI. Circles are obtained from individual fits, whereas the line corresponds to the modeled voltage dependence of SiC NBTI following (10.8). All voltage-dependent NBTI parameters are given in Table 10.3. **b)** Dependence of ΔV_{th} on the stress voltage for $t_{\text{str}} = 100\,\text{s}$ and $t_{\text{rec}} = 1\,\mu\text{s}$ for $T = 25°\text{C}$ and $T = 175°\text{C}$.

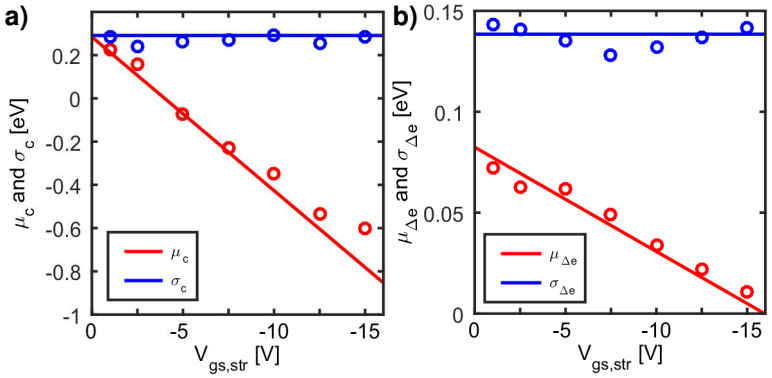

Figure 10.25: Voltage dependence of the model parameters for SiC NBTI **a)** μ_{c} and σ_{c} **b)** $\mu_{\Delta\text{e}}$ and σ_{e}. Circles are obtained from individual fits with the same τ_0, whereas the lines correspond to the modeled voltage dependence of SiC NBTI following (10.6) and (10.7). All voltage-dependent NBTI parameters are given in Table 10.3.

Table 10.3: Activation energy map parameters including the stress voltage dependence for NBTI obtained from MSM measurements shown in Fig. 10.25 and Fig. 10.24 with $V_{\text{gs,rec}} = \text{const} = 5\,\text{V}$.

	τ_0 [µs]	$\mu_{\text{c},0}$ [eV]	σ_{c} [eV]	$\mu_{\Delta\text{e},0}$ [eV]	$\sigma_{\Delta\text{e}}$ [eV]	k_{c} [eV/V]	k_{e} [eV/V]	$a_0[V]$	a_1 [V^{-1}]	r
R	2	0.28	0.29	0.08	0.14	0.07	0.005	5.25	0.17	0

10.3 Threshold Voltage Hysteresis and Application-Relevant AC Measurements

As mentioned in the beginning of Section 10.2, state-of-the-art power SiC MOSFETs show a drain current hysteresis between $I_{\text{ds}}V_{\text{gs}}$ up- and down-sweeps (from accumulation to inversion and vice versa) [59–61]. This hysteresis is a direct result of the reduction in V_{th} due to NBTI as discussed in Section 10.2. First, measurements of the $I_{\text{ds}}V_{\text{gs}}$-sweeps for different starting voltages as well as ramp rates are presented to analyze the sub-threshold voltage hysteresis as described in Section 2.1.3. Second, with the derived model for SiC NBTI including the recovery voltage dependence, the hysteresis is calculated in dependence of the starting voltage as well as the recovery during an $I_{\text{ds}}V_{\text{gs}}$ sweep.

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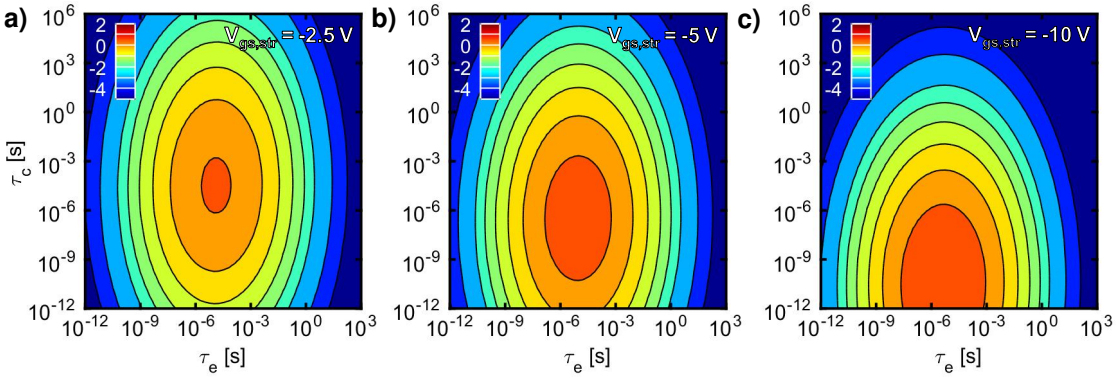

Figure 10.26: Stress voltage dependence of the CET maps shown for $T = 175°C$ and $V_{gs,rec} = 5\,V$ for **a)** $V_{gs,str} = -2.5\,V$, **b)** $V_{gs,str} = -5\,V$, and **c)** $V_{gs,str} = -10\,V$. All maps are shown on a logarithmic color scale, z corresponds to a ΔV_{th} of 20×10^z mV/decade[2] for the CET maps. The corresponding model parameters are given in Table 10.3.

10.3.1 Threshold Voltage Hysteresis

In the following, the threshold voltage hysteresis between $I_{ds}V_{gs}$ up- and down-sweeps and its effects and dependencies is discussed. In Fig. 10.27, the hysteresis is shown for different up-sweep starting voltages:

- The hysteresis is mainly visible in the sub-threshold region due to fast recovery with increasing gate voltage. It appears due to NBTI stress during the up-ramp shifting the V_{th} towards smaller values (negative ΔV_{th}). In Fig. 10.27 a), the hysteresis completely disappears at and above threshold (which is in this case around 4 V), due to the full recovery of the hysteresis when applying positive gate voltages.
- A strong correlation between $\Delta V_{th,hyst}$ and the up-sweep starting voltage of the $I_{ds}V_{gs}$-sweep, which corresponds to the NBTI stress voltage $V_{gs,str}$, is observed and shown in 10.27 b).
- As the hysteresis is induced by NBTI, faster recovery of the hysteresis is expected with increasing temperature compared to the measurements at $T = 25°C$ shown in Fig. 10.27.
- The used sweep rate in Fig. 10.27 of $r_{sweep} = 0.1\,V/s$ is quite slow. As seen in Fig. 10.29 b) with $V_{start} = -15\,V$, the recovery of the hysteresis during the up-sweep is slowed down for faster sweep rates due to shorter recovery times. However, the measurement noise (for the blue curve in Fig. 10.29 b)) is higher for the faster sweep, due to shorter integration time. To extract the hysteresis above the noise level instead of $I_{d,setpoint} = 10^{-11}\,A$, a higher readout current of $I_{d,setpoint} = 10^{-9}\,A$ is needed.

The voltage-dependent activation energy model for negative stress derived in Section 10.2.3 includes the temperature, stress and recovery voltage dependence of NBTI. As seen e.g. in Fig. 10.15 a), already applying stress of $V_{gs,str} = -5\,V$ with $t_{str} = 100\,ms$ to the gate induces a threshold voltage shift of $\Delta V_{th} = -2.3\,V$ at a measurement delay of $t_d = 1\mu s$.

- An up-sweep with a negative starting voltage thus reduces the threshold voltage in the same manner as a short NBTI stress with $V_{gs,str} = V_{start}$.
- A sweep of the gate voltage towards positive voltages causes a constant recovery of the threshold voltage shift during the up-sweep. Therefore, the hysteresis is not observed as a parallel shift in the $I_{ds}V_{gs}$-curves, but the ΔV_{th} observed in the sub-threshold is constantly recovering and not visible e.g. above the threshold voltage.

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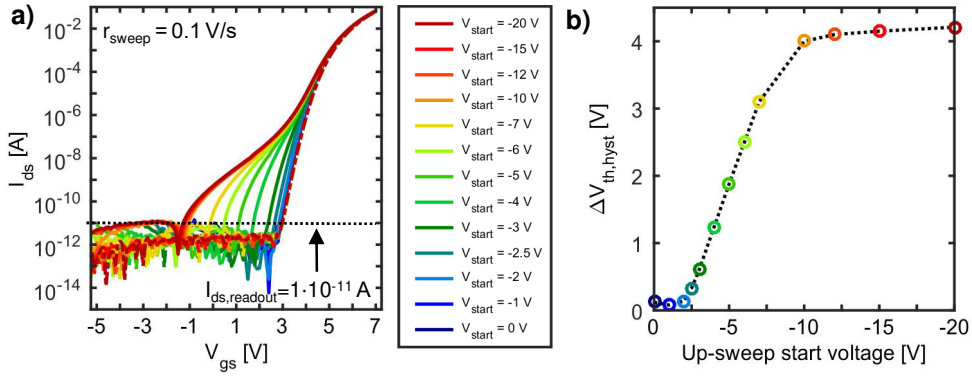

Figure 10.27: $I_{ds}V_{gs}$ up- and down-sweeps for different starting voltages with a sweep rate of $r_{sweep} = 0.1$ V/s (colors correspond to different starting voltages as shown in **a)** Full sweeps (solid lines up-sweep, dashed lines down sweep). All sweeps have been performed on the same sample. **b)** Extracted sub-threshold voltage hysteresis at $I_{d,setpoint} = 10^{-11}$ A dependent on the up-sweep starting voltage for $r_{sweep} = 0.1$ V/s.

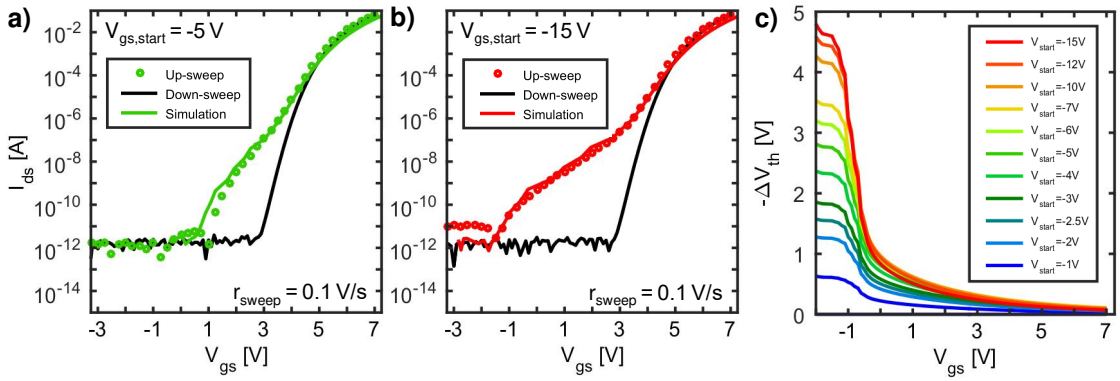

Figure 10.28: Simulation and measurement of the SiC threshold voltage hysteresis with $r_{sweep} = 0.1$ V/s, $T = 25°C$. **a)** $V_{start} = -5$ V, and **b)** $V_{start} = -15$ V. The simulated up-sweep (black dotted lines) are calculated using the down-sweep measurement and the simulated threshold voltage shift shown in c). **c)** Recovery of ΔV_{th} during an V_{gs} up-sweep for different V_{start}.

- As seen in Fig. 10.23 b), the recovery strongly depends on the recovery voltage and is about 10 times slower for $V_{gs,rec} = 0$ V than $V_{gs,rec} = 5$ V. This recovery voltage dependence is of utmost importance to correctly simulate the evolution of ΔV_{th} during a gate voltage up-sweep.

Simulation results for ΔV_{th} dependent on the recovery voltage for a sweep rate of $r_{sweep} = 0.1$ V/s are shown in Fig. 10.28 c) for different up-sweep start voltages. If the gate is still negative, the threshold voltage shift is the non-recovered ΔV_{th} due to NBTI at the starting voltage with the stress time being the sweep time. Recovery starts for $V_{gs} \approx -1$ V. Further increase of V_{gs} leads to accelerated recovery of V_{th} and at about $V_{gs} = 3$ V, most of the ΔV_{th} has already recovered. The reduction in V_{th} is now used to simulate the $I_{ds}V_{gs}$ up-sweep as shown in Fig. 10.28 a) and b) for up-sweep start voltages of $V_{start} - 5$ V and $V_{start} - 15$ V. For this purpose, the measured $I_{ds}V_{gs}$ down-sweep (unaffected by NBTI) is shifted by $\Delta V_{th}(V_{gs})$ to calculate the up-sweep $I_{ds}V_{gs}$-curve including the reduction of ΔV_{th} and its evolution with increasing up-sweep voltage. E.g. as seen in Fig. 10.28 b) for $V_{start} = -15$ V, the drain current of the up-sweep for $V_{gs} = -1$ V corresponds to the drain current of the down-sweep at $V_{gs} = -1 + \Delta V_{th}(-1) = 3.5$ V. The evolution of the $I_{ds}V_{gs}$ up-sweep is, in the same manner, recalculated for each measurement point in the $I_{ds}V_{gs}$ curve. Measurements and simulations of $I_{ds}V_{gs}$ up-sweeps dependent on the up-sweep start voltage as well as dependent on the sweep rate are shown in Fig. 10.29. If the sweep is

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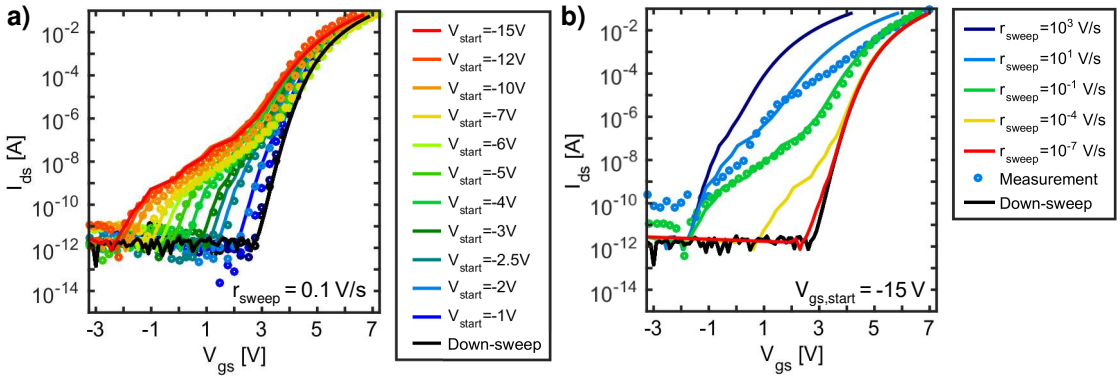

Figure 10.29: Simulation and measurement of the SiC $I_{ds}V_{gs}$-sweep hysteresis. Measurement (circles), simulation (lines) calculated using the down-sweep measurement and the simulated threshold voltage shift as shown in Fig. 10.28 c). **a)** Dependence on the start voltage with $r_{sweep} = 0.1$ V/s and $T = 25°C$. **b)** Dependence on the sweep rate for $V_{start} = -15$ V at $T = 25°C$. The sweep rate of the measured blue curve is estimated to be $\approx r_{sweep} = 10$ V/s as the measurement integration time is non-constant dependent on the measurement current, whereas the slower sweep rate of $r_{sweep} = 0.1$ V/s is not affected by the integration time and is thus constant for all V_{gs}.

too slow, no hysteresis is observed ($r_{sweep} \ll 10^{-6}$ V/s). For very fast sweeps ($r_{sweep} \gg 10^{4}$ V/s), barely any recovery occurs during the up-sweep and thus results in a nearly parallel shift of the $I_{ds}V_{gs}$ curve by ΔV_{th}.

Comparison of the measurements and simulation in Fig. 10.29 show very good agreement for all starting voltages and demonstrate that the hysteresis is induced by NBTI only. The evolution of the hysteresis can be fully explained by the dependence on the sweep rate (recovery time) and the recovery voltage.

10.3.2 Effect of Application-Relevant Bipolar AC Gate Stress

NBTI on SiC nMOSFETs and the correlated hysteresis discussed in this work show a striking difference between silicon and SiC-based MOSFETs. Nonetheless, these differences are an intrinsic feature of SiC MOSFETs and have been reported for all commercial manufacturers as well as for different crystal faces, lateral and trench MOSFETs [38, 59]. Applying typical $I_{ds}V_{gs}$ sweep parameters, the hysteresis is only visible in the sub-threshold regime as seen in Fig. 10.27 and shows a strong recovery voltage dependence (see Fig. 10.21). Previously published work on NBTI and PBTI of SiC MOSFETs only refers to static measurements. However, studying the impact of NBTI and PBTI on the device performance when introducing an application-like bipolar AC gate signal is of utmost importance.

To measure the threshold voltage shift during the bipolar AC stress, a new measurement technique has been developed as described in detail in Section 9.3.1. The ΔV_{th} is measured within the AC stress with a measurement delay of $t_d = 1\mu s$ with varied high level V_h and low level V_l with $V_h = 5$ V to $V_h = 25$ V and $V_l = -10$ V to $V_l = 0$ V. A frequency of $f = 50$ kHz is used, because this is a common frequency for applications of SiC MOSFETs for high-power applications, such as solar inverters and off-board electric vehicle chargers. The AC stress is interrupted at different positions in time within the AC signal. For each interruption, a full recovery curve is recorded. The first measurement points of a V_{th} recovery trace with a delay of $t_d = 1\,\mu s$ at $V_{gs,rec} = V_{th}$ are shown with respect to their timing position during the AC signal. As such, the behavior of V_{th} is measured in real-time during the AC stress only affected by an unavoidable measurement delay. The shift of the threshold voltage within two periods ($t_p = 20\,\mu s$) is shown in Fig. 10.30 for two different V_h at $T = 25°C$ and $T = 175°C$. Short-term

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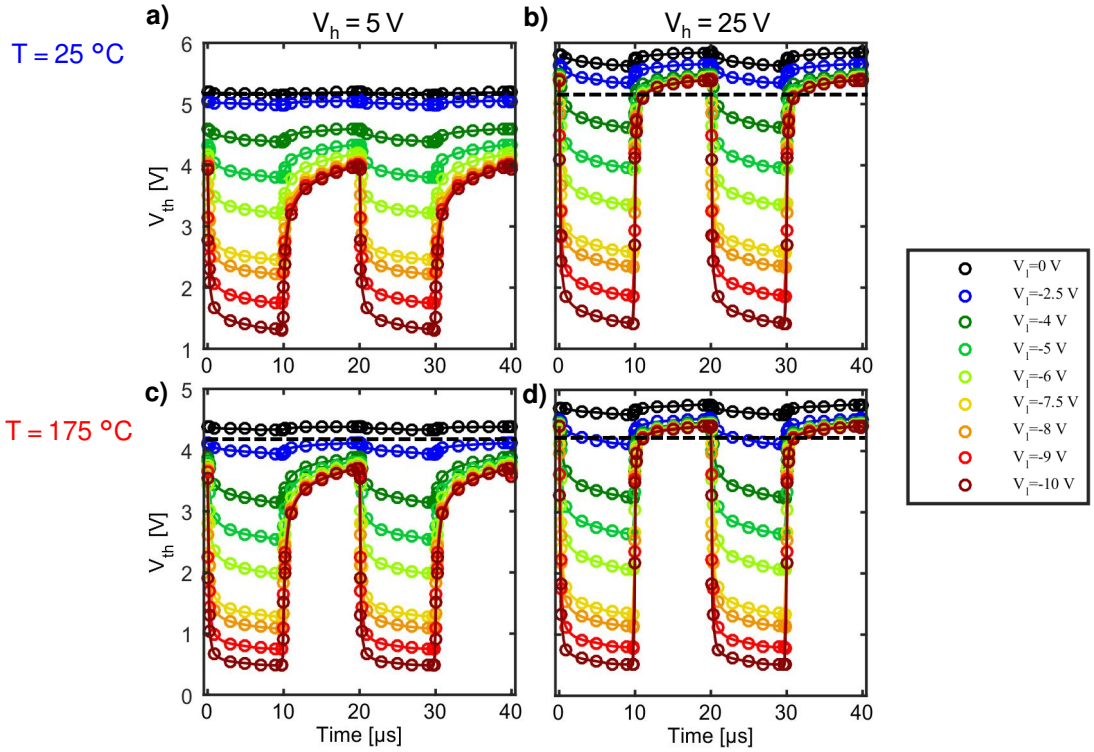

Figure 10.30: Threshold voltage shift at a bipolar AC signal with a frequency of 50 kHz. The measured V_{th} dependent on the AC signal with a varied low level V_l is shown for **a)** $T = 25°C$ with high level $V_h = 5\,V$, and **b)** $T = 25°C$ with $V_h = 25\,V$. **c)** $T = 175°C$ with $V_h = 5\,V$, and **d)** $T = 175°C$ with $V_h = 25\,V$. The initial V_{th} is marked in each sub-figure with a dashed line. Lines between the points serve as a guide to the eye.

variation of the threshold voltage of up to 4 V is observed for $V_l = -10\,V$ and $V_h = 25\,V$ (see Fig. 10.30 b).

Overlapping NBTI and PBTI stress and the corresponding recovery cause the variations in the shift in V_{th} in Fig. 10.30. The following effects are observed:

- The main effect is the fast decrease in V_{th} caused by NBTI during negative gate stress as described in Section 10.2.3 and shown in Fig. 10.25 with $\Delta V_{th} = -4\,V$ for $V_l = -10\,V$ and $T = 175°C$: This decrease is caused by the NBTI stress of $t_{str} = 10\,\mu s$. A direct explanation of the dependence on V_l gives the stress voltage dependence of NBTI (see Fig. 10.22 and Fig. 10.24). For further discussion, the magnitude dependent on V_l and V_h is shown in Fig. 10.31. It is observed that the capture times of SiC for hole capture are a lot faster than for electron capture, therefore ΔV_{th} saturates during V_l and is accelerated by decreasing V_l (see Section 10.2.3 and Fig. 10.26). The minimum V_{th} value shows barely any dependence on the high level V_h as recovery from positive stress is accelerated by the negative voltages (see Fig. 10.12). For $t_{str} = 10\,\mu s$, emission time constants for negative voltages are below $t_{str} = 1\,\mu s$, thus any influence of V_h during the V_l phase would be only visible in the sub-microseconds regime and is superimposed by the fast decrease in V_{th} due to V_l.

- A secondary effect is the increase in V_{th} during positive gate voltages: DC PBTI with $t_{str} = 10\,\mu s$ leads to $\Delta V_{th} = +600\,mV$ for $V_h = 25\,V$ and the dependence on V_h can be directly explained by the stress voltage dependence of PBTI (see Fig. 10.7 and Fig. 10.8). For $V_l = 0\,V$, ΔV_{th} is only caused by PBTI and ΔV_{th} is positive. Whereas for $V_h = 5\,V$, $-\Delta V_{th}$ after the negative stress does not fully recover within the V_h-phase and as such, V_{th}

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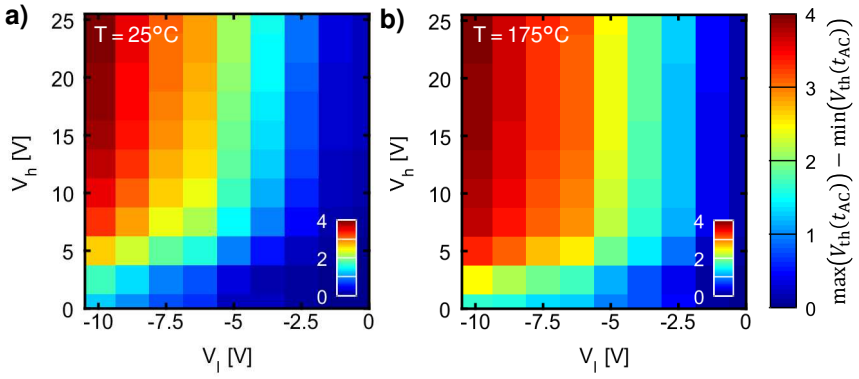

Figure 10.31: Maximum difference of the threshold voltage during application-relevant AC stress $\Delta = \max(V_{\text{th}}(t_{\text{AC}})) - \min(V_{\text{th}}(t_{\text{AC}}))$ dependent on V_{h} and V_{l} extracted from the measurements shown in Fig. 10.30: **a)** $T = 25°\text{C}$, and **b)** $T = 175°\text{C}$. With increasing V_{l}, ΔV_{th} mainly increases and for $V_{\text{h}} \geq 10\,\text{V}$ barely shows any dependence on V_{h}. On the one hand, the $+\Delta V_{\text{th}}$ during PBTI is higher for $T = 25°\text{C}$. On the other hand, $-\Delta V_{\text{th}}$ is higher for $T = 175°\text{C}$. Combining $+\Delta V_{\text{th}}$ and $-\Delta V_{\text{th}}$ during the AC stress results in a higher shift of V_{th} at high temperatures.

remains below its pre-stress value for $V_{\text{l}} < -4\,\text{V}$. The capture times for electron capture are longer than $t_{\text{p}}/2 = 10\,\mu\text{s}$, thus decreasing the frequency would increase $+\Delta V_{\text{th}}$ during the V_{h} phase. For $f = 50\,\text{kHz}$, V_{th} does not saturate within V_{h}. The maximum difference of the threshold voltage $\Delta V_{\text{th}} = \max(V_{\text{th}}) - \min(V_{\text{th}})$ shown in Fig. 10.31 shows a weaker dependence on the high level V_{h} than on the low level V_{l}. For $V_{\text{h}} \leq 10\,\text{V}$, the ΔV_{th} is influenced by the recovery voltage dependence of NBTI (see Fig. 10.23).

- A third component is the temperature. As the temperature dependence of NBTI is slight, the same qualitative observations are made for $T = 25°\text{C}$ and $T = 175°\text{C}$. Due to the intrinsic temperature dependence of the threshold voltage, the initial V_{th} at $T = 25°\text{C}$ is higher. On the one hand, the $+\Delta V_{\text{th}}$ during PBTI is higher for $T = 25°\text{C}$, which is due to the slower recovery at $T = 25°\text{C}$ compared to $T = 175°\text{C}$ within the measurement delay of 1µs. Nonetheless, without the measurement delay, a higher $+\Delta V_{\text{th}}$ is expected for $T = 175°\text{C}$ (as discussed in Section 10.1). On the other hand, $-\Delta V_{\text{th}}$ is higher for $T = 175°\text{C}$ due to accelerated capture of holes at high temperatures (as discussed in Section 10.2.1). Combining $+\Delta V_{\text{th}}$ and $-\Delta V_{\text{th}}$ during the AC stress results in a higher shift of V_{th} at high temperatures.

Contrary, to Si MOSFETs the short-term threshold voltage shift during AC stress amounts to only a few millivolts, due to the very small portion of traps with short capture and emission time constants.

10.3.3 Manufacturer Comparison of Application-Relevant AC Stress

To compare the application-relevant ΔV_{th} of different manufacturers, the new measurement technique for short-term bipolar AC stress as described in Section 9.3.1 has been applied to devices of four different manufacturers. Two devices are trench devices (T1 and T2) and three devices are devices with a lateral channel design: D1 Gen 2 and D1 Gen 3 from one manufacturer as well as D2 from a different manufacturer. The measurement results are shown in Fig. 10.32 for two temperatures and two different low levels V_{l}. All devices show a significant ΔV_{th} for application conditions, but there are some striking differences:

- The devices of D1 (Gen 2 and Gen 3) show the lowest ΔV_{th} for all stress conditions. The devices show similar behavior for $V_{\text{l}} = -5\,\text{V}$ as well as for $V_{\text{l}} = -10\,\text{V}$, which might be

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due to their thin oxide. It is remarkable that even for $V_l = -5\,V$, $-\Delta V_{th}$ almost immediately saturates during the negative stress phase. Other devices with a lateral channel design (not shown in this comparison) showed a comparable ΔV_{th} under the same bipolar AC stress conditions.

- Both trench devices T1 and T2 show a similar $V_{th}(t)$, especially at typical application conditions (e.g. $V_h = 15\,V$ and $V_l = -5\,V$). The ΔV_{th} is roughly twice that compared to D1 (both generations) and due to the temperature dependence of NBTI higher for $T = 175°C$ than for $T = 25°C$.

- Studies of transfer characteristics of different manufacturers [309] indicate that the main impact of the hysteresis on the $I_{ds}V_{gs}$ curves originates from the crystal plane of the inversion channel with a five to ten times higher number of trapped charges N_t per device area extracted from the $I_{ds}V_{gs}$-characteristics which could explain the lower ΔV_{th} for the lateral devices.

- An exceptional behavior compared to the studied lateral devices is seen in device D2. At $T = 25°C$, $+\Delta V_{th}$ due to PBTI is more than three times higher than for all other manufacturers (see also PBTI manufacturer comparison in Section 10.1.6). At $T = 175°C$, this strong increase is not observed due to the faster recovery within the measurement delay at higher temperatures. Contrary to D1, the device also shows a higher $-\Delta V_{th}$, which amounts to up to 2 V at $V_l = -10\,V$. The overall ΔV_{th} for this device is higher than for the trench devices, whereas the origin of the increased trap density is unknown.

In conclusion, all studied devices of different manufacturers show a short-term threshold voltage variation under typical application conditions. This effect has to be studied, modeled and the relevance of the effect on the *on* resistance has to be evaluated (see Section 10.4 and Section 10.5).

10.4 Modeling Application-Relevant AC Stress

The threshold voltage shift ΔV_{th} under positive and negative gate bias stress contains large fast recovering components as shown in Section 10.1 and Section 10.2. Furthermore, modeling $+\Delta V_{th}$ using PBTI and modeling $-\Delta V_{th}$ using NBTI activation energy maps including the stress and recovery voltage dependence have been demonstrated. In this section, the application of the concept of activation energy maps for the simulation of short- as well as long-term AC stress is demonstrated. To obtain the V_{th} response to a rectangular AC signal, the trap occupancy has to be evaluated. The occupancy for rectangular stress is calculated following (4.26) as described in Section 4.4.1. First, the variations of V_{th} under short-term bipolar AC stress are simulated and the simulation results are compared to the measurements shown in Fig. 10.30. The simulations enable the separate discussion of the parameters influencing the change in V_{th}. Considerations and understanding of short-term effects are important, but for lifetime estimations of course the understanding and simulation of long-term effects is crucial. Therefore, in the second part of this section, the results from long-term AC measurements and the corresponding simulations are presented.

10.4.1 Modeling Short-Term Bipolar AC Stress

It is of particular importance to provide a model to calculate ΔV_{th} for typical application conditions to simulate the MOSFET's behavior within a circuit not only for end-of-life calculations, but also to simulate short-term effects within the switching cycle. For the simulation of the short-term threshold voltage variations, the following has to be considered:

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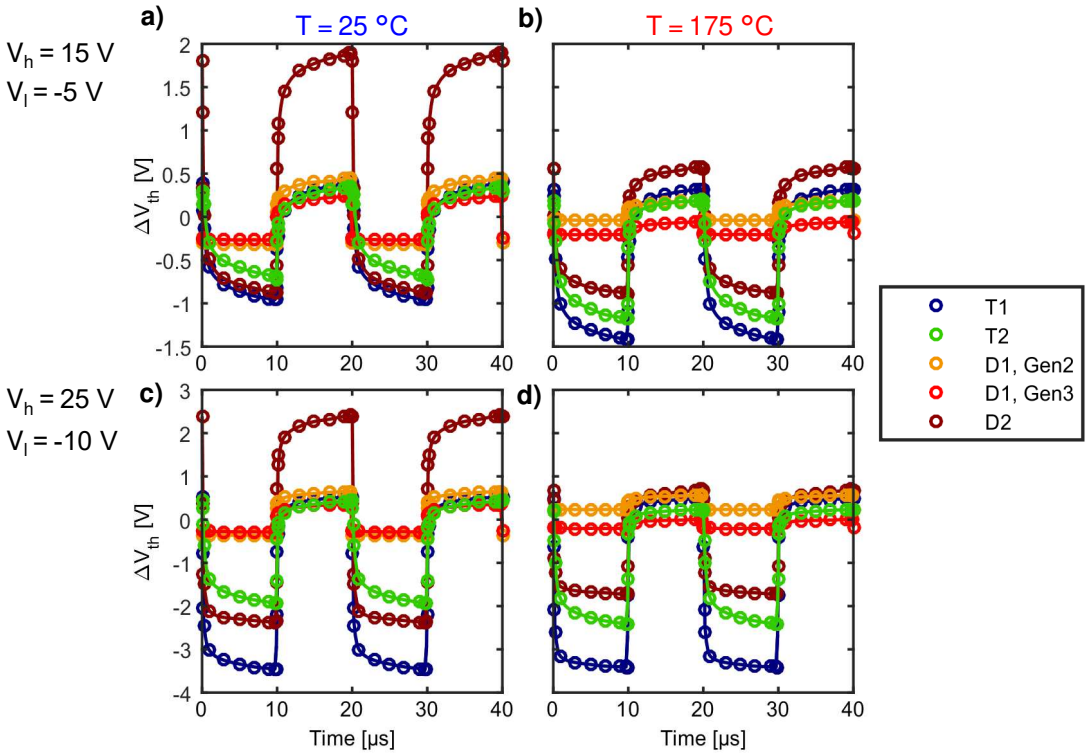

Figure 10.32: Threshold voltage hysteresis at a bipolar AC signal with a frequency of 50 kHz for four different manufacturers with trench design (T) and lateral design (D). The measured V_{th} dependent on the AC signal is shown for various stress conditions. Typical application conditions of $V_{\mathrm{h}} = 15\,\mathrm{V}$ and $V_{\mathrm{l}} = -5\,\mathrm{V}$: **a)** $T = 25°\mathrm{C}$ with **b)** $T = 175°\mathrm{C}$. Increased stress conditions $V_{\mathrm{h}} = 25\,\mathrm{V}$ and $V_{\mathrm{l}} = -10\,\mathrm{V}$: **c)** $T = 25°\mathrm{C}$ and with **d)** $T = 175°\mathrm{C}$. Lines serve as a guide to the eye.

- Due to the bipolar AC stress, the simulation results are obtained by the superposition of the negative and positive ΔV_{th} described by the PBTI and NBTI activation energy maps with the parameters given in Table 10.1 and Table 10.3.
- The negative ΔV_{th} during the V_{l} phase and its recovery during the V_{h} phase can be simulated with the NBTI activation energy map shown in Fig. 10.20. Furthermore, the accelerated recovery of the negative ΔV_{th} with increased recovery voltage has to be considered within the corresponding occupancy maps.
- The positive ΔV_{th} during the V_{h} phase and its recovery during the V_{l} phase can be modeled with the PBTI activation energy map shown in Fig. 10.5. Furthermore, the accelerated recovery of the positive ΔV_{th} with increased negative recovery voltage has to be considered within the corresponding occupancy maps.

For a comparison of the simulation results with the measurements, the experimental conditions are $V_{\mathrm{l}} = -5\,\mathrm{V}$ and $V_{\mathrm{h}} = 25\,\mathrm{V}$ as well as $V_{\mathrm{l}} = -10\,\mathrm{V}$ and $V_{\mathrm{h}} = 25\,\mathrm{V}$ with a frequency of $f = 50\,\mathrm{kHz}$. Measurement and simulated ΔV_{th} at $T = 25°\mathrm{C}$ and $T = 175°\mathrm{C}$ are shown in Fig. 10.33.

For short-term AC stress, $+\Delta V_{\mathrm{th}}$ recovers completely by the application of V_{l} for 10 µs. For long-term stress an additional build-up of the quasi-permanent component is observed and will be discussed in Section 10.4.2. As there is no permanent component of NBTI, no long-term $-\Delta V_{\mathrm{th}}$ is observed. With the simulations, the two effects can be separately discussed:

- The dependence on V_{l}: As discussed in Section 10.2.3, ΔV_{th} increases with decreasing V_{l} due to NBTI and roughly doubles for $V_{\mathrm{l}} = -10\,\mathrm{V}$ compared to $V_{\mathrm{l}} = -5\,\mathrm{V}$ (voltage

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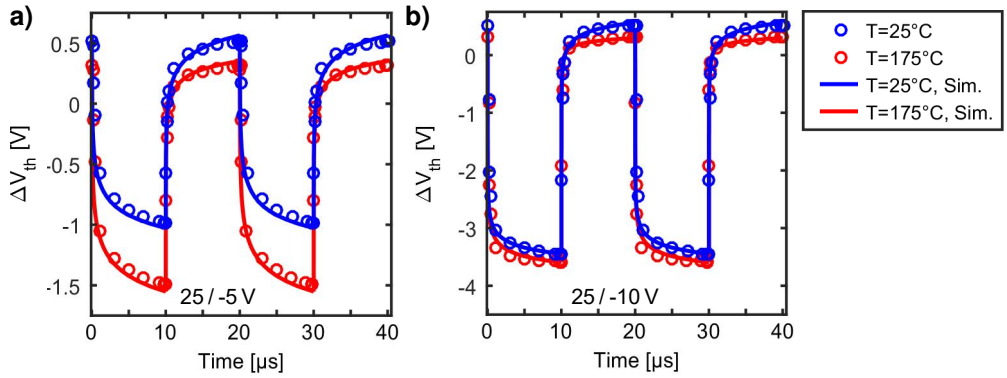

Figure 10.33: Hysteresis at a bipolar AC signal at $T = 25°C$ (blue) and at $T = 175°C$ (red) with $f = 50\,\text{kHz}$ at **a)** $V_\text{h} = 25\,\text{V}$ and $V_\text{l} = -5\,\text{V}$ and at **b)** $V_\text{h} = 25\,\text{V}$ and $V_\text{l} = -10\,\text{V}$. Symbols are experimental data recorded with a measurement delay of 1 µs. The solid lines show the simulations for each temperature and stress voltage obtained by the combination of the NBTI and PBTI CET maps shown in Fig. 10.5 and Fig. 10.20.

dependence of NBTI). For $V_\text{l} = -10\,\text{V}$, $+\Delta V_\text{th}$ after the positive stress phase recovers almost immediately after switching to V_l. The recovery of PBTI is accelerated during the V_l gate signal with decreased recovery voltage of $V_\text{gs,rec} = -5/-10\,\text{V}$ as seen in Fig. 10.12. V_th within the V_l phase is thus dominated by $-\Delta V_\text{th}$. Within the $t_\text{str} = 10\,\mu\text{s}$ of negative bias, $-\Delta V_\text{th}$ saturates. As seen in Fig. 10.22, due to the fast saturation of $-\Delta V_\text{th}$ at $V_\text{l} = -10\,\text{V}$, the temperature dependence is less pronounced.

- The dependence on V_h: The recovery after NBTI stress is accelerated due to $V_\text{h} = 25\,\text{V}$. Furthermore, for $V_\text{l} = -5\,\text{V}$ the contribution of PBTI to the overall ΔV_th is $\approx 30\,\%$ for $T = 25°C$; for $V_\text{l} = -10\,\text{V}$ it amounts to less than 15 %.

- The temperature dependence: The negative ΔV_th after $t_\text{str} = 10\,\mu\text{s}$ stress is higher for $T = 175°C$ than for $T = 25°C$ (especially at $V_\text{l} = -5\,\text{V}$). Whereas, ΔV_th after $t_\text{str} = 10\,\mu\text{s}$ positive stress is higher for the lower temperature. Combining both effects, the absolute ΔV_th is larger for $T = 175°C$ than for $T = 25°C$.

In conclusion, the simulated threshold voltage shift with the superposition of the contribution of both the positive and negative ΔV_th shows excellent agreement with the measurement results. A model of the short-term threshold voltage shift has been provided which covers the temperature, stress and recovery voltage dependencies of both $-\Delta V_\text{th}$ of NBTI and $+\Delta V_\text{th}$ of PBTI. An efficient and accurate approach for the consideration of the short-term threshold voltage shifts in circuit simulators has been demonstrated. It turned out that under long-term bipolar AC gate stress conditions, the measured ΔV_th showed an additional drift phenomenon which cannot be explained by DC stress models. The new phenomenon depends on the applied frequency, temperature, V_l and V_h. It is only present for negative V_l and increases with decreasing V_l (contrary to the observed recovery voltage dependence of DC PBTI). The study of the long-term application of bipolar AC stress is beyond the scope of this thesis. First investigations have been published in [310]. Therefore, in the following section, modeling of only unipolar long-term AC stress is presented.

10.4.2 Modeling Unipolar Long-Term AC Stress

Another important application of the activation energy maps is the calculation of ΔV_th after long-term AC stress. Fig. 10.34 shows the stress time-dependent ΔV_th after AC stress at two different low levels ($V_\text{l} = 5\,\text{V}$ and $V_\text{l} = 0\,\text{V}$) in comparison with DC stress at $V_\text{h} = 25\,\text{V}$. The threshold

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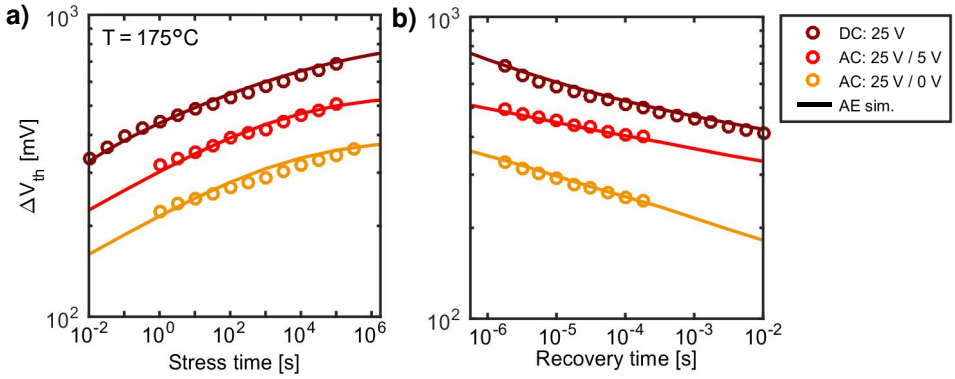

Figure 10.34: Long-term unipolar AC stress with different low levels in comparison with DC measurements and simulations at $V_{gs,str} = V_h = 25\,V$ with different low levels $V_l = 0\,V$ and $V_l = 5\,V$ at $T = 175°C$. **a)** Stress time dependence and **b)** recovery after $t_{str} = 100\,ks$. The AC measurements were performed at a frequency of 50 kHz and a duty cycle of 50% equivalent to alternating $t_{str} = 10\,\mu s$ and $t_{rec} = 10\,\mu s$. The solid lines are simulations obtained from the PBTI activation energy map shown in Fig. 10.9, including the recovery voltage dependence. Simulation and measurements show very good agreement.

voltage after AC stress is measured directly at the end of the high voltage period with a measurement delay of 1µs. As expected, a stress type independent power-law exponent n is observed (DC and AC). In the same manner, as demonstrated for Si-based MOSFETs, the AC ΔV_{th} is calculated with the PBTI activation energy map and the corresponding occupancy map as presented in Section 4.4.1 for rectangular AC stress following (4.26). Furthermore, the acceleration of the relaxation during the AC stress dependent on V_l has to be considered as shown in Fig. 10.12, which leads to a lower degradation with decreasing V_l. Therefore, the degradation after the 25/0 V AC stress is $\approx 40\,\%$ lower than for 25/5 V and $\approx 70\,\%$ lower compared to DC stress. Very good agreement of all simulations with the PBTI activation energy maps and the measurements has been achieved (see Fig. 10.34).

To understand the impact of each component of the PBTI activation energy map, the evolution of the recoverable and quasi-permanent component of ΔV_{th} for the 25/5 V AC stress is shown in Fig. 10.35.

The comparison of the two temperatures for $T = 175°C$ in Fig. 10.35 a) and $T = 25°C$ in Fig. 10.35 b) shows the differences between the contributions of the recoverable and quasi-permanent component to the total ΔV_{th} after AC stress:

- Already after a short-time AC stress ($t_{str} \approx 1\,ms$ at $T = 175°C$ and $t_{str} \approx 10\,s$ at $T = 25°C$), the contribution of the recoverable defects (dotted lines) does not increase anymore.
- There is constant charging and discharging of the recoverable defects (see dashed line in Fig. 10.35 showing ΔV_{th} at the end of the low phase V_l). This is due to the short-term threshold voltage variations, which of course also occur during the long-term AC stress as shown in the inset in Fig. 10.35 for $T = 25°C$. The short-term variation itself does not increase for the long-term AC stress, which has been verified with measurements before and after the AC stress.
- The recoverable component dominates the threshold voltage shift at $T = 25°C$, therefore between interruption at the end of the high V_h and low phase V_l, a difference of $\approx 180\,mV$ is observed.
- The quasi-permanent component increases with stress time and contributes more than half of the ΔV_{th} for $T = 175°C$ after $t_{str} = 100\,ks$, whereas at $T = 25°C$ less than 20% originate from the quasi-permanent component.

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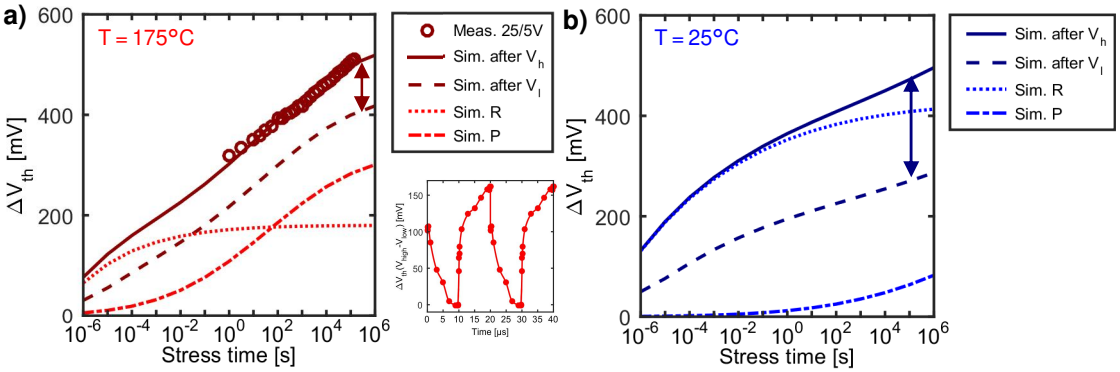

Figure 10.35: Contributions of the recoverable and the quasi-permanent component to ΔV_{th} for unipolar AC stress of 25/5 V AC gate stress at **a)** $T = 175°\text{C}$ and **b)** $T = 25°\text{C}$ with a measurement delay of $t_{\text{d}} = 1\,\mu\text{s}$. The AC measurements were performed at a frequency of 50 kHz and a duty cycle of 50% (circles). The lines correspond to the simulated ΔV_{th} using the activation energy map in Fig. 10.9. Solid lines: Interruption after the end of the high level V_{h}. Dashed lines: Interruption after the end of the low level V_{l}. The dotted lines show only the contribution of the recoverable component, whereas the dashed-dotted lines show only the contribution of the quasi-permanent component. In the inset, the short-term threshold voltage variation within the high and low pulse for $T = 25°\text{C}$ is shown and corresponds to $V_{\text{th}}(t)$ between the solid and dashed line.

- For $T = 175°\text{C}$ most of the threshold voltage shift recovers within the measurement delay of $t_{\text{d}} = 1\mu\text{s}$ and thus the contribution of the recoverable component is reduced.
- Neglecting the recovery due to the ΔV_{th} measurement would result in a higher ΔV_{th} at $T = 175°\text{C}$ due to a roughly three times higher permanent ΔV_{th} compared to $T = 25°\text{C}$.

In conclusion, the concept of analytic activation energy maps can be used to predict the temperature and voltage dependence of DC SiC positive as well as negative gate bias stress with very high accuracy. Moreover, the analytic activation energy maps of both polarities are also a versatile method to simulate different short- as well as long-term unipolar AC gate stress signals.

10.5 Relevance of the Threshold Voltage Shift for the *on* Resistance

The short-term threshold voltage shift of SiC-based MOSFETs presented in this work shows a remarkable difference compared to Si-based MOSFETs. For Si MOSFETs, the difference in V_{th} during a bipolar AC signal amounts to only a few millivolts and is uncritical as it does not influence $R_{\text{ds,on}}$. For SiC MOSFETs, the short-term threshold voltage shifts are mainly due to negative gate bias and may vary up to $\Delta V_{\text{th}} = 4\,\text{V}$. Fortunately, this effect is not permanent and recovers quickly within a fraction of the positive gate bias pulse. Within the measurement delay a portion of the threshold voltage shift recovers. In real applications, in contrast to the measurement, this *dVth* is still active.

To study the impact of ΔV_{th} on $R_{\text{ds,on}}$ during application conditions, recovery-free on-the-fly measurements are performed and shown in Fig. 10.36 for different V_{l} voltages. $R_{\text{ds,on}}$ can only be measured when the transistor is "on", therefore the measured $R_{\text{ds,on}}$ is shown during the high voltage phase V_{h} of the AC operation. At high temperatures, the impact of ΔV_{th} on $R_{\text{ds,on}}$ decreases due to the temperature dependence of $R_{\text{ds,on}}$ and the decreasing transconductance (see also Fig. 8.3 a)). Therefore, $T = 25°\text{C}$ is used for the comparison of $R_{\text{ds,on}}$ with ΔV_{th}. As discussed in Section 10.2.2, $-\Delta V_{\text{th}}$ recovery is accelerated with increasing recovery voltage. Hence, $V_{\text{h}} = 10\,\text{V}$ has been chosen to cause a clearly measurable change in $R_{\text{ds,on}}$ (see Fig. 10.30). Under these measurement conditions, the $R_{\text{ds,on}}$ is actually lower than the data-sheet values (typical characterization at $V_{\text{h}} = 15\,\text{V}$).

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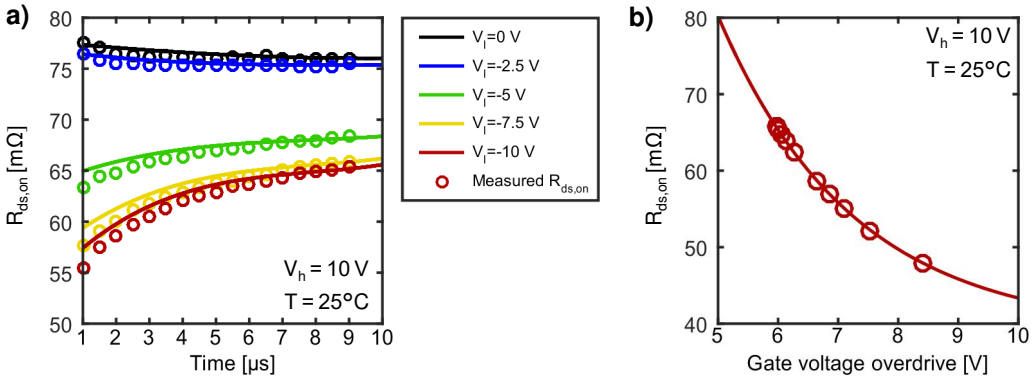

Figure 10.36: a) $R_{ds,on}$ during the V_h period of the AC stress for different values of V_l with $V_h = 10\,V$ and $I_{ds} = 100\,mA$ at $T = 25°C$. Circles: Directly measured $R_{ds,on}$ average for 50 successive periods. Lines: $R_{ds,on}$ calculated from measured static $I_d V_g$ curves and the ΔV_{th} from Fig. 10.30. The change in $R_{ds,on}$ is fully recoverable and reproducible during AC stress. **b)** Dependence of $R_{ds,on}$ on the gate voltage overdrive (from static $I_{ds} V_{gs}$ curves) at $T = 25°C$.

The measured ΔV_{th} at the application conditions (varied V_l, $V_h = 10\,V$ and $T = 25°C$ in Fig. 10.30) is used to calculate the change in $R_{ds,on}$ by considering the change in the gate voltage overdrive (from static $I_{ds} V_{gs}$ curves) when the V_{th} is decreased due to NBTI stress as shown in Fig. 10.36 b). The calculated $R_{ds,on}$ is shown as lines in Fig. 10.36 a). The good agreement between the calculated $R_{ds,on}$ and the measured $R_{ds,on}$ shows, that the dependence of $R_{ds,on}$ during AC stress is only correlated to the observed ΔV_{th} during AC stress. Note that ΔV_{th} is the only reason for $\Delta R_{ds,on}$ and can completely explain the changes in magnitude. Possible changes in the mobility apparently do not play a role. Therefore, it is also clear that the measured $R_{ds,on}$ shows the same dependencies as the hysteresis and hence depends on the low level V_l, the high level V_h, the temperature as well as the pulse length (see also Fig. 9.1 and Fig. 10.30). $R_{ds,on}$ increases back to its initial value with recovering V_{th} (as the hysteresis). An even lower $R_{ds,on}$ in Fig. 10.36 a) is expected for $t \leq 1\mu s$, but has not been shown due to a finite settling time of the measuring amplifier.

To summarize, the short-term threshold voltage shift at application conditions directly influences $R_{ds,on}$ and causes a reduction in $R_{ds,on}$ at the beginning of the turn-on phase. Furthermore, the influence on $R_{ds,on}$ has the following impact on the application of the SiC-based MOSFETs:

- The change in $R_{ds,on}$ is also fully recoverable and reproducible, just like the hysteresis. Since NBTI is the origin of both ΔV_{th} and $R_{ds,on}$, the change in $R_{ds,on}$ cannot be considered an independent degradation mechanism.
- $R_{ds,on}$ is lowered during the negative (V_l) period of the AC stress and increased during the positive (V_h) period. Hence it actively supports turn-on and turn-off of the transistor, reducing switching losses and thus helping to switch the SiC MOSFET faster.
- A turn-on from negative gate voltages leads to an earlier start of the Miller plateau. The name Miller plateau describes the effect that the gate-source voltage of the MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant [229]. The voltage during the Miller phase is lowered due to the negative ΔV_{th} and leads to a higher effective transconductance during the turn-on phase [63].
- When using fast switching slopes (high $\Delta V/\Delta t$), the resulting ΔV_{th} may cause a drain current overshoot due to a higher gate voltage overdrive and a lower channel resistance at the beginning of the high phase of the gate pulse. The overshoot strongly depends on the minority carrier density in the channel and is reduced for high (typically $V_{gs} \leq 15\,V$) turn-on voltages [309].

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- Accumulation pulses with $V_{gs} \leq -10\,V$ might lead to leakage currents around 0 V and thus increase the possibility of parasitic turn-on due to $-\Delta V_{th}$ [309].
- The short-term ΔV_{th} affects the short-circuit behavior. Turning on from $V_{gs} = -10\,V$ instead of $V_{gs} = 0\,V$ into short-circuit conditions results in a higher peak current and thus higher energy dissipation for a single chip. This has to be taken into account for short-circuit tests [63].

The effects on the application discussed above underline the necessity to integrate the model into circuit simulations to correctly assess the threshold voltage shift as well as correlated effects on the application.

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Part IV

Discussion, Conclusions, and Outlook

Chapter 11

On the Physical Meaning of Single Value Activation Energies for BTI in Si and SiC MOSFET devices[1]

In previous chapters, the temperature dependence of BTI is included in the activation energy map. Thereby, the distribution of activation energies takes the variety of available defects into account. Commonly, single value activation energies are used to model BTI [1, 153, 158]. As will be shown in the following, this apparent activation energy is a very rough approximation and is consequently a model parameter without physical justification.

There are two methods to extract the apparent activation energy, either by the threshold voltage shift increase (vertical method) or by the stress time acceleration (horizontal method). The framework of the activation energy maps enables an analytical mathematical approach to calculate the dependence of extracted apparent activation energies on the measurement parameters as the extraction point in the drift curve, the recovery time, and the stress voltage.

In this chapter, based on the model parameters for the silicon-based MOSFETs as presented in Section 6.1, the validity of single activation energy extraction is investigated. The conditions under which apparent activation energy-based modeling provides reasonable results and when activation energy map based modeling is required are determined. Based on the model derived in Section 10.1 with the parameters given in Table 10.1, the differences and challenges in comparison to silicon-based MOSFETs are presented. Furthermore, non-physical negative apparent activation energies for SiC MOSFETs are explained.

11.1 Single Apparent Activation Energy

The threshold voltage shift due to BTI with stress time is often empirically modeled with a power-law as discussed in Section 4.2 and shown in Fig. 11.1 a). The time exponent n in (4.1) is usually assumed to be temperature and stress time-independent. Note that this assumption does not hold for all time scales, as the degradation has been shown to saturate [51]. Usually, the temperature dependence of BTI is determined by MSM measurements with single threshold voltage readouts at different temperatures, e.g. at T_1 and T_2. Thereby, a single activation energy following (4.3) is determined. This apparent activation energy is commonly extracted in two different ways:

- The conventional vertical extraction method determines an apparent activation energy $E_{\mathrm{a,V}}^{\mathrm{app}}$ by the temperature-induced change of the threshold voltage shift ΔV_{th} after a certain stress

[1] This chapter is based on a publication by the author of this thesis [KWJ10] (submitted to Transactions on Electron Devices on 20.08.2020).

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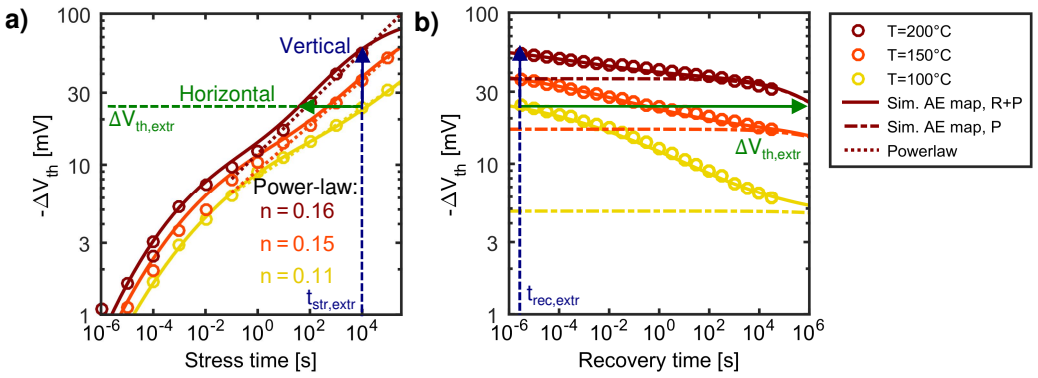

Figure 11.1: Threshold voltage shift ΔV_{th} from a stress voltage of $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$ at three different temperatures with a common power-law fit (data as shown in Fig. 6.1). **a)** Stress time dependence at a constant recovery time of $t_{\mathrm{rec}} = 1\,\mu\mathrm{s}$. **b)** Recovery time dependence after $t_{\mathrm{str}} = 10\,\mathrm{ks}$. The solid lines correspond to simulations with the activation energy map with the parameters given in Table 6.2, the dashed lines correspond to simulations with the quasi-permanent component only.

time as shown in Fig. 11.1 a) (ΔV_{th} after a certain stress time for different temperatures):

$$E_{\mathrm{a,V}}^{\mathrm{app}} = k_{\mathrm{B}} \frac{T_2 - T_1}{T_1 T_2} \log\left(\frac{\Delta V_{\mathrm{th}}(T_2)}{\Delta V_{\mathrm{th}}(T_1)}\right). \tag{11.1}$$

- In contrast, the horizontal extraction method determines an apparent activation energy $E_{\mathrm{a,H}}^{\mathrm{app}}$ from the temperature-induced change in time t_{str} needed to reach the same threshold voltage shift as shown in Fig. 11.1 a) (stress time until the drift target is reached for different temperatures):

$$E_{\mathrm{a,H}}^{\mathrm{app}} = k_{\mathrm{B}} \frac{T_2 - T_1}{T_1 T_2} \log\left(\frac{t_{\mathrm{s},1}}{t_{\mathrm{s},2}}\right). \tag{11.2}$$

The extracted activation energies are typically on the order of $E_{\mathrm{a,V}}^{\mathrm{app}} \approx 0.1\,\mathrm{eV}$ [1, 311] and $E_{\mathrm{a,H}}^{\mathrm{app}} \approx 1\,\mathrm{eV}$. A change in the apparent activation energy causes a variation in the extrapolated end-of-life of a MOSFET (exponential dependence). As an example, a variation of $\Delta E_{\mathrm{a}} = 0.1\,\mathrm{eV}$ in the activation energy leads to a variation by a factor of 1.4 in the lifetime (with $T_1 = 125°\mathrm{C}$ and $T_2 = 175°\mathrm{C}$). In addition, the apparent activation energies strongly depend on bias, stress, and recovery time. The differences are quite dramatic and the physical significance of these values is questioned. This is of fundamental importance insofar as these activation energies have often been used to claim certain physical processes to be responsible for the degradation, e.g. the diffusion of hydrogen [114, 165, 312].

11.2 Analytic Formulation of Single Activation Energy Extraction

The activation energy map as introduced in Section 4.4.1 and shown in Fig. 6.3 represents the contribution from different capture and emission activation energies to the overall threshold voltage shift and allows further approximation by an analytic approach for the calculation of the threshold voltage shift.

The defect occupancy O, after applying a stress or recovery bias for a stress time t_{str} and a recovery time t_{rec}, is given in (4.14). A simplification can be given by approximating

$$O(E_{\mathrm{c}}, E_{\mathrm{e}}, t_{\mathrm{str}}, t_{\mathrm{rec}}) \approx \Theta(E_{\mathrm{c,s}} - E_{\mathrm{c}})\,\Theta(E_{\mathrm{e}} - E_{\mathrm{e,r}}) \tag{11.3}$$

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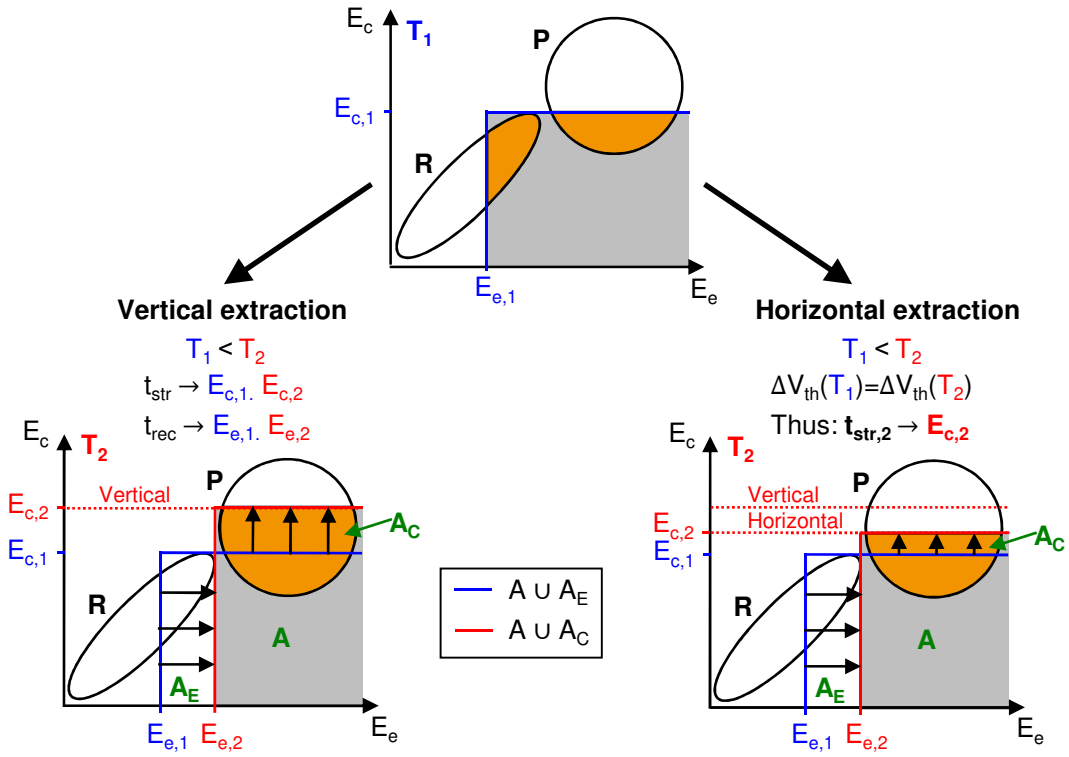

Figure 11.2: A schematic representation of the principle of activation energy extraction with the vertical and horizontal methods. **Top:** Defect occupancy at temperature T_1. T_1, t_{str}, and t_d are the same and define $E_{c,1}$ and $E_{e,1}$ for both methods. At T_1 the threshold voltage shift is obtained by integration of the activation energy map over the blue framed area. All defects are occupied with energies lower than $E_{c,1}$ and higher than $E_{e,1}$ (grey shaded area). The orange area indicates the occupation with a high density of defects (compare activation energy map in Fig. 6.3). The threshold voltage shift at the higher temperature T_2 is obtained by integration over the red-framed area in the bottom left for the vertical extraction and bottom right for the horizontal extraction method. **Bottom left, vertical extraction:** The extraction condition is $t_{str,1} = t_{str,2}$. With the same stress time and recovery time, T_2 defines $E_{c,2}$ and $E_{e,2}$. Defects with capture energies between $E_{c,1}$ and $E_{c,2}$ additionally contribute to the threshold voltage shift at T_2 (area A_C), whereas defects with emission energies in between $E_{e,1}$ and $E_{e,2}$ do not contribute to the overall threshold voltage shift (area A_E). **Bottom right, horizontal extraction:** While the measurement conditions $t_{str,1}$ and t_{rec} are the same as for the vertical method, $t_{str,2}$ is defined by the extraction condition $\Delta V_{th}(T_1) = \Delta V_{th}(T_2)$. As such, the stress time $t_{str,2}$ and thus implicitly $E_{c,2}$ are determined by the ΔV_{th} used for the extraction. Consequently, the contribution in area A_E that is lost by increasing the temperature from T_1 to T_2 has to be equal to the contribution from area A_C that is gained by increasing the temperature. As a result, under the condition of a comparably small contribution from A_E and a high amplitude of the distribution around $E_{c,1}$, the area A_C will be small and $E_{c,2}$ will be close to $E_{c,1}$. According to (11.2), the horizontal activation energy will under these circumstances be close to $E_{c,1}$.

with Θ as the Heaviside step function and $E_{e,r}$ and $E_{c,s}$ the energies corresponding to the recovery and stress times calculated with equation (3.6). The approximation assumes that all defects with capture times smaller than the stress time are occupied and that all defects with emission times smaller than the recovery time are unoccupied. Thus, the calculation of the threshold voltage shift in (6.4) simplifies to:

$$\Delta V_{th}\left(t_{str}, t_{rec}\right) \approx \int_{0}^{E_{c,s}} \int_{E_{e,r}}^{\infty} g\left(E_c, E_e\right) \, \mathrm{d}E_e \mathrm{d}E_c. \tag{11.4}$$

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The recoverable and the quasi-permanent distribution have a different temperature dependence, therefore also the τ_0, which relates energy and time domain, differs (see Table 6.2). Thus, the threshold voltage shift of each component has to be calculated separately for the recoverable and the quasi-permanent component. Since the focus of this section is on the qualitative interpretation of the two extraction schemes, for simplicity, τ_0 is assumed to be equal for both components.

Vertical Extraction

By considering the ratio of the threshold voltage shifts at two different temperatures T_1 and T_2, the vertical apparent activation energy is extracted following (11.1). The principle of the vertical activation energy extraction is illustrated in Fig. 11.2 with the extraction point defined by the stress time and the recovery time, after which the threshold voltage shift is measured. According to the Arrhenius law, the stress and recovery time at the chosen temperature (measurement conditions) correspond to energies in the activation energy map following (3.6). They are named $E_{\mathrm{c},1}$, $E_{\mathrm{e},1}$ and $E_{\mathrm{c},2}$, $E_{\mathrm{e},2}$ for the temperatures T_1 and T_2. These energies span the three areas A, A_{E} and A_{C} in the activation energy map. Defects within the measurement area contribute to the threshold voltage shift and determine the vertical activation energy. The threshold voltage shift at T_1 is obtained by integrating the two distributions R and P over the area $A \cup A_{\mathrm{E}}$. For the higher temperature T_2, the integration is performed over the area $A \cup A_{\mathrm{C}}$. Thus, the vertical activation energy can be written in the following form by introducing $I(S)$, the integral of the activation energy map over the area S:

$$E_{\mathrm{a,V}}^{\mathrm{app}} = k_{\mathrm{B}} \frac{T_1 T_2}{T_2 - T_1} \log\left(\frac{1 + \frac{I(A_{\mathrm{C}})}{I(A)}}{1 + \frac{I(A_{\mathrm{E}})}{I(A)}} \right). \tag{11.5}$$

As can be seen above, the vertical activation energy is controlled by the ratios of the two integrals. As the set of energies $\{E_{\mathrm{c},1}, E_{\mathrm{e},1}, E_{\mathrm{c},2}, E_{\mathrm{e},2}\}$ is determined by the temperature, stress time, and recovery time, the defined integration areas depend on the same parameters. As a result, these parameters determine the apparent vertical activation energy.

Horizontal Extraction

The principle of the horizontal activation energy extraction is illustrated in Fig. 11.2 and the same set of energies $\{E_{\mathrm{c},1}, E_{\mathrm{e},1}, E_{\mathrm{c},2}, E_{\mathrm{e},2}\}$ is used. For the same recovery times at both temperatures and the same stress time at temperature T_1, only the energy $E_{\mathrm{c},2}$ differs from the parameters in the vertical method. $E_{\mathrm{c},2}$ is determined by the condition that the threshold voltage shift is equal at both temperatures. This corresponds to a change of the integration area A_{C} in such a way that $I(A_{\mathrm{C}}) = I(A_{\mathrm{E}})$ is achieved. Therefore, the horizontal activation energy depends on the difference between the parameters $E_{\mathrm{c},2}$ and $E_{\mathrm{c},1}$:

$$E_{\mathrm{a,H}}^{\mathrm{app}} = E_{\mathrm{c},1} - \frac{T_1}{T_2 - T_1} \left(E_{\mathrm{c},2} - E_{\mathrm{c},1} \right). \tag{11.6}$$

If the amplitude of the quasi-permanent component is significantly higher than the amplitude of the recoverable component (compare Table 6.2), the defect contribution of $I(A_{\mathrm{C}})$ is significantly larger than the defect contribution to $I(A_{\mathrm{E}})$, thus the difference $E_{\mathrm{c},2} - E_{\mathrm{c},1}$ is smaller. In this case and for long stress times, the horizontal activation energy $E_{\mathrm{a,H}}^{\mathrm{app}}$ approaches $E_{\mathrm{c},1}$ and is on the order of the activation energies of the quasi-permanent component. Due to its dependence on the set of energy parameters and the condition of equal threshold voltage shift, the horizontal activation energy also depends on temperature, stress time and recovery time.

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A very precise approximation for the vertically extracted activation energy in analytical form can be deduced by using a formula for the threshold voltage shift suggested previously by Grasser in [76, 145]. A rougher and simpler but more explicit approximation is given in [KWJ10] for the horizontally as well as the vertically extracted activation energy. Recovery is neglected and the Gaussian profiles are approximated with logistic distributions of the same standard deviation [145].

11.3 Example I: Si MOSFET

In this section, the dependence of apparent activation energies on the measurement parameters is shown for the silicon-based MOSFETs studied in Chapter 6. As is common practice, the activation energy extraction is performed by fitting an Arrhenius plot at three different temperatures ($T = 100/150/200°C$). The differences between the vertical and the horizontal extraction method are discussed. The measurement data for all stress and recovery times is shown in Fig. 6.1, the parameters of the activation energy map are given in Table 6.2.

Vertical Extraction

An exemplary Arrhenius plot of three different stress times is shown in Fig. 11.3 a) for a constant recovery time $t_{rec} = 1\,\mu s$. For each stress time, a different activation energy is extracted. The stress time dependence of the vertical activation energy is shown in Fig. 11.3 b). The vertical activation energy ranges from below 0.01 up to 0.15 eV for stress times between $t_{str} = 10^{-4}$ to $t_{str} = 10^{5}$ s. For short stress times, only the defects associated with the recoverable component can be charged and contribute to the threshold voltage shift. As a consequence, the vertical activation energy increases between $t_{str} = 10^{-4}$ and $t_{str} = 10^{0}$ s until the first plateau in Fig. 11.3 b) (compare the activation energy map in Fig. 6.4). With increasing stress time, the contribution of the quasi-permanent component to the overall threshold voltage shift increases, consequently this leads to an increase in the vertically extracted activation energy between $t_{str} = 10^{0} - 10^{4}$ s. Finally, towards longer stress times above $t_{str} \geq 10^{4}$ s, the modeled quasi-permanent component flattens and leads to a plateau in the extracted apparent activation energy. Please note that extrapolation for $t_{str} \geq 10^{5}$ s at $T = 200°C$ is not backed up by the measurement data.

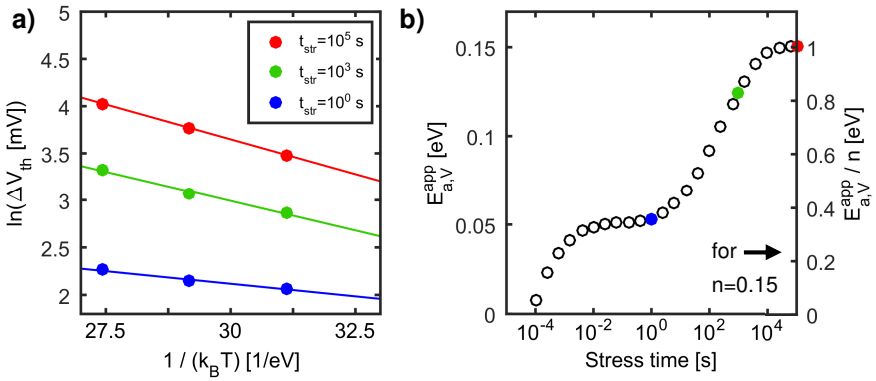

Figure 11.3: Vertical extraction method: **a)** Arrhenius plot for the extraction of the activation energy at different stress times. **b)** Dependence of the apparent activation energy on the stress time for a fixed recovery time of $t_d = 1\,\mu s$ and $V_{gs,str} = -2$ V. Assuming a constant n for all measurements, the vertically extracted activation energy can be translated into the horizontal apparent activation energy via $E^{app}_{a,H} = E^{app}_{a,V}/n$ (right axis with $n = 0.15$ from power-law fits as shown in Fig. 11.1 a).

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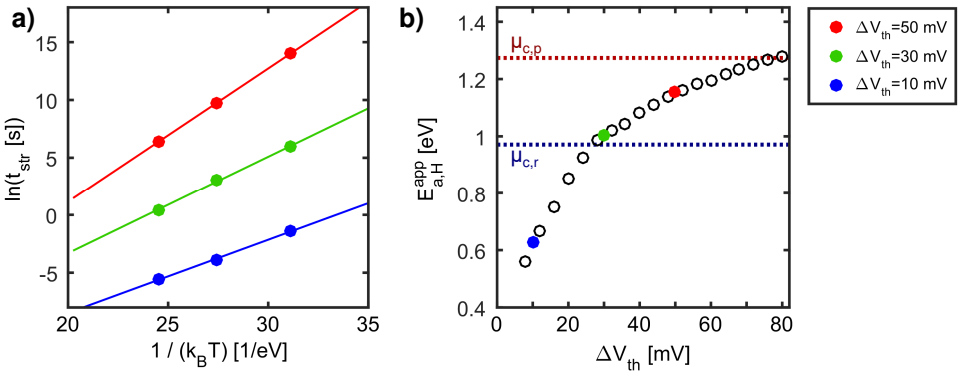

Figure 11.4: Horizontal extraction method: **a)** Arrhenius plot for the extraction of the activation energy at different ΔV_{th}. **b)** Dependence of the apparent activation energy on ΔV_{th} for a fixed recovery time of $t_{\mathrm{d}} = 1\,\mu\mathrm{s}$ and $V_{\mathrm{gs,str}} = -2\,\mathrm{V}$.

Horizontal Extraction

The horizontal method corresponds to measuring the stress time acceleration of the threshold voltage shift contribution of defects around the extraction point. The Arrhenius plot is shown in Fig. 11.4 a) for three different ΔV_{th} used for the extraction of the apparent activation energy. Undoubtedly, the extracted activation energy depends on the extraction point as shown in Fig. 11.4 b). The horizontal activation energies increase from 0.6 – 1.3 eV with increasing extraction point ΔV_{th}. Choosing a higher threshold voltage shift results in higher stress times. Thus, the horizontal method can access the acceleration in time of the quasi-permanent component at long stress times (mean activation energy μ_{c}).

A logarithmic dependence on the stress time of the horizontal activation energy at high threshold voltage shifts helps to reduce the deviation from the mean μ_{c} of the quasi-permanent component. Nonetheless, the already presented calculations show clearly that this only provides a rough estimate and does not replace the use of a whole activation energy map.

Comparison of Horizontal versus Vertical Extraction

The values between horizontal and vertical extraction differ considerably from the energies shown in the activation energy map (mean activation energy μ_{c} of the quasi-permanent component). Furthermore, since the vertical extracted activation energy is not a physically justified quantity. It is not surprising that the extracted values differ considerably from the mean activation energy μ_{c} of the quasi-permanent component. To some extent a physical meaning can be given to the vertical activation energy by dividing the extracted value by the time exponent n from equation (4.2):

$$E_{\mathrm{a,H}}^{\mathrm{app}} = \frac{E_{\mathrm{a,V}}^{\mathrm{app}}}{n} \tag{11.7}$$

Under the above assumptions, modeling the temperature dependence based on horizontal or vertical activation energies is equivalent. With $n = 0.15$, the extracted activation energy is 1 eV. However, n is not constant and not a physical parameter. In Fig. 6.16, the measurement technique has a significant influence on the power-law exponent ($n = 0.12 - 0.19$). As such, a division by n to obtain a physically relevant activation energy introduces further errors.

To discuss the impact of the single activation energy on the calculated lifetime, the following example typical for industrial device qualification is employed: Stress time of 2000 h $= 7.2 \times 10^6$, stress voltage $V_{\mathrm{gs,str}} = 1.2 \times V_{\mathrm{dd}}$, $t_{\mathrm{d}} = 10\,\mathrm{s}$ and the activation energy is extracted horizontally at two different temperatures $T_1 = 120°\mathrm{C}$ and $T_2 = 150°\mathrm{C}$. The extraction point threshold shift is $\approx 62\,\mathrm{mV}$ and the stress time at $T_2 = 150°\mathrm{C}$ corresponds to an energy of $E_{\mathrm{c},2} = 1.35\,\mathrm{eV}$.

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The extracted apparent activation energy is $E_{\mathrm{a,H}}^{\mathrm{app}} = 1.2\,\mathrm{eV}$, which is below the mean activation energy $\mu_{\mathrm{c}} = 1.27\,\mathrm{eV}$ of the quasi-permanent component. As the quasi-permanent component determines the lifetime of the device, subsequent calculations would only slightly underestimate the lifetime of the device. In contrast to that, the vertical activation energy at the same stress time would yield $E_{\mathrm{a,V}}^{\mathrm{app}} = 0.15\,\mathrm{eV}$, which is far away from the actual mean activation energy.

Influence of Recovery

The measured threshold voltage shift is strongly influenced by the measurement delay (recovery time), which affects the extracted activation energy [311]. Fig. 11.5 a) shows the dependence of the extracted horizontal activation energy on the recovery time for three different extraction points. The lowest extraction point of 10 mV exhibits the strongest dependence on the recovery time as the degradation is solely induced by the recoverable component. The dependence on the recovery time is reduced with increasing ΔV_{th} as the relative contribution of the recoverable component to the total threshold voltage shift decreases. The corresponding increase in stress time leads to an increase of the quasi-permanent component, which increasingly dominates the total threshold voltage shift with its high amplitude and determines the end-of-life. As such, the extraction of the activation energy is increasingly dominated by the temperature dependence of the quasi-permanent component which shows negligible recovery within these time scales. As a result, the recovery time dependence loses its influence with decreasing contribution of the recoverable component to the overall threshold voltage shift.

Influence of Stress Voltage

Additionally, the extraction of the activation energy is influenced by the gate stress voltage. Voltage-dependent activation energy map modeling has been demonstrated in Section 6.1.3 and the amplitudes of the recoverable and the quasi-permanent distributions are modeled to be stress voltage-dependent (compare (6.6)). Besides, a slight reduction of the mean values μ_{c} of the capture activation energy with increasing absolute stress voltage has been observed for the recoverable component (compare (6.7); the effect was found to be negligible compared to the bias dependence of the amplitudes).

The dependence of the horizontal activation energy on the stress voltage for three different extraction points is shown in Fig. 11.5 b). For all three cases, the extracted activation energy decreases almost linearly with increasing absolute value of the stress voltage. An increased stress voltage leads to a decreased stress time for the same threshold voltage shift, which leads to an increased contribution of the recoverable component to the overall threshold voltage shift. As the activation energies of the recoverable component are lower than that of the quasi-permanent component, the extracted activation energy decreases with increasing absolute stress voltage due to an increased contribution of the recoverable component.

As such, even under ideal conditions at long stress times, the horizontal activation energy depends on the recovery time for high absolute stress voltages. Thus, increasing the stress voltage is not a good means for the acceleration of measurements. For products, the most relevant quantity is the activation energy of the quasi-permanent component, therefore gate voltages around use conditions are recommended for lifetime predictions.

11.4 Example II: SiC MOSFET

The activation energy map model can also be applied to SiC Trench MOSFETs as shown in Chapter 10. Furthermore, NBTI and PBTI can be described in a unified manner as shown in Section 10.4.1. In Fig. 10.3, the PBTI activation energy map of a SiC Trench nMOSFET is shown. For Si devices, the contribution of the recoverable component to the overall threshold voltage

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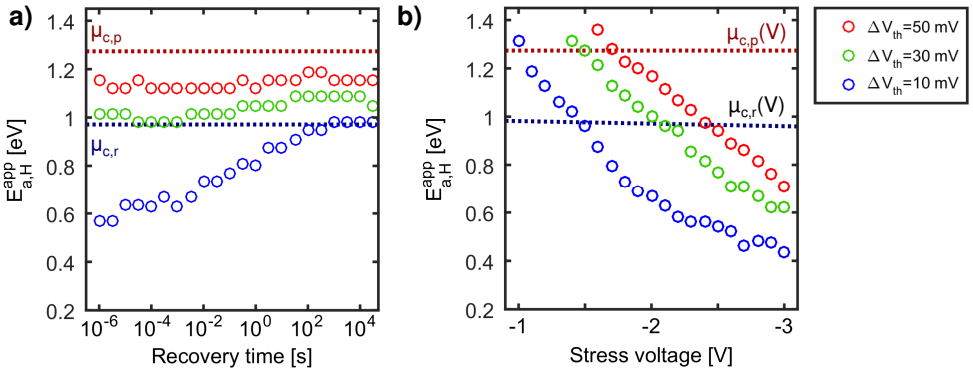

Figure 11.5: Horizontal extraction method: **a)** Dependence of the apparent activation energy on the recovery time at different ΔV_{th} ($V_{\text{gs,str}} = -2\,\text{V}$). A higher extraction point increases the contribution of the recoverable component to the overall threshold voltage shift which decreases the recovery time dependence. **b)** Dependence of the apparent activation energy on the stress voltage at different ΔV_{th} ($t_{\text{d}} = 1\,\mu\text{s}$). An increase in the absolute stress voltage leads to a reduced stress time for the same ΔV_{th}, as such the contribution of the recoverable component is increased leading to lower extracted activation energies.

shift cannot be neglected. As the major differences between SiC MOSFETs and Si devices are the huge concentration of defects with short capture and emission time constants, the recoverable component is in most cases even more important for SiC MOSFETs. Thus, the recovery time is of major importance for the interpretation and modeling of SiC threshold voltage shifts. In the following, apparent activation energies of SiC devices are discussed by applying the horizontal extraction method.

Horizontal Extraction

Measurements at two different temperatures as shown in Fig. 10.1 a) show that a higher temperature leads to a smaller threshold voltage shift implying an negative apparent activation energy. An explanation is provided by the activation energy map for SiC MOSFETs as shown in 10.3. The high and increasing density of defects towards short capture and emission time constants is responsible for this effect. Increasing the temperature leads to a reduction of the emission time constants according to (3.6). As such, some defects with short emission time constants will move out of the measurement window as their emission time constant becomes lower than the recovery time and therefore these defects do not contribute to the overall threshold voltage shift anymore.

For SiC MOSFETs for a fixed recovery time, it is possible that the reduced contribution of the recoverable defects is higher than the increased contribution of the quasi-permanent component (compare discussion and explanation in Section 10.1.1). As such, negative apparent activation energies are observed for SiC MOSFETs as shown in Fig. 11.6 a) for the extraction of the horizontal activation energy. Negative activation energies are non-physical and demonstrate the necessity for activation energy map based modeling to understand the relevant defect contributions.

The horizontal activation energy is negative for the whole range of extraction points ΔV_{th} with $t_{\text{d}} = 1\,\mu\text{s}$, whereas if only the permanent component is considered, the apparent activation energy increases with increasing extraction point. Furthermore, negative activation energies are only observed for short recovery times as a crossing of the recovery traces is observed in Fig. 10.1 b). The dependence of the horizontal activation energy on the recovery time is shown in Fig. 11.6 b). With increasing recovery time, the initially dominant recoverable component recovers and the apparent activation energy changes its sign. For a stress time of $t_{\text{str}} = 100\,\mu\text{s}$, the intersection is above 1 s, for $t_{\text{str}} = 10^5$ s, the intersection is at around 1 ms. Consequently, even the polarity of the extracted activation energy depends on whether the measurement delay is

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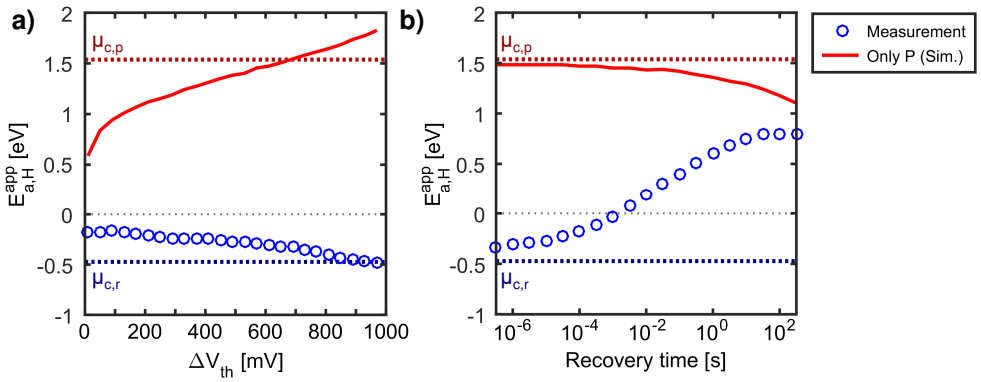

Figure 11.6: Horizontal apparent activation energy for a SiC nMOSFET: **a)** Extracted activation energy from the measurements shown in Fig. 10.2 and the simulated apparent activation energy in the absence of R versus ΔV_{th} ($V_{\mathrm{gs,str}} = 25\,\mathrm{V}$). The dependence is similar to the one observed for Si MOSFETs if only P is considered. **b)** Extracted and the simulated apparent activation energy in absence of R versus the recovery time t_{rec} for $\Delta V_{\mathrm{th}} = 500\,\mathrm{mV}$. The intersection point of the recovery traces in Fig. 10.1 b) determines the point where the sign of the extracted apparent activation energy changes.

below or above the intersection of the recovery traces for the stress time at different temperatures. Application of the preconditioning technique (compare Section 2.3) removes the contribution of the recoverable component to the threshold voltage shift, which enables reproducible measurements and extrapolation to end-of-life using only the quasi-permanent component with positive activation energies comparable to the mean activation energy of the activation energy maps as seen in Fig. 11.6 b).

11.5 Validity of Apparent Activation Energy Extraction

It has been demonstrated that regardless which extraction method is employed, apparent activation energies are not able to describe the temperature dependence of BTI which is actually determined by a wide distribution of capture and emission activation energies. Effective activation energies are especially vulnerable to their point of extraction. Depending on the extraction method, this is either the threshold voltage shift (horizontal method) or the stress time (vertical method). Vertical extraction results in small activation energies. The dependence of the activation energy on the stress time reflects the impact of the two bivariate Gaussian distributions, but the values are completely uncorrelated with physically meaningful values.

For long stress times, the horizontal extraction method leads to values closer to the mean activation energy μ_{c} of the quasi-permanent component. Thus, the horizontal method should be clearly preferred to the vertical method. In addition, the recovery influences the extracted activation energy for both methods, and the influence can be reduced by minimization of the measurement delay and use of long stress times.

Strikingly, SiC MOSFETs show an even stronger influence on the extraction point and recovery time. Most strikingly, in this case, the activation energy can even change its sign depending on the recovery time. Therefore, it is essential to either extract the full activation energy map or apply device preconditioning, leading to discharging of defects with short time constants. To reveal the physical origin of BTI, activation energy map modeling provides further insights and is the preferred method. The extraction of single activation energies for industrial device qualification with end-of-life estimation is only recommended under the condition of long stress times on the time scale of the quasi-permanent component.

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Chapter 12

Conclusions and Outlook

This thesis investigated the bias temperature instability of Si and SiC MOSFETs. BTI has been shown to be the collective response of an ensemble of defects to a gate voltage signal for a given temperature. Each defect can be described using first-order reactions for either charge trapping or defect creation with a broad distribution of time constants. Several differences between Si and SiC MOSFETs have been observed, nonetheless BTI of both technologies (130 nm Si MOSFET and trench SiC MOSFET) can be explained and modeled by a distribution of activation energies reflecting the variety of available defects called activation energy maps. In the following, first, the results of BTI modeling for circuit simulations of Si MOSFETs are summarized and an outlook to further improve the model is given. Second, the results of BTI modeling of SiC MOSFETs under PBTI, NBTI, and application-relevant AC stress are summarized and an outlook on further investigations and model improvements is given.

An accurate and efficient model based on activation energy maps has been developed to simulate the threshold voltage shift after arbitrary analog BTI stress. The model fulfills all five requirements for the purpose of circuit simulations: Good accuracy, consideration of stress history, consideration of different defect types, low simulation effort, and acceptable experimental and implementation effort.

The developed model provides the following benefits compared to other published compact models:

- All parameters are obtained from experiments. Performing TDDS experiments as well as the generation of a defect database is not required. A new measurement technique, the TA-MSM technique, has been introduced, which speeds up the measurement time by at least a factor of 10 compared to the time required for the same experimental window with MSM measurements at a minimum of three constant temperatures. In particular, only one measurement per stress and recovery voltage has to be performed. This decreases the influence of device-to-device variability on the extracted parameters and additionally enables to study variability by acquiring statistics for the same measurement condition.

- The closed form of the analytic activation energy map model includes the stress voltage, recovery voltage, and the temperature dependence of the recoverable and the quasi-permanent component. In addition, the model considers that different defects may be in different states of degradation or recovery at the same time, dependent on the stress history. Any desired lifetime with arbitrary stress voltages and temperatures including any temporal changes can be analytically calculated for arbitrary patterns. Contrary to TCAD simulations, the computation time is independent of the simulated stress time. The only

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restriction is a periodic stress pattern. However, analog circuit engineers always consider a repetitive stress pattern such as day-night cycles.

- Implementation in the INFINEON circuit simulator is feasible and has already been demonstrated. Simulations show excellent agreement for various measurements with different gate stress patterns.

Model demonstration and validation have been performed for a 130 nm Si MOSFET power technology. The 20 model parameters can be determined for various technologies with low experimental effort as the introduced TA-MSM technique could drastically reduce the experimental effort. However, the developed model simulates the mean degradation during BTI stress. Extensions of the model are straightforward to make it more versatile:

- BTI shows device-to-device, wafer-to-wafer, as well as lot-to-lot variability. Monte Carlo sampling of the defects could enable dealing with variability and should be elaborated in the activation energy maps in future studies.
- The interplay between BTI and HCS is still controversial even though in actual circuits a mixture of BTI and HCS occurs. Once the physical mechanisms are understood, the V_{ds} dependence as well as possible effects on the recovery behavior of BTI should be included in the model.
- The permanent component is modeled as being recovery voltage-dependent. Nonetheless, the exact recovery voltage dependence of the quasi-permanent component remains speculative and further investigations with measurements under long recovery conditions at various temperatures and recovery voltages should be conducted and the resulting recovery dependence should be included in the model.

Furthermore, BTI of SiC MOSFETs under DC PBTI/NBTI as well as under application-relevant AC stress were studied. The concept of analytic activation energy maps has been applied to model the temperature and voltage dependence of positive and negative gate bias stress. Very good agreement between measurement and simulation has been achieved for all stress conditions. Moreover, the model includes the stress and recovery voltage dependencies of both negative threshold voltage shifts of NBTI and positive threshold voltage shifts of PBTI.

A new measurement technique to study short-term AC BTI of SiC MOSFETs has been introduced. The observed short-term and long-term threshold voltage shifts under application conditions could be successfully modeled with the superposition of the analytic activation energy maps of both polarities. In addition, the evolution of the threshold-voltage hysteresis in $I_{ds}V_{gs}$ curves can be fully explained by the developed model. Implementation of the model in a circuit simulator is recommended to correctly assess the threshold voltage shift of SiC MOSFETs and correlated effects on the application.

To examine the impact of the device design, devices of different manufacturers have been studied and all devices show a short-term threshold voltage variation under typical application conditions. However, the magnitude of the observed voltage shift strongly depends on the crystal plane on which the inversion layer forms (lateral vs. trench). The short-term threshold voltage variations at application conditions directly influence $R_{ds,on}$. At turn-on, $R_{ds,on}$ is reduced and the change is fully recoverable and reproducible and fully correlated with ΔV_{th}. Even though the short-term threshold voltage variations do not harm the performance and reliability of the SiC MOSFET, the effect on $R_{ds,on}$ demonstrates the necessity for circuit simulations.

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Although considerable progress in the modeling of BTI of SiC MOSFETs has been accomplished in this thesis, several improvements and questions remain:

- The temperature dependence of PBTI has been studied for two temperatures. Therefore the temperature-independent time constants $\tau_{0,\mathrm{r}}, \tau_{0,\mathrm{p}}$ have not been determined independently ($\tau_{0,\mathrm{r}} = \tau_{0,\mathrm{p}}$). Further measurements at different temperatures are necessary to determine the exact temperature dependence.
- Comparison of the threshold voltage shift measured with the preconditioning method with the simulation of the activation energy map model shows that during preconditioning recovery of the quasi-permanent component is observed, too. Further investigations regarding the recovery voltage dependence with long-term stress and recovery sequences would provide comparability with preconditioned measurements and help to further understand the origin of the quasi-permanent component.
- The atomic origin of the defect states, which are responsible for NBTI as well as PBTI, requires further investigation such as TDDS.
- The effect of long-term bipolar AC stress on the device performance should be studied.

The results presented in this thesis may contribute to a successful transfer of the knowledge gathered on BTI in Si technologies to SiC MOSFETs.

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List of Publications

Scientific Journals

[KWJ1] C. Schlünder, **K. Puschkarsky**, G.A. Rott, W. Gustin, and H. Reisinger. "NBTI: Experimental investigation, physical modelling, circuit aging simulations and verification". In: *Microelectronics Reliability* 82 (2018), pp. 1–10. ISSN: 0026-2714. DOI: 10.1016/j.microrel.2017.12.043.

[KWJ2] **K. Puschkarsky**, H. Reisinger, C. Schlünder, W. Gustin, and T. Grasser. "Voltage-dependent activation energy maps for analytic lifetime modeling of NBTI without time extrapolation". In: *IEEE Transactions on Electron Devices* 65.11 (Nov. 2018), pp. 4764–4771. ISSN: 0018-9383. DOI: 10.1109/TED.2018.2870170.

[KWJ3] **K. Puschkarsky**, H. Reisinger, G. A. Rott, C. Schlünder, W. Gustin, and T. Grasser. "An efficient analog compact NBTI model for stress and recovery based on activation energy maps". In: *IEEE Transactions on Electron Devices* 66.11 (Nov. 2019), pp. 4623–4630. ISSN: 1557-9646. DOI: 10.1109/TED.2019.2941889.

[KWJ4] K.-U. Giering, **K. Puschkarsky**, H. Reisinger, G. Rzepa, G. Rott, R. Vollertsen, T. Grasser, and R. Jancke. "NBTI degradation and recovery in analog circuits: Accurate and efficient circuit-level modeling". In: *IEEE Transactions on Electron Devices* 66.4 (Apr. 2019), pp. 1662–1668. ISSN: 0018-9383. DOI: 10.1109/TED.2019.2901907.

[KWJ5] **K. Puschkarsky**, Hans Reisinger, Thomas Aichinger, Wolfgang Gustin, and Tibor Grasser. "Understanding BTI in SiC MOSFETs and its impact on circuit operation". In: *IEEE Transactions on Device and Materials Reliability* 18.2 (2018), pp. 144–153. ISSN: 1530-4388. DOI: 10.1109/TDMR.2018.2813063.

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[KWJ7] B. Ullmann, **K. Puschkarsky**, M. Waltl, H. Reisinger, and T. Grasser. "Evaluation of advanced MOSFET threshold voltage drift measurement techniques". In: *IEEE Transactions on Device and Materials Reliability* 19.2 (June 2019), pp. 358–362. ISSN: 1530-4388. DOI: 10.1109/TDMR.2019.2909993.

[KWJ8] B. Ullmann, M. Jech, **K. Puschkarsky**, G. A. Rott, M. Waltl, Y. Illarionov, H. Reisinger, and T. Grasser. "Impact of mixed negative bias temperature instability and hot carrier stress on MOSFET characteristics—Part I: Experimental". In: *IEEE Transactions on Electron Devices* 66.1 (Jan. 2019), pp. 232–240. ISSN: 1557-9646. DOI: 10.1109/TED.2018.2873419.

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[KWJ9] M. W. Feil, A. Hürner, **K. Puschkarsky**, T. Aichinger, W. Gustin, H. Reisinger, and T. Grasser. "The impact of interfacial charge trapping on the eeproducibility of measurements of silicon carbide MOSFET device parameters (invited)". In: *Crystals, Special Issue: Bias Temperature Instabilities in Modern Transistors* (2020). DOI: submittedforpublication.

[KWJ10] M. W. Feil, **K. Puschkarsky**, W. Gustin, H. Reisinger, and T. Grasser. "The significance of single value activation energy based BTI modeling of Si and SiC MOSFET devices". In: *IEEE Transactions on Electron Devices* (). DOI: submittedforpublication.

Conference Proceedings

[KWC1] C. Schlünder, **K. Waschneck**, P. Rotter, S. Lachenmann, H. Reisinger, F. Ungar, and G. Georgakos. "From device aging physics to automated circuit reliability sign off". In: *2019 IEEE International Reliability Physics Symposium (IRPS)*. Mar. 2019, pp. 1–12. DOI: 10.1109/IRPS.2019.8720457.

[KWC2] **K. Puschkarsky**, H. Reisinger, C. Schluender, W. Gustin, and T. Grasser. "Fast acquisition of activation energy maps using temperature ramps for lifetime modeling of BTI". In: *2018 48th European Solid-State Device Research Conference (ESSDERC)*. Sept. 2018, pp. 218–221. DOI: 10.1109/ESSDERC.2018.8486855.

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[KWC4] **K. Puschkarsky**, H. Reisinger, T. Aichinger, W. Gustin, and T. Grasser. "Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation". In: *2017 IEEE International Integrated Reliability Workshop (IIRW)*. Oct. 2017, pp. 1–5. DOI: 10.1109/IIRW.2017.8361232.

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[KWC7] C. Schlünder, F. Pröbster, J. Berthold, **K. Puschkarsky**, G. Georgakos, W. Gustin, and H. Reisinger. "Circuit relevant HCS lifetime assessments at single transistors with emulated variable loads". In: *Reliability Physics Symposium (IRPS), 2017 IEEE International*. IEEE. 2017, pp. 2D–2. DOI: 10.1109/IRPS.2017.7936262.

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Curriculum Vitae

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