DISSERTATION

Carrier Mobility and Reliability of 4H-SiC Trench MOSFETs

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November 18, 2020

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Abstract

The wide band gap semiconductor silicon carbide (SiC) is a very promising emerging material for high power electronics. It offers superior material properties compared to conventional silicon (Si) in terms of the band gap, the breakdown field, thermal conductivity and much more. Therefore, SiC devices can be operated at higher temperatures and higher power densities compared to Si-based metal oxide semiconductor field effect transistors (MOSFETs), allowing for more efficient and more compact devices. Nevertheless, the performance of 4H-SiC still stays behind its theoretical potential, especially with respect to the channel mobility in MOSFETs. The inversion channel mobility is far lower than the mobility in bulk SiC due to trapping and scattering effects at the interface. The detailed mechanism reducing the mobility is still not understood and therefore needs close investigation. At the same time, several reliability concerns such as the gate oxide reliability and bias temperature instability exist and cannot be excluded from any studies of process improvements. This thesis focuses on the carrier mobility in 4H-SiC trench MOSFETs and the device reliability. Trench devices are of special interest because they allow for smaller pitches and therefore for higher channel densities, reducing the total on-resistance compared to lateral device structures. In order to further improve the device performance, process optimizations such as different post oxidation anneals (POAs) are commonly investigated.

The first half of this thesis deals with the characterization of differently processed SiC metal oxide semiconductor (MOS) devices at room temperature. First, mobility improvements are attempted to be achieved by changing the (interface) trap density with different POAs. It will be demonstrated that a full device characterization, including the device performance as well as its reliability, needs to be conducted when benchmarking new process variants. Using the example of ammonia (NH_3) annealed trench MOSFETs it will be shown that an improved channel mobility may come with a worsened device performance. It has been found that the NH_3 POA can very well improve the device performance but at the same time leads to the formation of new traps in the oxide which degrade the oxide reliability and increase the leakage current. Thus, a detailed study of trap assisted tunneling and oxide breakdown will be presented and the experimental results will be connected with existing breakdown models from literature. The second mobility improvement approach deals with the formation of different interfaces by different oxidation techniques. It will be shown that plasma grown oxides, deposited oxides and thermal oxides result in mostly equivalent devices and similar interface state densities. Finally, to complement the performance studies, bias temperature instability (BTI) in SiC power MOSFETs compared to Si power MOSFETs has been investigated. BTI seems to be caused by an intrinsic trap band in silicon dioxide (SiO_2) which is present in both technologies. The different absolute drifts observed can be related to the different band structures of SiC and Si as well as a potentially different trap density.

The second half of this thesis deals with the understanding of the degraded channel mobility in 4H-SiC. With the help of cryogenic measurements, mobility degrading trap bands have been identified and their potential origin investigated. With two different measurement techniques interface trap bands were identified which at least partially have an impact on the channel mobility. One trap distribution is related to the p-doping of the device and is most likely somehow related to aluminum (Al).

Kurzfassung

Siliziumkarbid (SiC) ist ein vielversprechendes neues Material in der Leistungselektronik. Es bietet zahlreiche Vorteile gegenüber der konventionellen Silizium (Si) Technologie wie zum Beispiel eine größere Bandlücke, eine höhere Durchbruchsfestigkeit, eine hervorragende thermische Leitfähigkeit und viele weitere positive Eigenschaften. Diese Eigenschaften ermöglichen es, SiC-basierte Bauteile bei höheren Temperaturen und mit höheren Leistungsdichten zu betreiben als dies beispielsweise für Si möglich wäre. Gleichzeitig kann die Bauteilfläche verkleinert und die Effizienz der einzelnen Bauteile erhöht werden. Trotz der vielen positiven Eigenschaften bleibt das neue Material derzeit allerdings noch insbesondere im Bezug auf die Ladungsträgerbeweglichkeiten im Inversionskanal eines MOSFETs hinter den theoretischen Grenzen bzw. Möglichkeiten zurück. Derzeit ist die Ladungsträgerbeweglichkeit im Inversionskanal eines MOSFETs aufgrund von Streuung und dem Einfangen von Ladungsträgern in Defekten an der Grenzfläche zum Oxid deutlich geringer als die Ladungsträgerbeweglichkeit tief im Material weit von der Grenzfläche entfernt. Der genaue Degradationsmechanismus ist leider noch immer nicht vollständig verstanden und bedarf weiterer Untersuchung. Gleichzeitig werden Einschränkungen in der Zuverlässigkeit der Bauteile beobachtet, die ebenfalls noch nicht vollständig verstanden sind und bei der Untersuchung der Leistungsfähigkeit der Halbleiterbauelemente nicht vernachlässigt werden dürfen. Hierzu zählen beispielsweise die spannungs- bzw. temperaturbedingte Instabilität der Schwellspannung (engl. *bias temperature instability (BTI)*) oder die Zuverlässigkeit des Oxids. Der Schwerpunkt dieser Doktorarbeit liegt auf der Ladungsträgerbeweglichkeit im Inversionskanal von vergrabenen (engl. *trench*) MOSFETs, sowie auf deren Zuverlässigkeit. Wie bereits erwähnt lässt sich beides nicht voneinander trennen. Es werden *trench* Bauteile untersucht, da diese aufgrund der höheren Packungsdichte kleinere Einschaltwiederstände haben und deshalb eine bessere Leistung versprechen. Um die Leistungsfähigkeit der SiC basierten Leistungsbauelemente weiter zu verbessern, werden üblicherweise Prozesse wie zum Beispiel Ausheilschritte nach der Oxidation kontinuierlich im Hinblick auf Verbesserungen analysiert.

Die erste Hälfte dieser Doktorarbeit befasst sich mit der Charakterisierung von Halbleiterbauelementen hergestellt mit neuen Prozessvarianten bei Raumtemperatur. Ein Ansatz zur Verbesserung der Kanalbeweglichkeit besteht in der Reduktion der Defektdichte an der Grenzfläche zum Oxid durch Ausheilprozesse nach der Oxidation in verschiedenen Gasumgebungen. Je nach Prozess kann eine Verbesserung der Kanalbeweglichkeit zu einer Verschlechterung der Zuverlässigkeit des Bauteils führen. Am Beispiel eines Ausheilprozesses in Ammoniak (NH_3) wird eine detaillierte Bauteilcharakterisierung durchgeführt. Es wird gezeigt, dass in diesem Fall eine deutliche Verbesserung der Kanalbeweglichkeit mit einer Verschlechterung der Zuverlässigkeit, insbesondere BTI und Gateleckströme, einhergeht. In diesem Rahmen wird eine detaillierte Analyse von Defekt-basierten Tunnelströmen (trap assisted tunneling (TAT)) und Oxiddurchbruch durchgeführt und mithilfe bereits existierender theoretischer Modelle erklärt.

Ein weiterer Ansatz zur Verbesserung der Kanalbeweglickeiten ist die Verbesserung der Grenzflächenqualität zum Beispiel durch verschiedene Oxidationstechniken. In diesem Fall werden thermische Oxide, abgeschiedene Oxide und in Plasma gewachsene Oxide im Hinblick auf die Defektdichte an der Grenzfläche und die Charakteristiken der entsprechenden Bauteile miteinander verglichen. Es wird gezeigt, dass die verschiedenen Techniken zu vergleichbarem Bauteilverhalten und ähnlichen Defektdichten an der Grenzfläche führen. Zur Komplettierung der Untersuchungen bei Raumtemperatur wird weiterhin ein Vergleich von BTI in Si und SiC basierten Leistungshalbleitern vorgestellt. Dabei wird gezeigt, dass die Verschiebung der Schwellspannung in beiden Technologien höchst wahrscheinlich auf denselben Defekt in Siliziumdioxid (SiO_2) zurückzuführen ist. Unterschiede in den absoluten Verschiebungen sind größtenteils auf die verschiedenen Bandstrukturen, aber je nach Prozessierung auch auf unterschiedliche Defektdichten zurückzuführen.

Die zweite Hälfte der Dissertation befasst sich mit dem Verständnis der niedrigen Kanalbeweglichkeiten in SiC. Mithilfe von Tieftemperaturmessungen wird versucht, die verursachenden Defekte zu identifizieren und deren Ursache zu bestimmen. Mit zwei verschiedenen Messmethoden wurden verschiedene Grenzflächendefekte bestimmt, die zusammen mit weiterhin unbekannten Defekten negative Auswirkungen auf die Kanalbeweglichkeit haben. In einem Fall konnte der Defekt mit der p-Dotierung des Bauteils und damit mit Aluminium (Al) in Verbindung gebracht werden.

Contents

CHAPTER 1

Introduction

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1.1 Silicon Carbide Basics

1.1.1 Material Properties

The wide band gap (WBG) semiconductor SiC is an emerging new material especially in the field of high power electronics. SiC is a IV-IV compound semiconductor with an indirect band structure, allowing for long carrier lifetimes which is especially attractive for bipolar devices [1]. Because of its beneficial material properties such as the WBG (2.36 eV-3.26 eV), the high breakdown field, high saturation velocity, high thermal conductivity and high carrier mobility, it is well suitable for power electronics [1], offering some advantages compared to conventional Si-based technology. Additionally, the well-controllable n- and p-doping and the native oxide SiO_2 make the fabrication of MOS structures possible and allow to transfer part of the large Si know-how to SiC technology.

SiC consists of an equal amount of Si and carbon (C) atoms which are bound covalently with a binding energy of 4.6 eV. The SiC molecules form a tetravalent structure in which the valence electrons are shared in sp^3-hybrid orbitals [1]. In contrast to Si, SiC exists in several different crystal structures, so-called polytypes. Figure 1.1 shows the most important polytypes 3C-, 4H- and 6H-SiC. The names in Ramsdell's notation [2] result from the stacking order repeating sequence of the Si−C unit cell in the crystal. A, B and C represent the Si−C bilayers at distinct positions. Whereas 3C-SiC (β-SiC) consists of the only cubic lattice structure formed by SiC, 4H- and 6H-SiC have hexagonal lattices. The different polytypes offer different electrical, optical, thermal and mechanical properties, as can be found in Table 1.1. In contrast to these material characteristics, the thermal conductivity is independent of the polytype. Nevertheless, it is anisotropic and depends on the doping concentration and the temperature. Because of their ability to form large crystals, 4H-SiC and 6H-SiC are at the moment the most commonly used polytypes for electronic devices. Because of the higher electron mobility, 4H-SiC is especially attractive for n-channel MOSFETs. Especially along the c-axis (a-plane, cf. Figure 1.2), high electron bulk mobilities are expected.

1.1.2 Motivation for Silicon Carbide Power Devices

SiC is an emerging material especially in the field of high-power electronics, competing predominantly with Si insulated-gate bipolar transistors (IGBTs). Even though several

Table 1.1 Properties of the most important SiC polytypes at room temperature. [1, 4, 5]

Property	3C-SiC	4H-SiC	6H-SiC
Stacking sequence	ABC	ABCB	ABCACB
Band gap energy [eV]	2.39	3.26	3.02
Lattice constant c [Å]	n.a.	10.05	15.12
Lattice constant a [Å]	4.36	3.07	3.07
Electron mobility $\perp$ c [$cm^2V^{-1}s^{-1}$]	1000	1020	450
Electron mobility $\parallel$ c [$cm^2V^{-1}s^{-1}$]	1000	1200	100
Hole mobility [$cm^2V^{-1}s^{-1}$]	100	120	100
BFOM (relative to Si)	61	626	63

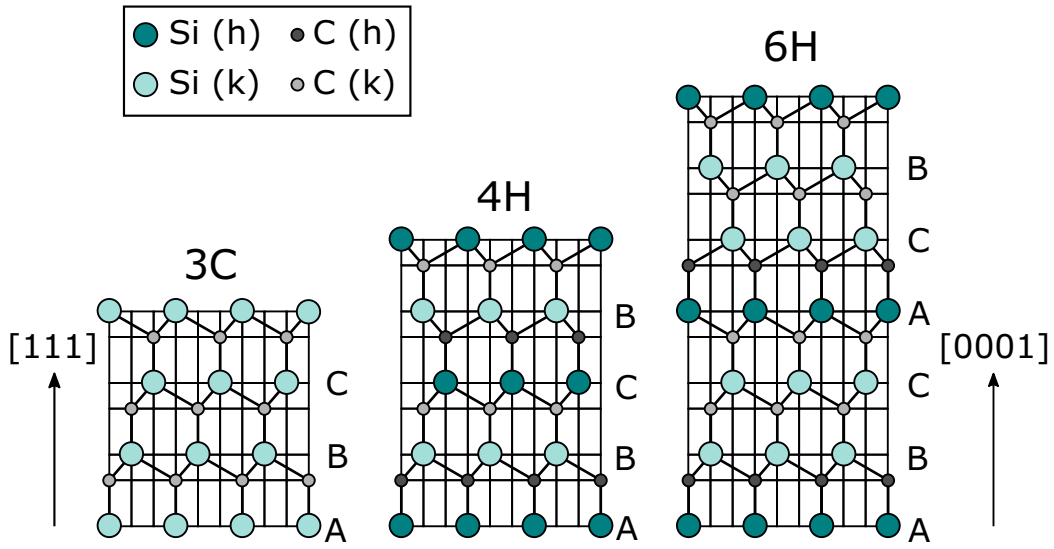
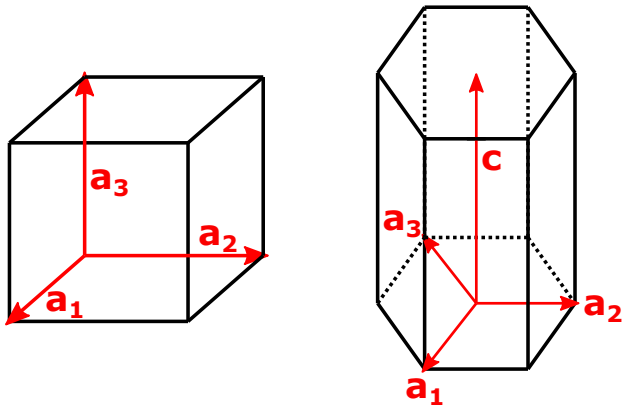


Fig. 1.1 Stacking order and lattice sites (hexagonal (h) or cubic (k)) of popular SiC polytypes (cf. [1, 3]).



(a) Cubic SiC (b) Hexagonal SiC

Fig. 1.2 Basic lattice cells with translation vectors of (a) cubic and (b) hexagonal SiC. Picture modified from [1].

promising WBG materials exist, e.g. gallium nitride (GaN), gallium arsenide (GaAs) and SiC, SiC offers several advantages compared to the other WBG materials and especially Si. An overview over the properties of the most popular WBG materials in comparison to Si can be found in Table 1.2. First of all, many WBG semiconductors offer higher breakdown fields than Si. Due to the WBG, SiC has a lower ionization rate than Si. Since the maximum field at breakdown depends on the inverse logarithm of the ionization rate (cf. [8] for detailed formulas), higher critical fields must result for WBG semiconductors like SiC. This enables the development of devices with high blocking capabilities [1] so that higher maximum fields can be applied for the same material thickness or the material

can be thinned at a constant blocking field. On the other hand, SiC offers a high melting point (mainly sublimation) and high hardness, making material growth and processing more difficult (cf. [1] for details about processing). At the same time, the material is more robust for the use in harsh environments such as high-temperature environments [9–11].

Furthermore, SiC has a high thermal conductivity. Therefore, heat produced by Joule heating during device operation (conduction losses) can be easier emitted to the environment so that less measures for device cooling are needed [9]. Therefore, the total package size can be shrunk. In addition, a comparable electron bulk mobility and lower switching losses compared to Si-based devices due to a better on-resistance promise to improve the efficiency [1, 9]. Note that currently the electron mobility close to the interface in MOS structures is significantly reduced due to trapping and scattering effects (for details see Section 1.3). A parameter to describe the conduction losses in power field effect transistors (FETs) as a function of the material parameters is the so-called Baliga figure of merit (BFOM) [6, 12]

$$\mathrm{BFOM} = \varepsilon_{\mathrm{r,SiC}} \varepsilon_0 \mu E_{\mathrm{B}}^3 \tag{1.1}$$

with the mobility μ, the dielectric constant of SiC $\varepsilon_{\mathrm{r,SiC}}$, the vacuum permittivity ε_0 and the bandgap E_{B}. The BFOM of 4H-SiC is significantly higher than for most other polytypes which is why 4H-SiC is so popular for power electronics.

Finally, one main advantage of SiC compared to other WBG materials is the fact that it forms SiO_2 as native oxide, as is the case for Si. Even though the processing or oxidation of SiC and Si is not exactly the same, knowledge can be transferred from one technology to the other.

1.2 Device Concepts

In SiC, different device concepts for designing power MOSFETs exist. Depending on the device structure, the conducting channel forms along different lattice planes and allows to use the anisotropy of the charge carrier mobilities. Furthermore, different interface properties are observed.

Most commercially available SiC substrates provide a (0001)-surface (Si-face) and a $(000\bar{1})$-surface (C-face) with an off-cut of 4° or 8°. The simplest device concept is a

Table 1.2 Comparison of material properties of 4H-SiC, Si and other wide bandgap materials. [1, 5–7]

Property	4H-SiC	Si	GaAs	Diamond	GaN
Bandgap energy [eV]	3.26	1.12	1.43	5.45	3.45
Breakdown field [MV/cm]	3.2	0.3	0.4	5.7	3.0
thermal conductivity [$\mathrm{Wcm^{-1}K^{-1}}$]	4.9	1.5	0.46	22	1.3
electron drift velocity [10^7 cm/s]	2.2	1.0	1.0	2.7	2.2
electron mobility [$\mathrm{cm^2V^{-1}s^{-1}}$]	1200	1500	8500	2200	1250
Melting point [°C]	2830	1420	1240	4000	2500
BFOM (relative to Si)	626	1	16	2700	650

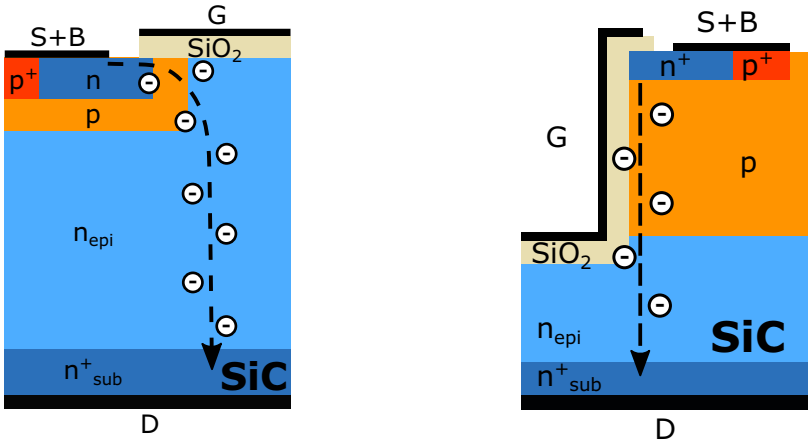


Fig. 1.3 Different SiC device concepts: (a) lateral DMOSFET (b) vertical trench MOSFET [17].

lateral MOSFET, in which the conductive channel forms along the Si-face or the C-face, depending on the substrate orientation. A common design for lateral MOSFETs is the double-diffused metal oxide semiconductor field effect transistor (DMOSFET), as shown in Figure 1.3 (a), whose name derives from Si technology [1], even though the structure is formed by implantation of SiC and not by diffusion. Lateral devices offer a simple device structure and no etching step is required [1].

In recent years, vertical trench MOSFETs have emerged (Figure 1.3 (b)). Trench structures allow to form the conductive channel along different lattice planes, e.g. the *a*-face $(11\bar{2}0)$ which offers a high electron mobility in 4H-SiC [1]. Furthermore, a higher packing density or a smaller pitch is possible. Due to the higher channel density per area, the on-state resistance can be significantly reduced [1, 13–16], leading to a superior device performance compared to lateral SiC devices. On the other hand, in trench devices the channel forms along an etched interface with different properties compared to a standard planar interface [1]. This interface is challenging to align with the desired crystal plane [14]. Furthermore, the gate oxide (GOX) reliability in the trench corners is critical. There, field crowding may occur, leading to a reduced breakdown field. However, this disadvantage can be well compensated with an additional p-implantation to shield the bottom corners of the trench from high electric fields in the off-state [1, 14] (cf. p+ trench implantation Figure 1.3). Overall, a well-designed trench technology can outperform lateral device structures.

Lateral SiC MOSFETs are commercially available by e.g. Wolfspeed, Inc. and STMicroelectronics. The trench technology is currently used by Infineon Technologies AG and ROHM Semiconductor. In this work, trench device test structures as shown in Figure 1.3 (b) are used unless stated differently. The oxide was formed by a chemical vapor deposition (CVD) process using tetraethylorthosilicat (TEOS). After oxidation, a so-called post oxidation anneal (POA) at high temperatures above 1000°C in different annealing ambients is performed. By this, electrically active defects at or near the interface can be reduced and the device performance and reliability improved.

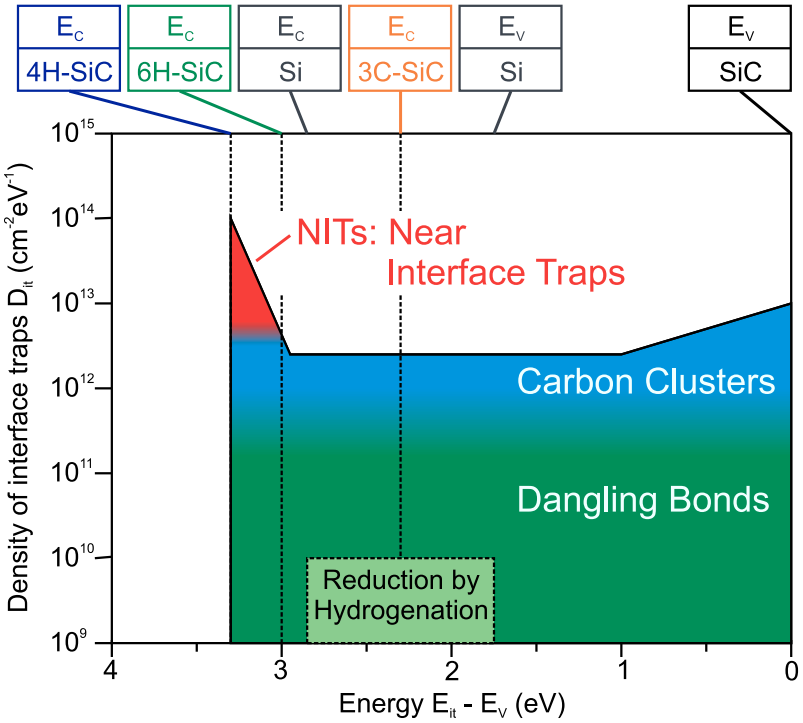


Fig. 1.4 Composition of the density of interface states for several SiC polytypes and Si. For 4H-SiC, NITs, carbon clusters and dangling bonds contribute to the whole density of interface traps. Modified from [20].

1.3 Challenges in Silicon Carbide Technology

SiC is a relatively new material in high power electronics still suffering from a relatively high number of defects, making the production of high-performant and reliable devices challenging. Over the years, growth related defects, e.g. vacancies, carbon impurities, stacking faults, and micropipes have already been strongly reduced [1] and different type of dislocations have been reduced by special growth methods such as the repeated a-face growth [1]. As was shown for example in [18], the substrate quality is essential for growing high-quality epitaxial layers on top and therefore, for producing reliable SiC devices. Extended defects in epitaxial SiC layers may reduce the oxide reliability, increase leakage and decrease the breakdown voltage [1].

1.3.1 The SiC/SiO_2 Interface

It is commonly assumed that the interface quality and the interface trap density are strongly related to each other [19]. The SiC/SiO_2-interface strongly influences the performance and reliability of MOS structures, especially the performance of MOSFETs since the conductive channel forms close to the interface region. For this reason, much research effort is put into improving the interface quality e.g. in form of reduced interface roughness, and into the reduction of interface and near interface traps (NITs) by various post oxidation treatments such as POAs.

Electrically active defects in general can be donor-like, acceptor-like or amphoteric, depending on the defect type. The trap occupation is determined by the location of the

Fermi level. Defects can have several charge states compared to defect-less states, e.g. single positively or negatively charged or even multiply charged. In thermal equilibrium, each defect has a certain probability of being in a certain charge state depending on the position of the Fermi level. The probability for being in a certain charge state is determined by its charge transistion level (CTL). The CTL, e.g. for the $(0/-1)$ transition, determines the energy above which the trap level is more likely to be in a negatively charged state than in the neutral state. This is only a probability and means that some traps of the same type in a different charge state may as well exist and that dynamic charge transitions may exist (cf. random telegraph noise). If the $(0/-1)$ CTL permanently lies below the Fermi level, the defect is most likely permanently charged and acts as fixed charge.

A proposed composition of the interface state density is shown in Figure 1.4 [20]. The total density of interface traps D_{it} may consist of NITs (red), dangling bonds (green) and carbon clusters (blue) in varying concentrations depending on the polytype [20, 21]. NITs are located approximately 3 eV above the SiC valence band edge E_{V}, which is slightly below the 4H-SiC conduction band edge E_{C} and above the conduction band edge of 3C- and 6H-SiC. In contrast, dangling bonds and carbon clusters form trap states throughout the SiC band gap. Si dangling bonds or so-called Pb-centers form due to the structural misfit between the SiO_2 and the SiC lattice and are found in similar concentrations as in Si/SiO_2-systems. Their share of the total D_{it} is rather small compared to the other defect types [21]. In Si technology, dangling bonds are successfully annealed by hydrogen (H) treatments. In SiC, however, no positive effect of H passivation has been observed so far [19, 22, 23].

Carbon Clusters

About the existence of carbon clusters at the interface, no established opinion exists in the SiC community. On one hand, many theoretical publications predict the formation of carbon clusters [19, 21, 22, 24]. On the other hand, several experimental publications do not observe any carbon accumulations at the interface [25].

During the oxidation of SiC, carbon dissociates and migrates through the oxide. During the diffusion process, part of it can react and form interstitials and clusters or graphitic regions, preferably close to the interface [22, 25]. However, this theoretical prediction could not be validated. Pippel *et al.* [25] could not find any graphite structures, carbon clusters or double-bound C-atoms with high-resolution electron microscopy. In their experiments, all carbon at the interface was bound to Si-atoms. Additionally, Deák *et al.* [23], who also predicted the formation of interfacial carbon clusters from their simulations, could not find any experimental support for their existence. Therefore, from the experimental point of view, the existence of carbon clusters is still to be established.

Near Interface Traps

The term “near interface trap” is unfortunately inconsistently used in the SiC-community. On one hand, it is used as an acronym for border traps and in this context, generally stands for trap levels which are located close to but not directly at the interface. On the other hand, Afanasev *et al.* [24] established the term NIT for a special type of an electron oxide trap which is located approximately 1.5 nm to 2 nm away from the interface, 2.8 eV below the SiO_2 conduction band edge [24]. The NIT is presumably an intrinsic trap in SiO_2 [24, 25], however, its chemical nature is not known. The presence of Si at the interface seems to

enhance the formation of NITs [24, 25]. A contradicting theory stipulates that the NIT is not intrinsic but related to carbon dimers [23]. Another candidate for NITs is the intrinsic electron trap in SiO_2 described in [26, 27].

In contrast, the description of their electrical behavior is less controversial. NITs are typically neutral unless an electric field is applied. For charging them, high fields are necessary, which is commonly in the strong inversion region for MOSFETs. Because of the higher conduction band minimum in SiC, NITs can be filled more easily compared to Si and therefore have a stronger impact [24]. Among the different polytypes, 4H-SiC is affected the most because the traps are located slightly below its conduction band edge. For most other polytypes, NITs lie above the conduction band edge where they are more difficult to fill and therefore, electrically less active [24].

1.3.2 Oxide Defects in Amorphous SiO_2

In addition to defects directly at or close to the interface, a whole zoo of oxide defects is expected from density functional theory (DFT), e.g. intrinsic electron traps in SiO_2 [26, 27], different kinds of vacancies and interstitials, hydrogen related defects etc.

Oxygen Vacancies

The oxygen vacancy (OV) is the most frequently studied defect in silica and is formed when an oxygen (O) atom is missing. This defect forms during the oxidation process in dependence of the processing parameters, e.g. temperature, oxygen partial pressure etc. [28]. Additionally, it can form due to trapping effects and subsequent defect formation during high voltage stress [29] (cf. Section 2.3.3). The OV can be described with a 4-state non-radiative multi-phonon (NMP) model of which not all states are detectable in spin-resonance measurements. Two prominent states of the OV are the experimentally observed E' center and the E'_γ center [28].

Hydrogen-related Defects

Hydrogen-related oxide traps are currently in the focus as a possible trap candidate causing negative bias temperature instability (NBTI) in Si devices [28]. Especially in Si MOSFETs, hydrogen is deliberately brought into the system in order to passivate Si dangling bonds at the interface to the oxide. However, this step unfortunately also increases the density of active oxide traps with increasing hydrogen concentration. Two prominent candidates for hydrogen-related defects are the hydrogen bridge and the hydroxyl-E' center [28].

The hydrogen bridge (HB) is formed when atomic hydrogen reacts with an OV. The reaction from an interstitial hydrogen to form the hydrogen bridge is nearly barrierless whereas the backwards reaction has a relatively high barrier. This type of trap might cause stress-induced leakage currents in gate oxide [28].

Hydroxyl-E' Center

In amorphous SiO_2, sites with distorted but intact Si−O bonds can form new defects by the interaction with atomic hydrogen. As an example, the hydroxyl-E' center (H-E') center is formed by the interaction of H with a stretched Si−O bond by breaking one of the bonds. As a result, a hydroxyl group facing a Si dangling bond is formed. This configuration is more favorable than an interstitial H atom and is expected to exist in

significantly larger quantities than any other defect. The H-E' center is currently a major suspect for explaining NBTI and random telegraph noise in pMOS devices. [28]

1.3.3 Passivation Strategies of Interface and Oxide Traps

In order to reduce the number of defects, several passivation strategies can be followed. Common attempts are the following [30–48]:

- post metallization anneal (PMA) with e.g. forming gas and dinitrogen (N_2)
- plasma (pre-) treatment, e.g. with NH_3
- processing steps before oxidation (e.g. cleaning steps, introduction of sacrificial layers)
- improvement of oxidation techniques and parameters
- pre-oxidation anneal (e.g. nitric oxide (NO), NH_3)
- post oxidation anneal (e.g. NO, nitrous oxide (N_2O), N_2, dihydrogen (H_2) etc.)

Additionally, the different passivation strategies can be combined. At the moment, various annealing strategies before and after oxidation are studied the most. Without any treatment, the interface is of low quality after the oxidation, resulting in high defect densities and low charge carrier mobilities [49]. At the moment, interface nitridation is the most promising, of which annealing in NO is currently the most common POA.

Nitrogen (N) incorporation in general significantly reduces the density of interface states and the incorporation of negative charges for electron injection, which results in improved device performance and reliability [35, 49]. The NO POA leads to a reduction of the interface state density close to the conduction band edge in n-doped SiC but at the same time, to a slight increase of the trap density close to the valence band edge of p-doped SiC [32, 49, 50]. The passivation efficiency depends on the amount of nitrogen at the interface and only indirectly on the annealing temperature and time [33]. During the anneal, according to [51], the NO molecule migrates preferably through 7-membered ring structures in the oxide towards the interface, where it passivates the interface. In addition to nitridation, re-oxidation of the interface is observed [50]. On one hand, nitrogen is incorporated at the interface but simultaneously, oxidation with nitrogen removal takes place. The nitrogen from the interface moves into the bulk oxide and may be reincorporated at the new interface. However, both processes are competing and especially the re-oxidation may lead to the formation of new defects [36, 42]. N is incorporated directly at the interface or close to it but not in bulk SiO_2 [34, 36, 42, 52]. At the interface, Si−C−N and Si−O−N bonds were detected with hard x-ray photoelectron spectroscopy (HAXPES), compensating Si−C dangling bonds and compensating oxide defects close to the SiC/SiO_2-interface [53]. Other research groups believe that NO POA removes different types of carbon-related defects at the interface [22, 23, 54].

Another popular annealing ambient is NH_3. In contrast to NO, NH_3 does not contain any oxygen so that no re-oxidation takes place during the anneal, avoiding the competition between oxidation and annealing described above. For NH_3 annealed devices, an even further improved mobility compared to NO is reported [45, 55] together with a similar density of interface states [43]. The NH_3 POA acts differently than the NO POA: In the bulk oxide, reactions mainly take place with SiO_2 leading to the formation of water.

Table 1.3 Temperature dependence of the different mobility components [58–60].

Component	Temperature dependence
surface acoustic phonons	T^{-1} or $T^{-\gamma}$
surface roughness	T^{0}
coulomb scattering	T^{1}

Additionally, dissociation might take place [56]:

$$NH_3 \longleftrightarrow NH_2 + H \tag{1.2}$$

$$NH_2 \longleftrightarrow NH + H \tag{1.3}$$

These species, however, tend to react with hydrogen to form NH_3 or with SiO_2 and therefore loose their mobility rather quickly. The nitridation increases with increasing temperature. Nevertheless, at the same time the hydrogen amounts within the oxide decrease [56]. Similar migration behavior and reactions in bulk SiO_2 are likely to take place in SiC/SiO_2 systems.

In contrast to NO, NH_3 POA incorporates N in large amounts throughout the whole oxide and not only at the interface [43, 45, 52]. With regard to the studies of Baumvol [56] conducted on Si/SiO_2 structures described above, the nitrogen incorporation throughout the bulk oxide might result from the dissociation of NH_3 into NH_2 or NH and following reactions with SiO_2. In total, more N is incorporated than for the NO POA [33, 52]. This leads to a change of the oxide stoichiometry [42], an increase of the dielectric constant [42], a decrease of the breakdown field [42, 43] and an increased charge-to-breakdown [44]. A more detailed analysis of the NH_3 POA and a direct comparison with NO annealed devices will be presented in Section 2.2.

Furthermore, many other annealing ambients have been tried in recent years of which so far none has proven to be as effective as the NO and the NH_3 anneals when considering not only device performance but also oxide reliability. Common other annealing ambients are H_2, N_2, N_2O, argon (Ar) and phosphoryl cloride ($POCl_3$) (cf. e.g. [31, 34, 36, 40, 57]).

1.3.4 Inversion Channel Mobility

The inversion channel mobility is strongly influenced by the interface quality. Scattering at surface acoustic phonons (μ_{ac}), Coulomb scattering ($\mu_{Coulomb}$) at fixed charges or charged interface states, surface roughness of the interface (μ_{sr}) and bulk scattering mechanisms (μ_{bulk}) [1, 58–60] all lead to a reduction of the total channel mobility μ, becoming significantly lower than the SiC bulk mobility. Approximately, the following relationship holds [58, 59]:

$$\frac{1}{\mu} = \left(\frac{1}{\mu_{bulk}}\right) + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{Coulomb}} \tag{1.4}$$

Each component has a different temperature dependence T (Table 1.3). This makes it possible to determine the dominant mobility components at different temperatures and by this to find the dominant cause for mobility limitations at a certain temperature.

1.3.5 Subthreshold Hysteresis

Because of the large number of interface states, hysteresis effects between voltage up- and down-sweeps (e.g. transfer characteristic (I_D-V_G) or capacitance-voltage (CV) measure-

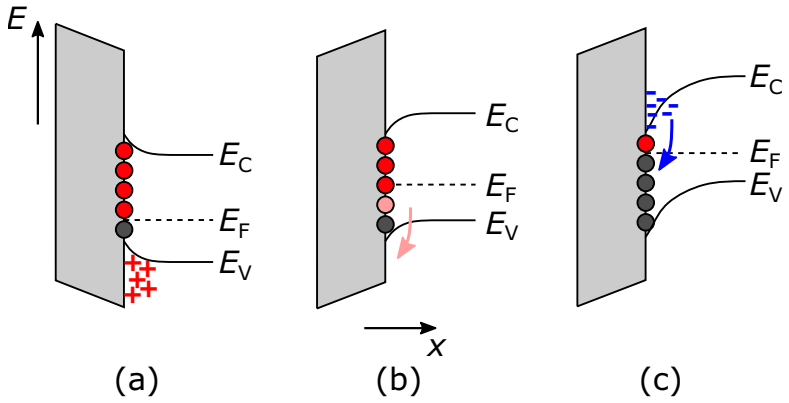


Fig. 1.5 Band diagrams illustrating charge capture and recombination at the interface causing sweep hysteresis.
(a) In accumulation, holes are captured.
(b) When the Fermi level rises close to midgap, slow recovery takes place (long emission times).
(c) For a Fermi level position close to the conduction band edge, recombination with electrons takes place.

ments) in SiC MOS devices are observed [61]. Therefore, the definition of a single threshold voltage is not suitable anymore in SiC technology.

Figure 1.5 shows the band diagram during a voltage sweep. When starting the sweep in accumulation (Figure 1.5 (a)), the Fermi level is close to the valence band edge and all hole traps lying above are positively charged. During the up-sweep of the voltage, the Fermi level moves upwards towards the conduction band edge. Positively charged defects below the Fermi level slowly emit their charges (Figure 1.5 (b)). When the gate voltage exceeds the threshold voltage, i.e. the Fermi level moves close to the conduction band edge, electrons from the conduction band can recombine with the trapped holes and neutralize the charges or can be trapped themselves (Figure 1.5 (c)) [61]. The change of interface trapped charges during a sweep from accumulation to inversion and back causes a measurable change in the threshold voltage, which is especially pronounced in the subthreshold region. The hysteresis increases the deeper accumulation is reached during the sweep. Since the Fermi level moves through the whole band gap, (sub)threshold voltage hysteresis correlates with the total trap density of defects with states within the band gap. The effect is fully reversible [61].

1.3.6 Bias Temperature Instability

BTI is a serious and often studied reliability concern in SiC [62–64] leading to threshold voltage drifts caused by repeated gate bias and temperature stress. When applying a gate bias to the MOSFET, charge trapping at and close to the SiC/SiO_2-interface takes place, leading to a threshold voltage drift. BTI can be observed under positive (positive bias temperature instability (PBTI)) and negative gate bias stress (NBTI), resulting in a shift of the threshold voltage in the positive and negative direction, respectively. Furthermore, BTI may lead to an increased on-resistance at fixed gate bias, a decreased device efficiency, increased leakage and other undesirable effects [63, 65, 66].

BTI is caused by charge trapping at or near the SiC/SiO_2-interface in preexisting defects in addition to the creation of new defects [67, 68]. Even though BTI has been intensively investigated in Si-technology for years, no commonly accepted physical model about the atomistic origin and its modeling exists [69, 70]. Currently, the following defect candidates are under investigation: interactions with hydrogen [71, 72], intrinsic electron traps in SiO_2 [26, 27], dangling bonds [73, 74], and oxygen vacancies [28, 75]. In contrast to Si, BTI in SiC has only been investigated for the last decade [76], often showing significantly higher drifts (cf. [65] for example). As will be shown in Chapter 3 in this thesis, BTI in SiC and Si share many similarities [17]. For this reason, a common cause for at least PBTI in both technologies has been suggested [17, 24, 77]. A more detailed discussion and a detailed comparison of BTI in SiC and Si power MOSFETs can be found in Section 3.2.

Empirical Prediction of Bias Temperature Instability Drifts

When modeling BTI mathematically, the prediction of threshold voltage drifts is of considerable interest. The simplest way of modeling BTI data for lifetime prediction is the use of empirical models. When plotting experimentally determined BTI threshold voltage drifts over stress time on a double-logarithmic plot, a straight line is often obtained over a certain time range. This behavior can be described with an empirical power law model [78]. Such a model lacks any physical background and usually results in an overestimation of the drift because it does not account for any saturation effects of the degradation [79, 80]. For a perfect power law, an indefinitely increasing distribution of time constants would be needed, which is not reasonable [80]. The time-evolution model for the power law approach predicts the threshold voltage shift ΔV_{th} as a function of the gate bias V_{G} and the stress time t [78]:

$$\Delta V_{\mathrm{th}}(t) = A(V_{\mathrm{G,ref}}, t_{\mathrm{ref}}) \cdot \left(\frac{t}{t_{\mathrm{ref}}}\right)^{n} \tag{1.5}$$

with the reference time t_{ref}, the prefactor A depending on the point of reference and the time evolution exponent n. The reference point A is the measured drift after a certain stress duration with a fixed gate voltage. This model is commonly applied to extract end-of-lifetime drifts (typically 5-10 years) from shorter stress times ($t < 10^6$ s) [78].

Furthermore, power law and exponential descriptions can be used to describe the voltage acceleration of BTI [78]:

$$\Delta V_{\mathrm{th}}(V_{\mathrm{G}}) = A(V_{\mathrm{G,ref}}, t_{\mathrm{ref}}) \cdot \mathrm{e}^{M(V_{\mathrm{G}} - V_{\mathrm{G,ref}})} \tag{1.6}$$

$$\Delta V_{\mathrm{th}}(V_{\mathrm{G}}) = A(V_{\mathrm{G,ref}}, t_{\mathrm{ref}}) \cdot \left(\frac{V_{\mathrm{G}}}{V_{\mathrm{G,ref}}}\right)^{m} \tag{1.7}$$

with the gate voltage V_{G}, the reference gate voltage $V_{\mathrm{G,ref}}$, the power law voltage acceleration factor m and the exponential voltage acceleration factor M.

A more accurate approach to predict BTI drifts is the use of capture and emission times which describe the kinetics of capture and emission processes in the NMP model [80–82]. In this model, the capture and emission time constants for charge exchange can be described as [80]

$$\tau = \tau_0 \exp\left(\frac{\varepsilon}{k_{\mathrm{B}} T}\right) \tag{1.8}$$

with the capture/emission time τ, the effective capture/emission time τ_0, the Boltzmann constant k_B, the temperature T and the capture/emission barrier ε. Since the emission barrier is strongly temperature dependent, the time constants are a function of bias and temperature. Additionally, the barriers are considered statistically distributed [80], i.e. they consist of a mean activation energy with a standard deviation.

Now, when modeling a threshold voltage drift, a set of defects with distributed capture and emission time constants is assumed. This means that several combinations of capture and emission times exist and their distribution can be visualized in so-called capture/emission time (CET) maps. The resulting drift for certain bias and measurement conditions and the considered defect distribution is obtained by the sum of the defects which were charged in the measurement time window and not yet discharged after a certain recovery time [80]. Detailed reports about CET maps can be found in [80, 82, 83].

In case the recovery is of less interest and only a worst-case degradation under constant voltage stress needs to be evaluated, it is sufficient to only study the charge capture process, i.e. a marginal distribution of the CET or activation energy map. This can be done by evaluation the threshold voltage drift as a function of the stress time. As already mentioned above, a linear threshold voltage drift is observed in the log-log plot for sufficiently small measurement windows which can be describe to a certain degree with a power law. However, a perfect power law description would require an infinite number of time constants which is unlikely to exist. Another approach to describe this behavior, which can also model the experimentally observed saturation of the drift, is a Gaussian or normal distribution. A power law in time can be as well produced in a limited time window when considering a wide Gaussian distribution of the activation energy [80]. When neglecting recovery effects, a thermal activation model can be derived as [80]

$$\Delta V_{\mathrm{th}} = \frac{\Delta V_{\mathrm{th,\,max}}}{2} \mathrm{erfc}\left(\frac{E_{\mathrm{A}} - k_{\mathrm{B}} T \log\left(\frac{t}{\tau_0}\right)}{\sqrt{2}\sigma} \right) \tag{1.9}$$

with the maximum threshold voltage drift $\Delta V_{\mathrm{th,max}}$, the mean effective activation energy of the Gaussian trap distribution E_{A}, the Boltzmann constant k_{B}, the temperature T at which the measurement is performed, the stress time t, an attempt frequency τ_0 and the width σ of the Gaussian trap distribution. As already mentioned, this model considers the trap energy to be normally-distributed, where E_{A} is the mean activation energy for charge capture, comparable to the expectation in a normal distribution [80].

Note that all these models for lifetime prediction were developed for Si technology. As will be shown in Section 3.3, these modeling approaches have been demonstrated to also apply for SiC technology.

1.4 The Non-Radiative Multi-Phonon Theory

In many old models, charge trapping is described using a Shockley-Read-Hall (SRH) approach [84, 85]. Over the years, this was found not to accurately describe all experimental observations and was therefore partially extended (e.g. [86]). Even though the SRH model seems to be compatible with fast interface states, however, several experimental observations exist which cannot be explained with this approach [28, 68].

For this reason, a more advanced model to describe trapping effects in semiconductors, the so-called non-radiative multi-phonon (NMP) model, has been developed. There, different charge states of a defect are described by parabolic functions in the configuration

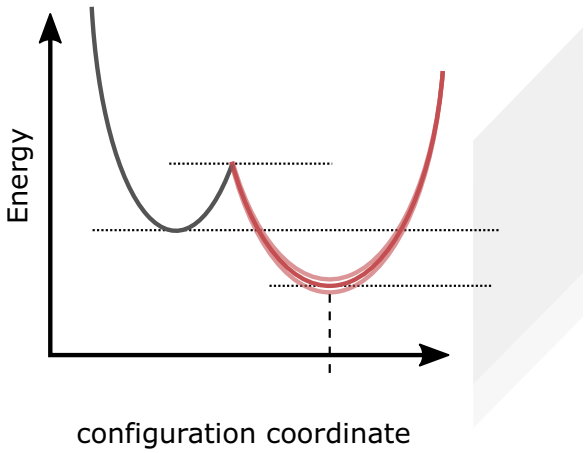
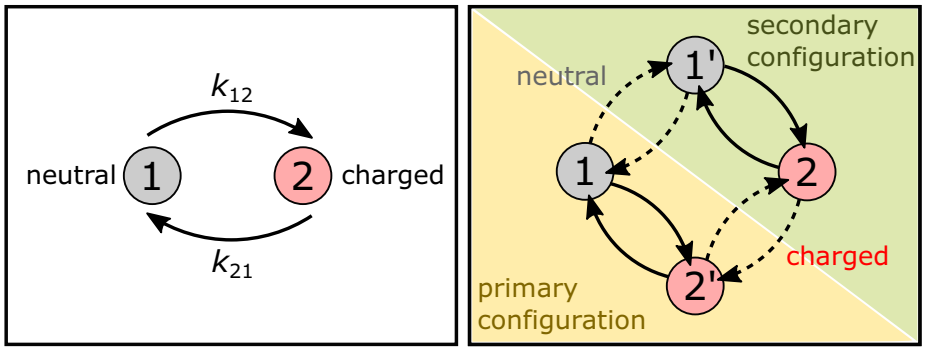


Fig. 1.6 Schematic energy profile of a 2-state NMP model. The states are given by the minima of the parabolic energy profiles. Modified from [5].

coordinate diagram (Figure 1.6). The minima of each paraboly represents the equilibrium state. Depending on the complexity of the underlying mechanism, a neutral state, several charged states and several transition states may be required to adequately describe the trapping behavior. In general, a charge transfer is described by a transition from one parabola (charge state) to another. Thereby, the transition rate $k_{i,j}$ is determined by the overlap of the wave functions of each state [87]. This charge transition may take place by a radiative transition, which means that the configuration coordinate does not change, or by a non-radiative transition including a change of the configuration coordinate. Even though the energy barrier for a radiative transition is significantly lower than for the non-radiative one, the latter can only occur with the help of a phonon [87]. From the mathematical point of view, the transitions are treated as Markov chains which means they are only influenced by the current charge state [28, 68].

In the simplest model, the 2-state NMP model, a charged and neutral state exist between which charge transitions can take place (Figure 1.7 (a)). In many cases, the 2-state model is sufficient to describe trapping effects. Nevertheless, experimental data exist which require additional transition states, which led to the development of the 4-state NMP model [88]. The 4-state model consists of two stable charge states (e.g. 1 - neutral, 2 - charged) which may have metastable charge states 1' and 2', respectively (Figure 1.7 (b)) [28, 68, 88]. A shift of the threshold voltage is only observed for transitions $1' \Leftrightarrow 2$ and $1 \Leftrightarrow 2'$ because here, the defect changes its charge state. The transitions $1 \Leftrightarrow 1'$ and $2 \Leftrightarrow 2'$ are thermal transitions and represent structural changes of the defect without any charge transfer [28].

As was already discussed in detail in the previous section, capture and emission time constants are considered temperature and bias dependent (Equation (1.8)) [68] due to experimental findings. This is one main difference compared to the SRH model.



(a) 2-state NMP model (b) 4-state NMP model

Fig. 1.7 State diagram for a (a) 2-state and (b) 4-state NMP model. The states 1 and 2 represent the stable neutral and charged state. In the 4-state model, additional metastable states $1'$ and $2'$ of each charge state exist which account for structural relaxations during trapping. Thermal transitions are illustrated with dashed lines, NMP charge transitions with solid lines.

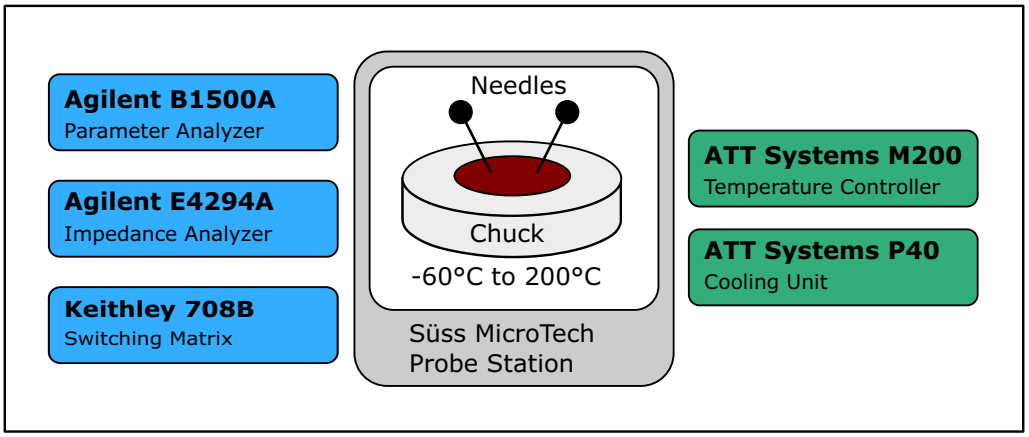
1.5 Methodology

In order to characterize the SiC/SiO_2-interface of 4H-SiC trench MOSFETs, many different measurement techniques have been used. In this section, a short overview on the experimental setup and the characterization methods is given.

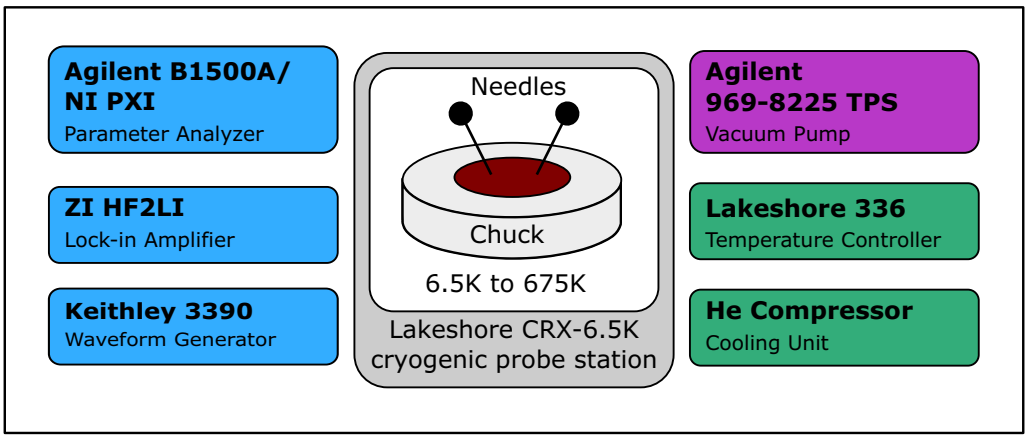
1.5.1 Measurement Setup

The measurements presented in this thesis were obtained using mainly two different test systems, a Süss MicroTech probe station or a Lakeshore CRX-6.5K cryogenic probe station (Figure 1.8). The Süss probe station is equipped with an Agilent B1500A parameter analyzer including four high-resolution source-measurement units (SMUs) and one high-power SMU, a Keithley 708B switching matrix and an Agilent 4294A impedance analyzer. The chuck temperature can be controlled in the range −60°C to 205°C with an ATT Systems M200 temperature controller and an ATT Systems P40 cooling unit. All measurements which do not require a wafer stepper, cryogenic temperatures or temperatures above 200°C were performed at this probe station. If not stated differently, the chuck temperature is 30°C (room temperature).

Low temperature measurements such as thermal dielectric relaxation current (TDRC) were performed using the cryogenic probe station which covers a temperature range between 6.5 K to 675 K, using a Lakeshore 336 temperature controller. The system consists of a closed cycle helium compressor for cooling and a probe chamber which is operated under high vacuum using an Agilent Technologies 969-8225 TPS compact vacuum pump. At the cryogenic probe station, 5 National Instruments PXI-4138 SMUs, a Zurich Instruments HF2LI lockin-in amplifier and a Keithley 3390 arbitrary waveform generator are available. For every kind of deep level transient spectroscopy (DLTS) measurements, a lock-in amplifier combined with a waveform generator is at our disposal. For TDRC, the Agilent B1500A was used. CV measurements at the cryogenic probestation were performed using



(a) Room temperature setup



(b) Cryogenic setup

Fig. 1.8 Standard measurement setup for (a) the room temperature measurements conducted at a needle prober and (b) cryogenic measurements performed at a cryogenic probe station.

the Agilent 4249A impedance analyzer. Optionally, at both systems an Oriel Instruments 74100 monochromator and an Oriel Instruments 66901 xenon lamp can be used.

A few measurements, when larger statistics were needed, were performed at an MPI TS3000-HP automated probe station equipped with Keithley 2636B SMUs, Agilent E5250 switching matrices and an AC3 Thermal System TS010 (ERS® electronic GmbH). The chuck temperature can be regulated from −60°C to 200°C.

1.5.2 Transfer Characteristics

The transfer characteristics of a MOSFET describe the drain current I_D as a function of the gate voltage V_G for a fixed drain potential V_D. Figure 1.9 shows a typical transfer characteristic of a SiC trench MOSFET. It already contains a significant amount of information about trapping effects at the interface between SiC and SiO_2. Trapping and scattering events influence the charge carrier flow in the channel and therefore impact the

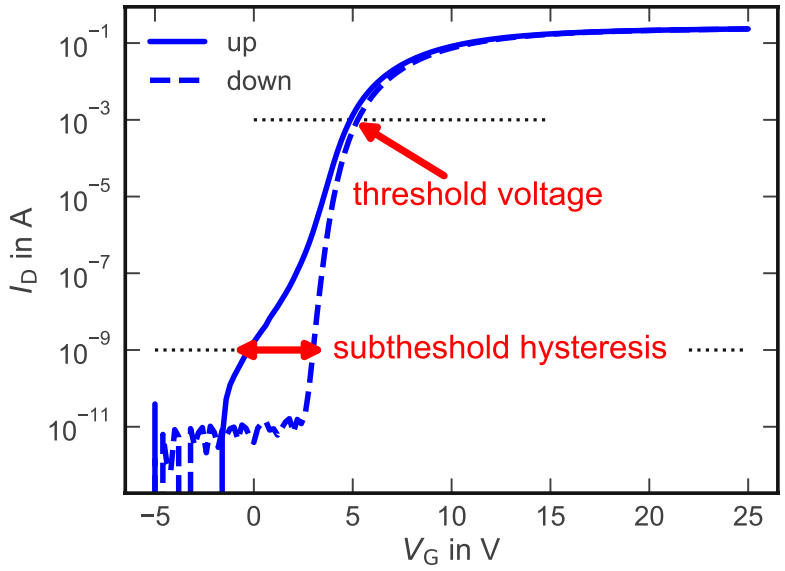


Fig. 1.9 Typical transfer characteristics of a SiC trench MOSFET. The threshold voltage is extracted at 1 mA and the subthreshold sweep hysteresis at 1 nA.

drain current or other characteristics like the inversion channel mobility, threshold voltage and the on-resistance.

In this work, the threshold voltage and the channel mobility are of considerable interest. The threshold voltage can be extracted in many ways. In this thesis, it is commonly extracted with a current criterion ($I_D = 1\,\text{mA}$ or a comparable current density for different active device areas) out of the transfer characteristics. Since the threshold voltage is strongly influenced by trapping effects, it is a suitable parameter to monitor device degradation. Additionally, the channel mobility is of considerable interest. The channel mobility and the on-resistance times the active device area are key characteristics for the performance of a MOSFET and therefore important parameters in order to benchmark process changes.

Ghibaudo Mobility vs. Field Effect Mobility

The inversion channel mobility of a MOSFET is a key parameter to determine the device performance. There exist many different methods for mobility extraction, all having certain advantages and disadvantages. A very accurate method to determine the mobility for example in the bulk material are Hall measurements [60]. However, these measurements cannot be conducted on most fully processed MOSFETs, especially trench devices, so that the mobility is commonly extracted from the transfer characteristics. However, the transfer characteristics are strongly influenced by parasitic components such as parasitic resistances, making it difficult to extract the "real" channel mobility. Two popular methods to extract an apparent channel mobility out of experimentally determined transfer characteristics are the field effect mobility and the Ghibaudo method [89].

For the extraction of the field effect mobility, the standard textbook formula for the drain current in long channel transistors for operation in the ohmic region can be used [8]:

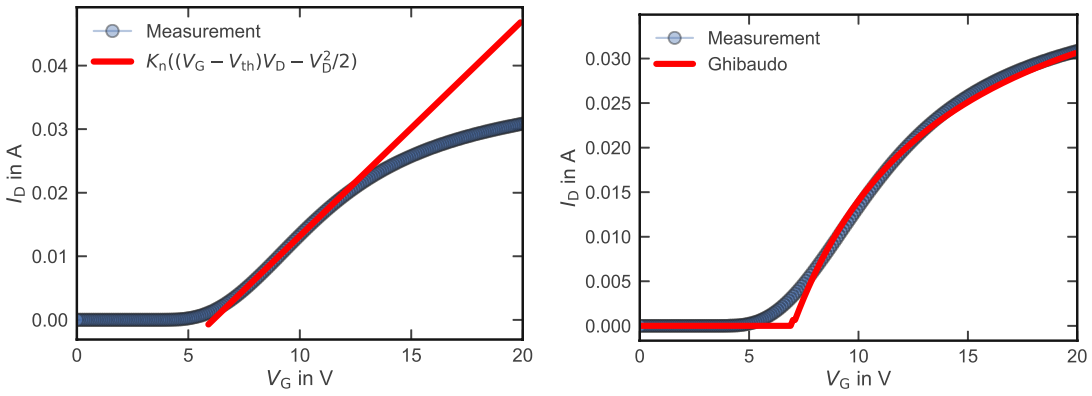
$$I_D = K_n \left[(V_{GS} - V_{th}) \cdot V_{DS} - \frac{{V_{DS}}^2}{2} \right] \tag{1.10}$$

with the gate-source voltage V_{GS}, the threshold voltage V_{th} (extracted with linear extrapolation) and the drain-source voltage V_{DS}. The factor K_n is given as:

$$K_n = \mu_n \frac{C'_{OX} W}{L} \tag{1.11}$$

with the electron mobility μ_n, the oxide capacitance per active device area C'_{OX}, the channel width W and the channel length L. According to Equation (1.10), the drain current depends linearly on the gate bias for operation in the ohmic region. The slope of the linear curve is determined by the factor K_n, which is given in Equation (1.11). K_n is directly dependent on the channel mobility and constant device parameters. Therefore, the field effect mobility can be easily obtained by fitting the slope K_n of the transfer characteristics for operation in the ohmic region. Figure 1.10 (a) shows a measured transfer characteristics and a fitting for the extraction of the field effect mobility. It is obvious that the simple textbook formula can only model the device characteristics in a very narrow voltage range. This is caused by the fact that it does not include a number of physical effects which cause the experimentally observed characteristic and can therefore, neither model the region around the threshold voltage nor the saturation of the drain current due to parasitic series resistances (cf. [90]). Therefore, the field effect mobility commonly underestimates the real channel mobility [90]. However, it is well suitable for the qualitative comparison of different processes or devices.

A more accurate method for modeling the measured transfer characteristic of a MOSFET has been developed by Ghibaudo [89]. In contrast to the field effect mobility, Ghibaudo's method can model the saturation of the drain current for high gate voltages caused by parasitic series resistances [89, 90]. The Ghibaudo method can be applied for transfer characteristics measured in strong inversion at high gate voltages where the characteristics



(a) Textbook formular ohmic region

(b) Ghibaudo formular

Fig. 1.10 Comparison of the accuracy of the drain current textbook formula in the ohmic region and the drain current formula modified by Ghibaudo [89]. The textbook formula from which the field effect mobility can be derived can only model the linearly increasing part of the I_D-V_G curve correctly whereas the Ghibaudo method can additionally model the saturation of the drain current for high gate voltages. Neither model can map the voltage region close to the threshold voltage.

are still linear. The method is a modification of the simple textbook formula for the drain current, adding a so-called mobility reduction coefficient Θ [89]:

$$I_{\mathrm{D}} = \frac{WC'_{\mathrm{OX}}}{L} \frac{\mu}{[1 + \Theta(V_{\mathrm{GS}} - V_{\mathrm{th}}^{\mathrm{G}})]} (V_{\mathrm{GS}} - V_{\mathrm{th}}^{\mathrm{G}}) V_{\mathrm{DS}} \tag{1.12}$$

with the charge threshold voltage $V_{\mathrm{th}}^{\mathrm{G}}$. Note that the charge threshold voltage is extracted from the linear extrapolation to the x-axis of the $I_{\mathrm{D}}/g_m^{1/2}$ vs. V_{GS} characteristics. The charge threshold voltage and the threshold voltage extracted by linear extrapolation from the transfer characteristic are identical in case the mobility is independent of the gate voltage [89].

From Equation (1.12), the transconductance g_{m} can be obtained by the differentiation of the drain current with respect to the gate-source voltage, leading to

$$g_{\mathrm{m}} = \frac{W}{L} C'_{\mathrm{OX}} \frac{\mu}{[1 + \Theta(V_{\mathrm{GS}} - V_{\mathrm{th}}^{\mathrm{G}})]^2} V_{\mathrm{DS}}. \tag{1.13}$$

When dividing Equation (1.12) by the square root of Equation (1.13), a term can be obtained which only depends on the mobility and not on the mobility reduction coefficient:

$$\frac{I_{\mathrm{D}}}{{g_{\mathrm{m}}}^{1/2}} = \left(\frac{W}{L} C'_{\mathrm{OX}} \mu V_{\mathrm{DS}} \right)^{1/2} (V_{\mathrm{GS}} - V_{\mathrm{th}}^{\mathrm{G}}) \tag{1.14}$$

This equation linearly depends on the gate-source voltage with a slope depending on the channel mobility and constant device or measurement parameters. Therefore, when fitting the straight line and extracting the slope m, the Ghibaudo mobility can be extracted as:

$$\mu = \frac{m^2}{C'_{\mathrm{OX}} V_{\mathrm{DS}}} \left(\frac{W}{L} \right)^{-1}. \tag{1.15}$$

This method is a more accurate way to determine the channel mobility from measured transfer characteristics since it accounts for parasitic series resistances and can therefore model the saturation of the drain current for high gate voltages (cf. Figure 1.10). However, the method is still not capable of modeling the threshold voltage in the transfer characteristics correctly [90]. Since it does not consider any trapping effects it also leads to an underestimation of the real channel mobility, however, it gives a more accurate estimate than the field effect mobility.

When modeling as well the region around the threshold voltage of a transfer characteristics, trapping effects need to be considered additionally. These methods are more sophisticated. Examples for a more accurate modeling of the transfer characteristics of SiC MOSFETs or the channel mobility can be found in [90] and [91].

Subthreshold Sweep Hysteresis

As already mentioned in Section 1.3.5, the subthreshold sweep hysteresis is an indicator for the number of trap states throughout the SiC band gap. During a sweep from accumulation to inversion, trapped charge carriers get emitted or recombine during the voltage sweep, leading to a shift between the up- and down-sweep of the transfer characteristics which is especially pronounced in the subthreshold regime. In order to provoke this phenomenon for hysteresis studies, the devices were charged for 5 s at -20 V in order to trap holes at

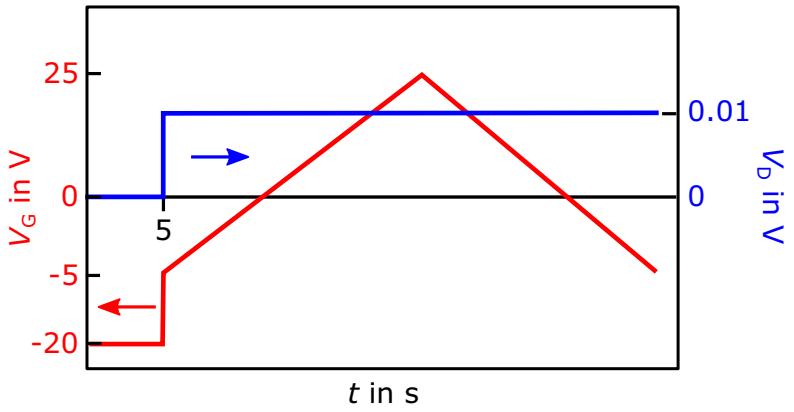


Fig. 1.11 Measurement sequence for measuring the subthreshold sweep hysteresis. First, the device is charged in accumulation for a few seconds. Afterwards, the up- and down-sweeps of the transfer characteristics are conducted. The drain bias is kept constant.

the interface between the p-doped SiC channel region and the SiO_2 GOX (Figure 1.11). Afterwards, standard transfer characteristics with a fixed drain bias are measured starting from small negative voltages and sweeping up into strong inversion. The subthreshold hysteresis for the standard device layout is extracted at a fixed current of 1 nA or a comparable current density for different device designs (cf. Figure 1.9).

1.5.3 Preconditioned Bias Temperature Instability Measurements

As described in Section 1.3.6, BTI is a serious reliability concern in MOSFETs. In order to determine BTI drifts, many different measurement procedures exist. In the interest of establishing comparable routines for BTI stress, industrial standards for reliability testing have been developed, such as e.g. JESD22 [92] and its extension AC-Q101 [93]. These standards were developed for Si technology and allow for delays between the device stress and the drift readout of several hours. The effect of readout timing has been known in Si based MOSFETs for a long time [94]. In SiC, recent studies have shown that this effect is even more pronounced due to a relatively large electron trapping component at the interface, which may lead to ambiguous drift results [95–99]. Because of fully reversible hysteresis effects, the obtained threshold voltage drift strongly depends on the readout timing (Figure 1.12) and the device history. Therefore, an alternative measurement sequence is needed which separates the quasi-permanent and the fast-recovery drift component in order to enhance the reproducibility.

To obtain readout values which are less sensitive to short delays and therefore more stable in SiC devices, a preconditioning pattern can be introduced, as shown in Figure 1.13. The preconditioning pattern consists of an inversion and an accumulation pulse (±15 V), the pulse with the opposite polarity to the stress bias coming first. This method has been suggested in [63, 95]. After each preconditioning pulse, respectively, a readout is performed. Due to the preconditioning, the interface states are brought into a defined charge state and the recovery of the fast trapping component (subthreshold sweep hysteresis [61]) is removed, therefore leading to more stable readout values which barely depend on the readout timing

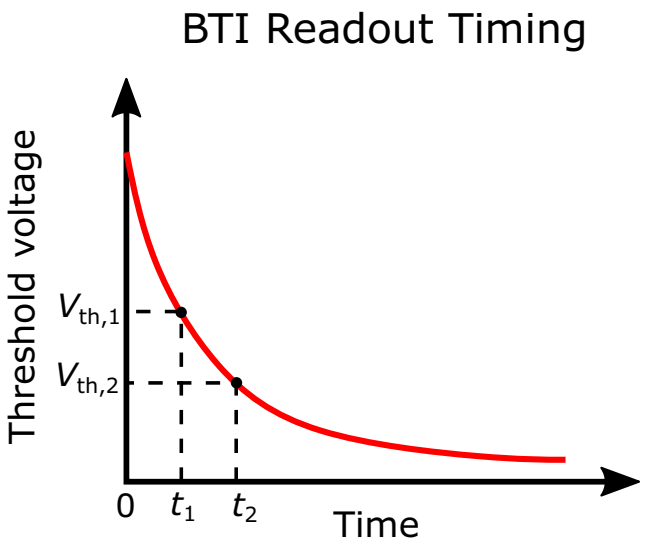


Fig. 1.12 The impact of a readout delay in the recovery phase on the extracted threshold voltage for BTI measurement patterns without any form of preconditioning. Due to the recovery of the fast trapping component, small delays between stress and readout may lead to different threshold voltage readouts.

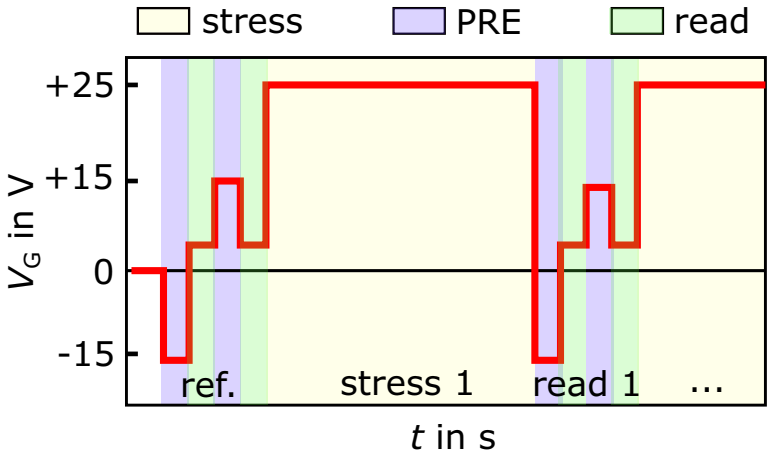
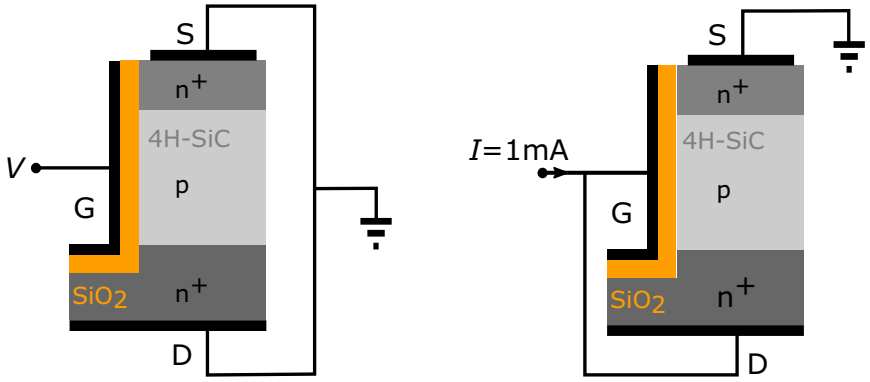


Fig. 1.13 Measurement pattern for preconditioned PBTI. After the stress phase, a first preconditioning pulse in accumulation, a readout, a second preconditioning pulse in inversion and a second readout phase are added. For NBTI, the polarity of the preconditioning pulses is reversed. Picture modified from [17].

and the short-term device history anymore [95]. Thus, mainly the quasi-permanent drift component as described in Section 1.3.6 is monitored. In order to monitor the drift of the hysteresis, the difference between the readout after the first and the second preconditioning pulse can be monitored [95].

If not stated otherwise, the readout is conducted in the gated diode configuration (Figure 1.14), using a current criterion. In this configuration, the gate and drain terminals of the MOSFET are shorted and the source terminal grounded. A gate and drain current of



(a) stress configuration (b) gated diode readout configuration

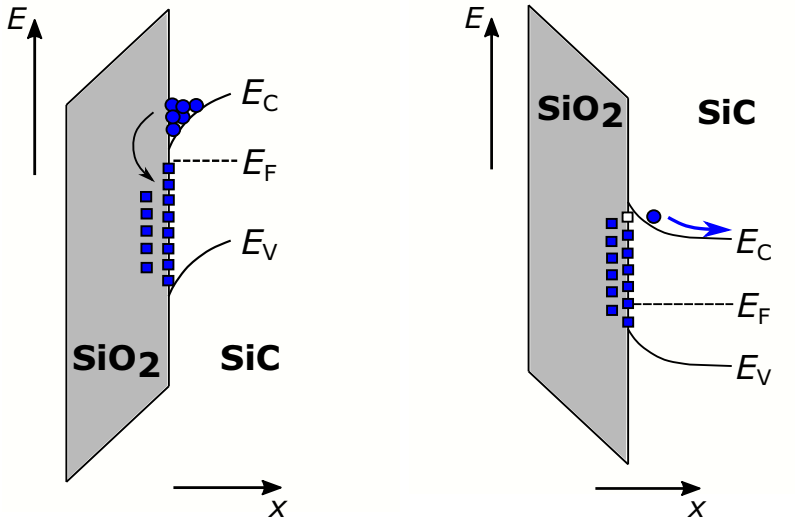
Fig. 1.14 BTI measurement configuration during (a) the stress phase and (b) the readout. During stress, the MOSFET is connected as a MOS capacitor, i.e. drain and source terminal are shorted and grounded and the stress bias applied to the gate. In the readout phase, the MOSFET is connected in gated diode configuration, i.e. drain and gate terminal are shorted and the source terminal grounded.

1 mA is forced and the resulting gate and drain voltage monitored. Compared to a readout with a fixed recovery bias, this configuration offers the advantage that no back-mapping to the current to an initial transfer characteristics is needed. The resulting gate voltage is defined as threshold voltage.

1.5.4 Thermal Dielectric Relaxation Current

The TDRC method is a cryogenic measurement technique to determine interface trap energies and trap densities in MOS devices. In contrast to methods based on CV measurements, trap densities can be extracted without knowledge about the band bending at the interface and it is less sensitive to fluctuations of the surface potential [100]. The method belongs to the group of dielectric relaxation current (DRC) measurements, consisting of TDRC and isothermal dielectric relaxation current (IDRC). IDRC measurements are performed at a constant temperature with different gate biases whereas TDRC is performed with a constant gate bias for change of temperature with a constant heating ramp [101]. More information about IDRC can be found in [102].

Figure 1.15 shows the band diagram during the charging and discharging of the interface in TDRC measurements. Figure 1.16 shows the measurement signals over time. First, the MOS interface is positively biased at room temperature or slightly below in order to attract electrons to the interface where they may get trapped. In case MOSFETs are used, they need to be connected as metal oxide semiconductor capacitors (MOSCAPs), i.e. drain and source are shorted and grounded. With the gate bias still applied, the device is cooled down to cryogenic temperatures, e.g. 20 K. Due to the still applied bias and the low temperatures the emission of trapped charges is unlikely. At low temperatures, capture and emission processes are slowed down so that the trapped charges are literally "frozen" in their trapped state. Then, the gate bias is switched to a small negative bias in depletion (discharging voltage V_{dis}) and the temperature gradually increased with a



(a) Charging Phase (b) Discharging Phase

Fig. 1.15 Band diagrams of the interface region for (a) the charging and (b) discharging phase of a TDRC measurement. Modified from [103].

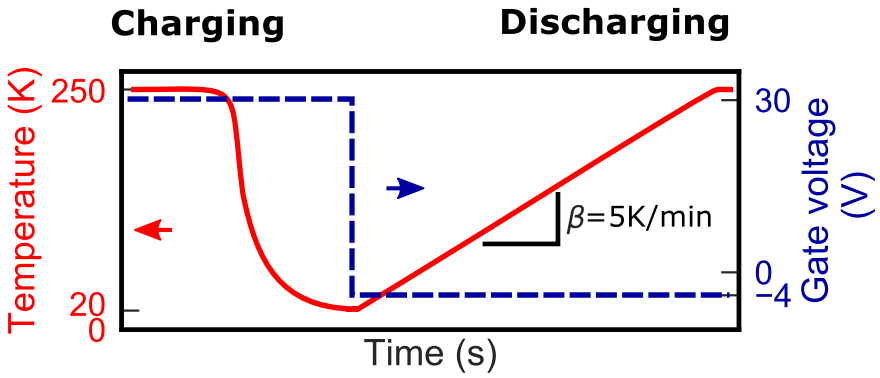


Fig. 1.16 Measurement procedure of a TDRC measurement. First, a high positive gate bias is applied at room temperature or slightly below. Therefore, electrons are attracted to the interface and may get trapped there. Then, with the gate bias still applied, the temperature is reduced to cryogenic temperatures. Afterwards, the gate bias is switched to a small negative bias in depletion and the temperature gradually increased with a constant ramping rate β and the resulting temperature dependent gate displacement current measured. [104].

constant heating ramp β. Meanwhile, the temperature and time dependent gate current is measured [20, 25, 100, 101, 105–107]. Depending on the temperature, traps start to emit their charges into the SiC conduction band where they are pushed away from the interface due to the discharging bias and can be measured as temperature dependent gate displacement currents [25, 100, 101], showing peaks at certain temperatures. The gate current is proportional to the density of states D_{it} and the energetic trap location in the band gap to the temperature at which the peak is observed. With the following relation

based on a SRH model, the current over temperature signal can be transformed into a density of states D_{it} and a trap energy [101]:

$$E_{\mathrm{C}} - E_{\mathrm{T}} = 10^{-4} T[1.98 \cdot \log_{10}(\nu/\beta) + 3.2] - 0.0155 \tag{1.16}$$

$$D_{\mathrm{it}} = \frac{I_{\mathrm{TDRC}}}{qA\beta[1.98 \cdot \log_{10}(\nu/\beta) + 3.2] \cdot 10^{-4}} \tag{1.17}$$

with the SiC conduction band minimum E_{C}, the trap energy E_{T} and the temperature T. The area A is the active area during the measurement and in this case a value between the active channel area and the whole trench area.

Furthermore, an attempt-to-escape frequency ν can be extracted. For the simplest way of extraction, measurements with two different heating rates are needed. Then, ν can be extracted with the following relation [105]:

$$y = \frac{T_{\mathrm{max},1}\log(\beta_1) - T_{\mathrm{max},2}\log(\beta_2)}{T_{\mathrm{max},1} - T_{\mathrm{max},2}} \tag{1.18}$$

$$\nu = 10^{y} \tag{1.19}$$

with the temperature $T_{\mathrm{max},i}$ at which the peak maximum occurs for the respective heating rate β_i. This method is rather imprecise because only two heating rates are used. A more precise method to determine the attempt-to-escape-frequency is fitting from a T_{max} vs. β plot, where T_{max} is the temperature at which the current peak occurs:

$$T_{\mathrm{max}}(\beta) = \frac{(E_{\mathrm{C}} - E_{\mathrm{T}}) + 0.0155}{10^{-4}[1.98 \cdot \log_{10}(\nu/\beta) + 3.2]} \tag{1.20}$$

Figure 1.17 exemplarily shows the extraction of the attempt-to-escape frequency.

For traps with similar energies, TDRC peaks may overlap in temperature (Figure 1.18). The current signals of several overlapping peaks are additive and it is nearly impossible to distinguish between a single trap and multiple traps without further knowledge [108]. The so-called half-width ΔT_{TDRC} (Figure 1.18) may give a hint whether multiple traps are involved and can be calculated for a single trap as [108]:

$$\Delta T_{\mathrm{TDRC}} = 2k_{\mathrm{B}}T_{\mathrm{max}}^2/(E_{\mathrm{C}} - E_{\mathrm{T}}) \tag{1.21}$$

In case the measured half-width is larger than the calculated one, several traps with similar trap energies might overlap [107]. However, it is not possible to distinguish between electron and hole traps so that the different peaks can originate from different carrier types.

In the presented experiments, no temperatures below 40 K are evaluated because according to [100], the signal below 50 K is ascribed to bulk traps.

1.5.5 Deep Level Transient Spectroscopy

DLTS describes a high frequency, thermal measurement of capacitance transients in order to determine trap levels, densities and capture cross sections [1, 109–111]. A signal is received in form of positive or negative temperature dependent peaks in the measurement signal that correspond to charge capture or emission. DLTS is a very sensitive, fast and easy method applicable also to non-radiating centers. In contrast to thermal methods such as TDRC, majority and minority traps are distinguishable. Furthermore, information on thermal emission rate, concentration profile and capture rate can be obtained [109]. In

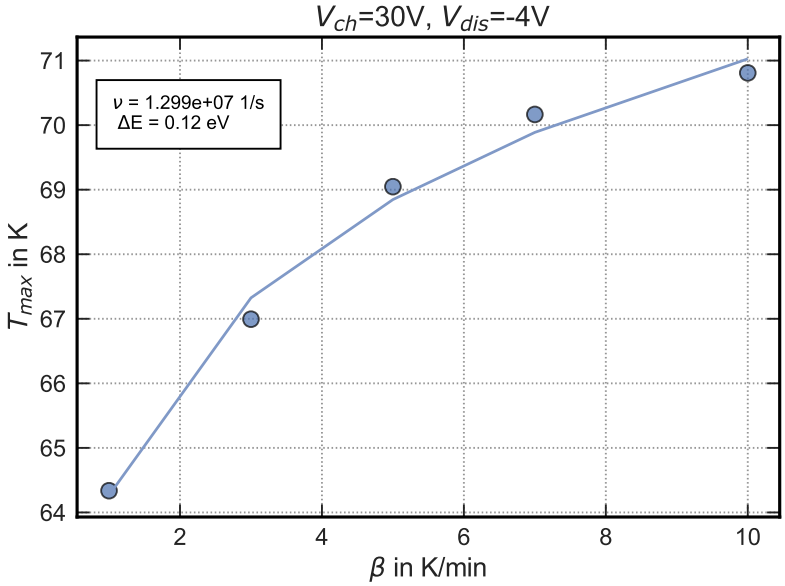


Fig. 1.17 Temperature of TDRC peak maximum as a function of the heating rate of a SiC MOSFET annealed in N_2. The attempt-to-escape frequency is determined by fitting. Modified from [103].

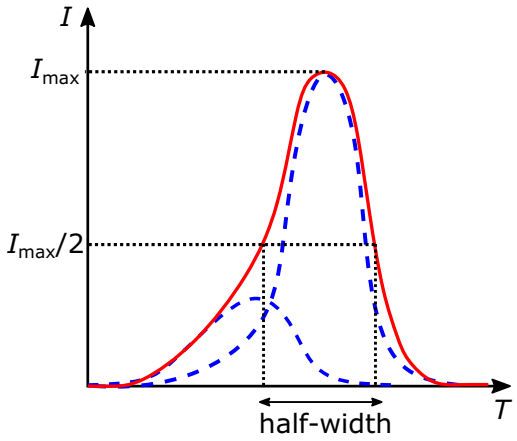


Fig. 1.18 Current-temperature characteristic (TDRC) of several overlapping discrete trap levels with similar trap energies. The single signals add up to one wider peak with a larger half-width.

DLTS, several pulses are applied to the device under test and the capacitance transient is observed. The pulse leads to a deflection from steady state so that the system strives to get back resulting in a measurable transient. The corresponding time constant is temperature dependent. With this knowledge it is possible to extract the activation energy of trap bands. The trap concentration is obtained from the original transient amplitude [109].

The pulsed voltage charges and discharges traps (Figure 1.19). Commonly, the principle of DLTS measurements is explained in the sense of the SRH model. In steady state, the

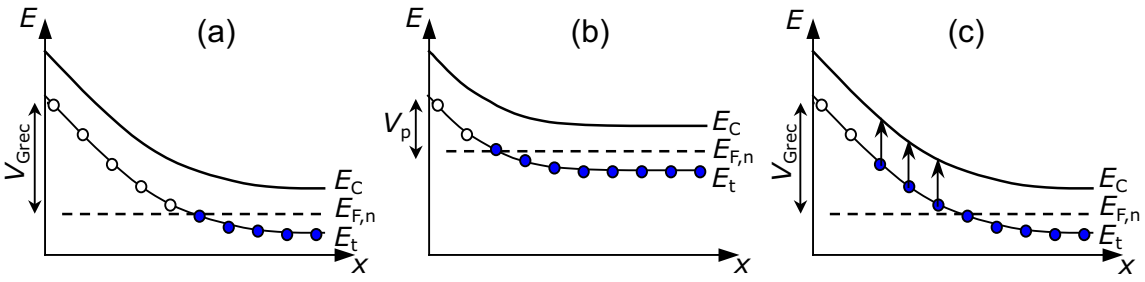


Fig. 1.19 Band diagram of mechanisms taking place in Schottky diodes during DLTS.
a) reverse bias in equilibrium
b) pulse bias
c) after pulse bias while re-establishing equilibrium. Modified from [110].

width of the space charge region defines the capacitance. When a pulse is applied e.g to a diode (Figure 1.19 b)), traps might get charged due to imbalances caused by a change of the space charge region. Depending on the pulse section (high or low), traps are located above the Fermi level compared to the steady state condition so that they emit their electrons to the conduction band (Figure 1.19 c)). However, this mechanism happens delayed relative to the applied pulse so that the emission process becomes visible as a capacitance transient re-establishing steady state conditions [1, 109, 110]. The transient of minority charge carriers is positive (forward bias needed) and the one of majority charge carriers negative (reverse bias needed) [1, 109]. Furthermore, the transient depends on the temperature. In contrast to the SRH-based interpretation from above, the capture and emission processes in the NMP-based model would be ascribed to the temperature and bias dependence of the capture and emission time constants. The parabolas of the different state are shifted relative to each other in the different pulse phases leading to different transition barriers and therefore a change in transition rates.

In order to obtain the common DLTS signal an emission window needs to be chosen. To do so several different methods exists which are explained in detail in [111]. The easiest way to chose an emission window is done by choosing two points in time t_1 and t_2 (boxcar DLTS). The capacitance transient is measured at these points and the difference ΔC determined (Figure 1.20). The plot ΔC vs. temperature T delivers the DLTS-signal [109] and the trap concentration can be calculated as follows:

$$N_\mathrm{t} = 2\frac{\Delta C}{C}(N_\mathrm{A} - N_\mathrm{D}) \tag{1.22}$$

with the number of trapped charges N_t, the capacitance change ΔC at $t = 0$ because of saturation injection pulse, the capacitance C under quiescent reverse bias, the acceptor concentration N_A and the donor concentration N_D [109]. The activation energy is determined by the slope of the $\log(e)$ vs. $1000/T$ plot, with the emission rate e [109]. Nowadays, the time window is commonly set by the use of correlation functions with a characteristic time constant. Depending on the match of the time constants between measured signal and correlation function the DLTS signal is amplified or not. A more detailed description of correlation functions can be found later on in this Section.

The DLTS measurements presented in this thesis were performed with a Zürich Instruments Lockin amplifier with an external pulse generator as illustrated in Figure 1.8 (b).

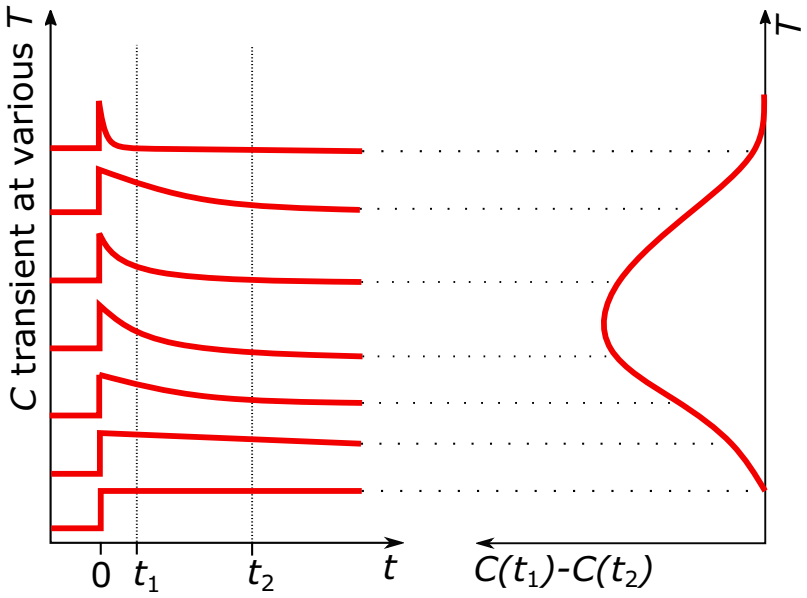


Fig. 1.20 DLTS-signal construction with double boxcar signal integrator. Various capacitance transients at different temperatures are analyzed at two time points. The capacitance difference is calculated and plotted against temperature. Modified from [109].

The pulse duration was 1 ms with the pulse levels 0 V for the stress bias and −9.5 V for the recovery phase.

Correlation Functions

Instead of choosing a time window with two points as proposed in [109], Miller *et al.* [112] introduced correlation functions in order to improve the signal-to-noise ratio (SNR). This concept has been further improved by the suggestion of other correlation functions by Hodgart [113] and Crowell and Alipanahi [114]. Each correlation function has its own characteristic time constant τ. In the post-processing step, the DLTS signal $C(t,T)$ is modulated with a correlation function $w(t)$ in order to obtain the DLTS spectrum $S(T)$:

$$S(T) = \frac{1}{t_{\mathrm{mes}}} \int_{t_0}^{t_0+t_{\mathrm{mes}}} C(t,T)w(t)\mathrm{d}t \tag{1.23}$$

with the measurement point t_0 in time and the measurement window length t_{mes}. Depending on the match of the time constants of the DLTS signal, i.e. the trap level, and of the correlation function, the signal is more or less amplified. The maximum signal height is received when the time constant of the correlation function and of the measured trap distribution match. Note that the time constants of the transients strongly vary with temperature, resulting in the characteristic DLTS peaks at certain temperatures. The choice of the correlation function influences the peak position of the DLTS spectrum along the temperature axis, i.e. different correlation functions lead to different peak positions. The activation energy ΔE_{A} and the capture cross section σ can be obtain from an Arrhenius-plot of $\ln(\tau T_{\mathrm{max}}^2)$ vs. $1/k_{\mathrm{B}}T$. [115]

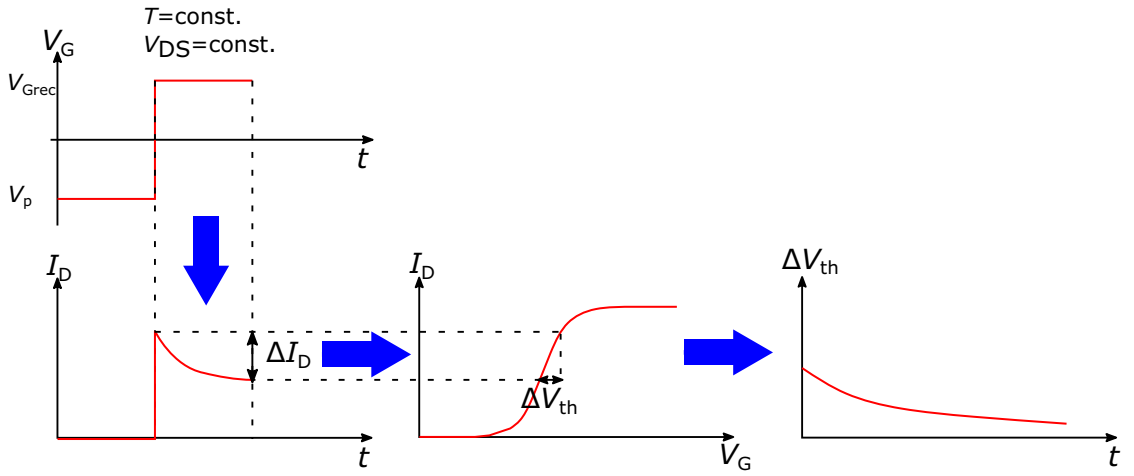


Fig. 1.21 Measurement principle of I_D-DLTS. Rectangular pulses are applied to the gate terminal and the resulting drain current transient measured in on-state of the MOSFET. With the help of regularly measured I_D-V_G curves the drain current transient is converted into a transient of the threshold voltage shift.

Drain Current Deep Level Transient Spectroscopy

Instead of capacitance transients, it is also possible to measure drain current transients when studying MOSFETs. The evaluation is based on the same DLTS theory as for capacitance transients (cf. [109]), however, it is based on the transformation of the current transients to a threshold voltage shift [116]. Figure 1.21 shows the acquisition of a threshold voltage transient out of a drain current deep level transient spectroscopy (I_D-DLTS) measurement. Rectangular pulses are applied to the gate terminal consisting of a stress and a recovery phase. In the recovery phase, a drain current transient is measured. The decay of the drain current can be transformed into a decay of the threshold voltage over time using the transfer characteristics. Since the threshold voltage of a SiC MOSFET strongly depends on the temperature, it is important to regularly measure an I_D-V_G for large temperature sweeps. Here, the stress level $V_p = 0\,V$ and the recovery bias $V_{Grec} = 8\,V$ (peak at 70 K) or 7 V (peak around 120 K) are used. The pulse length is 10 s at each pulse level, respectively. The pulses are chosen rather long because they determine the measurement window and therefore the peak position over temperature. Since I_D-DLTS spectra are supposed to be compared to the channel mobility over temperature, which is obtained from rather slowly measured I_D-V_G curves, long pulses are needed in order to being able to correlate the two characteristics. Every four DLTS pulses, a new I_D-V_G is measured in order to account for the shifting threshold voltage with temperature.

CHAPTER 2

Analysis of Different Annealing Strategies

Contents

2.1 Introduction and Motivation

The device performance and reliability of a MOSFET is strongly influenced by the quality of the interface between the gate oxide and the conductive channel and therefore requires special attention. At the moment, the inversion channel mobility is with up to e.g. $60\,\mathrm{cm^2V^{-1}s^{-1}}$ for NH_3 annealed devices still far smaller than theoretically possible bulk mobilities of up to $1200\,\mathrm{cm^2V^{-1}s^{-1}}$ in lowly doped material [1, 25, 54]. Even though it might be unlikely to reach the bulk mobility in the conductive channel, significantly higher values than are currently reached are expected to be possible. As was already mentioned in Section 1.3.3, different annealing strategies are currently used in order to reduce electrically active trap levels at the interface and in the GOX as well as to improve the overall interface quality.

In this chapter, interface nitridation by POA in NO, NH_3 and a combined anneal consisting of a NO POA followed by an additional POA in NH_3 ($NO + NH_3$) will be discussed. Currently, NO POA is the preferred annealing strategy because it leads to a good device performance and at the same time to an outstanding GOX reliability [117–119]. As already mentioned in Section 1.3.3, NO annealing has a competing oxidizing and a passivating component. The advantage of NH_3 POA is that due to the lack of oxygen, no oxidation takes place, which should theoretically reduce the number of oxidation related defects. Furthermore, an additional trap reduction by hydrogen passivation is expected. The $NO + NH_3$ POA is expected to combine the effects of both POAs. Nevertheless, hydrogen is linked to numerous reliability concerns in Si technology [120–123] and most likely also in SiC.

In addition, as described in Section 1.3.4, the inversion channel mobility in MOSFETs is limited by different scattering mechanisms which contain a contribution by surface roughness. The surface roughness is determined by the interface quality. In order to find out whether different oxidation techniques might have a noticeable impact on the device performance, thermal oxides, plasma-grown oxides and deposited oxides (TEOS) were studied.

2.2 Correlation between Device Performance and Reliability for NH_3-containing Anneals

Even though NO POA leads to well-performing and reliable devices, other nitrogen containing species might result in a better passivation behavior. Recent studies report that annealing in NH_3 POA can lead to even higher channel mobilities compared to the NO anneal [45]. Most research groups focused in their publications on the channel mobility or the D_{it} resulting after NH_3 POA [36, 38, 39, 46]. As will be discussed in the following sections, it is important to also investigate the device reliability, such as the subthreshold hysteresis and the GOX reliability. Often, one has to deal with a trade-off between the device performance and its reliability [55].

For this study, trench MOSFETs as presented in Section 1.2 Figure 1.3 (b) were used. The MOSFETs received different POAs in NO, NH_3 and $NO + NH_3$. Here, the best process of each type of POA is presented. In the following sections, a complete reliability and performance study will be presented (cf. [55]).

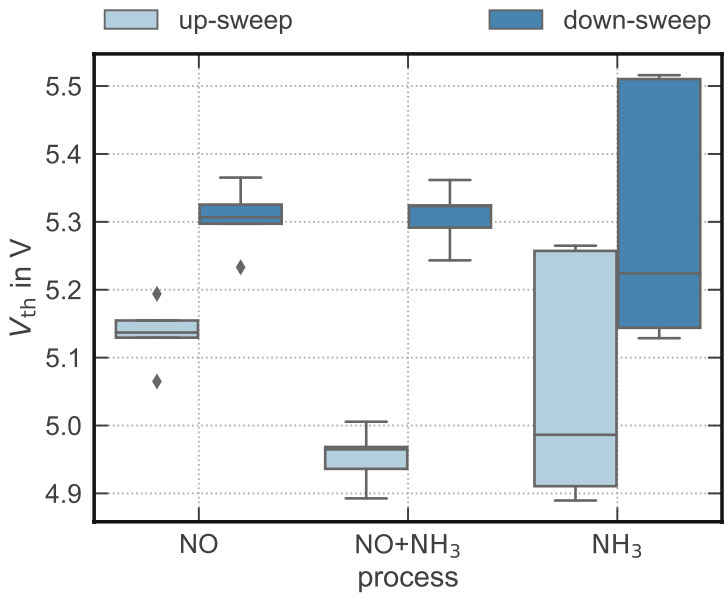


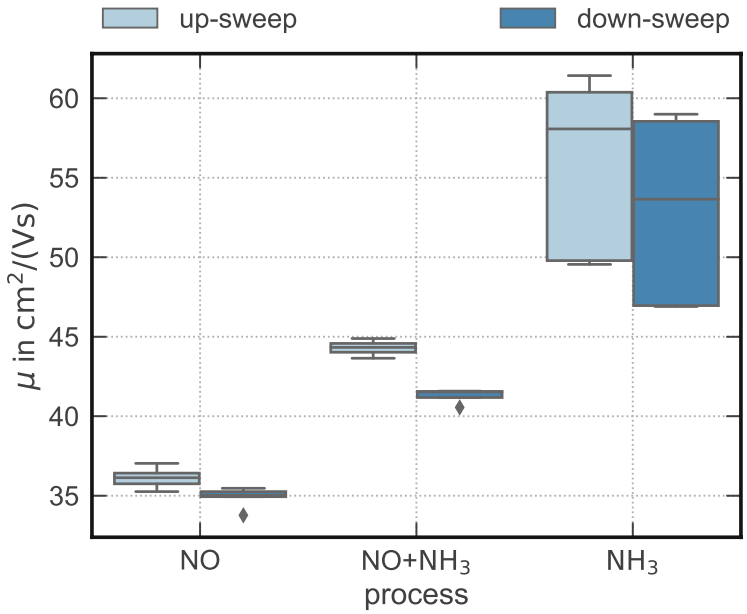
Fig. 2.1 Threshold voltage V_{th} of differently annealed trench MOSFETs. All processes result in similar mean V_{th} but widely different variances.

2.2.1 Transfer Characteristics and Channel Mobility

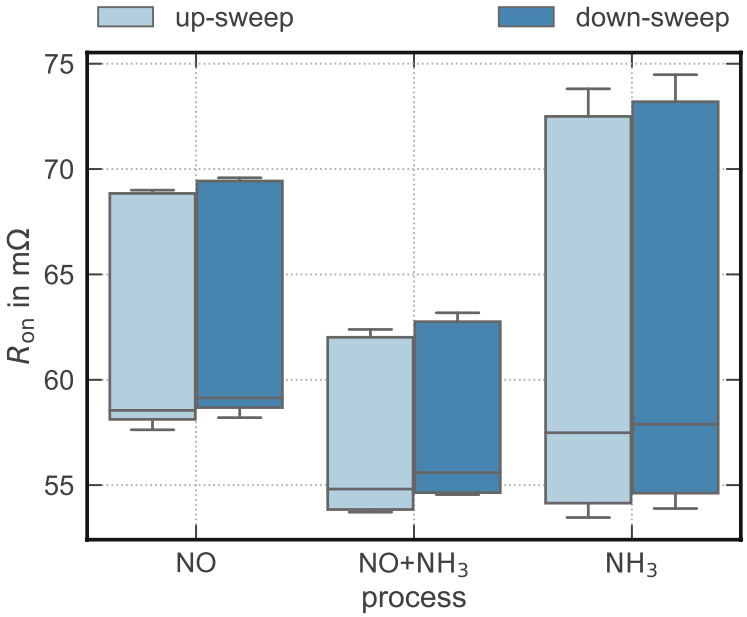
In order to study the device performance, I_D-V_G transfer characteristics were measured as described in Section 1.5.2 and analyzed. Measurements were performed starting the sweep from 0 V, sweeping the gate bias up to 25 V with a fixed $V_D = 0.01V$ and swept backwards to 0 V without any bias interruption. From these curves, the threshold voltage was extracted using a constant current criterion of $I_D = 1\,mA$, the on-resistance at a gate voltage of $V_G = 15\,V$, and the channel mobility with the method of Ghibaudo (cf. Section 1.5.2).

Figure 2.1 shows the threshold voltage resulting for NO, NH_3 and NO + NH_3 annealed trench MOSFETs. Since different POAs may change the net oxide charges it is worth noting that all three processes result in similar threshold voltages around 5 V, indicating similar charge distributions in the channel after the anneals.

Figure 2.2 shows the Ghibaudo mobility and the on-state resistance R_{on} of the studied MOSFETs. In good agreement with existing literature [45], a mobility increase is observed for the devices treated with NH_3. For NO, a Ghibaudo mobility of $35\,cm^2V^{-1}s^{-1}$ was extracted. The combined NO + NH_3 anneal results in $\mu = 40 - 45\,cm^2V^{-1}s^{-1}$ and NH_3 in $\mu = 50 - 60\,cm^2V^{-1}s^{-1}$. The on-state resistance shown in Figure 2.2 (b) is similar for all devices but shows large device to device variations. From X-ray photoelectron spectroscopy (XPS) studies of POAs with similar (but not identical) annealing conditions it is known that NH_3 containing POAs result in a larger amount of interfacial nitrogen (Figure 2.3). NO+NH_3 results in approximately twice the amount of N directly at the interface compared to NO, NH_3 in a 6-times higher amount of N [52]. Additionally, hydrogen is expected to passivate additional interface traps. Overall, NH_3 or NH_3-containing POAs significantly improve the inversion channel mobility in SiC MOSFETs compared to NO. However, it is



(a) Ghibaudo mobility



(b) On-resistance

Fig. 2.2 Ghibaudo mobility (a) and on-state resistance R_{on} (b) of trench MOSFETs with differently nitrided oxides during POA. A higher channel mobility is observed when NH_3 treatment is used. Simultaneously, the mean R_{on} is roughly the same while device to device variations are larger. [55]

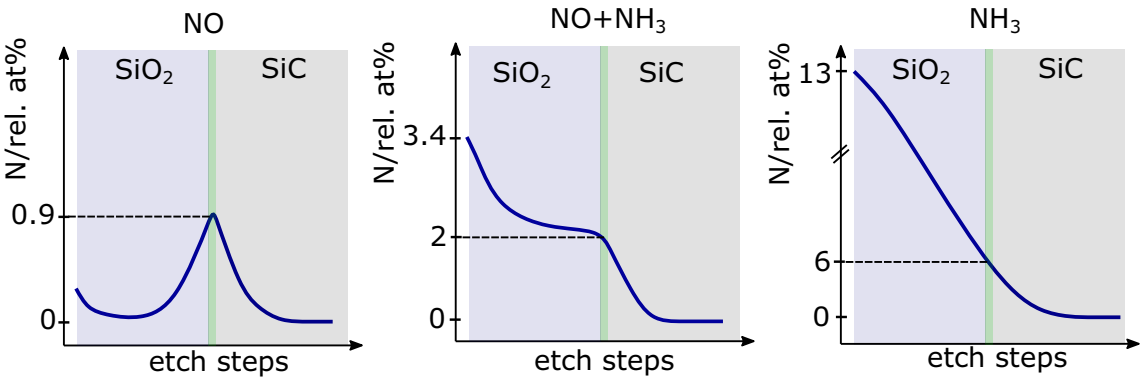


Fig. 2.3 Illustration of the XPS results from Regoutz *et al.* [52] for the nitrogen content of differently annealed SiC/SiO_2 MOS structures. NH_3 in any form leads to nitrogen incorporation throughout the whole oxide in large amounts whereas NO only nitrides the interface.

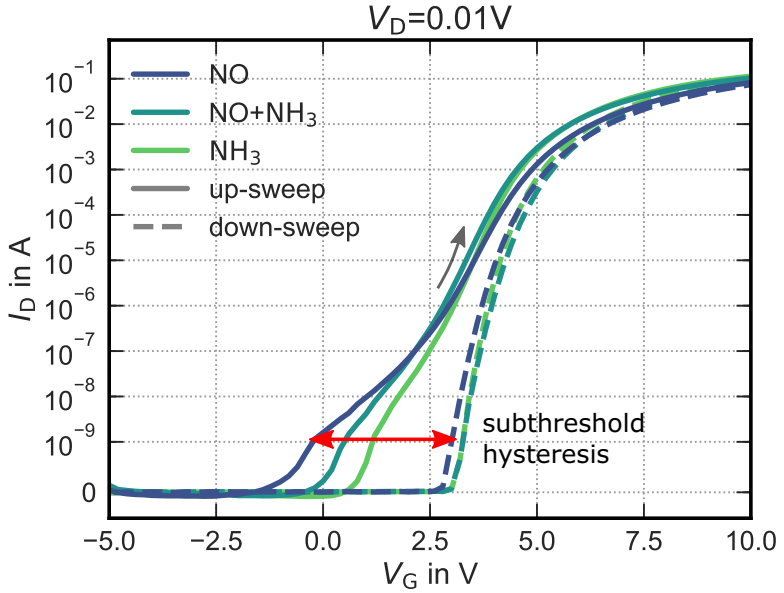


Fig. 2.4 I_D-V_G characteristics showing subthreshold sweep hysteresis in SiC trench MOSFETs with different POAs. The curves show a significant hysteresis extracted at 1 nA between up- and down-sweep. [55]

not clear if the improvement results from the larger interface nitridation or if hydrogen results in an additional passivation at the interface.

From a performance point of view, the NH_3 and $NO + NH_3$ POAs are very attractive for the production of commercial high-performance power MOSFETs. However, as will be shown in the following subchapters, some reliability concerns may arise. [55]

2.2.2 Subthreshold Sweep Hysteresis

The subthreshold sweep hysteresis is a common phenomenon in SiC MOSFETs (cf. Section 1.3.5). While this effect is not critical from an application perspective since it turns the

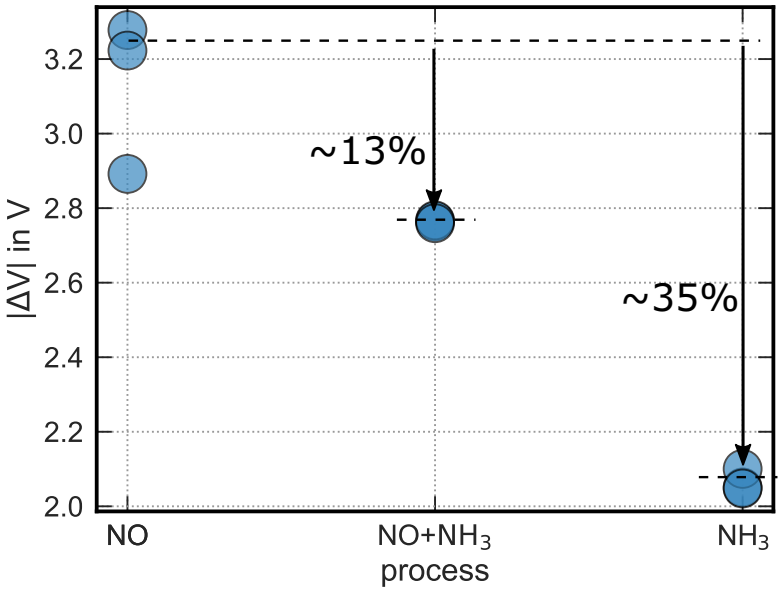


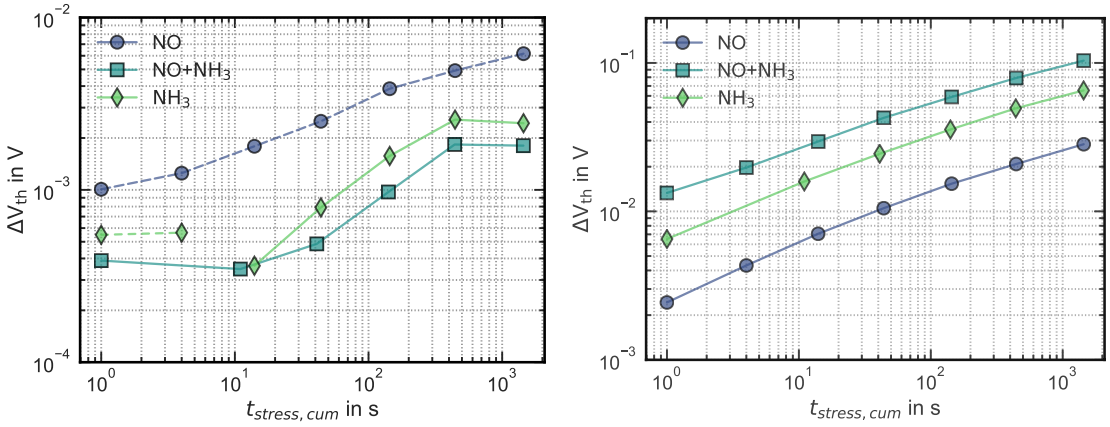
Fig. 2.5 Subthreshold voltage shift for the differently annealed devices, extracted from I_D at 1 nA. [55]

device earlier on and off [63], its analysis is of significant importance for the development of a fundamental understanding of the SiC/SiO_2-interface.

Figure 2.4 shows the transfer characteristics of an NO, NH_3 and $NO + NH_3$ annealed MOSFET. The subthreshold hysteresis depicted in Figure 2.5 was extracted at 1 nA as indicated in Figure 2.4 after preconditioning in accumulation (−20 V for 5 s). The largest subthreshold hysteresis is observed for the NO device. NH_3 reduced the hysteresis by 35% and $NO + NH_3$ by about 13%. Since the subthreshold hysteresis correlates with the number of trap states in the band gap, this indicates that NH_3 containing POAs reduce the number of interface traps with trap states in the middle of the band gap. Note that the threshold voltage hysteresis extracted at 1 mA (cf. difference between up- and down-sweep in Figure 2.1) behaves differently. Here, the NO POA shows a slightly lower hysteresis than the other two POAs. This indicates that NH_3 annealing might additionally affect hole traps at midgap and that states close to the conduction band edge are either less or similarly reduced as for the NO POA. In this thesis, it is assumed that the higher amount of nitrogen at the interface or the additional hydrogen passivation causes the improvement. As expected, the combined $NO + NH_3$ POA combines both processes and therefore leads to a result in between its two single annealing gases. [55]

2.2.3 Bias Temperature Instability

BTI with DC bias stress at room temperature was measured as described in Section 1.5.3. Figure 2.6 shows the preconditioned (a) NBTI and (b) PBTI drift for the three studied POAs. All drifts below 1 mV are considered to be in a similar range as measurement variations and are therefore negligible. For NBTI, in general a very small drift is observed at room temperature. Whereas the NO annealed sample shows negative drift as expected, the NH_3 and $NO + NH_3$ annealed samples show a slight positive drift. However, the



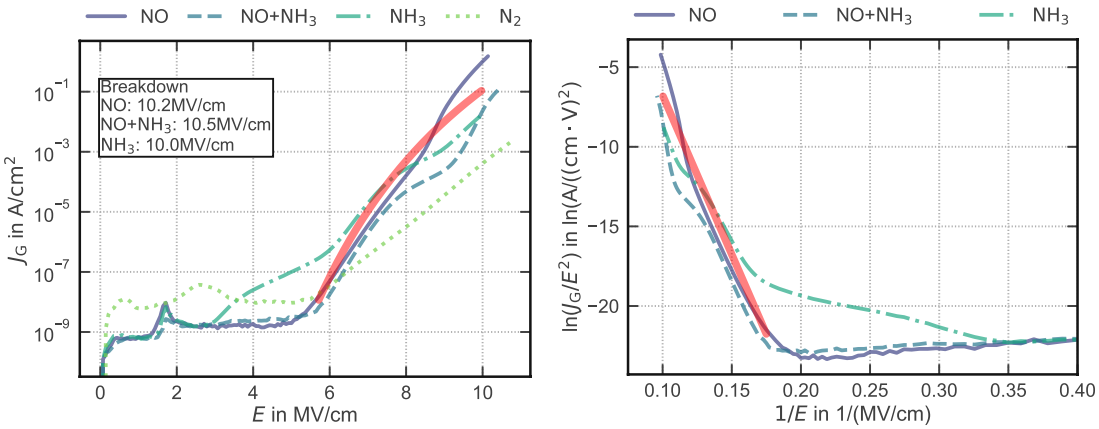
(a) Preconditioned NBTI (b) Preconditioned PBTI

Fig. 2.6 Preconditioned BTI drift for the different annealing variants, extracted after the full preconditioning sequence. The solid lines represent positive drift, the dashed lines negative drift. (a) NBTI (b) PBTI

observed positive drift is rather small and therefore not crucial. If the "wrong" drift direction is a real phenomenon, this could be an indication for ion formation during the stress. Nevertheless, when comparing the absolute drifts of the three POAs, all drift in a similar low voltage range with the NO annealed samples showing slightly higher drifts ($\approx 6\,\mathrm{mV}$) than the other two processes ($\approx 2\,\mathrm{mV}$).

For PBTI slightly higher drifts in the positive direction are observed. After 1.4 ks positive bias temperature stress (PBTS) with 25 V the NO annealed MOSFETs drift the least with a total drift of 30 mV, followed by devices annealed in NH_3 with around 65 mV and in $NO + NH_3$ with 100 mV drift. Therefore, it is concluded that the NH_3 POA either anneals electron traps close to the conduction band less efficiently (e.g. less traps passivated or passivation less stable) or creates additional states leading to the increased PBTI drift. For the higher drift in $NO + NH_3$ compared to its single components it is suggested that new defects are created during the subsequent NH_3 anneal or that the passivation is less stable than for the single anneals. Since BTI can be a serious reliability concern which may lead to an increased on-state resistance and increased static losses, decreased efficiency and a reduced reliability of the transistor [15, 63], higher drifts than the current NO standard are not acceptable.

When recalling the mobility and subthreshold hysteresis results from the previous sections, NH_3 and $NO + NH_3$ anneals both resulted in better results than the NO annealed devices. This clearly demonstrates that a better device performance due to process changes does not necessarily improve the device reliability at the same time. For this reason, a characterization including performance and reliability studies needs to be done for benchmarking new process variants. Often, a trade-off between performance and reliability is needed. For the moment being, the NO POA is still the most appealing from the reliability perspective. [55]



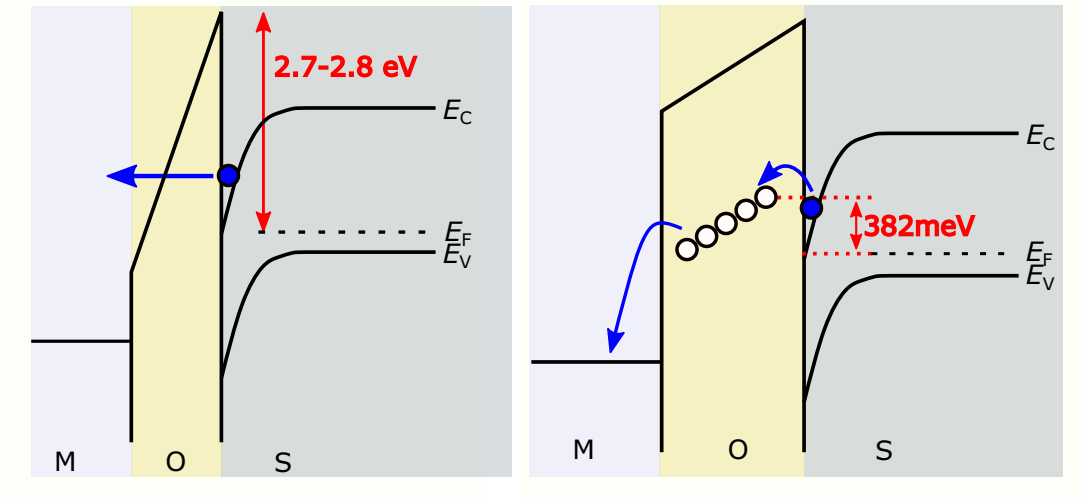
(a) Breakdown/Tunneling (b) Fowler-Nordheim (FN) Plot

Fig. 2.7 Gate current density as a function of the oxide field for the different POAs. NO and NO + NH_3 follow FN-characteristics whereas NH_3 shows different low-field tunneling behavior. (a) GOX breakdown and tunneling characteristics of differently annealed trench MOSFETs. The curves end at breakdown, the breakdown field is given in the inset. (b) FN plot of the studied devices. The red line represents the calculated theoretical FN curve. [55]

2.2.4 Gate Oxide Reliability

Last but not least, GOX reliability is crucial for commercial MOSFETs. Therefore, the tunneling and breakdown characteristics were studied [55, 124]. To do so, a gate bias sweep up to device breakdown was measured (Figure 2.7(a)). As a reference, an N_2 annealed trench MOSFET from a different lot but with the same device design was added. According to XPS studies [52], the N_2 POA does not lead to any measurable modifications of the GOX and should therefore behave similarly to a GOX which received only a high temperature treatment in vacuum. Nevertheless, it leads to a densification of the oxide compared to an as-deposited GOX because of the high-temperature treatment. This process results in barely functional MOSFETs with very low drain currents, extremely high threshold voltage and strongly distorted CV characteristics indicating the presence of numerous interface and oxide traps.

The breakdown fields for NO, NH_3 and NO + NH_3 annealed MOSFETs are shown in the inset of Figure 2.7 (a). GOX breakdown occurs at similar oxide fields on all devices. However, NH_3 annealed devices tend to break at slightly lower fields than NO reference samples even though only very small statistics were recorded (3-4 devices measured). Small variations can be partially explained with the variation of the oxide thickness across a wafer. Note that the NH_3 process presented here in general resulted in larger variations of the device characteristics across the wafer than e.g. the well-established NO POA. In addition, other studies [42, 43] have reported a lower breakdown field for oxides treated with NH_3 POA which matches the tendency observed for the few devices studied here. Therefore, it is concluded that the breakdown of NH_3 annealed samples is lower or the same as for the NO reference.



(a) FN Tunneling (b) TAT

Fig. 2.8 Band diagrams for (a) FN tunneling and (b) trap assisted tunneling (TAT).

However, in the region of tunneling below breakdown, significant differences between the differently processed devices are observed. Whereas the NO annealed MOSFET follows ideal FN tunneling characteristics, both, NH_3 and $NO + NH_3$ POA lead to a distorted tunneling behavior. The tunneling of the $NO + NH_3$ annealed device can also be explained with FN tunneling, however, showing a kink for around 7-8 MV/cm. The same kink is observed for the NH_3 annealed sample, which in addition suffers from increased tunneling at low oxide fields. A more detailed discussion of the different tunneling regions can be found in the following section. With regard to the fact that NH_3-containing POAs lead to nitrogen incorporation throughout the oxide [52] and distorted tunneling characteristics are observed, NH_3 in any form seems to degrade the gate oxide reliability.

Summarizing the overall observations for the comparison of NO, NH_3 and $NO + NH_3$ annealed trench MOSFETs, a higher channel mobility, a lower on-state resistance and less subthreshold sweep hysteresis is observed for the two NH_3 containing processes, i.e. a better device performance is observed. On the other hand, increased PBTI drift and GOX leakage were found, resulting in a significantly degraded device reliability reducing the device lifetime. So overall, the conventionally used NO anneal still offers the best trade-off between performance and reliability. This study also showed the importance of a full device characterization covering performance and reliability studies when analyzing the impact of new processes since performance and reliability are not always correlated. [55]

2.3 Trap Assisted Tunneling in NH_3 Annealed Trench MOSFETs

2.3.1 Tunneling in MOS devices

In MOS devices with oxides thicker than about 5 nm, the dominant tunneling mechanism is FN tunneling. FN tunneling describes the tunneling of charges through a triangular barrier of the conduction band, i.e. only through part of the barrier compared to direct

tunneling (Figure 2.8 (a)) [8]. The barrier height which needs to be overcome depends on the crystal face as well as on the SiC polytype [1] and is reported to be 2.7 eV to 2.8 eV for 4H-SiC Si-face, which resembles the trench bottom of the devices studied here. This barrier equals the expected conduction band offset between 4H-SiC and SiO_2 but it may be reduced by trapping effects [125]. The FN tunneling current can be calculated as [8]:

$$J = \frac{q{E_{\mathrm{OX}}}^2}{16\pi^2\hbar\Phi_{\mathrm{ox}}}\exp\left(\frac{-4\sqrt{2m^*}(q\Phi_{\mathrm{ox}})^{3/2}}{3\hbar E_{\mathrm{OX}}}\right) \tag{2.1}$$

with the elementary charge q, the oxide electric field E_{OX}, the tunneling barrier height Φ_{ox} (expected to be 2.7-2.8 eV for SiO_2/SiC), the effective electron mass m^* (0.39 times the electron mass [126]) and the reduced Planck constant $\hbar$. With the equation given above, it is possible to extract a tunneling barrier for evaluation of the measurements in the appropriate voltage range. Note that FN tunneling is barely temperature dependent.

In addition, trap assisted leakage mechanisms (e.g. TAT) may exist. The existence of trap levels within the oxide may enable charges to tunnel through the oxide even before FN tunneling or direct tunneling starts (Figure 2.8 (b)). This process is highly temperature dependent [127, 128] and can therefore be identified by measuring temperature dependent tunneling characteristics.

2.3.2 Tunneling behavior

Figure 2.9 shows the tunneling characteristics for an NO (reference) and NH_3 annealed trench MOSFET. The reference sample shows GOX tunneling for $E_{\mathrm{OX}} \geq 5$ MV/cm. Literature reports tunneling currents to start around 5.5-6 MV/cm on (0001) 4H-SiC and

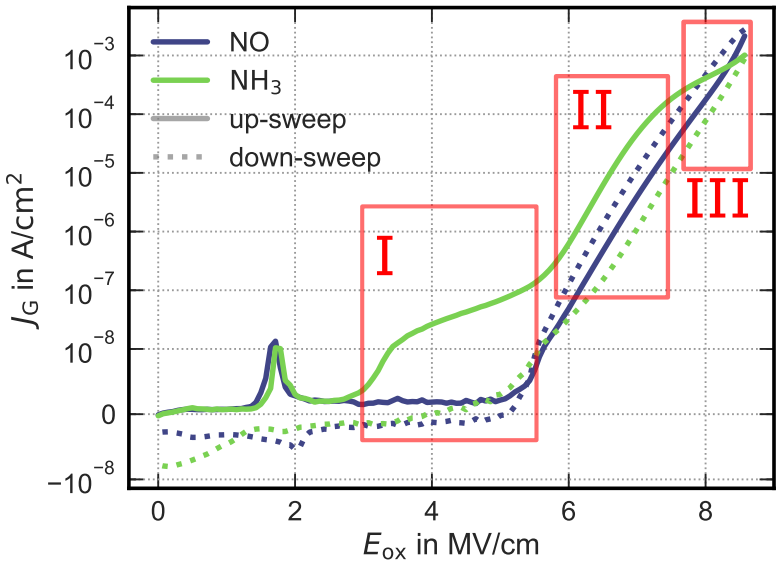
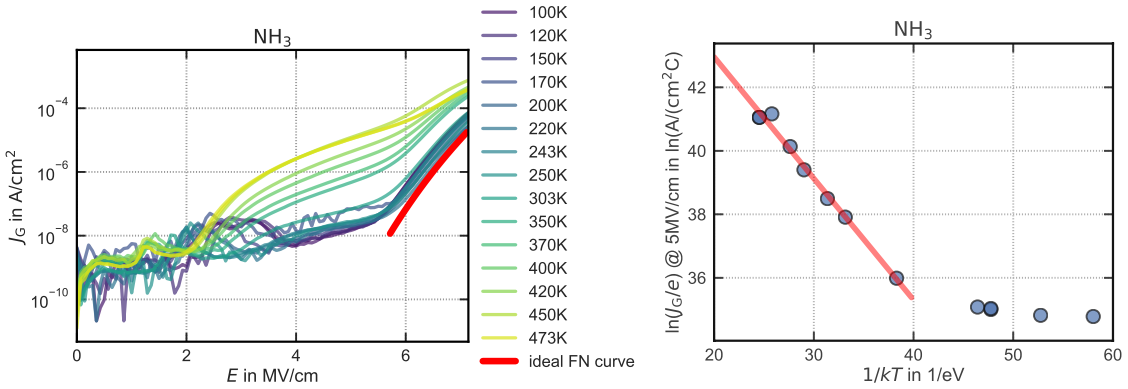


Fig. 2.9 GOX tunneling characteristics for differently nitrided trench MOSFETs. The tunneling behavior of the NO annealed MOSFET can be explained with FN-tunneling. In contrast, the NH_3 annealed MOSFET tunneling characteristic consists of three different tunneling regions: I TAT, II FN tunneling, and III trapping. [124]



(a) Tunneling Characteristics (b) Arrhenius Plot

Fig. 2.10 Temperature dependence of the GOX tunneling characteristics of NH_3 annealed trench MOSFETs (a) and the resulting Arrhenius plot (b) of the TAT region extracted at 5 MV/cm. A strong temperature dependence is observed, resulting in an activation energy of 382 ± 17 meV in the Arrhenius plot. [124]

4.0-4.5 MV/cm on $(000\bar{1})$ 4H-SiC [1], which is in good agreement with the observations presented here. So, the tunneling behavior of the reference sample can be accurately modeled with a theoretical FN curve, resulting in a (fitted) barrier height Φ_{ox}= 2.7 eV, matching barriers reported in [1] and [125] (2.7-2.8 eV) for the Si-face. The fact that the tunneling barrier matches the one of Si-face indicates that the breakdown most likely occurs at the trench corner or the trench bottom. There, the interface forms along the Si-face and the trench corner is known to be the weakest point. In conclusion, FN tunneling is the dominant tunneling mechanism in NO annealed MOSFETs.

In contrast, the NH_3 annealed device shows a different tunneling behavior. For these samples, the gate leakage current can be divided into three different sections which are indicated in Figure 2.9. In region I (2.5-3 MV/cm), an increased leakage current is measured compared to the reference sample which does not show any significant leakage at all in this region. In region II (5.5-7 MV/cm), a comparable tunneling behavior to the NO annealed samples is observed, where it was identified as FN tunneling. At high gate biases in region III (7-8 MV/cm), a kink with a reduced slope of the gate current density is found. In the following sections, the tunneling characteristics of the different regions will be determined. Most results from this section were published in [124]. Note that each tunneling curve was measured on a fresh device because significant trapping took place.

Region I and II

First, since the tunneling behavior in region II resembles FN tunneling in the NO annealed device, the characteristics were fitted to an ideal FN curve. A satisfying fit can be achieved for a barrier height of 2.8 eV which matches the literature values mentioned above and is similar to the barrier extracted from the reference sample. Therefore, region II seems to be dominated by FN tunneling as well.

In order to determine the dominant tunneling mechanism in region I, the temperature dependence was studied (Figure 2.10 (a)). Theoretically, TAT is strongly temperature dependent [127] whereas FN tunneling is only weakly affected. As can be seen in Figure 2.10

(a), region I shows a strong temperature dependence whereas region II seems to be less dependent on the temperature. The small temperature dependence which is observed in region II can be explained with the initially higher tunneling current to which FN tunneling adds up from a certain bias on. This observation is in good agreement with the assignment of region II to FN tunneling. Region I, in contrast, follows a trap enhanced tunneling mechanism. With the help of an Arrhenius plot (Figure 2.10 (b)), the tunneling barrier for TAT was determined. From the slope of the Arrhenius plot, an activation energy $E_A = 382 \pm 17\,\text{meV}$ was extracted. A detailed discussion about the possible origin of TAT and suitable trap candidates will be presented in one of the following sections.

Region III

Finally, the kink in region III was studied. The decrease of the gate current density suggests that charge carriers might get trapped in the oxide. In order to test this, hysteresis measurements can be conducted. If charges are trapped in the oxide, different gate current characteristics for up- and down-sweep should be measured. Figure 2.11 shows gate current sweeps with variable turning points at the gate high level. In the TAT region, a strong hysteresis is observed, indicating that some traps may stay occupied. In region II, the FN region nearly no additional hysteresis effects are measured. However, as soon as region III is entered, an additional hysteresis component appears in the gate current density, indicating that trapping effects take place. Therefore, region III is assigned to charge trapping in the oxide. This behavior is not only observed in NH_3 annealed samples but also for $NO + NH_3$ POA (cf. Figure 2.7). Since charge trapping can lead to a permanent degradation of the device it should be avoided. The XPS results presented in [52], which show nitrogen incorporation throughout the whole GOX (Figure 2.3), indicate that N might play a role in the observed behavior. However, these samples presumably also contain large amounts of hydrogen which could be involved. Unfortunately, no information about the hydrogen content of both samples is available so that neither of the two candidates can be proven or excluded.

2.3.3 Possible Origin of Trap Assisted Tunneling

As described in the previous sections, the NH_3 POA leads to an increased GOX leakage in form of TAT. From XPS results presented in [52, 53] it is known that any form of NH_3 containing POA leads to nitrogen incorporation throughout the gate oxide (Figure 2.3). Therefore, the impression arose that nitrogen in SiO_2 might be the origin of TAT in the studied samples. However, as can be seen in Figure 2.7, $NO + NH_3$ does not always lead to TAT even though N is incorporated in variable amounts in the GOX. Therefore, N in the GOX and at the interface can be excluded as the cause of TAT. As a first guess, intrinsic electron traps were suggested as possible trap candidates [124]. At this point, the hypothesis was that NO, which is able to anneal the majority of traps in a-SiO_2 [51], anneals an intrinsic trap band which is not affected by the pure NH_3 POA. This hypothesis was based on the fact that no TAT was observed in samples which received any form of NO POA. The intrinsic electron trap reported in [26] would lie in a suitable energy range. However, lately, indications have been found that this hypothesis is not correct.

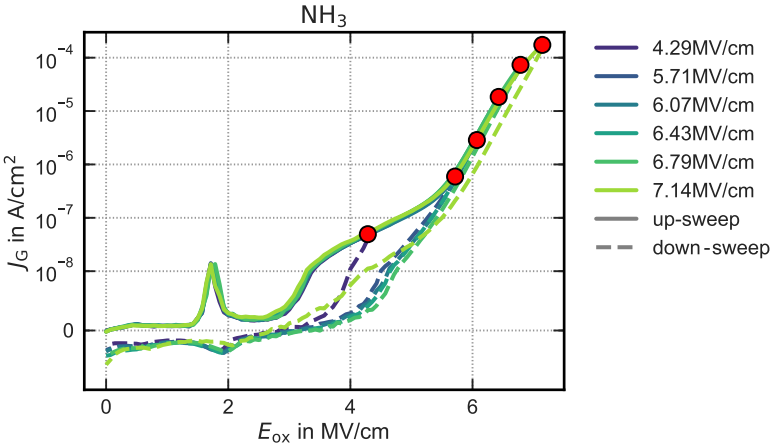


Fig. 2.11 Gate current measurements for several turning points between up- and down-sweep showing hysteresis effects. In the TAT region, a hysteresis between up- and down-sweep is observed. In the FN region, no hysteresis is measured. When region III is entered, an additional hysteresis component can be observed, indicating an additional charge trapping component in the oxide. [124].

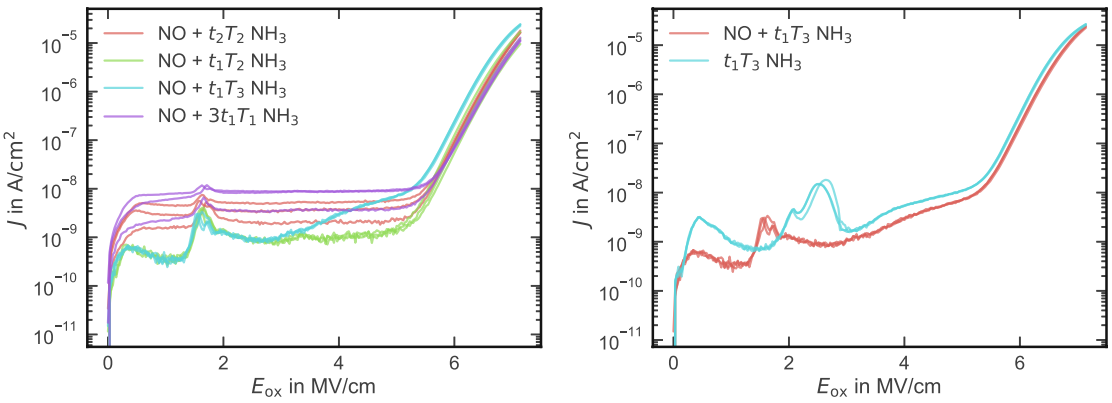
Impact of the Processing Parameters

A study of the gate leakage current for different annealing temperatures and times ($t_2 < t_1$) for the NH_3 and $NO + NH_3$ POA was conducted. For the $NO + NH_3$ POA it was found that a certain threshold in the annealing temperature needs to be exceeded before TAT occurs (Figure 2.12 (a)). The $NO + NH_3$ process presented in Figure 2.7 was annealed below this threshold and is therefore not affected by TAT. Therefore, it is assumed that NH_3 itself leads to the formation of a new trap level in SiO_2 enhancing GOX tunneling. Baumvol [56] mentioned the possibility of the dissociation of NH_3 during the anneal. Therefore, it is assumed that a certain annealing temperature needs to be exceeded to enable the dissociation. This hypothesis so far perfectly matches the experimental observations for the $NO + NH_3$ POA presented here. It is also supported by the observations from the different NH_3 POA parameters in Figure 2.13. All annealing temperatures for this process lie above or equal the temperature at which the first TAT behavior was measured in the $NO + NH_3$ annealed samples. Here, it has been observed that higher annealing temperatures and longer annealing times further enhance TAT. Thus, more NH_3 or its dissociates can react with the interface and the oxide and therefore form more defects. Note that for the same NH_3 annealing temperature and time, pure NH_3 and $NO + NH_3$ POA lead to comparable tunneling characteristics (Figure 2.12 (b)). Since the previous NO anneal for $NO + NH_3$ obviously does not have any impact, this strongly supports the hypothesis that new defects are created by NH_3. Since N-related defects could already be ruled out from the experimental point of view, from the current state of knowledge the creation of hydrogen related defects seems to be the most likely origin of TAT in NH_3 treated oxides.

TAT and Breakdown Mechanism

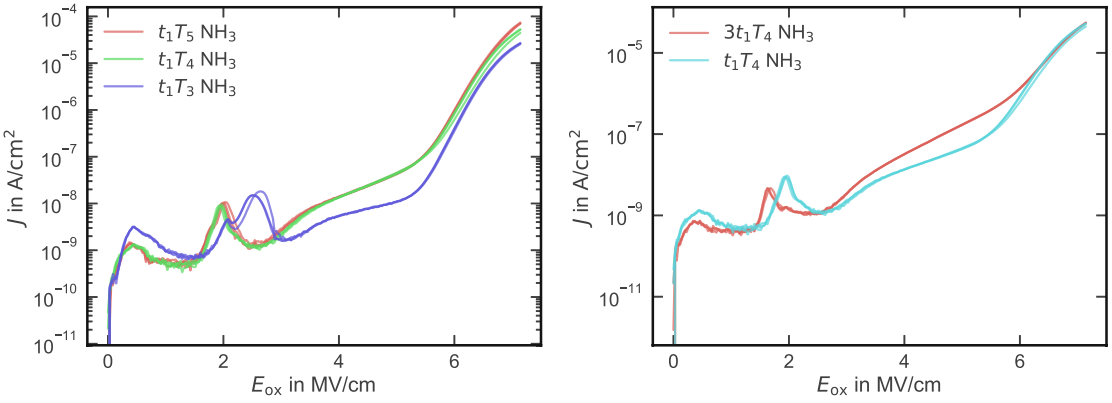
At this point, the question arises which defect causes the observed TAT and breakdown behavior and what the breakdown mechanism in general looks like. Literature shows that

electron injection may enhance the breaking of atomic bonds and by this generate more defects [29, 129]. One hypothesis in order to explain GOX breakdown is electron trapping at stretched Si−O−Si bonds with subsequent trap formation [29, 130, 131] which then facilitates oxide breakdown [29]. According to DFT simulations presented in [29, 130], electrons can trap at precursor sites in amorphous SiO_2. These precursor sites are for example wide O−Si−O bond angles ($> 132°$) [29, 131]. By trapping one electron, $[SiO_4]^-$ is formed, which has deep electron states in the band gap of SiO_2 and further stretches the already elongated bond. Afterwards, another electron can be trapped which stretches the bond length and angle even further. The activation energy to break the bond is therefore significantly reduced, leading to the formation of oxygen vacancies (cf. [29] for a detailed description). The formation of new oxygen vacancies strongly depends on the local strain



(a) NO + NH_3 (b) NH_3 vs. NO + NH_3

Fig. 2.12 GOX tunneling characteristics for (a) different NO + NH_3 POAs and (b) a comparison with a NH_3 anneal with same parameters. TAT only occurs for annealing above a certain threshold temperature and is similar for pure NH_3 and NO + NH_3 POA.



(a) Annealing Temperature (b) Annealing Time

Fig. 2.13 GOX tunneling characteristics for different NH_3 POAs. The TAT current increases with increasing annealing temperature and time.

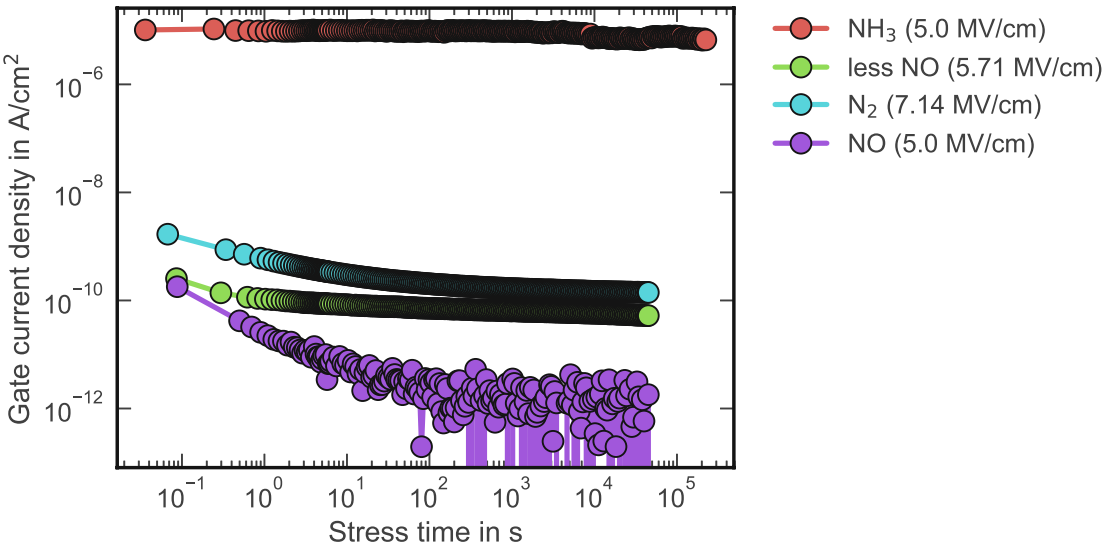
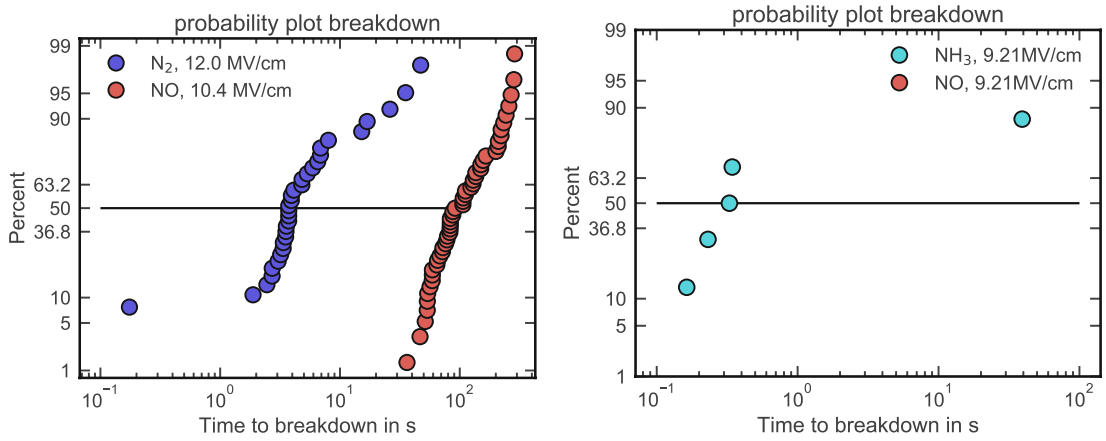


Fig. 2.14 Gate bias stress in the TAT region for various POAs. The stress bias is given in the legend and was adjusted according to the threshold voltage in order to stress with a constant overdrive for all samples. None of the devices breaks during the measurement. The lowest leakage current is observed for the NO annealed device.

[130], which is increased by the trapping mechanism described above and is in general significantly higher at the interface than deeper in the oxide. Additionally, trapping of two electrons in an oxygen vacancy can create additional precursor sites for electron trapping close by. The aggregation of vacancies may strain the surrounding lattice and increase the local electric field, thereby, facilitating the formation of new vacancies [29, 131]. The larger the size of the oxygen vacancy clusters, the more likely new elongated O−Si−O bonds are formed. So, the trapping of two electrons at the created precursor sites may generate new oxygen vacancies and interstitial O^{-2} ions what in turn enhances the formation of further trapping sites. This defect formation mechanism has been suggest to strongly affect the dielectric breakdown of the oxide [130].

As a general hypothesis for breakdown and GOX tunneling, we suggest that NO POA reduces the precursors (elongated Si−O−Si bonds) of the defect formation for the oxide breakdown. In other POAs such as N_2 or NH_3, more precursor states are present, leading to a faster time dependent dielectric breakdown (TDDB) or lower breakdown voltage. Theoretical investigations by our research partners using DFT are still ongoing.

In order to test this hypothesis, TDDB measurements were conducted for NO, N_2 and NH_3 annealed devices. In these experiments, the stress bias was chosen to be 5 MV/cm for the NO reference sample and adjusted for the other samples to a constant threshold voltage overdrive of the stress bias if needed. For this oxide field, TAT can be observed in the NH_3 annealed devices. Figure 2.14 shows the gate current density over time. Even though none of the devices could be stressed to breakdown within reasonable amounts of time, different leakage levels were still observed. Discussing the different POAs in more detail, the NO annealed samples show the lowest leakage current which increases with decreasing NO content during the anneal. N_2 annealed devices lead to a higher leakage



(a) NO vs. N_2 (b) NO vs. NH_3

Fig. 2.15 Probability plot for the time to breakdown of TDDB stress with constant stress bias overdrive with respect to the threshold voltage of each MOSFET. (a) shows NO and N_2 annealed devices stressed with a constant V_{th} overdrive. The legend gives the absolute oxide field. (b) shows NO and NH_3 annealed devices stressed with the same threshold voltage overdrive. The figure contains no data points for NO POA because there was no breakdown observed in the measurement time window for the corresponding devices.

current. In contrast, the highest leakage current, which is constant over time, is measured for the NH_3 annealed device due to the additional TAT component. For all samples besides NH_3, a slight decrease of the gate current with stress time is observed which is especially pronounced in NO. This decrease is most likely caused by a blocking of the defects during the tunneling process. It is not permanent since the decrease in the gate current can be reproduced after bias removal. Additionally, the subthreshold hysteresis before and after the stress phase does not change which means that neither new traps are created nor existing traps disappear. One likely hypothesis is that tunneling takes place via a defect with three different states (cf. 4-state NMP model) of which two represent the charged and neutral state and the third one is a metastable configuration. When electrons tunnel through the oxide, this trap level gets negatively charged. Eventually, it is able to enter the third charge state (also negatively charged) and stays there. As an effect, this trap level cannot be used by other electrons anymore to tunnel through the oxide so that the gate current density decreases over time until it mainly stops in the case of the NO annealed device. In any case, the number of trapped charges is smaller than the measurement accuracy of both the Agilent B1500 and Keithley 2636B SMUs and can therefore not be experimentally determined. Nevertheless, a PBTI drift is observed during the measurements which might be related to the trapping effects mentioned above. The precise configuration of the responsible defect is still under investigation.

In order to better understand the breakdown process itself, the previous TDDB experiment was repeated at higher bias levels. To find suitable and comparable bias conditions, first, breakdown as a function of the threshold voltage overdrive was determined. In this case, the threshold voltage overdrive is chosen instead of the absolute voltage because the devices strongly differ in their amount of oxide charges and therefore, also in their threshold

and breakdown voltages. Then a constant overdrive (approxiamtely same effective oxide field) which results in a stress bias slightly below the breakdown voltage was chosen for a the stress. These measurements can be found in Figure 2.15 (a) for NO and N_2 POA and in Figure 2.15 (b) for NO and NH_3 POA. Note that for the comparison of NO anneal and NH_3 anneal only data points for NH_3 POA are included since NO annealed devices do not break under these bias conditions in the same time frame. As can be seen in both plots, both N_2 and NH_3 annealed MOSFETs break significantly earlier than NO annealed devices. This strongly supports the breakdown hypothesis presented above. At the same time, it shows that NO annealed devices are the most robust with respect to GOX breakdown among the presented process variants likely due to a lower number of precursor sites for breakdown, i.e. the elongated Si−O−Si bond angle.

2.4 Comparison of Different Oxidation Techniques

The channel mobility in MOSFETs is limited by scattering mechanisms such as surface roughness (cf. Section 1.3.4). Scattering at the interface is strongly influenced by the interface quality which in turn may be affected by the oxidation technique. In Si technology, several publications about plasma-enhanced oxidation can be found (cf. the review in [132]). Plasma-enhanced oxidation enables the controlled growth of thin and high-quality SiO_2 films at low temperatures [132], at least for Si. There, similar oxide properties compared to thermal oxidation are found [132]. In special applications, a lower surface roughness and therefore mobility improvement, which however strongly depends on the plasma oxidation conditions, is observed [132]. The oxidation is thought to be caused by O^- [133]. In SiC technology, plasma-enhanced oxidation seems to be a barely studied technique. Goelz *et al.* [134] presented p-type 6H-SiC MOSCAPs with plasma-grown oxides in 1997. They demonstrated that SiC can be oxidized in plasma and claim to have found differences in the bonding chemistry at the interface. According to their results, no C−O bonds are formed during plasma-enhanced oxidation in contrast to thermal oxidation. Furthermore, they expect the resulting oxide to suffer from less strain-induced interface defects due to a lower SiC consumption during the oxidation [134]. Since the realization of an improved interface seems possible when using plasma enhanced oxidation, in this thesis, the trap density and the device performance of MOS devices with a thermally grown oxide (n-MOSCAP), plasma grown oxide (plasma oxide (PGOX), n-MOSCAP and trench MOSFET) and deposited oxide (TEOS CVD, trench MOSFET) were studied. Since thermal oxidation is technically not possible in the trench technology, lateral MOSCAPs have been used for this study.

The MOSCAPs were processed on commercial n-type 4H-SiC (0001) wafers with 4° off-axis on which an n-type epitaxial layer was grown. The surface of this layer was either oxidized thermally or in a plasma, resulting in an oxide thickness around 3-5 nm. The MOSFETs were fabricated using standard industrial processes. The GOX deposition of the CVD oxide also followed a standardized process. For the plasma oxidation, first a few nanometers of PGOX were grown directly at the interface. Afterwards, a CVD oxide was deposited on top to increase the oxide thickness to the same level as for the deposited oxide. A considerable advantage of PGOX is that it can be homogeneously grown in trenches. In contrast, thermal oxidation can only be applied to lateral structures because the trench would oxidize inhomogeneously. For all oxide variants, different POAs were tested, namely no POA, N_2, NH_3 and NO POA or oxidation in NO. This analysis will focus on the unannealed oxides for the MOSCAPs and the NO annealed MOSFETs. The

unannealed oxide gives larger trap signals in TDRC which are easier to measure. However, for the study of the MOSFETs, NO annealed devices were chosen because the N_2 POA leads to barely working devices and can therefore not be properly investigated.

2.4.1 Comparison of Plasma-Grown Oxide and Thermal Oxide

Figure 2.16 shows the CV curves of the MOSCAPs with PGOX and thermal oxide. The curves were obtained for a fixed frequency of 10 kHz, conducting a sweep from depletion to accumulation and backwards. The curves are normalized to the accumulation capacity for better comparison. It can already be seen at a first glance that the differently oxidized devices behave very similarly. The two not annealed samples result in CV curves lying on top of each other, only very slightly parallely shifted. A parallel shift results from fixed oxide charges. Both, the thermally oxidized and the PGOX sample show similar hysteresis between up- and down-sweep. Additionally, both processes result in large differences between the first and the second up-sweep, indicating the presence of a large number of traps. The NO annealed process variants lead to very similar CV curves as well. The NO POA in general led to a reduction of the "threshold voltage" and the hysteresis. Additionally, the slope of the annealed devices is larger than that of the not annealed ones. Therefore, presumably both, oxide charges and interface states were reduced by the NO POA. Overall, the different oxides can be barely distinguished from each other with regard to CV curves.

Second, the breakdown behavior of the different oxides was studied (Figure 2.17). The curves end at the point of GOX breakdown or at the current compliance which was set to $I_G = 1\,\text{mA}$. Again, all samples behave very similar regardless of their type of oxide, resulting in very similar breakdown voltages. Considering device to device variation and that only one sample for each process is shown, it can be assumed that thermal oxides and PGOXs have roughly the same breakdown field at least for thin oxides. Surprisingly, breakdown far exceeds the theoretical breakdown field of around 10 MV/cm in SiO_2 given in textbooks (note that sometimes higher fields might also be reported in literature). Here, breakdown was observed slightly below 20 V for an oxide thickness of 3-5 nm. This can be explained with more tunneling before breakdown compared to thick oxides, reducing the effective oxide field.

Finally, the trap density of the PGOX and thermally grown oxide without POA were compared with TDRC measurements. For the NO annealed samples, the current signal was too small to achieve reliable, noise-free results. The basic measurement principle of TDRC can be found in Section 1.5.4. Here, the MOSCAPs were charged in full accumulation with $V_{ch} = 4\,\text{V}$ in order to attract electrons to the interface. The discharging voltages were either $-1\,\text{V}, +1\,\text{V}$ or $+2\,\text{V}$. For positive discharging voltages, it is possible to detect NITs in addition to interface traps [20, 135] and therefore, to determine the different trap types (cf. Section 1.5.4). The signal obtained by NITs shows a different dependence on the discharging voltage compared to interface states. Figure 2.18 (a) shows the TDRC trap densities as a function of the effective trap energy. Both oxides suffer from one broad trap level with a trap density of around $10^{13}\,\text{cm}^{-2}\text{eV}^{-1}$. In previous studies [135], trap levels in this region were identified as NITs due to the change of the measurement signal for different discharging voltages as was described above. However, the same TDRC spectrum is obtained for positive and negative discharging biases, as can be seen in Figure 2.18 (b). Commonly, a small positive discharging bias in TDRC leads to an increased signal of NITs. According to Krieger *et al.* [20], this is due to the fact that for discharging in depletion their

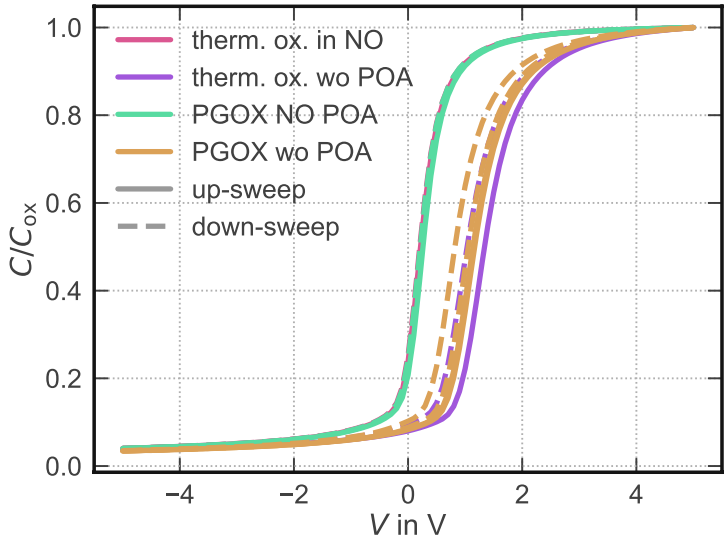


Fig. 2.16 CV characteristics of MOSCAPs with different oxides. Devices with different oxides but identical POAs have comparable CV curves. The curves were measured on devices from identical positions on the different wafers.

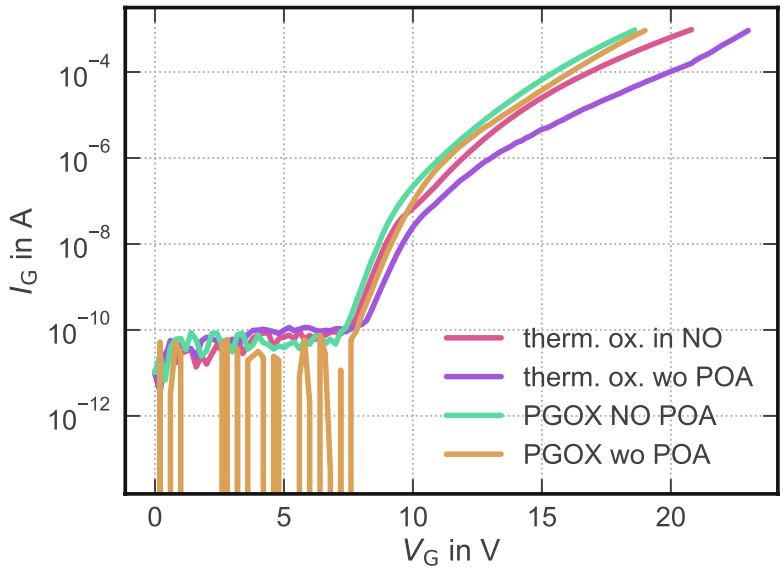
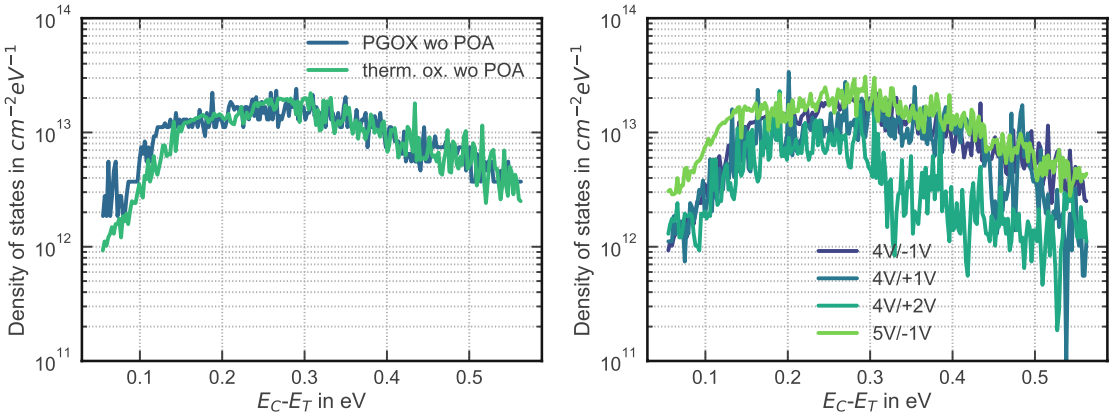


Fig. 2.17 Gate current characteristics of MOSCAPs with different oxides. The curves end at breakdown (current limit or sudden breakdown). All devices break at similar voltages.

trapped charges can directly tunnel in the conduction band which is independent of the temperature and too fast to be conveniently detected. For small positive discharging biases, however, they suggest that NITs also have to at least partially emit their trapped charges thermally as is the case for interface states, leading to an increased signal [20]. Thus, NITs are only partly detectable with TDRC and therefore, cannot be counted reliably. In total, it cannot be said for sure if the detected peak belongs to NIT or interface traps. Comparing



(a) Process Variations

(b) Parameter Variations (thermal oxide without POA)

Fig. 2.18 Defect density as a function of the apparent trap activation energy measured with TDRC. (a) Thermal oxide and PGOX without POA, respectively, have the same trap densities. (b) Parameter variations for a thermal oxide without POA. The first number gives the charging voltage, the second number the discharging voltage. No change of the signal is observed for the different measurement parameters.

the results to existing literature [135], NITs are likely to cause the signal. However, these trap levels lie approximately 2 nm away from the interface in the oxide which is in our case the middle or the top of our oxide. Therefore, there is the possibility that the oxide is too thin to contain any NITs.

In summary, MOSCAPs with an oxide grown by a plasma process show similar behavior as devices which were thermally oxidized. In the CV characteristics both oxides have nearly identical curves within the measurement accuracy. The breakdown behavior is also the same. Finally, interface states were studied with TDRC resulting in the same trap distributions with identical trap densities. Therefore, it can be concluded that at least in the selection of experiments studied here, plasma-grown oxides and thermal oxides lead to equivalent interfaces.

2.4.2 Performance of MOSFETs with Deposited and Plasma-Grown Oxides

Since in trench technology no thermal oxidation can be used due to inhomogeneous oxidation along the trench, possible differences of deposited oxides compared to plasma-grown oxides are of greater interest. Plasma oxidation leads to very thin oxides which cannot be used for power MOSFETs. Therefore, in addition, TEOS is deposited on top of the PGOX in order to reach the final oxide thickness. In this case, only the device performance and hysteresis effects were studied. Figure 2.19 shows the transfer characteristics for the different oxide types with either NO or N_2 POA, respectively. Within the measurement accuracy and device to device variation, very similar I_D-V_G characteristics are measured with comparable threshold voltages. This already indicates that PGOX neither leads to a significant improvement of the channel nor to a significant degradation. When comparing

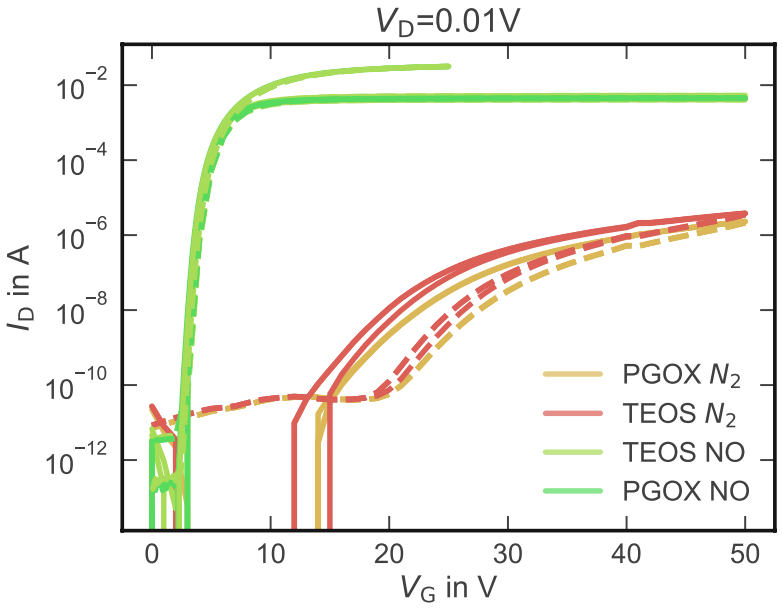


Fig. 2.19 Transfer characteristics of trench MOSFETs with PGOX or deposited oxide. MOSFETs with the same POA result in similar transfer characteristics. The differences in the "saturation" current of the NO annealed samples can be ignored since they result from different parasitic series resistances from the measurement system, limiting the maximum current (2-point measurement).

the subthreshold sweep hysteresis of an NO annealed PGOX with an NO annealed TEOS, both variants result in the same hysteresis within the normal device to device variations. Therefore, in total, the different interface due to plasma oxidation does not lead to any significant improvement of these parameters relevant for the device performance. Nevertheless, note that the effect of the POA might have eliminated possible differences caused by the oxide growth process. At least with regard to the device performance, PGOX and TEOS seem to be equivalent. Note that no information about the device reliability (e.g. BTI, TDDB, GOX breakdown) is available. Since thermal oxides and PGOX were also equivalent for the MOSCAPs, it is concluded that thermal oxides, plasma-grown oxides and TEOS result in similar oxide quality. This result on one hand contradicts the observations for p-type 6H-SiC/SiO_2 presented in [134] who claim to have observed a different interface chemistry for plasma-enhanced oxides compared to thermal oxides. On the other hand, the observations presented here are in good agreement with previous studies on plasma-enhanced Si/SiO_2-interfaces where in most cases also, according to the review provided by Taylor *et al.* [132], no differences were found. Even though no improvement could be achieved with the new technique this result is nevertheless of great importance for any kind of simulations including oxide material parameters. Often, parameters determined for thermal oxides are used and the simulation results are transferred to different oxides without knowing if the results are applicable. This study indicates that simulations from different oxide types should be comparable.

2.5 Summary and Conclusion

Much research is currently done on improving the interface quality and the performance of MOS devices. Part of this research focuses on improved POA techniques. Here, annealing in NH_3 and an anneal in $NO + NH_3$ were presented and compared to the common NO anneal. Even though an improved device performance could be achieved, some drawbacks with regard to the device reliability were found, namely increased BTI and reduced GOX reliability. Furthermore, it was found that NH_3 containing POAs might suffer from TAT depending on the annealing conditions. The mechanism and the origin of TAT was studied and explained linking DFT calculations from the literature with experimental results. NH_3 POA at high temperatures likely leads to the formation of hydrogen related defects which offer additional pathways for an increased TAT current. Furthermore, the GOX breakdown hypothesis presented in [29] and [130] combined with our hypothesis that NO POA reduces precursor sites enabling TAT and leading to GOX breakdown was experimentally proven.

Last but not least, plasma-enhanced oxidation was compared to conventional thermal oxidation and deposited CVD oxides. The performance and interface state density of the resulting devices was studied, which were barely distinguishable from each other. Note that no study of the device reliability was performed. As a consequence of the similar performance of the MOSFETs with different oxides, it was concluded that PGOX, thermal oxide and deposited oxides lead to devices with comparable properties, at least with regard to transfer characteristics and hysteresis effects.

CHAPTER 3

Bias Temperature Instability in SiC Power MOSFETs

Contents

3.1 Introduction and Motivation

As described in Section 1.3.6, BTI is a serious reliability concern in power MOSFETs regardless of the particular technology. It occurs under positive and negative gate bias and temperature stress during which charge carriers are trapped at or near the interface, leading to threshold voltage drifts. Because of this drift, the operating point changes at constant bias conditions. As a consequence, an increased on-resistance, decreased device efficiency, increased leakage currents and other undesirable effects [63, 65, 66] may occur. BTI can be observed under both, direct current (DC) bias and alternating current (AC) bias stress. In industrial standards such as JEDEC [92] or comparable automotive standards [93] only DC stress is covered. Even though AC stress is much more application relevant, normally only DC drifts are characterized and published.

BTI in general is an intensively studied reliability topic in Si as well as SiC technology. Even though it has been studied for decades on Si MOS structures, no generally accepted physical model exists and the underlying mechanism is still heavily debated [69, 70]. Over the years, several mathematical approaches to predict the drift of Si MOSFETs have been developed (cf. Section 1.3.6). In contrast, BTI in SiC has only been studied for the last decade [76] and in many cases significantly higher drifts are reported compared to what is observed for Si technology (cf. [65] for example). Already in the late 90$^{\text{th}}$, Afanasev *et al.* [24] reported that similar trap levels may exist in SiC and Si MOS structures. In addition, recent studies also indicate the same origin of bias temperature instability for Si and SiC based devices [77]. Nevertheless, so far no direct comparison between SiC and Si power MOSFETs has been presented.

In this chapter, a direct comparison of mainly PBTI in SiC trench MOSFETs and Si superjunction MOSFETs will be presented [17], using measurement methods as described in Section 1.5.3. Additionally, different fitting methods have been tested and a physical model derived in order to explain the similarities and differences in both technologies. Finally, a benchmarking study comparing the main SiC MOSFET manufacturers will be shown.

3.2 Comparison of BTI in SiC and Si Power MOSFETs

3.2.1 Studied Devices

For the direct comparison of BTI in SiC and Si power MOSFETs, SiC trench MOSFETs as shown in Figure 1.3 (b) and commercially available Si superjunction MOSFETs as shown in Figure 3.1 were studied. Both devices have thick SiO_2 as gate oxide with comparable oxide thicknesses larger than 50 nm. Since in SiC devices as-oxidized GOX lead to barely working MOSFETs due to a higher trap density, different POAs were applied and the resulting BTI behavior studied. The processes differ in the annealing ambient, temperature and time. In the following, the different POAs will be referred to as $SiC_{(A)}$, $SiC_{(B)}$ and $SiC_{(C)}$.

The BTI measurements were conducted using different stress biases, temperatures and times and compared to each other. Most stress parameters are significantly higher than the range the test structures were designed for. Because of a higher interface state density in SiC, the readout timing is here even more crucial as for Si devices. In order to minimize the impact of the readout timing, i.e. delays between stress and readout, and of the device history, a preconditioning pattern with preconditioning pulses of ±15 V were used, as

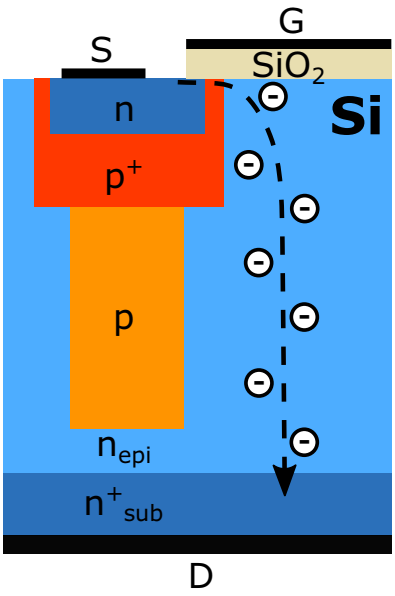


Fig. 3.1 Schematic cross-section of the studied Si power MOSFETs.

described in Section 1.5.3 and depicted in Figure 1.13. The readout was performed in gated diode configuration with 1 mA as current criterion for the threshold voltage for both technologies.

3.2.2 Negative Bias Temperature Instability

Figure 3.2 shows the time evolution of the absolute threshold voltage drift for NBTI gate bias stress with −25 V at 200° C. Note that the Si device has a negative drift whereas the SiC devices have positive drifts. The latter might be an indication for ion transportation during stress (ion drift oppositely to the regular drift), however, this is at least in the case of $SiC_{(B)}$ and $SiC_{(C)}$ not crucial since the drift level is in general very low.

The measurement results show that the NBTI drift is strongly influenced by device processing. By improving the POA, a reduction of the drift level by one order of magnitude could be achieved resulting in a drift level which is at least for moderate stress times similar to the one of the studied Si devices.

Additionally, the experimental data were fitted with the empirical power law time evolution model as described in Section 1.3.6. The fit with the resulting power law exponents n is also indicated in Figure 3.2 and additionally in Figure 3.6 (a). The empirical fitting approach can conveniently model the drift behavior for short stress times. The fact that lower power law exponents are extracted for SiC than for Si with similar absolute drift levels further supports the impression that lower or at least similar drifts can be expected for the improved SiC samples $SiC_{(B)}$ and $SiC_{(C)}$. With regard to the fact that older publications [65] showed significantly higher drifts for SiC than what was common for Si at that time, the drift reduction is already very satisfying. Therefore, NBTI is for the moment being of rather low interest. In addition, note that most SiC power MOSFETs are designed to operate between roughly −5 V and 20 V, depending on the manufacturer,

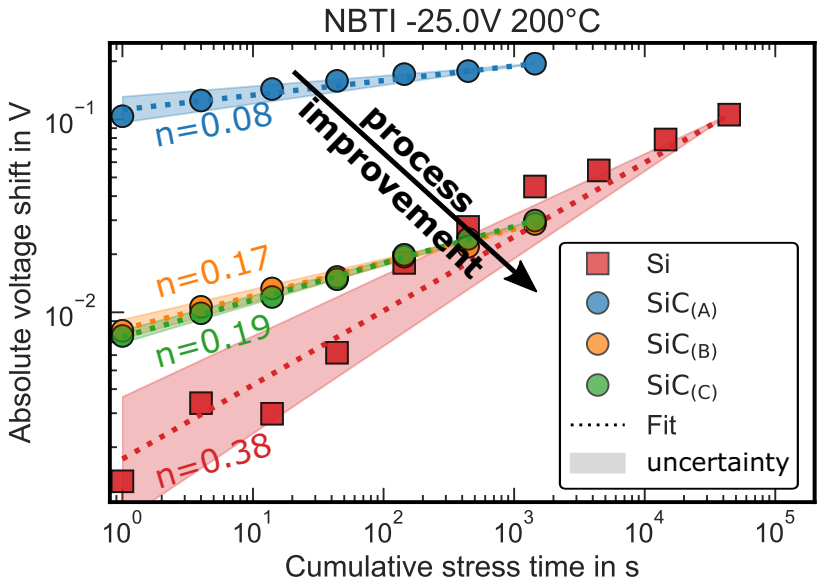


Fig. 3.2 Absolute NBTI drift as a function of the cumulative stress time. The markers represent the measurement data, the dotted lines the power law fit with the power law exponent n. The bands represent the uncertainty of the fit. Improved device processing resulted in similar NBTI drifts as for the Si device. Note that the Si sample presented here has a negative drift whereas the SiC samples show a positive drift. Modified from [17].

so that in the application even lower drifts will be observed. Therefore, the rest of the analysis will focus on PBTI. [17]

3.2.3 Positive Bias Temperature Instability

Time Evolution

Figure 3.3 shows the time evolution of a PBTI stress with +25 V at 200°C. All devices drift towards higher threshold voltages. With increasing stress times, traps with long capture time constants can trap charges from the channel, increasing the total drift. It can already be seen at a first glance that regardless of the semiconductor technology tested, the measurement curves are mainly parallely shifted along the drift axis. This means that SiC and Si power MOSFETs show the same time evolution with regard to PBTS. This impression is supported by the results of power law fitting, which will be presented in the next section.

As was already shown for NBTI, PBTI drift can also be significantly reduced by optimized POA. Here, a reduction by a factor 10 from $SiC_{(A)}$ to $SiC_{(B)}$ and $SiC_{(C)}$ has been achieved. Therefore, these changes in processing affect both NBTI and PBTI drift. Unfortunately, the resulting PBTI drift level for $SiC_{(B)}$ and $SiC_{(C)}$ is still around 8 times higher than drifts extracted for comparable Si MOSFETs. Therefore, with regard to the time evolution, it can be said that SiC and Si power MOSFETs show the same degradation with stress time but different absolute voltage drift values. Nevertheless, already a significant reduction of

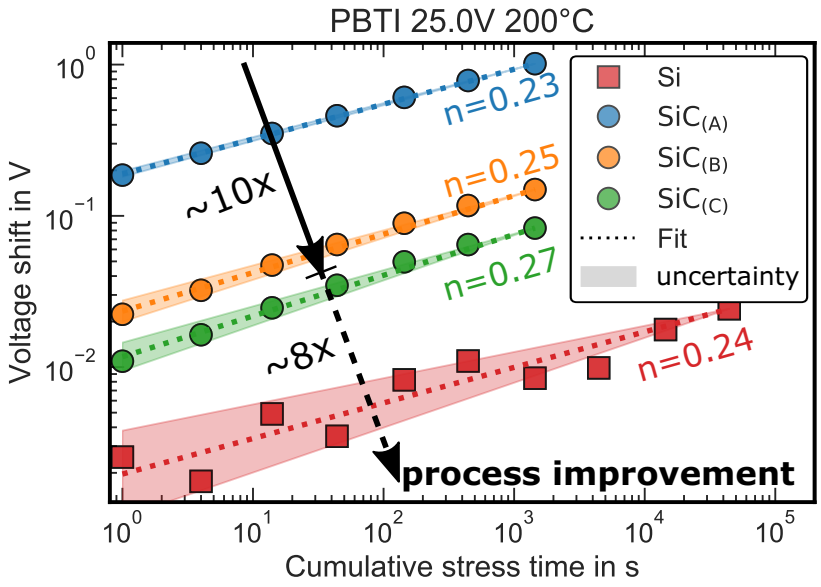


Fig. 3.3 PBTI drift as a function of the cumulative stress time. The markers represent the measurement data, the dotted lines a simple power law fit with the power law exponent n. Depending on the SiC oxide treatment, a significant reduction of the drift can be achieved. However, still higher drifts than for Si devices are observed. Modified from [17].

the drift has been achieved by improved device processing. Therefore, a further reduction of the drift for SiC by using more efficient POA techniques in the future appears realistic. [17]

Stress Bias Dependence

Furthermore, the dependence of PBTI on the stress bias was studied. Figure 3.4 shows the voltage acceleration for different stress biases measured at 200°C. As was already the case for the time evolution, again a similar correlation is found for SiC and Si MOSFETs. For higher stress voltages a larger drift can be observed. Because of the higher bias, a larger active energy region is available which might therefore provide access to more trap states in the oxide or at the interface. The curves are once more mainly parallely shifted along the drift axis showing a similar voltage acceleration. This is again supported by power law fitting (Section 3.3.1). Overall, the same voltage acceleration was observed for both technologies as will be shown later (Figure 3.6 (b)). [17]

Temperature Dependence

Last but not least, the temperature dependence of the PBTI drift was investigated (Figure 3.5) resulting from a 1.4 ks cumulated stress in the case of SiC and 44 ks in the case of Si with 25 V, respectively. For the Si devices, longer stress times needed to be chosen in order to provoke larger drifts and therefore a better SNR. Note that the PBTI drift for the Si MOSFETs is very low and for this reason difficult to extract for short stress

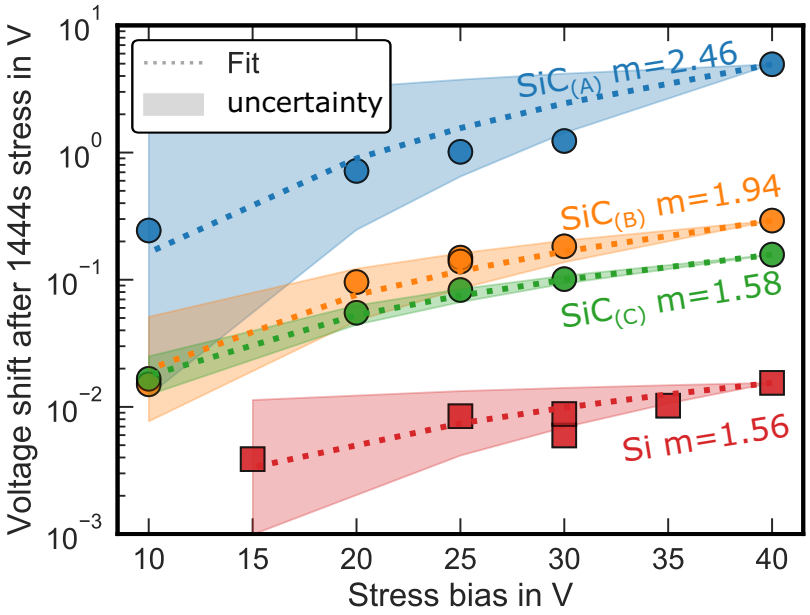


Fig. 3.4 PBTI drift as a function of the stress bias, extracted after a cumulated stress time of 1.4 ks at 200°C. All devices show a similar voltage acceleration. Modified from [17].

times and low stress voltages. In order to compare the results, the obtained drift values were normalized to the drift extracted at 200°C. All devices show a higher drift at higher temperatures. At 30°C all MOSFETs regardless of the technology drift 15-20% of the drift at 200°C. At 100°C and 150°C, the Si devices seem to drift a little bit less than SiC but then show a slightly larger increase of the drift with the temperature. This might result either from the longer stress times or from the very low drift of the Si MOSFETs leading to larger uncertainties in the extracted drifts. In addition, note the small number of studied devices. Therefore, it is nevertheless concluded that SiC and Si power MOSFETs show at least a similar temperature acceleration even though it might not be exactly the same. [17]

Summarizing the overall experimental observations, many similarities were identified for the PBTI drift of SiC and Si power MOSFETs. First of all, the same time evolution was observed. Additionally, the same voltage acceleration and a similar temperature dependence was found. However, both technologies result in different absolute voltage shifts, i.e. mainly an offset along the drift axis. For this reason, the impression arose that the same trap level in SiO_2, which would be most likely intrinsic ([68, 136], cf. [27] for details on intrinsic traps) might be causing PBTI in both semiconductor technologies. This hypothesis will be discussed in more detail in Section 3.4.

3.3 Modeling of Positive Bias Temperature Instability

For applications, the drift during the lifetime is of fundamental importance. Therefore, several different methods have been developed in order to extract the end-of-life drift. Details about the different methods are provided in Section 1.3.6. These methods were

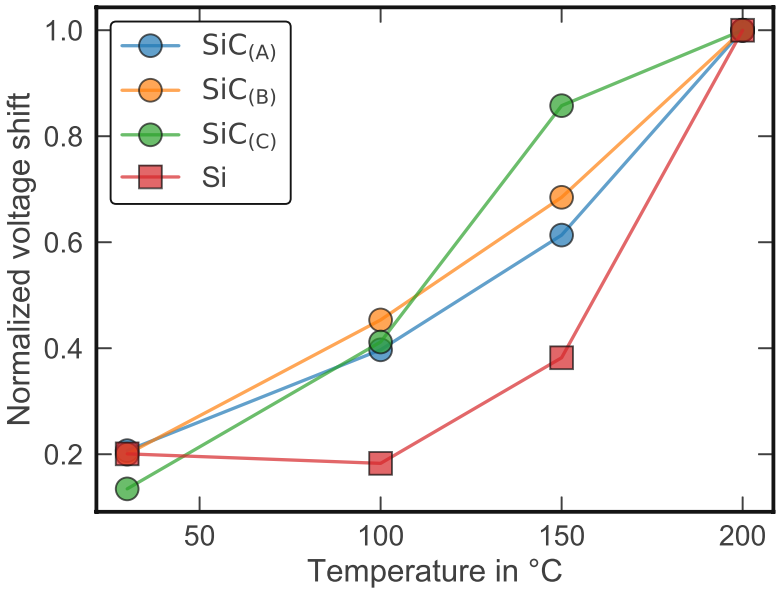
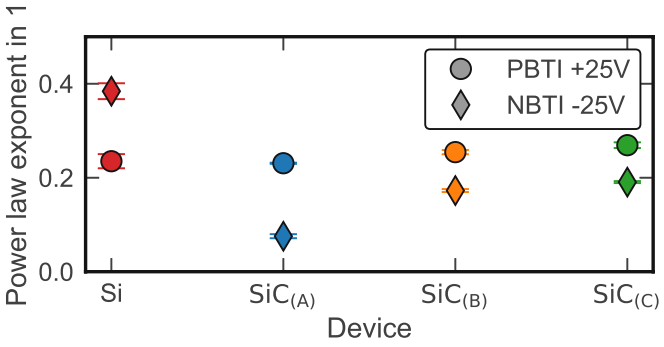


Fig. 3.5 Normalized voltage shift as a function of the temperature, stressed with a stress bias of 25 V for 1.4 ks (SiC) or 44 ks (Si). The values are normalized to the drift at 200°C. [17]

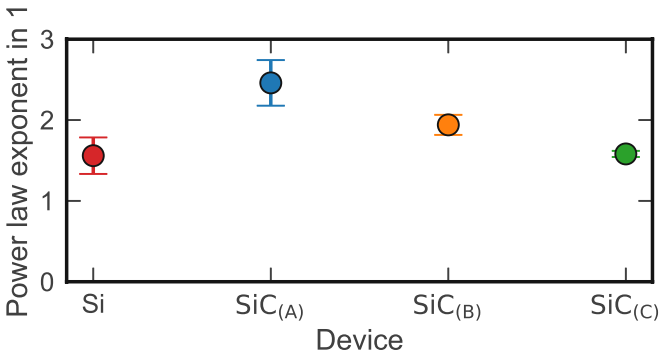
developed for Si technology. Here, the empirical power law and a more physical thermal activation model will be applied to the previously presented measurement data and the characteristic model parameters will be extracted. It will be shown that these models also apply for SiC.

3.3.1 Power Law

The simple power law approach [78] as described in the introduction is an empirical approach to determine an estimated value for the end-of-life drift in BTI. This model lacks any physical background but is nevertheless still used because of its simplicity. The previously presented measurement data from Figure 3.2, Figure 3.3 and Figure 3.4 were modeled with the simple power law approaches for the time evolution and the voltage acceleration. As can be seen in all three plots, very convenient fit results can be obtained for short stress times for both technologies, proving that this model developed on Si devices can also be applied to SiC. The extracted power law exponents can be found in Figure 3.6. For the time evolution of NBTI, similar values for the SiC samples are extracted. The Si sample shows a slightly higher power law exponent but in total a lower drift level. Since already at the end of the measurement window an intersection of the best SiC curves with the Si device is observed, the power law time evolution model predicts lower end-of-life drifts for these SiC samples than for Si. Nevertheless, note that this model is purely empirical and does not account for saturation effects which must show up at some point. Since it is not clear where the saturation starts for the different processes it cannot be predicted for sure which of the processes results in the larger end-of-life NBTI drift. In contrast, for the PBTI time evolution very similar power law exponents were extracted for both technologies. The extracted parameters lie in the range 0.23 to 0.27 which is in the typical range reported for Si devices ($0.1 < n < 0.25$) [78].



(a) Time Evolution



(b) Voltage Acceleration

Fig. 3.6 Power law exponent for (a) the time evolution of NBTI and PBTI and (b) the voltage acceleration of PBTI in SiC and Si power MOSFETs. The error bars represent the fitting error. For all devices, similar exponents are obtained which means that a similar degradation with the stress time and stress bias is observed.

Additionally, the power law voltage acceleration model was used to extract the voltage power law exponents. Here, the fitting was not as accurate as for the time evolution but still very reasonable. The resulting power law exponents shown in Figure 3.6 (b) are very similar when considering the fitting errors. Therefore, it can be concluded that the empirical power law model can also be applied to SiC technology. Furthermore, the similar parameters extracted for PBTI indicate that both technologies might be governed by the same trap type. [17]

3.3.2 Thermal Activation Model

A more physical model to approach the measured data is a thermal activation model described in detail in Section 1.3.6, as suggested in [80]. This model assumes the activation energy of a trap band to be normally-distributed with a mean activation energy E_A and a standard deviation (width of the distribution) σ. In order to accurately capture the Arrhenius laws underlying the model, measurements at different temperatures are needed. For SiC, experimental data obtained for a stress with 25 V at 30°C, 100°C, 150°C and 200°C were used and the activation energy was provided as a fixed value of $E_A = 0.9\,\text{eV}$.

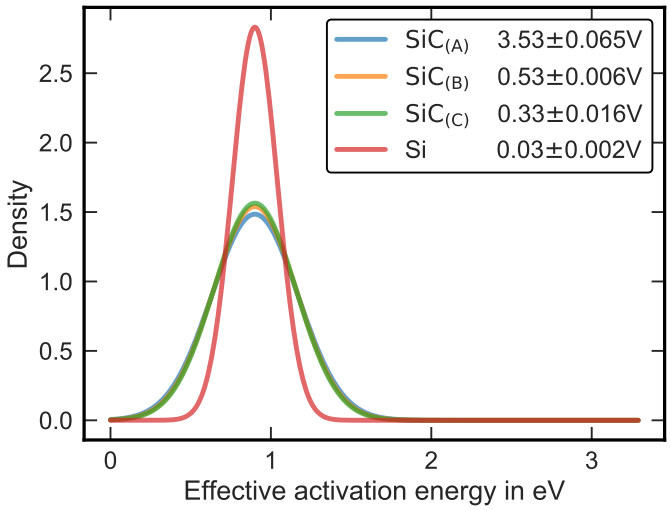


Fig. 3.7 Normal distribution of the effective activation energy obtained by fitting of the PBTI measurements at different temperatures. SiC samples were stressed with 25 V and the Si samples with 40 V in order to get higher drifts for more accurate fitting results. A fixed $E_A = 0.9\,\text{eV}$ was assumed and the maximum voltage drift extracted (see legend). [17]

For Si, the same temperatures were chosen but for a stress bias of 40 V. Smaller gate biases result in too low drifts which could not be fitted accurately. Since the impression arose that PBTI in both technologies might be caused by the same trap type, the same activation energy as for the Si samples was chosen. The measurement data were fitted to Equation (1.9), resulting in sufficient fitting accuracy, especially regarding the fact that the simulations were conducted with a rough estimate for the mean activation energy. Figure 3.7 shows the resulting normal distributions of the activation energies obtained by the fitting. In addition, the maximum voltage shifts, i.e. the end-of-life drift for all trap levels filled, is given in the legend. These drifts are based on physical models (cf. [80] for details) and therefore most likely give more accurate estimates for the maximum threshold voltage drift. Comparing the end-of-life drift of $SiC_{(C)}$ (330 meV) and Si with 30 meV, roughly the same offset by a factor 10 is observed as in the experimental data. With regard to the drift values from the experiments, the extracted maximum drifts are only a little higher. This either suggests that the measured curves should soon saturate for longer stress times (roughly around 10^6 s) or that the model tends to underestimate the total drift. Due to the limited measurement time, this cannot be tested.

In total, the experimental data for SiC and Si power MOSFETs can be conveniently modeled with the same mean trap activation energy E_A. This strongly indicates together with all the similarities found in the experimental study that a trap band in SiO_2, which is the same in both technologies and therefore most likely intrinsic, might be responsible for the obtained PBTI results. [17]

3.4 On the Origin of Similarities and Differences of PBTI in SiC and Si Power MOSFETs

In the previous section, a direct comparison of PBTI in SiC and Si MOS devices was presented. Thereby, it was found that both technologies show the same time evolution, the same voltage acceleration and a similar temperature dependence but different absolute drift values. For this reason, the impression arose that PBTI in both technologies might be caused by a common origin. Since BTI is caused by trapping at the interface or in the oxide and since the interface is quite different for SiC/SiO_2 and Si/SiO_2, this trap band is most likely an oxide trap in SiO_2. Because of the fact that it seems to be present in both technologies, it is suggested that this band is intrinsic (cf. e.g. [27] for intrinsic trap levels in SiO_2).

Already in the late nineties, Afanasev *et al.* [24] reported in a different context that the same trap bands exist in SiO_2 for different technologies (SiC, Si) which, however, affect the devices differently because of different offsets between the conduction band minimum and the trap band. Also recently, Schleich *et al.* [77] observed by the fitting of BTI trap bands on lateral 4H-SiC MOSFETs that similar trap distributions resulted for SiC as have been previously published for Si [136].

Therefore, combining the observations presented here with those from literature, the hypothesis is formed that an intrinsic trap band in SiO_2 exists in both, SiC and Si technology, which is accessible in both materials. Nevertheless, SiC and Si differ in their band structure, i.e. the Si conduction band minimum lies 450 meV below the conduction band minimum of SiC. Thus, different active energy regions result during stress. As shown in Figure 3.8, SiC and Si have a different overlap of their active energy region with the trap band during the stress measurements. Because of the higher conduction band minimum of SiC it is easier to fill this trap band than for Si, resulting in higher absolute drifts but with a similar dependence on the stress parameters.

In order to test this hypothesis, the impact of the position of the conduction band minimum relative to the trap band on the resulting PBTI drift was studied. Since it is impossible to experimentally produce drift values for material systems with identical

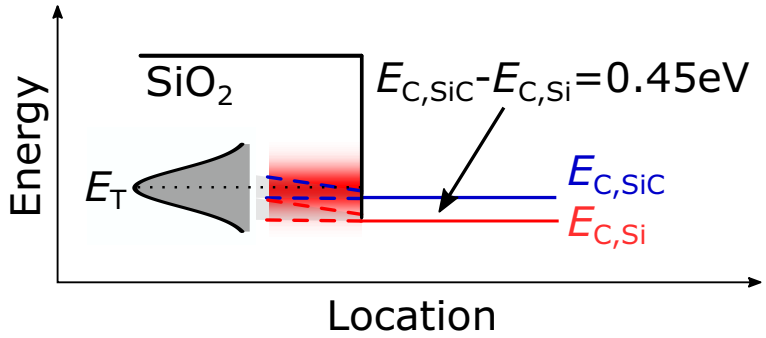


Fig. 3.8 Band diagram for SiC and Si MOS structures illustrating the hypothesis to explain the similarities and differences found in PBTI. Both technologies are affected from the same trap band in SiO_2. Because of the different conduction band minima leading to different offsets between conduction band and trap band, the trap band can be filled more easily in SiC than in Si.

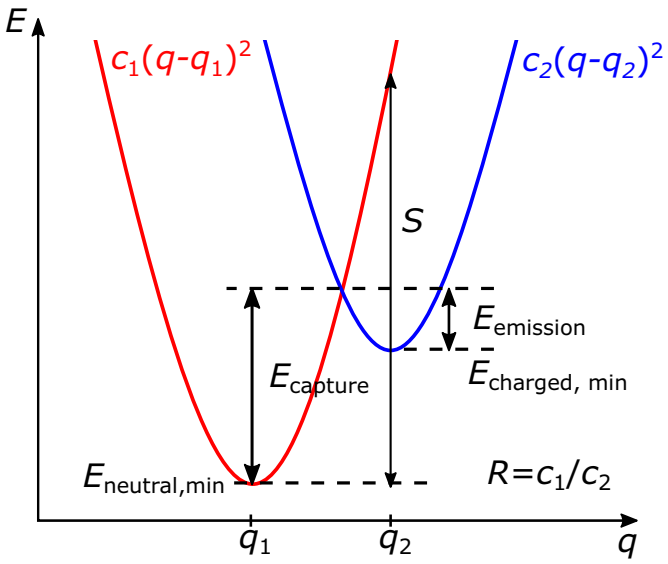


Fig. 3.9 2-state NMP model used in Comphy illustrating the trap band parameters specified in the simulator. [17]

properties (same threshold voltage, surface potential etc.) with only a different but defined offset between trap and conduction band, the 1D simulator Comphy [136–138] was used in order to simulate the PBTI drifts needed and to test the presented hypothesis.

Simulation Setup with Comphy

A more accurate way to model BTI drifts than the analytical expressions used so far is provided by the 1D simulator Comphy [136–138]. Comphy is based on an effective 2-state NMP model as described in Section 1.4. It calculates transient threshold voltage shifts based on charge capture and emission processes for given, pre-existing trap bands in the oxide. As an input, Comphy receives a set of trap bands, material and device parameters and the voltage sequence to simulate the BTI stress. For the given voltages, trap occupations and resulting voltage shifts are determined, using the 2-state NMP model and the relations derived in [68]. A first set of trap bands for BTI on lateral 4H-SiC MOSFETs has been extracted recently by Schleich *et al.* [77]. There, a fast and a slow electron trap band were identified. It has also been shown that at least for PBTI at room temperature, this set of traps can also describe the BTI drifts in trench MOSFETs.

For the study conducted here, Comphy was roughly calibrated to the device parameters of the trench technology. The BTI degradation was calculated for a measure-stress-measure (MSM) sequence using the slightly modified slow trap band from [77] as a basis. Only the slow trap band was used in order to address the same traps as in the preconditioned BTI measurements presented in the previous chapter. Note that preconditioning minimizes the fast BTI component, i.e. the influence of the fast trap band. In order to get a broader trap distribution the width of the activation energy distribution was slightly increased. The trap band parameters are given in Table 3.1. The 2-state NMP model and the meaning of the trap band parameters are illustrated in Figure 3.9. In order to test the above mentioned hypothesis and to study the influence of the location of the conduction band minimum

relative to the trap level on the PBTI drift, two different configurations were simulated: First, a SiC/SiO_2 system with the trap band "as-is" from literature; second, a SiC/SiO_2 system with trap band shifted up by 450 meV. This is based on the hypothesis that the lower conduction band minimum of Si with $E_{C,SiC} - E_{C,Si} = 450\,meV$ makes trapping more difficult in the same trap level compared to SiC. For both configurations different stress biases and temperatures similar as in the experiments were used. The recovery bias was chosen to be 4 V which is close to the devices' threshold voltage. The drift is extracted after 1 s. In order to study the impact of the energy offset between trap level and conduction band minimum on the PBTI drift level only, the same material properties and surface potentials, threshold voltages, same active energy region etc. need to be assured. For this reason, the trap band is shifted in the second configuration instead of shifting the conduction band minimum. The resulting band diagrams are shown in Figure 3.10. By doing so, the pure influence of the offset on trap occupation and the resulting drift can be studied. The obtained threshold voltage drifts are afterwards modeled with the thermal activation model and the maximum voltage drifts extracted, as was previously done for the experimental results. Even though this is only a qualitative study it provides valuable information in order to explain the different drift levels in SiC and Si MOSFETs.

Simulation Results

Consistent with the fitting of the experimental results, the simulated Comphy PBTI drifts can also be fitted with a fixed mean activation energy. Surprisingly, the same mean activation energy for all stress biases could be used. Here, $E_A = 1\,eV$ was used. The resulting maximum threshold voltage shift as a function of the stress bias can be found in Figure 3.11. For each data point, measurements at 30°C, 100°C, 150°C and 200°C were simulated and fitted for a fixed stress bias. "As-is" represents the left configuration in Figure 3.10 with the real band offset between the SiC conduction band minimum and the trap band and "shifted" represents the modified offset between the two, mimicking a conduction band offset as it would be the case for a Si-based device. A clear offset with an otherwise similar voltage dependence can be observed. The additional offset of 450 meV between the conduction band minimum and the trap band leads to a significant reduction of the maximum drift by a factor 8 to 10. As can be seen in Figure 3.10, the active energy region of the "shifted" configuration has a smaller overlap with the trap band than the "as-is" configuration, leading to less charges trapped and in total lower drifts.

Table 3.1 Electron defect bands used for the Comphy simulation, with the mean trap energy E_T, the relaxation energy S, the ratio of the curvatures R and the trap density N_T. The original trap bands were taken from [77] and the trap energy distribution slightly broadened (original: $E_T \pm \sigma = 1.73\,eV \pm 0.16\,eV$). [17]

Parameter	Defect Band	Defect Band Shifted
$E_T \pm \sigma$(eV)	$1.73 \pm 0.3^*$	2.18 ± 0.3
$S \pm \sigma$(eV)	4.93 ± 1.95	4.93 ± 1.95
R (1)	0.44	0.44
N_T (cm^{-3})	3.44×10^{19}	3.44×10^{19}

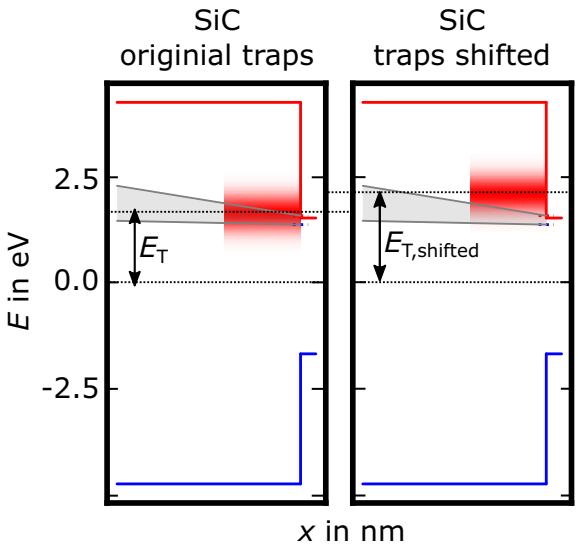


Fig. 3.10 Band diagrams of 4H-SiC with the two configurations of simulated trap bands. The left band diagram shows the original offset between the trap bands and the conduction band edge E_C. The right diagram shows the trap bands which were shifted up by the conduction band offset between SiC and Si. The gray shaded area is the maximum active energy region for the simulated stress biases (40 V, upper gray line) and a readout at 4 V (lower gray line). [17]

Interestingly, the observed differences in the maximum drift almost perfectly match the difference observed in the experiments. Here, as well a factor of around 8 was seen, which might be a coincidence due to the choice of exemplary trap band parameters. Therefore, it can be concluded that the different band structure of SiC/SiO_2 and Si/SiO_2 can well explain the different absolute drift levels observed. Furthermore, it supports the findings in [77] and the hypothesis that PBTI in SiC and Si technology is caused by the same oxide trap. Assuming that the trap bands roughly match the real trap situation in our devices, this would mean that the band offset is an important factor leading to the higher drifts in SiC compared to Si, in addition to different trap densities.

Summarizing the experimental findings for PBTI in SiC and Si power MOSFETs, the same time evolution, voltage acceleration and a similar temperature dependence were observed. In SiC, the total drift can be significantly reduced by adequate POA. Nevertheless, an 8 to 10 times higher drift was observed in SiC compared to Si. This can be explained with the different band structures of the two semiconductors. In both technologies, PBTI seems to be caused by the same trap level in SiO_2. In SiC, due to the higher conduction band minimum compared to Si and therefore a smaller offset to the trap level, trapping is facilitated. This leads to the overall higher drift. [17]

3.5 Comparison of Different Manufacturers

A benchmarking study for four important manufacturers of SiC power MOSFETs has been conducted with the main focus on BTI. In the following, the manufacturers will be called A, B, C and D. While A and B are trench devices, C and D are lateral DMOS-

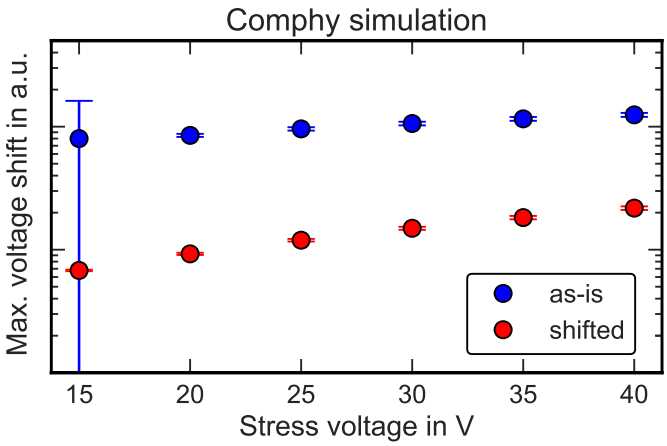


Fig. 3.11 Maximum PBTI voltage shift extracted by fitting a simulated set of PBTI measurements at various temperatures and stress biases using the thermal activation model and a fixed $E_A = 1\,\text{eV}$. The "as-is" configuration represents the left configuration in Figure 3.10, the "shifted" data the right one. An offset of a factor 8 to 10 is observed between the two setups. [17]

FETs. Nevertheless, all devices have similar ratings for the operation with regard to the recommended positive use voltages and maximum junction temperatures. However, the recommended negative operation limit strongly varies. Because of the similar datasheet ratings, all devices were tested with the same measurement parameters. Furthermore, they differ in the maximum drain source blocking voltage.

3.5.1 General Characterization

To begin with, the transfer and output characteristics were measured at room temperature. To do so, the gate voltage was swept from $-15\,\text{V}$ to $+25\,\text{V}$ and backwards without interruption with the drain voltage set to $V_D = 10\,\text{mV}$. All curves are inconspicuous and the threshold voltages lie between 3 V and 5 V, defined for a drain current $I_D = 1\,\text{mA}$. Furthermore, the given on-resistances in the datasheets can be confirmed. Out of the transfer characteristics measured as described above, the subthreshold hysteresis was extracted using a current criterion of $I_D = 1\,\text{nA}$ (Figure 3.12). The subthreshold hysteresis is an indicator for the trap density throughout the whole band gap since the Fermi level moves from the valence band edge to the conduction band edge and back during the conducted voltage sweep. A higher subthreshold hysteresis therefore most likely correlates with the density of states in the band gap. Manufacturer D achieves the lowest hysteresis (DMOSFET) followed by manufacturer A (trench MOSFET) and C (DMOSFET). The highest hysteresis is observed for manufacturer B (trench MOSFET). Therefore, device D has the lowest density of border traps whereas device B suffers from the highest. In the past, a higher subthreshold hysteresis has been reported for trench devices with the channel forming along the *a*-face compared to lateral MOSFETs with a channel along the Si-face due to a higher density of border traps [61]. Regarding the fact that device A (trench) and device C (DMOSFET) result in similar subthreshold hystereses despite the different device designs, this demonstrates that similar trap densities are possible for the different lattice planes. This observation either indicates that manufacturer A succeeded in significantly

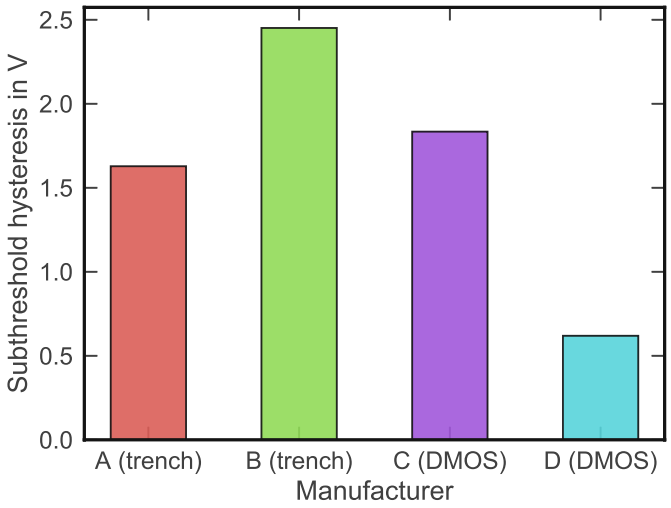


Fig. 3.12 Subthreshold sweep hysteresis for different manufacturers. The subthreshold hysteresis correlates with the number of trap states in the band gap.

reducing the number of border traps in the *a*-face compared to the lateral devices or that manufacturer C suffers from especially high hysteresis effects and therefore many border traps for this device design. A detailed investigation on the origin, however, cannot be conducted without further, not available knowledge about the device design parameters.

Additionally, the GOX breakdown was studied, as shown in Figure 3.13. Among the here tested devices, the highest breakdown voltage is achieved by manufacturers A and B, which are both trench devices. The breakdown voltage is significantly determined by the oxide thickness which is similar for devices A and B (both trench) and C and D (DMOSFETs), respectively. Because the trench devices have a thicker oxide than the lateral ones, the breakdown occurs at higher voltages. As was mentioned in a previous chapter, the trench corner is the weak point of this MOSFET design. Because of the higher breakdown voltage of device A, it is concluded that this manufacturer more efficiently reduces the increased oxide field at the trench corner compared to manufacturer B. Nevertheless, note that only limited statistics are available so that no information about the spreading of the breakdown voltage is available.

3.5.2 Bias Temperature Instability

BTI was studied for the different manufacturers using a simple MSM sequence. Before and between the stress phases, transfer characteristics (up- and down-sweep) in the range between $-15\,\mathrm{V}$ and $+18\,\mathrm{V}$ were measured. They were used to extract the threshold voltage using a current criterion of $I_\mathrm{D} = 1\,\mathrm{mA}$. The readout was started with the sweep starting voltage close to the stress bias and then sweeping towards the opposite polarity. This means for NBTI, the up-sweep was conducted first, for PBTI the down-sweep. By doing so, information about hysteresis and recovery can be retained. Additionally, the use of the I_D-V_G for the readout in comparison to the gated diode configuration allows to extract the drift of the on-resistance. The following results all show the readout for the down-sweep. The down-sweep is less effected by hysteresis effects because the Fermi level moves downwards form the conduction band. At the threshold voltage, it is still close to

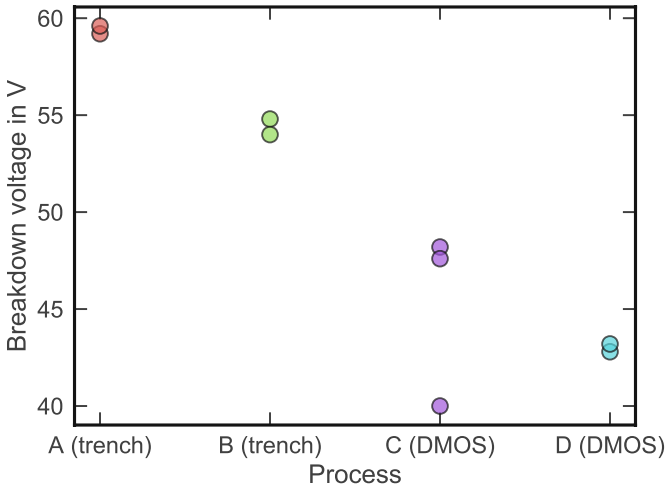


Fig. 3.13 Breakdown voltages for different manufacturers.

E_C and the readout is therefore less affected by hole capture or resulting recombination and emission processes. Since the conducted sweeps go from full accumulation to full inversion or vice versa, no preconditioning is needed. Note that drifts in between −10 mV and +10 mV are negligible due to the accuracy of the measurements and the extraction method.

Negative Bias Temperature Instability

Figure 3.14 shows the threshold voltage shift resulting from short NBTI stress (4.4 ks) with −25 V at 150°C. The chosen stress bias is significantly larger than the recommended voltage limit in the negative voltage region given in the datasheets. For manufacturer D, a drift in the negative direction is observed, for all other manufacturers in the positive direction. In general, NBTI should result in a negative drift due to the attraction of positive charge carriers to the interface during the stress. A different drift direction can be an indication for ion formation but also other effects are possible. In case of the manufacturers A and B, the NBTI drift is very low, barely larger than the accuracy limit of 10^{-2} V. Therefore, the observed behavior is not worrisome in this case. In contrast, manufacturer C shows drifts of up to 100 mV in the rather short measurement window so that the measurement accuracy can be excluded as possible cause. Nevertheless, all those drifts are still in an acceptable voltage range even though the drift direction is different. In contrast, device D results in very large negative drifts of up to 1 V after 4.4 ks of stress. This magnitude is quite serious because the point of operation might be significantly shifted during application. However, note that device D has presumably the thinnest GOX of all tested devices and is therefore stressed with the highest field.

Overall, rather low and similar drifts are observed for manufacturers A, B and C. The trench devices A and B show a superior drift behavior compared to the lateral devices and result in barely measurable drifts for short stress times.

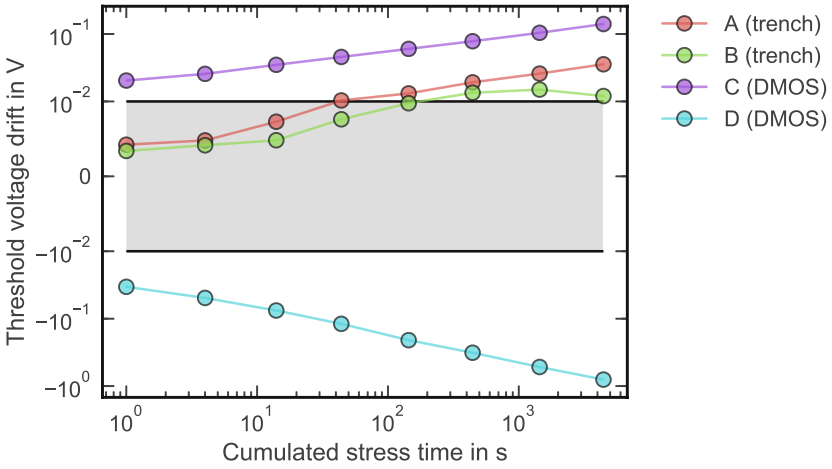


Fig. 3.14 NBTI threshold voltage drift as a function of the cumulated stress time for a stress with −25 V at 150°C. Besides manufacturer D, all other manufacturers drift in the positive direction instead of the negative.

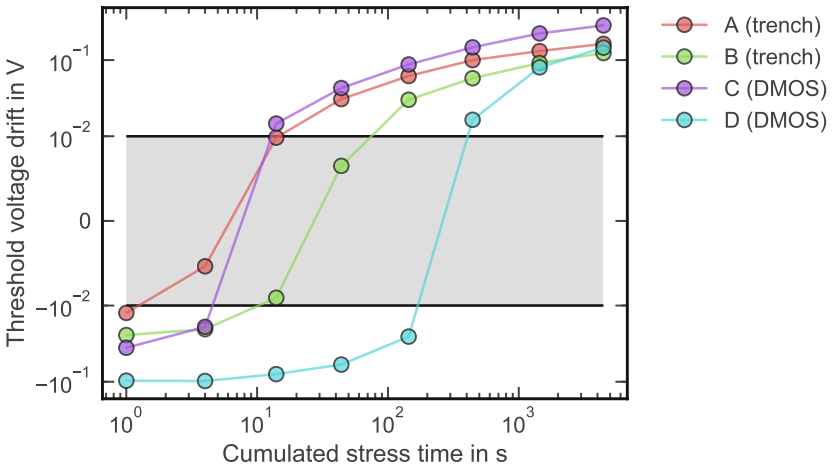


Fig. 3.15 PBTI threshold voltage drift as a function of the cumulated stress time for a stress with +25 V at 150°C. For short stress times (4.4 ks), all devices show similar drifts.

Positive Bias Temperature Instability

The PBTI results for a stress with 25 V at 150°C is depicted in Figure 3.15. For short stress times (4.4 ks), all devices drift very similar and all very little. After a cumulated stress time of 4.4 ks, a shift of only slightly more than 100 mV is observed. This is a quite satisfying drift level for SiC, especially with regard to reports showing drifts in the range of Volts [65].

Since 25 V is still very close to the use-conditions and only slightly out of specs, a second PBTI stress with $V_G^{str} = 2 \times V_{use}$ is conducted at 150°C (A, B, C: 2 × 18 V, D: 2 × 15 V). The resulting threshold voltage drift can be found in Figure 3.16. Whereas for short stress times barely a difference between the manufacturers was found, now, for longer stress,

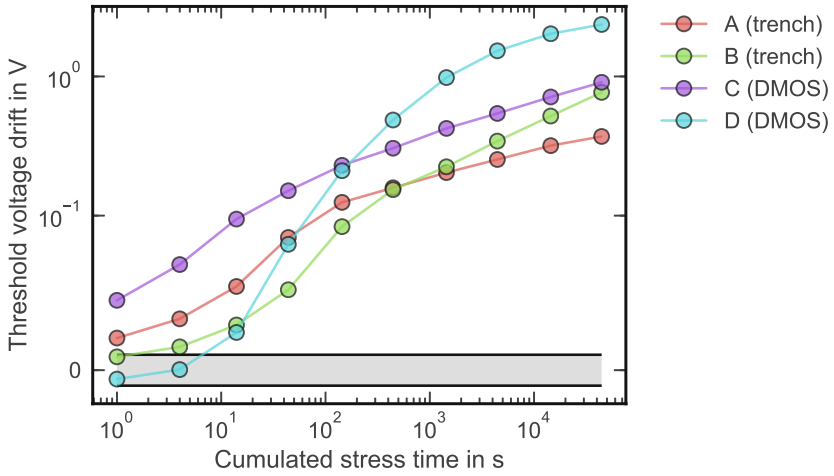


Fig. 3.16 PBTI threshold voltage drift as a function of the cumulated stress time for stress with two times the recommended use-voltage from the datasheet at 150°C. For this significant overstress, differences between the manufacturers become visible.

significant drifts are measured and differences between the devices become visible. For this significant overstress, drifts of up to 1 V are obtained. Devices A, B and C follow nicely a power law. Whereas device A and C seem to drift with a similar power law exponent, device B drifts with a higher slope. Note that in Figure 3.15, device B resulted in a slightly lower drift than device A. For the longer stress with higher gate bias, the drift of device B "overtakes" those of device A. Device D drifts with the highest slope in the log-log plot and also results in the highest drift at the end of the stress sequence. Nevertheless, this device seems to enter saturation towards the end of the measurement window with a drift of slightly above 1 V. In the end, device A shows the lowest total drift and a rather low slope compared to its competitors.

Additionally, the drift of the subthreshold hysteresis was studied for the longer PBTS with high gate bias (Figure 3.17). An increase of the subthreshold hysteresis indicates the formation of new traps during stress. In the experiments presented here, the drift of the hysteresis behaves similar to the threshold voltage drift. For all manufacturers an increasing subthreshold hysteresis drift is observed, i.e. new traps are formed. The lowest hysteresis drift is measured for the two trench devices A and B, which means that they show the least trap formation. Generally, the time evolution of the hysteresis drift is very similar for all manufacturers which might indicate a similar mechanism for the defect formation. This is in total agreement with literature and the results presented for this stress bias can be linked to the observations and the given explanation in Section 2.3.3. As was already explained there, certain precursor states for charge trapping may exist in the oxide. When charges are trapped, the formation of new defects might be enhanced. Therefore, an increasing subthreshold hysteresis is observed with increasing stress times.

Last but not least, the drift of the on-state resistance was studied. The drift of this parameter is of special interest since it strongly determines the device performance and overall the conduction losses during operation. Whereas for short stress times and the smaller stress bias barely a drift of the on-resistance was observed (not shown), significant changes become visible for the higher bias and the longer stress. The two trench devices from manufacturers A and B only show low drifts of R_{on} of up to 2% within our measurement

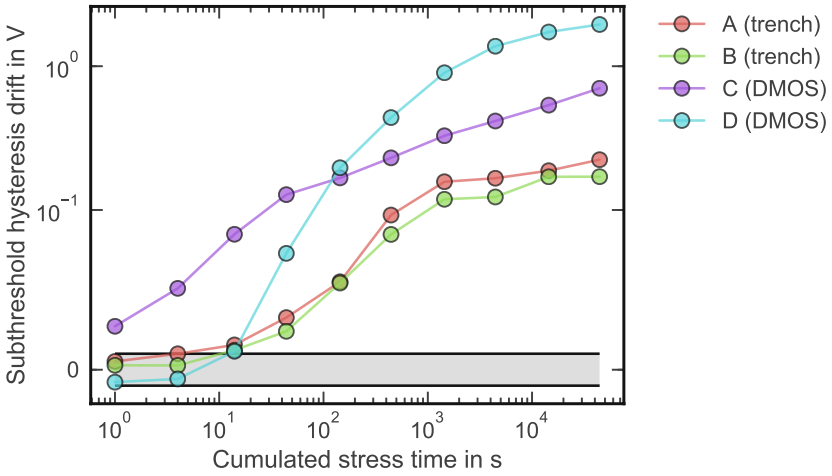


Fig. 3.17 Drift of the subthreshold voltage hysteresis for a PBTI stress with two times the use voltage at 150°C. A similar increase of the subthreshold hysteresis for all manufacturers is observed.

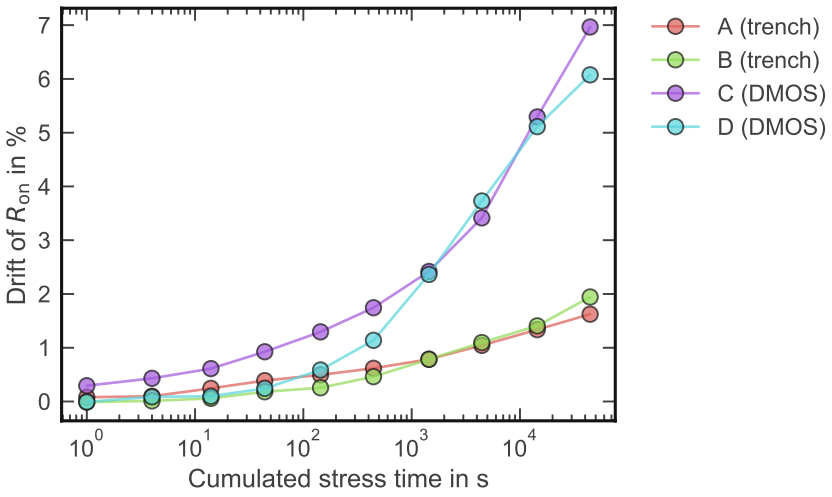


Fig. 3.18 Drift of the on-state resistance R_{on} for a PBTI stress with two times the use voltage at 150°C. The R_{on} of manufacturers A and B drift around 2% whereas those of devices C and D drift up to 7% after 40 ks.

window. The DMOSFETs from manufacturers C and D, however, drift up to 7%. For those two manufacturers, the samples are significantly damaged during stress leading to a worsened performance.

Overall, very similar low drifts for different BTI cases were measured for four important manufacturers. For NBTI stress, the trench devices A and B seem to be slightly superior with regard to the total drift compared to the lateral MOSFETs C and D. In contrast, the devices perform similar regarding PBTI threshold voltage drifts. Nevertheless, the trench devices A and B outperform the studied lateral devices with regard to subthreshold hysteresis drift and drift of the on-resistance. Even though negligibly small differences in the drift resulting from large and long PBTI stress were found, different amounts of

device damage were observed. Again, the trench devices A and B showed less formation of new defects and a significantly lower drift of the on-resistance compared to its lateral competitors C and D. Therefore, it is concluded that the state-of-the-art trench devices from manufacturers A and B are slightly more robust than the DMOSFETs presented here for the same stress biases (different oxide fields!). Even though all devices are rated with the same or similar typical use gate voltages, the lateral devices have slightly thinner oxides, i.e. they are operated with higher oxide fields than the trench MOSFETs. The fact that the trench devices seem to be more robust reveals the importance of a sufficient "safety margin" for device operation which is significantly smaller for devices with a thinner oxide but the same use-voltage.

3.6 Summary

In summary, a similar BTI drift was observed for SiC and Si MOSFETs. For SiC, a drift reduction by one order of magnitude for both, NBTI and PBTI, was achieved by improved device processing. For NBTI the best SiC devices can already compete with Si. For PBTI, the same time evolution, voltage acceleration and a similar temperature dependence were observed. At the same time, SiC devices drift around 8 times more than comparable Si devices. This was explained with a trap level in SiO_2 which is present in both technologies. Due to the lower conduction band in Si, it is more difficult to fill this trap level compared to SiC.

CHAPTER 4

Cryogenic Characterization of SiC Trench MOSFETs

Contents

4.1 Introduction

Cryogenic device characterization offers the opportunity to study trapping and emission effects in more detail than at room temperature. As described in Section 1.4, each trap is well characterized by its capture and emission time constants [68]. These are strongly temperature dependent and become larger for lower temperatures. Therefore, capture and emission processes are significantly slowed down at cryogenic temperatures making it easier to measure effects which are too fast to be accessible via typical measurement systems at room temperature. Traps become visible at certain temperatures. This means that below that temperature, the capture and emission time constants are larger than the measurement time window so that these traps are not seen in the measurement. Because of this, it is possible to determine certain trap bands with their activation energy and their impact on the device characteristics.

In this section, TDRC studies of NH_3 annealed devices will be presented. Different POAs were studied and several different trap bands and trap types were identified. Furthermore, it was tried to correlate the findings with the room temperature channel mobility. Additionally, the field effect mobility as a function of the temperature has been investigated. These studies were related with trap bands found in I_D-DLTS. In I_D-DLTS, several trap bands were found and their possible origin and their impact on the device characteristics are investigated.

4.2 Characterization of NH_3 Annealed Trench MOSFETs using TDRC

As already explained in detail in Section 2.2, the NH_3 POA is an attractive process with regard to the resulting apparent channel mobility in trench MOSFETs. In order to better understand the improved mobility and the nature of the underlying defect distribution, TDRC measurements were conducted. The resulting interface state densities of NO, two different NH_3 and N_2 annealed trench MOSFETs were studied and compared to the room temperature mobility. So far, TDRC has only been applied to either n-MOS structures or lateral MOSFETs [20, 100, 139]. NH_3 annealed MOS structures were mainly investigated using CV measurements [42]. There, a reduction of deep interface states was found for NH_3 pre-oxidation annealed 6H-SiC MOSCAPs with additional N_2 or N_2O POA compared to devices without the NH_3 pre-anneal. However, as we previously showed in [103, 135] the obtained trap distributions are not identical for MOSCAPs and MOSFETs. Therefore, it is important to not only study simplified test structures but also fully processed MOSFETs in order to being able to interpret their behavior. Most of the following studies are published in [104].

TDRC measurements were conducted on trench MOSFETs as shown in Figure 1.3 (b). The oxides were annealed with either NO, N_2 or NH_3 (NH_3 (1): t_1, T_1 and NH_3 (2): $t_2 = 3t_1, T_2 = T_1 + 15\%$). For this study, the measurements were performed as described in Section 1.5.4, using a charging voltage of $V_{ch} = 30\,V$, a discharging voltage of $V_{dis} = -4\,V$ (depletion) and a constant heating ramp $\beta = 5\,K/min$. In order to distinguish between different kinds of traps, the charging and discharging voltages were varied as suggested in [20, 103] . For the measurements itself the MOSFET is connected as a MOSCAP as already shown in Figure 1.8 (b).

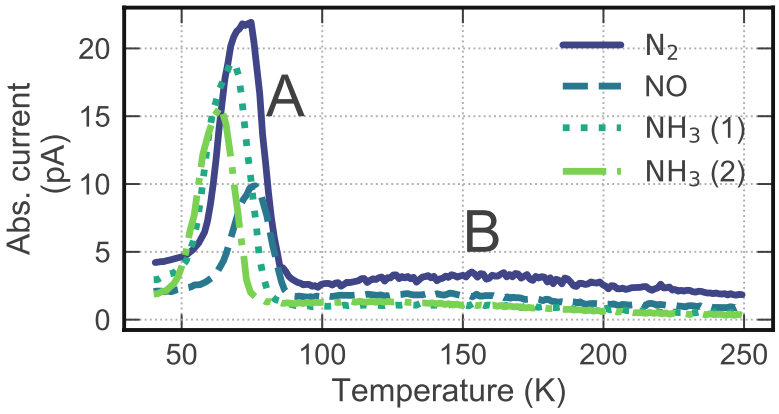


Fig. 4.1 TDRC as a function of the temperature. In total, two peaks are observed. [104]

4.2.1 Process Comparison

Figure 4.2 shows the TDRC signal. As can be seen, the signal consists of two peaks regardless of device processing. The first peak A is observed at 70 K. In addition, a second much broader and smaller peak appears between 100 K and 200 K. Note that MOSCAPs only show peak B [135]. With Equation (1.16) and Equation (1.17), the temperature dependent current can be transformed into a density of states D_{it} and an apparent activation energy $E_C - E_T$ using the SRH theory. Even though this model might only apply for a certain kind of trap, these methods can nevertheless be used for comparison of the relative changes. Figure 4.1 shows the resulting characteristics. The apparent activation energy of peak A is determined to be approximately 130 meV, the one of peak B around 300 meV below the SiC conduction band edge. When comparing the trap densities resulting after the different POAs, the highest trap density in peak A is observed for the N_2 annealed device, followed by the two NH_3 anneals. NO POA results in the lowest trap density. This result is in good agreement with reports by [42] and [45] who also observed reduced trap densities close to the conduction band edge. For peak B, no clear conclusion concerning the trap density can be drawn, as will be explained later.

In order to determine the type of traps, the charging and discharging parameters were varied. Figure 4.3 shows the measured trap density for the variation of the charging voltage V_{ch}. An increased signal is measured for higher charging voltages. Due to the stronger fields, more electrons are attracted to the interface such that in total, more electrons can be trapped. Since both peak maxima increase, it is concluded that electron traps are observed. Second, the impact of the discharging voltage was studied. The resulting signals are displayed in Figure 4.4. For peak A, an increase in the signal is observed when varying the discharging voltage from small positive to small negative voltages. This is the typical behavior expected from interface states. From inversion to depletion, the Fermi level at the interface moves away from the conduction band edge so that trap states lying above E_F are likely to emit trapped charges, leading to a higher TDRC signal. In contrast, peak B decreases until it is barely visible when the discharging voltage is varied small positive to small negative voltages. This behavior is ascribed to NITs [20]. NITs are trap states in SiO_2 which are located about 2 nm away from the interface in the oxide. They were first reported by Afanasev *et al.* [24] and later reported to be found with TDRC in [20] and [135]. The NIT is currently assumed to be an intrinsic trap in SiO_2, however, its

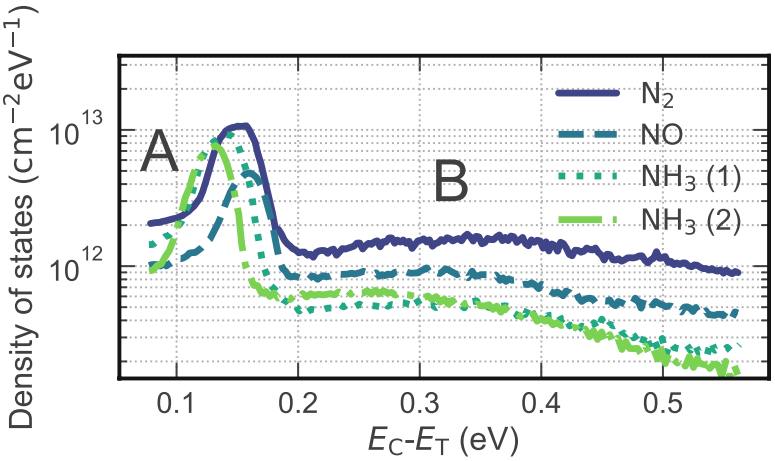


Fig. 4.2 Density of trap states as a function of the effective activation energy resulting from TDRC measurements conducted on test structures which received different POAs. [104]

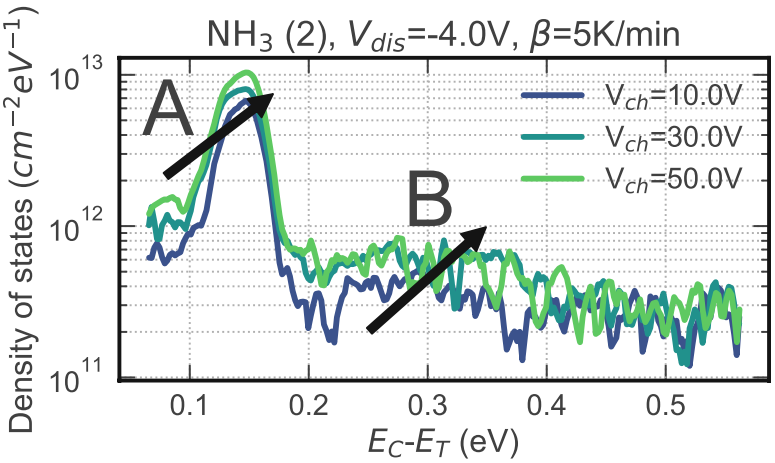


Fig. 4.3 Density of states as a function of the effective activation energy for different charging voltages. Both peaks increase with increasing charging voltages. This behavior is typical for electron traps. [104]

microscopic nature is not fully identified. NITs are very difficult to measure and to quantify with TDRC. Krieger *et al.* [20] suggest that because of the proximity to the interface, charges can tunnel directly into the conduction band for discharging in depletion or weak accumulation (Figure 4.5 (a)). This relaxation happens very quickly, which renders the measurement difficult. For discharging in weak inversion (small positive gate bias), however, the trapped charges cannot tunnel directly anymore but need to be thermally emitted into the conduction band, as is the case for "normal" interface states (Figure 4.5 (b)) [20]. Therefore, at least part of the NIT distribution can be measured. Nevertheless, with TDRC it is not possible to determine the total density of NITs in the oxide. Therefore, peak B will not be further interpreted.

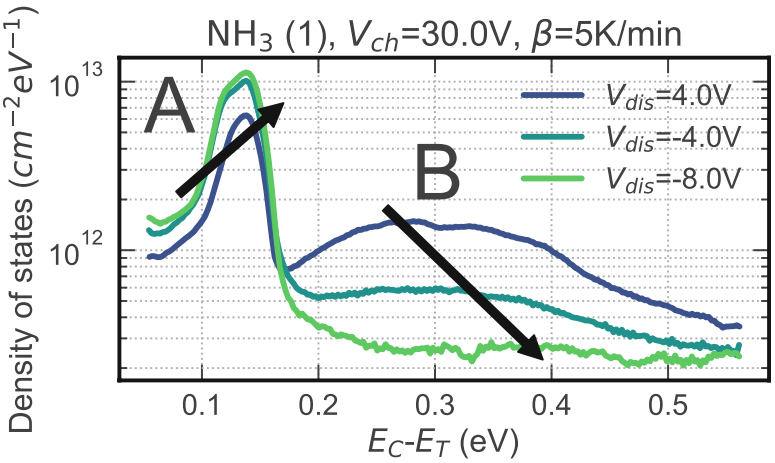
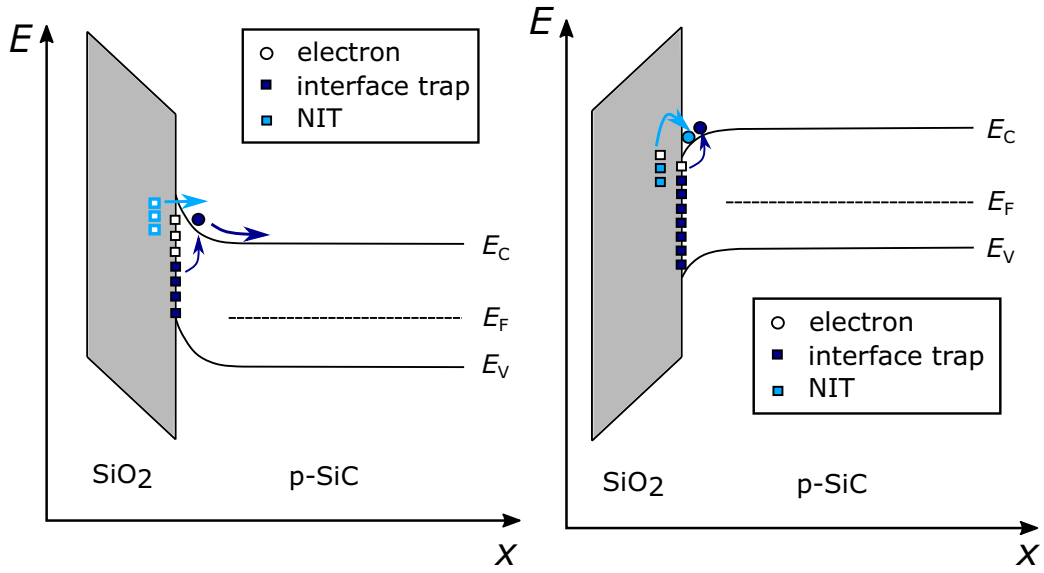


Fig. 4.4 Density of states as a function of the effective activation energy for different discharging voltages. Peak A increases for more negative discharging voltages, peak B decreases. Therefore, peak A is ascribed to interface states and peak B to NITs. [104]

Now, combining the observed trap densities with the determined trap origins, it can be concluded that NO and NH_3 POAs can both reduce interface states. Nevertheless, the reduction seems to be more efficient for the NO POA than for NH_3. Note that the processing of the NO and N_2 annealed samples was slightly different which might also have a small impact on the results. Nevertheless, these results are quite consistent with the observations reported in Section 2.2. There, a lower subthreshold sweep hysteresis and a higher BTI drift were observed for the NH_3 annealed MOSFETs compared to the NO, which indicated that the NH_3 POA might be more efficient in trap passivation in the middle of the band gap whereas the NO anneal seems to be more active close to the conduction band edge. [104]

4.2.2 Correlation with the Room Temperature Mobility

In earlier work, a possible weak correlation between peak A and the apparent channel mobility was suggested [103, 135] since an improved mobility was observed for devices with lower densities of trap A. Therefore, the correlation between the room temperature Ghibaudo mobility and the trap density of peak A was further investigated. The resulting (anti-) correlation can be found in Figure 4.6. The Ghibaudo mobility was extracted as described in Section 1.5.2. The highest mobility was extracted for NH_3 (2), followed by NO POA. NH_3 (1) and N_2 POA both result in very low channel mobilities. The data presented here prove that indeed an improved mobility comes with a reduction of the interface state density (peak A). However, no clear direct correlation is found. As an example, both NH_3 processes result in very similar densities of interface states (note that rather large measurement to measurement variations might be observed in TDRC due to the overall very low currents) on one hand, but on the other hand have very different channel mobilities. Therefore, it has to be concluded that even though peak A might have an influence on the channel mobility, it does not seem to be the main mobility-limiting defect. Therefore, it is assumed that a different trap band most likely further away from the SiC conduction



(a) depletion/weak accumulation (b) weak inversion

Fig. 4.5 Discharging process for interface traps and NITs for discharging biases in (a) depletion and (b) inversion. In depletion, NITs can tunnel directly into the conduction band. In inversion, the charges need to be thermally emitted into the conduction band as is the case for interface traps.

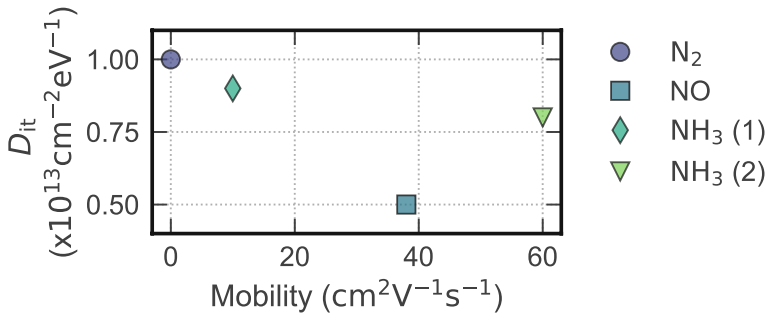


Fig. 4.6 Correlation between the interface state density of peak A and the Ghibaudo mobility at room temperature. A direct correlation cannot be confirmed. [104]

band might have a stronger negative impact on the device performance. Since NITs cannot be reliably quantified with TDRC and because traps close to the conduction band are expected to reduce the mobility [140] it is suggested to further study the impact of NITs on the device performance. [104]

4.2.3 Conclusion

The annealing effects of N_2, NO and two different NH_3 POAs have been investigated using the TDRC method. A trap band caused by interface traps and a second trap band caused by NITs were identified. NO and NH_3 both seem to reduce the interface trap band, however, NO most likely does so more efficiently. Furthermore, the interface trap

density was correlated with the apparent channel mobility extracted at room temperature. Even though a reduced interface state density comes with an improved mobility, no direct correlation could be identified. It was concluded that these interface traps might have a weak negative impact on the device performance but are not the main limiting defect.

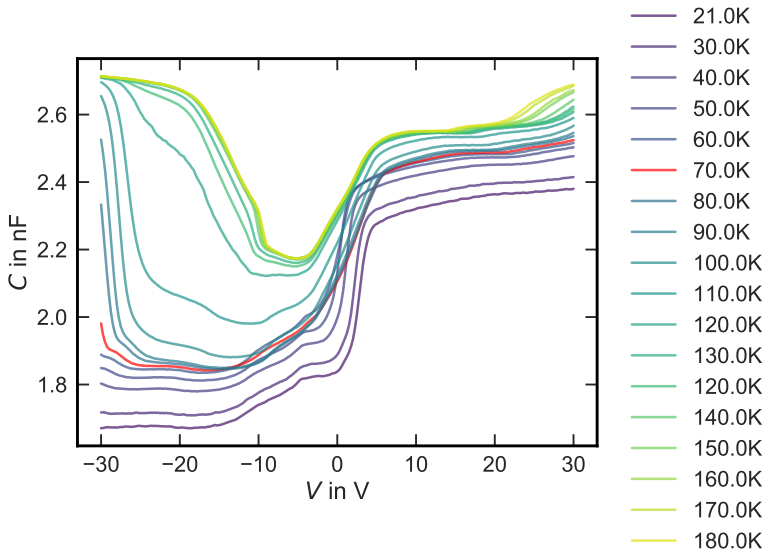
4.3 Cryogenic Mobility of SiC Trench MOSFETs

Low temperature studies or in general studies of different temperatures offer the opportunity to identify different physical processes and improve the understanding of trapping related effects. As described in Section 1.3.4, the mobility consists of several contributions of scattering mechanisms which all have different temperature dependencies. In order to better understand the channel mobility in SiC MOSFETs and to identify mobility limiting defects, transfer characteristics were measured over a wide temperature range and the field effect mobility and threshold voltage extracted.

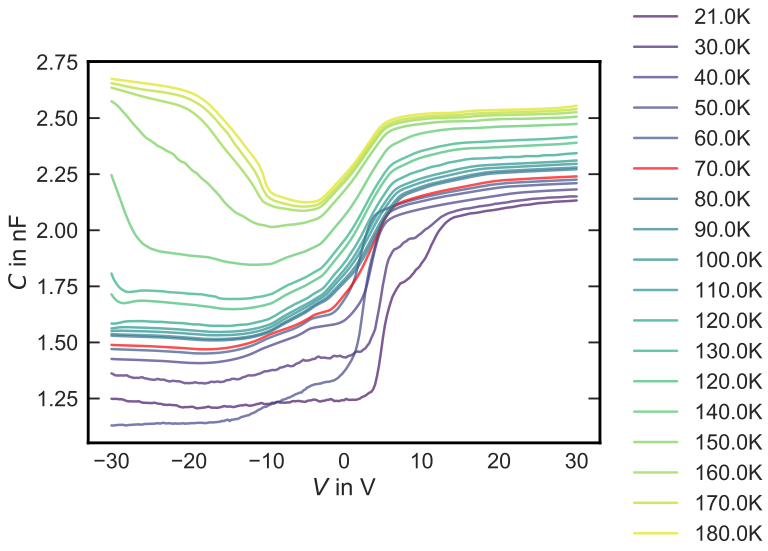
4.3.1 Capacitance Voltage Characteristics at Cryogenic Temperatures

At low temperatures, the device characteristics are determined by several different factors. On one hand, the intrinsic carrier concentration n_i is strongly temperature dependent (exponential relation) [8]. On the other hand, the carrier concentration is additionally reduced due to incomplete dopant ionization. Therefore, when decreasing the temperature the semiconductor slowly changes from a doped to an intrinsic material. The amount of ionized dopants strongly depends on the dopant and the material. A detailed description of the basics on incomplete ionization in SiC can be found in [1]. In SiC, the N donor freezes out at significantly lower temperatures ($< 50\,\mathrm{K}$) than the Al acceptor states (below 75-100 K, cf. [141] for ionization time constants).

In order to determine temperature ranges in which the device or material properties significantly change, e.g. due to dopant ionization, CV curves were measured. In a first step, CV curves were determined at discrete temperatures sweeping the gate bias from $-30\,\mathrm{V}$ to $+30\,\mathrm{V}$ and backwards, using a frequency of 100 kHz and 1 kHz and an AC amplitude of $\pm 0.1\,\mathrm{V}$. The resulting curves are shown in Figure 4.7. At room temperature, the CV curves of the trench MOSFETs usually consist of an accumulation, depletion and inversion branch. At low temperatures, these regions change significantly. For the lowest temperatures, the curves consist of an inversion and depletion branch only. The inversion capacitance is significantly reduced compared to the value reached at higher temperatures. Nevertheless, it can form at all temperatures. This means that at all temperatures studied here, electrons can be brought to the interface. In contrast, the accumulation branch significantly changes with temperature. At low temperatures, the MOSFET cannot be brought into accumulation within the measured voltage range anymore because there are no positive charge carriers available. Below a certain temperature corresponding to the activation energy E_A of the dopant ($E_\mathrm{A,Al} \approx 200\,\mathrm{meV}$ [142]), the dopant is not ionized. In this case, a small section of the accumulation branch starts to form at 70 K for the 1 kHz curve, i.e. from this temperature on already a small share of the Al p-dopants is notably ionized and therefore providing positive charges. For the higher frequency, the accumulation branch is observed at significantly higher temperatures. According to Lades *et al.* [141], the ionization time constant of Al is around 1 s around 70 K and thus, quite long. So, only a very small share of it is expected to be active and it can only be measured with



(a) 1 kHz



(b) 100 kHz

Fig. 4.7 CV curves measured at different temperatures for 1 kHz (a) and 100 kHz (b). The measurement speed significantly influences the temperature at which first doping influences can be observed because the dopant ionization time constants are very large at these temperatures.

sufficiently slow measurements. With increasing temperature, the accumulation branch forms more clearly. For roughly around 140 K or higher, it does not change significantly anymore. So, full accumulation can be reached which indicates that the majority of the p-doping is active. At this temperature, the ionization time constant of Al [141] is smaller

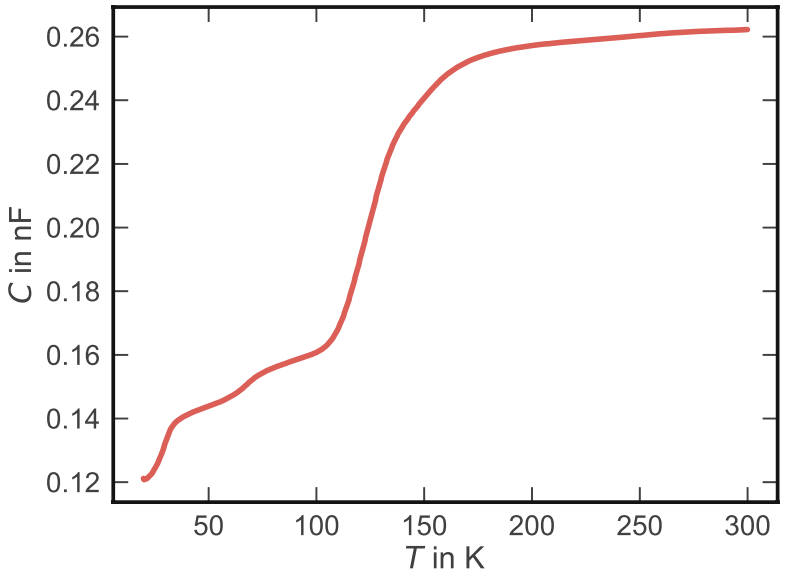


Fig. 4.8 Gate capacitance as a function of the temperature. The capacitance was extracted as the last point from capacitance transients (10 s, $\beta = 0.5\,\mathrm{K/min}$ for $V_\mathrm{G} = -9.5\,\mathrm{V}$).

than the time constant of the discrete CV measurement so that the accumulation branch can be fully measured. Therefore, depending on the speed of measurement, a significant change in the device characteristics is expected for $70\,\mathrm{K} \leq T \leq 140\,\mathrm{K}$.

In addition, the depletion capacitance at $V_\mathrm{G} = -9.5\,\mathrm{V}$ was measured for a temperature sweep ($\beta = 0.5\,\mathrm{K/min}$) during DLTS measurements with a lockin amplifier as described in Section 1.5.1. By doing so, more detailed information about the dopant ionization can be obtained. The stress and recovery pulses were 10 s each. Figure 4.8 shows the resulting capacitance over temperature curve. In general, similar observations are made as for the discrete measurements. Between 30 K and 40 K, the capacitance increases. This is most likely caused by the activation of the N donor level getting ionized. A second significant increase is observed between 120 K and 150 K. In this temperature range, the p-doping is getting active so that the accumulation branch starts to form and increases the measured capacitance. In the range between, only a slight increase of the capacitance is observed, indicating that only a very small share of the Al acceptor is ionized. The main changes are deeper in the accumulation branch and therefore not visible for the bias conditions chosen here. The temperature from which on full accumulation can be observed matches the observations from the discrete measurements. Note that the curve may shift along the temperature axis for different ramping rates and measurement frequencies.

4.3.2 Transfer Characteristics at Cryogenic Temperatures

Figure 4.9 shows several I_D-V_G curves at cryogenic temperatures. All MOSFETs can be operated down to rather low temperatures ($< 50\,\mathrm{K}$). This observation matches older reports by Chen *et al.* [143]. Nevertheless, some changes in the I_D-V_G characteristics are

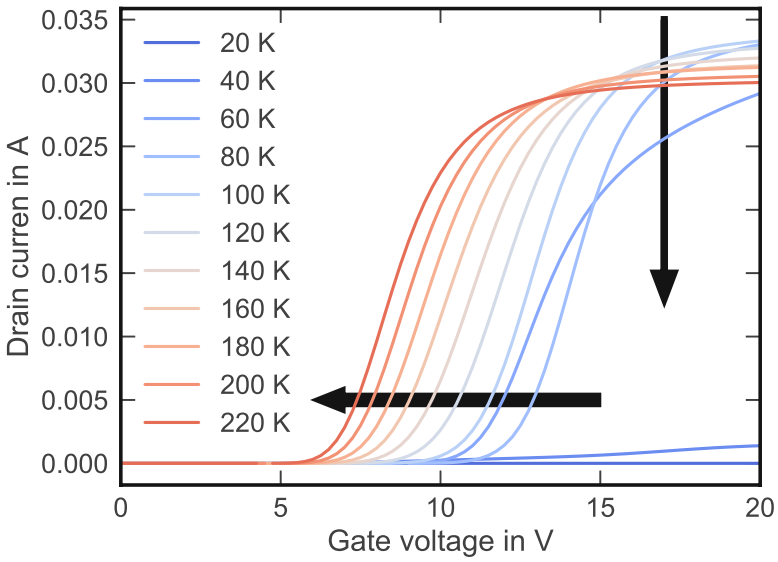


Fig. 4.9 I_D-V_G measured at different temperatures. With increasing temperature, the threshold voltage and the saturation current decrease.

observed. First of all, a strong shift of the threshold voltage is observed depending on the temperature. Second, the saturation drain current changes.

Figure 4.10 shows the threshold voltage of nitrided 4H-SiC trench MOSFETs extracted with a current criterion (constant current density for both designs). In [143], an increase of the threshold voltage with decreasing temperature is reported. Here, a similar behavior is found but more regimes are observed. Below 40 K or 50 K, a decrease of the threshold voltage with increasing temperature is observed. In this temperature region, the I_D-V_G curve is barely measurable since only very small currents exist. Therefore, it is not certain if the extracted values are reliable or not. Considering the capacitance as a function of the temperature, all dopants might be inactive for these low temperatures and the measurement speed. An increase of the capacitance at around 40 K indicates that around this temperature regime N dopants are ionized. This is also supported by Dalibor *et al.* [144] who measured a DLTS peak at around 50 K in 4H-SiC which was attributed to nitrogen on cubic lattice sites. The temperature dependence can be explained with the very large ionization time constant of more than 1 s [141] below 50 K and different measurement speeds. Thus, in this regime, there is nearly no N-doping (donor) visible and therefore nearly no mobile charge carriers. With increasing temperatures, the number of ionized N donors increases and thus, also the number of electrons leading to a decreasing threshold voltage. Dopant freeze-out effects are visible in this region.

Between 50 K and 70 K an increase of the threshold voltage is observed. In this regime, the N donor is ionized and most likely also first p-dopants start to get ionized so that the semiconductor behavior changes from undoped (intrinsic) to the behavior of a p-doped semiconductor. This leads to the observed increase of the threshold voltage.

Above 70 K, the threshold voltages decreases again. In slowly measured CV curves (Figure 4.7 (a)), first indications of a starting accumulation, i.e. holes getting active, can be seen. This means that starting from 70 K on, a small amount of the Al acceptors is ionized. At 70 K, the ionization time constant of Al is about 1 s [141] so that the dopant

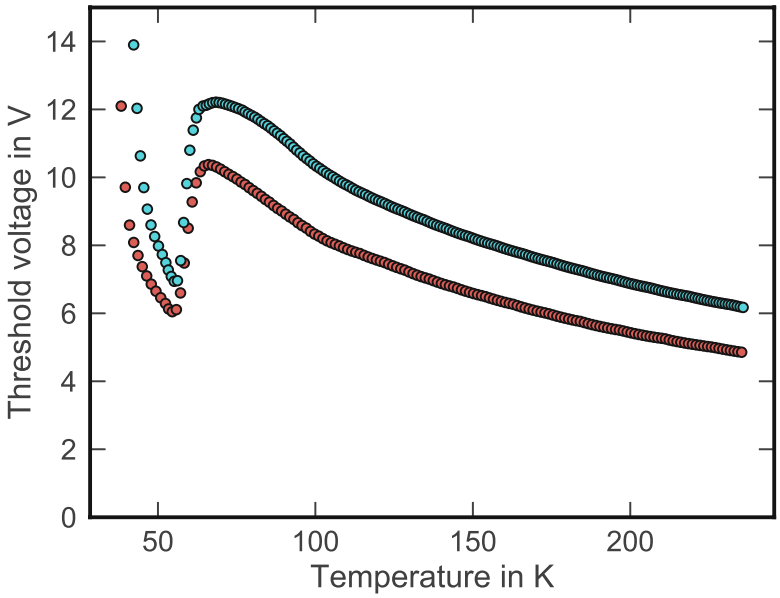


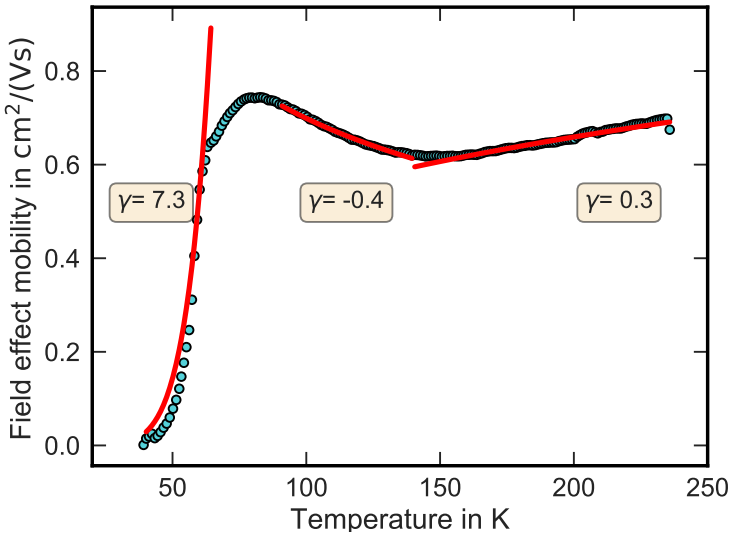
Fig. 4.10 Temperature dependent threshold voltage for two different trench layouts.

can only be ionized and its influence detected in very slow measurements. For faster CV curves as for example in Figure 4.8, the influence of the p-doping most likely shifts towards higher temperatures due to a measurement window which is smaller than the ionization time. The main Al doping peak is expected to be seen at higher temperatures, roughly between 100 K and 150K because of the activation energy of $E_A \approx 200\,\text{meV}$ [141, 142]. Furthermore, the intrinsic carrier concentration rises with increasing temperature on which the threshold voltage exponentially depends [143]. This effect seems to be stronger than the incomplete Al dopant activation, leading to a decreasing threshold voltage with increasing temperature.

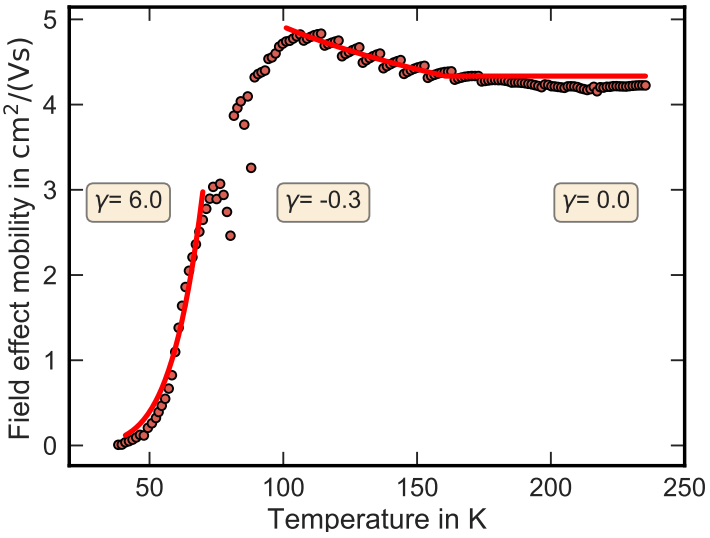
Additionally, it is observed that the saturation drain current in the I_D-V_G characteristic changes. For low temperatures, an increase of the saturation current with increasing temperatures is observed. This behavior can be as well explained with the intrinsic carrier concentration [143] and increased dopant ionization. At lower temperatures, both n_i and the effective number of ionized dopants get smaller. The higher the temperatures, the more charge carriers are available to contribute to the drain current. For higher temperatures, the behavior changes and a decrease of the saturation current with increasing temperatures is observed. This is most likely caused by increasing shares of scattering.

4.3.3 Field Effect Mobility

The channel mobility as a function of the ambient temperature is a very interesting parameter in order to determine possible origins of the reduced channel mobility in SiC MOSFETs. As already described in Section 1.3.4, there exist several mobility limiting influences such as Coulomb scattering, scattering at surface acoustic phonons and surface roughness. According to Matthies rule, as shown in Equation (1.4), the reciprocal values of the single components add up to the reciprocal value of the total mobility. All these contributions have different temperature and field dependencies. This fact enables us to identify and



(a) Trench MOSFET layout 1, reference POA



(b) Trench MOSFET layout 2, improved POA

Fig. 4.11 Field effect mobility as a function of the temperature. The mobility was extracted in the ohmic region, in the turning point of the I_D-V_G curves. Two different types of trench MOSFETs with different POAs are shown. For each curve, the power-law exponent γ of the temperature dependence was extracted by fitting.

distinguish between the different mechanisms and to gain a better understanding of the limitations of the SiC technology. Table 1.3 shows the temperature correlation for the most important mobility limiting mechanisms. In general, the temperature dependence of each

mobility component μ can be described as [145]:

$$\mu = \mu_{\text{ref}} \left(\frac{T}{T_{\text{ref}}} \right)^{\gamma} \tag{4.1}$$

with the mobility μ_{ref} and the temperature T_{ref} in a reference point and the exponent γ.

In order to study the temperature dependence of the mobility, I_{D}-V_{G} curves were measured at discrete temperatures or during temperature sweeps with a ramping rate of 0.5 K/min using a 2-point configuration. From these curves, the field effect mobility was extracted as described in Section 1.5.2. In this case, the field effect mobility was used because the extraction of the Ghibaudo mobility is more sophisticated and rather difficult at very low temperatures because of the very small currents and partly degraded I_{D}-V_{G} curves. For the extraction of the field effect mobility, only data from the linearly increasing branch of the transfer characteristics of the MOSFET were used. To do so the turning point of the rising current branch was extracted by differentiation and only a small region around it used to extract the mobility. This method ensures that over the wide temperature range studied the mobility is always extracted at comparable points of operation. Different regions of temperature dependence were fitted with the model presented above and the temperature exponent γ extracted. Figure 4.11 shows the field effect mobility as a function of the temperature for two MOSFETs with different active areas and different POAs. Note that the resulting curves depend on the measurement speed of the I_{D}-V_{G} curves which was different for the two devices. Therefore, shifts of approximately ± 10 K or even more along the temperature axis are possible. For the studied trench devices, a similar temperature dependence as for the threshold voltage is observed. The extracted mobility itself is at least at cryogenic temperatures significantly higher for the improved POA compared to the reference process. Starting from the lowest temperatures, an increase in the mobility is observed with rising temperatures. Between 70 K and 100 K, a maximum is observed. Above the peak temperature, a short range with slightly decreasing mobility follows and finally, either a constant mobility over temperature or slightly increasing mobility is extracted. The peak mobility is slightly shifted along the temperature axis for both processes. Because of the possible influence of different measurement speeds and delays this is not considered significant.

For low temperatures both devices show an increase of the mobility with $\approx T^6$. This increase is significantly larger than anything reported in literature and thus, does not match any of the mobility degrading mechanisms. Since it is similar for both devices, the same origin is expected. In this temperature range, most donor doping is still inactive and only starts to become ionized. Therefore, the significant dopant ionization especially of N might be one cause for the increasing mobility. Another cause could be very strong Coulomb scattering of the very few charge carriers available at these temperatures.

Between 70 K and 100 K, a local maximum of the mobility is observed and the temperature dependence changes. Reconsidering the CV curves presented in the previous section, in this temperature range first influences of the ionization of the Al acceptors can be observed depending on the measurement speed. This indicates that the channel doping in some way might have a negative impact on the channel mobility at low temperatures. This hypothesis was already formed in a different context in [135]. Many publications (e.g. [146]) exist which report a decreasing mobility with increasing channel doping dose. Therefore, the p-doping itself or a doping related defect might cause the field effect mobility to decrease from this temperature on. For higher temperatures, a small regime up to approximately

150 K with a decreasing mobility is observed ($\propto T^{-0.3}$ or $\propto T^{-0.4}$). A negative temperature exponent is e.g. reported for phonon scattering ($\propto T^{-1}$). Therefore, most likely weak phonon scattering alone or in a combination with the other scattering mechanisms causes the observed behavior.

Above 150 K, small differences are observed for the two presented devices. It is not clear if they are significant or result from the method of extraction and the device design. The reference sample with trench design 1 results in a regime which is mainly temperature independent and can therefore be ascribed to surface roughness as limiting factor. Noguchi *et al.* [147] report that "surface roughness scattering is not the most dominant mobility limiting factor" [147]. Since the room temperature mobility is significantly higher than in this regime, surface roughness as reported in [147] is most likely not the main limiting factor but still not negligible. In contrast to the reference sample, the improved sample from Figure 4.11 (b) with a slightly different device layout shows a slight increase of the mobility with increasing temperature ($\propto T^{0.3}$). If this behavior is not related to the changed design, this reveals an improved mobility with temperature for the improved process. The positive temperature exponent indicates that the influence of surface roughness has been reduced even though most likely not been totally eliminated. For the moment being, a mixture of Coulomb scattering and surface roughness seems to be the most likely limitation in this temperature range. So, overall a region dominated by dopant activation and Coulomb scattering at low temperatures, phonon scattering at the intermediate studied temperature range and a mixture of Coulomb scattering and surface roughness at the higher temperatures in the measurement window were identified.

4.4 Id-DLTS Characterization

In order to better understand the behavior of the mobility at different temperatures, trap bands and their behavior with temperature have been studied. Most trap bands possess strongly temperature dependent capture and emission time constants according to the NMP model [68]. In contrast, in the SRH model only one of the time constants is temperature dependent. At lower temperatures, the time constants become larger such that below a certain threshold capture and emission are too slow to become visible in the measurement time window. The main idea is to correlate the characteristic curve track of the mobility vs. temperature plot with the "activation" of certain traps. The identification of mobility limiting mechanisms and defects can help to specifically anneal these defects and by this, improve the device performance. In DLTS measurements, the pulse length (10 s for stress and recovery, respectively) significantly influences the measurement time window and therefore the temperature at which trap bands are detected. Here, the pulse stress bias is chosen to be 0 V and the recovery bias 7 V or 8 V depending on the peak studied. 0 V was chosen as stress bias in order to study mainly electron trapping effects. The temperature ramping rate was chosen as $\beta = 0.5\,\mathrm{K/min}$. Such a slow ramp is necessary in order to get a suitable temperature resolution for such long DLTS pulses. After four I_D-DLTS measurement sequences, a new I_D-V_G curve was measured for back-mapping of the current transients to a voltage transient. This is necessary because of the shift of the transfer characteristics with the temperature (cf. Figure 4.9). For the extraction of a spectrum from the current transients, first the currents are transformed into the corresponding voltage shift and the voltage transients transformed into a number of traps per area using the well-known relation $\mathrm{d}Q = C \cdot \mathrm{d}V$.

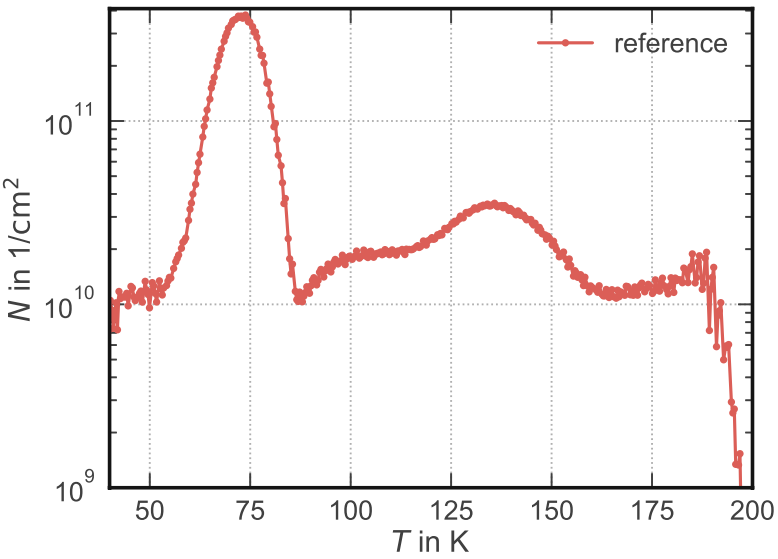


Fig. 4.12 Trap density as a function of the temperature. Two large peaks are detected.

4.4.1 Id-DLTS Spectra

In order to identify a trap distribution I_D-DLTS measurements were conducted using a lockin amplifier as described in Section 1.5. To be able to roughly correlate the trap bands in I_D-DLTS with the temperature dependent mobility characteristics, very slow pulses were chosen.

In order to obtain a first overview, I_D-DLTS measurements in the temperature range 40 K and 200 K were conducted. The stress bias was chosen as 0 V and the recovery bias as 8 V. Figure 4.12 shows the resulting I_D-DLTS spectrum as a function of the temperature. As was already the case for TDRC measurements previously presented, two peaks are detected in the studied temperature range: one at around 70 K ($E_A \approx$ 135-180 meV) and one broad peak around 120 K to 150 K. Interestingly, the position of the first peak correlates with the temperature at which first influences of the p-type doping are observed. Therefore, it is concluded that the first peak is somehow related to the Al doping. A detailed analysis on the origin of this peak will be given in the following sections.

Furthermore, the impact of the measurement parameters on the resulting spectra was studied. First, different stress and recovery times were tried (Figure 4.13). It was found that the peak position strongly shifts with the chosen pulse times. In this case, a shift of 15 K is observed. Every trap charges and discharges with a certain time constant which is strongly temperature dependent. At lower temperatures, these time constants get larger. For different pulse lengths, traps can be differently charged or discharged at a given temperature. If the measurement window is larger than the traps' time constants, a trap band can be detected and otherwise not. Therefore, the same peak may be observed at different temperatures for different pulse parameters, i.e. measurement time windows. This means that slight shifts along the temperature axis are insignificant.

Second, the impact of the speed of the transfer characteristics for the back-mapping of the current transients was studied (not shown). The faster the transfer characteristics, the lower the threshold voltage. Mainly a parallel shift to lower voltages is observed. This strongly impacts the value of the extracted V_{th} (cf. Figure 4.10) and also the mobility

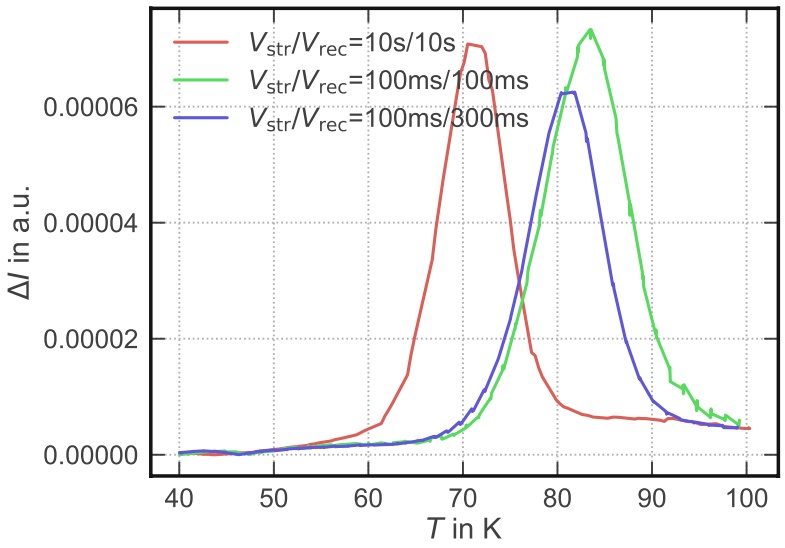


Fig. 4.13 First I_D-DLTS peak resulting for different pulse lengths. The pulse length strongly determines the measurement window and therefore the peak position. The temperature at which the peak is detected might be shifted by more than 10 K.

(cf. Figure 4.11). Nevertheless, the resulting I_D-DLTS spectrum is barely influenced. However, the shift of the transfer characteristics with the measurement speed needs to be considered when directly comparing the mobility with the I_D-DLTS spectra. Therefore, all temperatures at which characteristic behavior is observed need to be considered with an accuracy of about ±10 K or more.

4.4.2 Correlation of DLTS Spectra with the Channel Mobility

When comparing the full I_D-DLTS spectrum with the mobility as a function of the temperature, a correlation is found. On one hand, the I_D-DLTS spectrum reveals a trap distribution at 75 K. On the other hand, the mobility limiting mechanism changes at 70-100 K. Therefore, a correlation between the first I_D-DLTS peak and the mobility is concluded.

As was already shown previously, from 70 K on first influences of the Al doping become visible. This is the same temperature at which the mobility behavior changes and an I_D-DLTS peak is observed. Therefore, most likely a correlation with the doping exists. In general, it is possible to measure doping peaks with DLTS. However, in this case, an activation energy $E_A \approx$ 135-180 meV ($E_A \approx 155 \pm 25$ meV) is extracted for the peak which is lower than the activation energy of the Al acceptor ($E_A \approx 200$ meV [142, 148]). Therefore, it is not clear if the first peak is a doping peak, even though influences of doping should be visible for slow measurements (cf. ionization time constants extracted by Lades *et al.* [141]). In any case, the first impression indicates that either the Al dopant itself or a doping related defect might lead to the observed trap band. In the following section, a detailed analysis of the origin of the trap band will be presented.

4.4.3 On the Origin of the First Peak

As already mentioned in the previous section, the CV and I_D-DLTS studies presented here suggest that the first peak might be somehow doping related since it is detected in a similar temperature range in which first dopant ionization is detected. However, the trap activation energy is slightly lower than the activation energy of the Al dopant which is commonly given in literature. Weisse *et al.* [148], however, report that the ionization energy ranges from approximately 100 meV to 300 meV. The group presented a dependence of the ionization energy on the acceptor concentration. Especially for low concentrations, significantly larger energies were determined than theoretically expected. Their data show that for activation energies of 150 meV or below, an acceptor concentration equal to or larger than $10^{19}\,\mathrm{cm}^{-3}$ is needed [148]. This is significantly larger than what was implanted into the test structures presented here. Additionally, the time constants in [141] in combination with the slow CV curves previously presented suggest that only a small share of the Al dopants can be expected to be ionized at this temperature. Therefore, with regard to ionization energies, it appears rather unlikely that the first peak represents the Al dopant even though it cannot be totally excluded due to the limited accuracy of the extracted energies. Nevertheless, to find out if the peak results from the dopant itself, lattice defects by the doping procedure or defects created by the dopant used, further process variations were studied.

Variation of the Channel Implantation Dose

First of all, the impact of the channel doping dose was studied. To do so, a split with different channel doses was investigated by increasing the dose in 15% steps. Figure 4.14 shows the trap density of the first peak for different Al channel doses. Even though only small differences in the trap density are observed, a trend of a higher peak with higher doping dose is observed. Note that I_D-DLTS has a very good repeatability for several devices with regard to the trap density. In Figure 4.15, it can be seen that the first peak has a strong impact on the drain current measured at this specific temperature. Note that due to the different doping doses also the threshold voltages change (cf. Figure 4.26). This change does not influence the extracted I_D-DLTS spectrum because of the back-mapping of the current to the I_D-V_G but the current extracted at a fixed bias. Therefore, the drain currents need to be investigated for a fixed threshold voltage overdrive for a direct comparison. In doing so for all samples, a dip in the current extracted at $V_{Grec} - V_{th,303K} = \text{const.}$ from the I_D-V_G measured for the mapping is observed. This strongly proves the negative impact of this trap band on the device performance. Additionally, it reveals that the currents are very similar for higher measurement temperatures even though the trap density is slightly different. Unfortunately, this result is not sufficient to determine the specific origin of the I_D-DLTS peak. The doping itself (doping peak), doping related damage to the lattice or defects created by interaction with the dopant could be possible causes.

Hot Implantation

In order to determine between doping damage and the other options mentioned above, hot implanted samples were compared to conventionally cold implanted samples. Hot implantation means that the wafer is heated to high temperatures during the implantation process which reduces the implantation damage to the lattice especially for doses above a certain amorphization threshold due to in-situ annealing [142]. This means that higher

doses can be implanted at elevated temperatures without resulting in permanent damage to the lattice. For low doses, less damage is expected in case the standard post implantation anneal cannot eliminate all lattice damage. Note that the channel implantation dose is significantly lower than the dose of surrounding areas and might be therefore less affected by the hot implantation. The resulting I_D-DLTS spectra and the drain current at the recovery bias as a function of the temperature are shown in Figure 4.16 and Figure 4.17. As can be seen in Figure 4.16, the trap density of the first I_D-DLTS peak is identical for

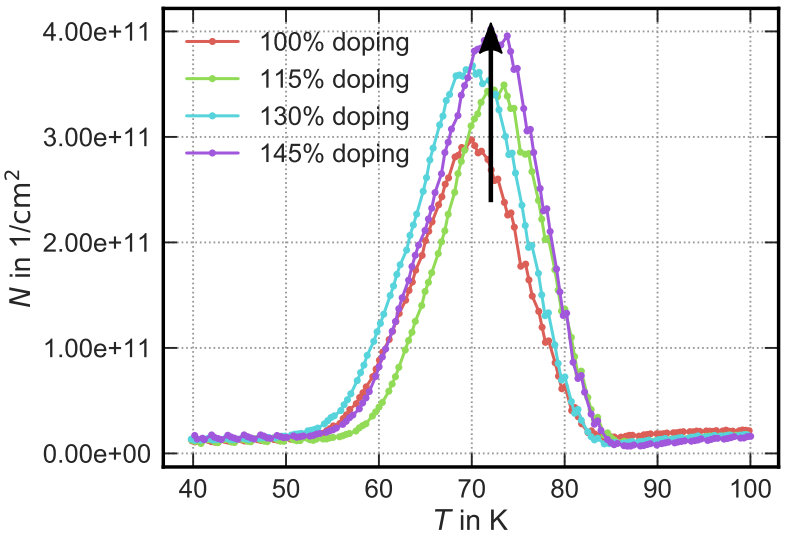


Fig. 4.14 Trap density as a function of the temperature determined with I_D-DLTS on MOSFETs which received different channel implantation doses. The trap density increases with higher channel doses.

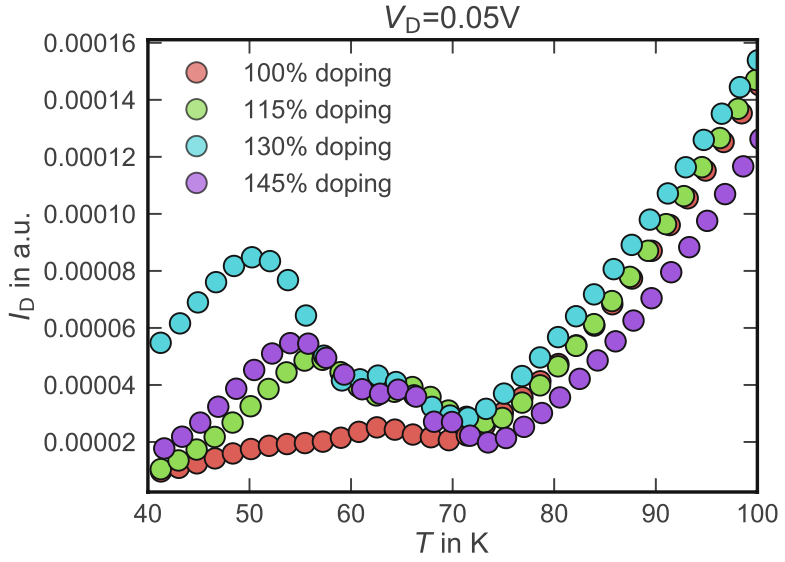


Fig. 4.15 Drain current as a function of the measurement temperature extracted for $V_{Grec} - V_{th,303K} = \text{const}$. A dip in the current is observed around 70 K.

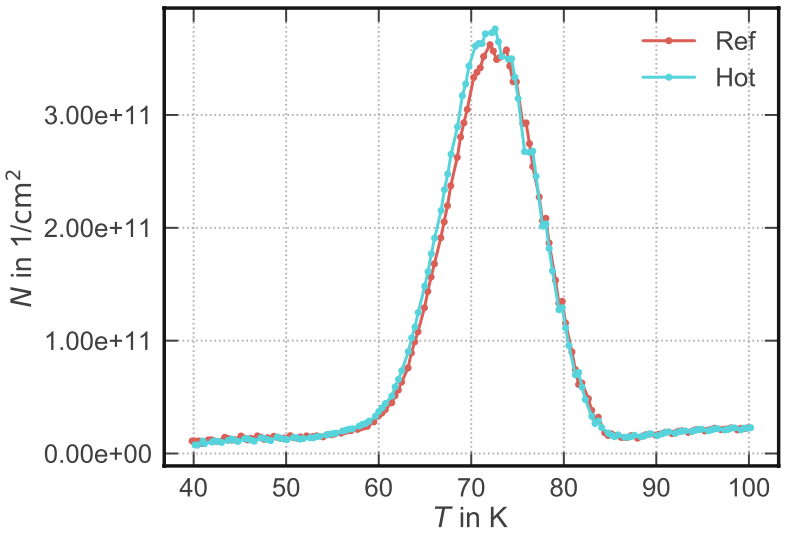


Fig. 4.16 Trap density as a function of the temperature determined with I_D-DLTS on MOSFETs which were implanted either at room temperature or at elevated temperature ("hot"). The trap density is not changed by the different implantation techniques.

both processes. Therefore, assuming that the hot implantation led to a reduction of the lattice damage, implantation damage is rather unlikely as possible cause. Nevertheless, at temperatures below 70 K, the hot implanted sample shows a significantly higher drain current than the cold implanted device. Therefore, hot implantation seems to improve the device performance at cryogenic temperatures but the positive effect is compensated by the 70 K trap band. For temperatures above the first peak level, the performance of both samples is the same. Thus, the key for an improved device performance at cryogenic temperatures seems to be the elimination of this trap band.

Post Implantation Annealing

Furthermore, the impact of the post implantation annealing temperature (high temperature anneal (HTA)) was studied. The HTA is applied after the implantation process itself. On one hand, it is used in order to reorganize the lattice structure which was damaged by implantation. On the other hand, it is needed in order to incorporate the interstitial dopant into the lattice.

Figure 4.18 shows the resulting I_D-DLTS spectrum for trench MOSFETs which received different HTAs. In the plot, it is HTA 1 < HTA 2 < HTA 3 < HTA 4. The trap density can be influenced by the annealing temperature but it is not a simple linear correlation. Starting from the lowest temperature, a decrease of the trap density with increasing HTA temperature is achieved. However, above a certain temperature, the trap density increases again and seems to saturate. Therefore, the optimum annealing temperature among the process variants would be HTA 2. In general, higher HTAs lead to a higher dopant activation in the lattice and at the same time to a better annealing of lattice damage. Both would lead to a change of the peak height in opposite directions. Since the trap density saturates above a certain temperature and also 100% dopant activation can be expected

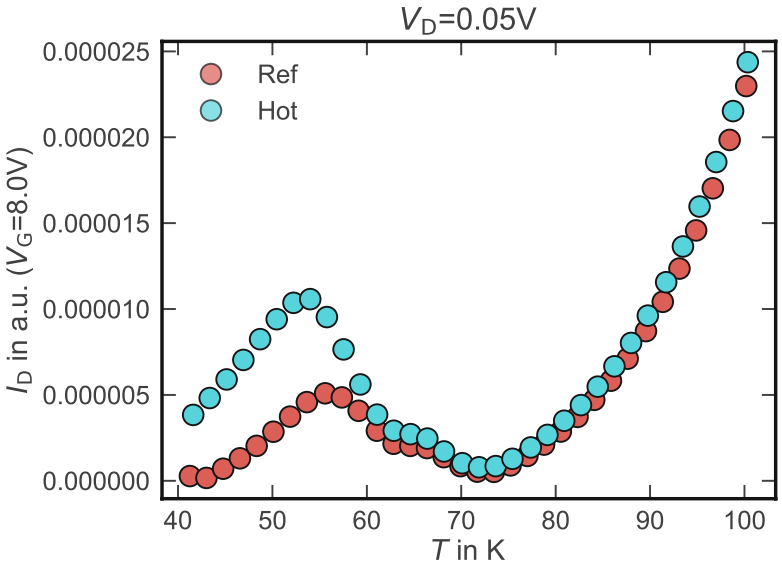


Fig. 4.17 Drain current as a function of the measurement temperature extracted for $V_G = 8\,V$. A dip in the current is observed around 70 K.

above a certain threshold, it is likely that the studied I_D-DLTS trap band is caused by Al itself or Al-related defect formation rather than lattice damage due to the implantation process.

Figure 4.19 shows the current over temperature extracted at the recovery bias from the reference I_D-V_G measurements. Since all devices have comparable threshold voltages, the currents can be directly compared to each other. It can be nicely seen that the current decreases at the same temperature where the traps become active. Below, different currents are measured following no clear trend. However, above this temperature, a higher current is observed for the devices with a lower trap density, nicely showing the impact of this trap band on the device performance at low temperatures.

Boron Implantation

In order to further investigate if the first trapping peak is caused by the Al dopant itself or related defects, Al doping was partly replaced by boron (B). B also acts as an accepter in SiC. Its ionization energy is with 285 meV to 390 meV on Si lattice sites in 4H-SiC approximately 100 meV higher than for Al. Accordingly, for the same temperature of operation, lower effective doping is expected for B implanted samples due to less ionized dopants. Further differences exist with regard to the dopant activation. B has larger ionization time constants than Al [141] and it is reported that higher HTAs are needed in order to achieve the same dopant activation (so-called electrical activity) as for Al [149–151]. At the same time, B shows more diffusion in SiC [142, 152], especially for high temperatures, making B implantation more challenging. Here, the co-implantation of Al and B was tested. Therefore, 100% Al doping, 90% Al +10% B and 70% Al +30% B were studied. The total implantation dose was kept constant. Note that the different dopant combinations lead to devices with significant differences in the threshold voltage. On one hand, this might be caused by the different electrical activity. On the other hand,

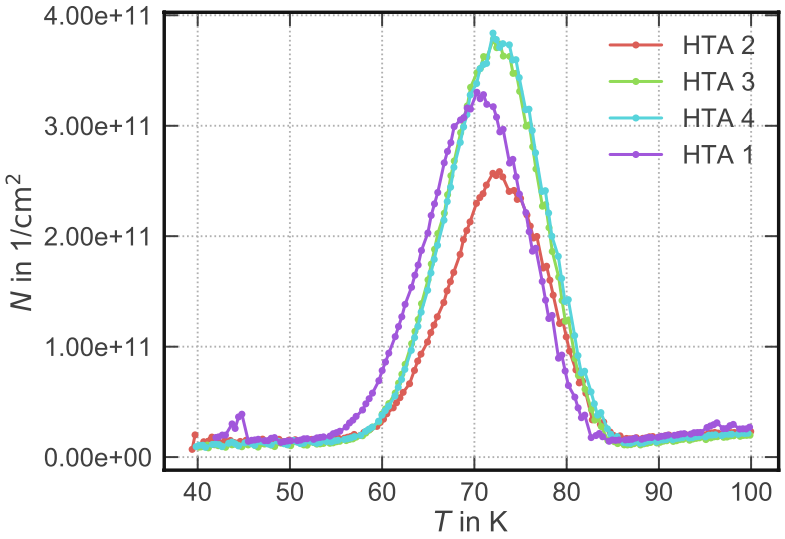


Fig. 4.18 Trap density as a function of the temperature determined with I_D-DLTS on MOSFETs with different post implantation annealing temperatures with HTA 1 < HTA 2 < HTA 3 < HTA 4. The smallest trap density is obtained with HTA 2.

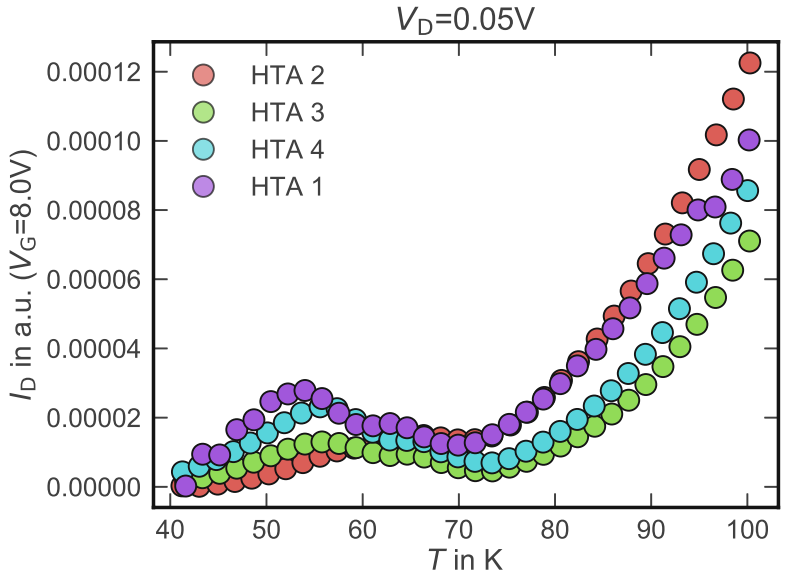


Fig. 4.19 Drain current as a function of the measurement temperature for different post implantation annealing temperatures. Increasing process numbers correspond to higher temperatures. A dip in the current is observed around 70 K.

out-diffusion of B also needs to be considered. In the samples studied here, it is not clear if any B remained in the material due to too high HTA or if the B ionization was just too small to lead to any significant contribution. Even with the threshold voltage method presented by Feldbaumer and Schroder [153] it could not be determined if B is still in the SiC lattice in the channel region. Furthermore, even though no additional peaks were

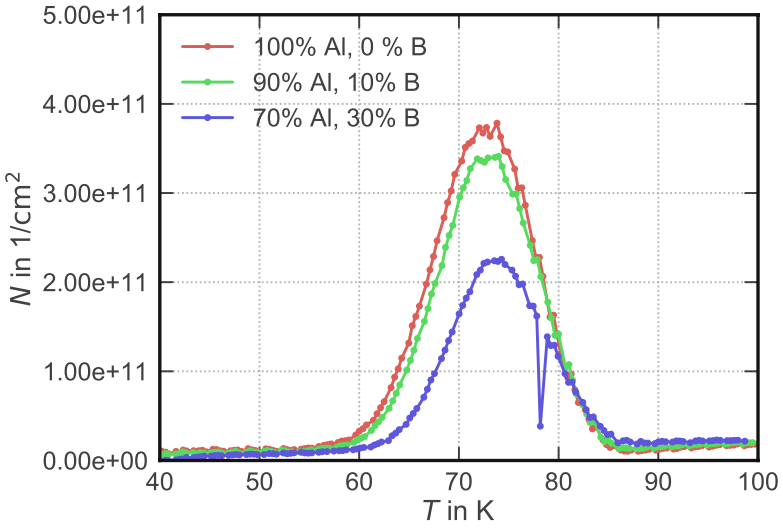


Fig. 4.20 Trap density as a function of the temperature determined with I_D-DLTS on MOSFETs with different acceptors for the p-doped region. With decreasing Al content, a decrease in the trap density is observed. Note that no information about the diffusion of B during the HTA are available so that the effective B concentration is unknown.

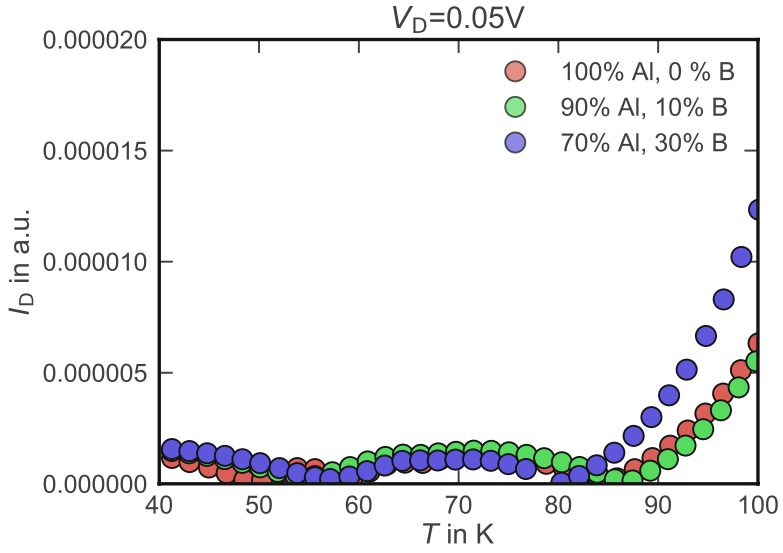


Fig. 4.21 Drain current as a function of the measurement temperature extracted at $V_G - V_{th,303K} = \text{const.}$ for an Al/B co-implantation. A low current is observed around 70 K.

detected in both DLTS (not shown) and I_D-DLTS, it is not clear if doping peaks become visible for the bias conditions used. The 100% B wafer did not result in any functioning MOSFETs.

Figure 4.20 and Figure 4.21 show the I_D-DLTS spectra and the drain current at the recovery bias as a function of the temperature. Again, a correlation between the drain

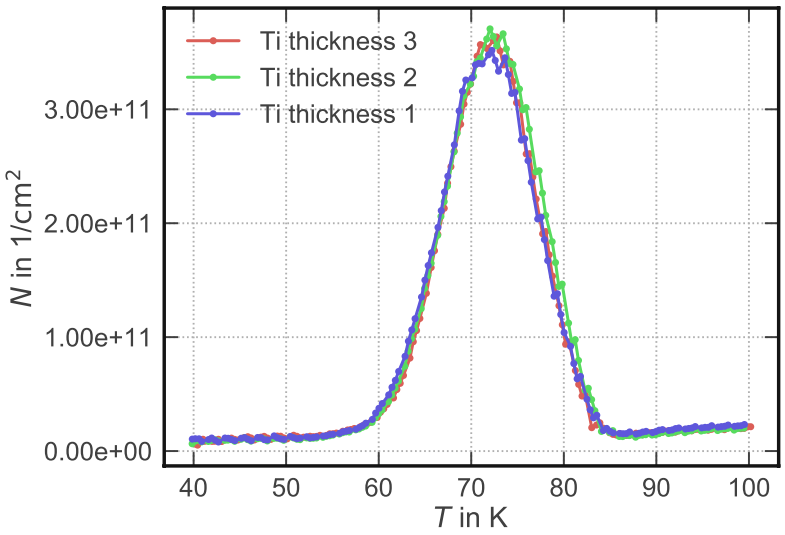


Fig. 4.22 Trap density as a function of the temperature determined with I_D-DLTS on MOSFETs with different Ti barrier thicknesses. The Ti barrier does not affect this trap band so that Ti can be excluded as possible origin of the measured peak.

current and the trap band can be seen. The trap density itself changes in a similar way as the Al dose is reduced. The less Al was implanted, the lower the measured trap density. Therefore, it is once more concluded that the detected trap band is Al related. Nevertheless, it still cannot be said for sure if the peak is caused by Al itself or Al related defects.

Titanium Contamination

As an alternative, literature reports titanium (Ti) on hexagonal lattice sites as cause for the DLTS peaks at 70 K [144, 154, 155]. No test structures were available to test this hypothesis directly. Nevertheless, to find out if Ti from the gate stack might have diffused to the interface and led to the defect level, test structures with different Ti/titanium nitride (TiN) contents were studied. Ti/TiN layers in the gate stack are commonly used as H getter. In case Ti diffuses through the gate stack towards the oxide and the interface, a larger peak should be measured for a higher Ti content. Note that no Ti has been implanted into the samples as in [144] so that only the possible Ti contamination coming from the gate stack is studied. Figure 4.22 shows the I_D-DLTS spectra for trench MOSFETs with different Ti/TiN barriers. As can be seen, all process variants result in the same trap density. Therefore, Ti diffusion through the gate stack can be excluded as possible origin.

Capacitance DLTS

Capacitance DLTS measurements were conducted to gain more information about the device doping, especially the ionization temperatures. The measurements were performed using a lockin amplifier with symmetrical pulses with a stress and recovery time of 10 s each. The heating ramp was chosen to be $\beta = 0.5\,\mathrm{K/min}$ which is the same as for the I_D-DLTS measurements. The doping was studied via DLTS measurements in the blocking direction of the MOSFET's body diode. In order to only see the bulk material and minimize the

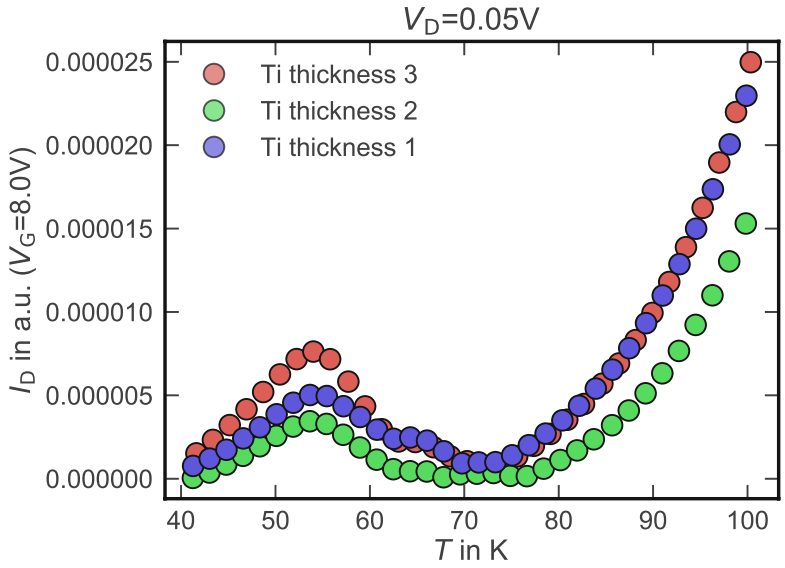


Fig. 4.23 Drain current as a function of the measurement temperature extracted at $V_G = 8\,V$ for different thicknesses of the Ti barrier in the gate stack.

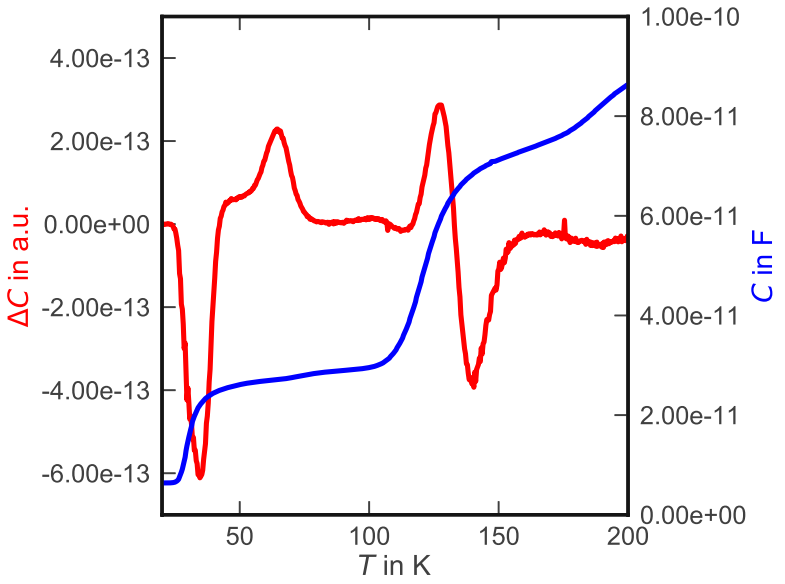


Fig. 4.24 Capacitance DLTS spectrum and capacitance as a function of the temperature for the body diode of a trench MOSFET reference sample, measured in the blocking direction. During the measurement, the gate was biased with $V_G = -9.5\,V$. Several minority and majority trap peaks are found.

influence of the interface, a negative gate bias was applied to the gate terminal. By doing so no inversion channel and therefore no current flow along the interface can form. With this configuration, it should be possible to measure levels in the bulk material only where it should be easier to identify doping levels.

The resulting DLTS spectrum and capacitance as a function of the temperature for a reference sample are depicted in Figure 4.24. Different minority and majority carrier traps were found, which will not be discussed in detail. Comparing the DLTS spectrum with the capacitance curve, correlations with peaks can be observed. Around 40 K, a peak and an increase in the capacitance are measured. This level is most likely caused by the activation of the n-doping. Around 110 K a second increase in the capacitance due to the ionization of the p-doping is observed. At the same temperature, the DLTS spectrum shows a rather small hump in the opposite direction than the 40 K-peak, which could corresponds to the Al-doping level. Therefore, the 70 K I_D-DLTS peak does most likely not show the Al dopant itself. Nevertheless, doping peaks seem to be difficult to identify with DLTS in such sophisticated test structures. For this reason, different measurement techniques such as admittance spectroscopy might be helpful to validate the doping levels.

Summary of the First Peak

The investigations on the first I_D-DLTS peak at 70 K revealed that it is related to the Al doping concentration and reduces for lower doping doses. Its activation energy is smaller than the ionization energy of the Al dopant but in a similar range. Furthermore, the trap density changes for different HTAs but has no linear correlation with this parameter. Other publications ascribed this defect level to Ti impurities. However, Ti currently appears rather unlikely as possible cause in the test structures presented here. The experimental results rather suggest an Al-related defect causing the observed DLTS peak. From the current state of knowledge, defect formation due to the presence of Al is the most likely cause for the observed trap band.

Since this trap band strongly degrades the drain current and the field effect mobility at cryogenic temperatures, it is recommended to eliminate it. However, as will be shown in one of the following sections, no direct impact on the room temperature performance is observed, at least for the channel doping split. Currently, one option under investigation to eliminate these traps is to replace the Al acceptor by a B acceptor. B atoms tend to sit on different lattice sites than Al acceptors [142] which might therefore lead to the formation of different or hopefully no trap bands. On the other hand, B p-doping is quite challenging due to a higher ionization energy (less ionized dopants at room temperature), diffusion and lower dopant activation compared to Al. Additionally, B is known to form some new defects [142, 156] of which it is not clear if they are harmful for the device performance or reliability.

4.4.4 Correlation with the Room Temperature Device Performance

As was reported in the previous section, the 70 K I_D-DLTS peak has a strong negative impact on the device performance in form of a reduced field effect mobility and a reduced drain current at cryogenic temperatures. Since SiC devices are commonly used either at room temperature or elevated temperatures, the performance in that temperature range is of higher interest. In order to determine if the negative impact is also present at room temperature or above, a simple device characterization was conducted for the channel dose split. The channel dose split resulted in a reduced trap density for a lower channel doping.

Figure 4.25 and Figure 4.26 show the Ghibaudo mobility and threshold voltage extracted at room temperature for a fixed V_{th} overdrive, obtained by wafer stepping of one column of devices from top to bottom of the wafer. For this amount of tested devices, a rather

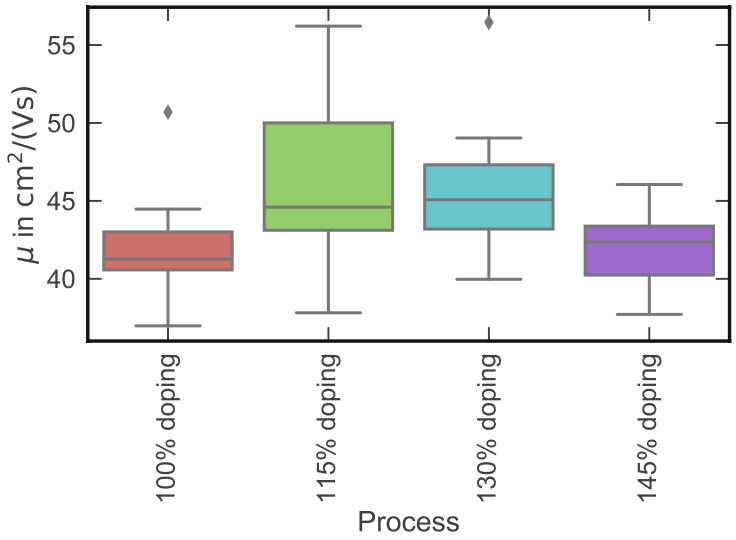


Fig. 4.25 Ghibaudo mobility extracted at room temperature for devices with different channel implantation doses. The variation from device to device is larger than between the process variants. Therefore, no significant differences can be observed.

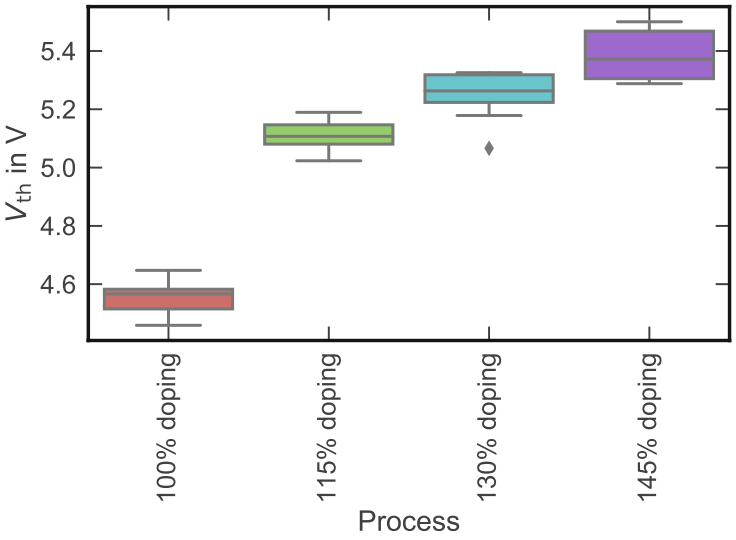


Fig. 4.26 Threshold voltage of devices with different channel implantation doses. The higher the doping concentration, the higher the threshold voltage.

high variation across the wafer is observed. The threshold voltage (Figure 4.26) shows a clear correlation with the doping concentration. The higher the doping, the higher also the threshold voltage. In contrast, for the Ghibaudo mobility, no clear trend is observed. Even though small variations might exist between the devices with the different doses, these

variations are smaller than the device to device variations. Similar observation can be found in the drain current in Figure 4.15, showing rather small differences above 70 K. In contrast, obvious differences in the trap density were measured. Therefore, it is not clear how strong the impact of this trap level on the mobility really is. Even though it has an impact on the drain current, there might be additional different impact factors which are not yet understood or identified. Nevertheless, in order to improve the inversion channel mobility in SiC devices, every reduction of mobility limiting defects is important. For this reason, it is essential to eliminate these traps if possible. Even though an improvement might not be visible for the moment being, it might become important in the future.

Comment on TDRC Results

In the first section of this chapter, TDRC results with similar trap distribution positions with regard to the temperature were presented as were observed with I_D-DLTS. There was also a peak detected at 70 K which seems to have an impact on the mobility but is not the main limiting factor. These findings resemble observations made for the 70 K I_D-DLTS peak. One might think that both trap bands could be related. However, a direct correlation of TDRC and DLTS/I_D-DLTS results is not possible because both methods show different mechanisms. TDRC measurements monitor the charge emission from trap bands whereas I_D-DLTS can monitor both. For the measurement parameters presented here, mainly capture processes are studied. Based on the NMP model described in Section 1.4, different barriers for capture and emission exist. Therefore, peaks at the same temperature for both measurements do not have to be related to the same trap band.

Additionally, the 70 K peak has also been studied in TDRC for the channel dose split (not presented) showing different results than with I_D-DLTS. Therefore, both peaks are most likely not related to each other.

4.4.5 On the Origin of the Second Peak

The second I_D-DLTS peak is observed for temperatures around 125 K. Its trap density is approximately one order of magnitude smaller than for the first peak and therefore more difficult to measure. In the same temperature range, only slight changes in the mobility over temperature are observed. Since these changes are very small and cannot be clearly assigned to one of the typical scattering mechanisms it is assumed that this trap band, if at all, only has a minor impact on the mobility. Additionally, no abnormalities in the I_D vs. T plots are observed. Therefore, it is concluded that this trap band is not limiting the field effect mobility.

Note that the recovery bias was reduced to 7 V for some devices. Because of the higher temperature, the threshold voltage is lower and therefore the point for the optimal extraction shifted as well so that for devices with lower threshold voltages an adjustment was needed. The impact of the recovery level on the resulting spectrum has been tested. It was found that as long as the recovery bias is in the rising branch of the I_D-V_G curve, the backmapping of the currents to the transfer characteristics compensates the different recovery biases, leading to identical DLTS spectra. In the following analysis, the possible origin of this trap band is studied. To do so, the same process variants as for the first trap band were investigated.

First of all, the impact of the HTA was studied. The same HTAs as previously presented were used. The results are shown in Figure 4.27. The HTA impacts the second trap band

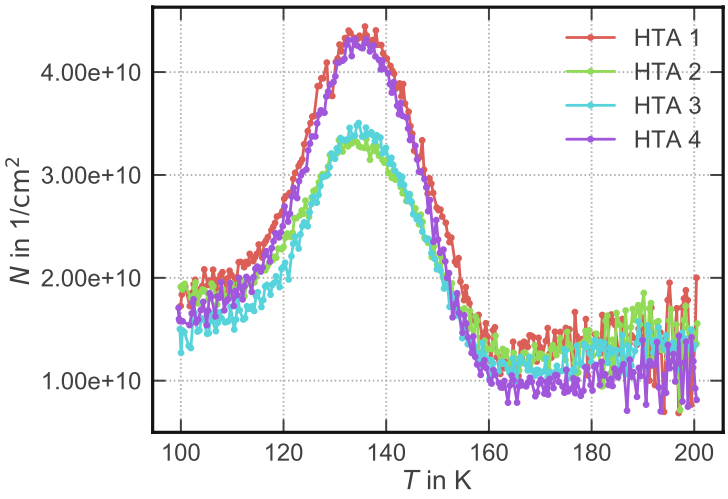


Fig. 4.27 Trap density as a function of the temperature measured with I_D-DLTS for MOSFETs with different HTAs. The lowest trap density is measured for HTA 2 and HTA 3.

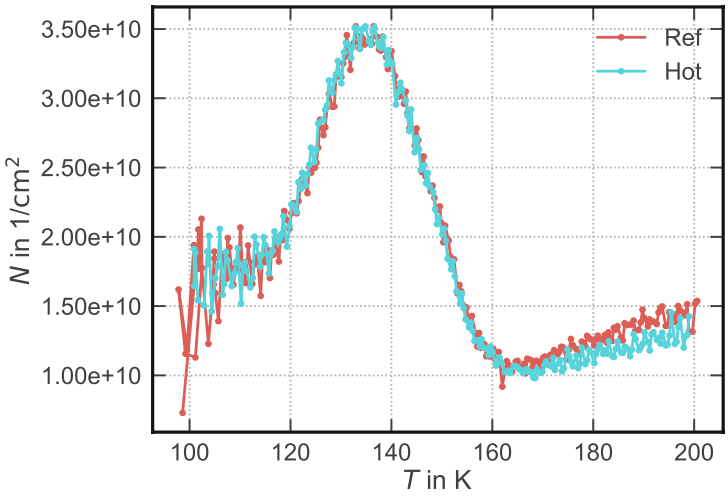


Fig. 4.28 Trap density as a function of the temperature measured with I_D-DLTS for MOSFETs implanted at different temperatures. No differences were found.

in a similar way as the first one. HTA 1 and HTA 4 result in a higher trap density whereas HTA 2 and HTA 3 reduce the density of this trap type. Since HTA 2 also leads to a minimum trap density of the first I_D-DLTS peak, this HTA seems to be the optimum in order to reduce the density of both trap bands. The fact that the trap band can be affected by the HTA after the implantation reveals that it could be related to the doping process or the dopant or dopant activation. Doping damage is unlikely as possible origin because regular and hot implanted samples do not show any differences with respect to these traps (Figure 4.28). However, due to the low channel dose compared to surrounding implanted regions it cannot be totally excluded.

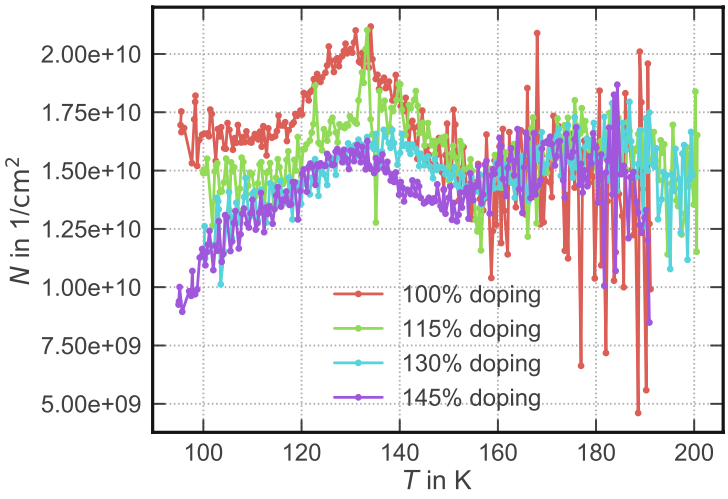


Fig. 4.29 Trap density as a function of the temperature measured with I_D-DLTS for MOSFETs with different channel implantation doses. A reduction of the trap density with increasing channel implantation dose is observed.

Furthermore, the impact of the channel doping concentration on the trap band was studied (Figure 4.29). Interestingly, a decrease of the trap density is measured with increasing channel doping. This is the opposite behavior which was observed for the trap band detected at 70 K. Therefore, when trying to reduce both peaks by adjusting the implantation dose, a trade-off is needed and an optimum needs to be determined. Additionally, the low trap density resulting from the combination of HTA and implantation dose reveals the possible existence of an additional trap distribution around 170 K. At this temperature, a very small peak in a similar range as the noise is forming. However, this hypothetical peak is not visible for any of the other processes. Therefore, it is not clear if this is an additional trap band or just an artifact.

Finally, a B/Al co-implantation split was studied. Figure 4.30 shows the resulting trap densities. In good agreement with the channel doping split devices, a reduction of the trap density with increasing Al content is observed. Since it is not clear if any B at all remained in these samples, as was mentioned in the previous section, the influence of the B cannot be determined. Nevertheless, it can be concluded that Al seems to eliminate or neutralize the trap states causing this I_D-DLTS peak. Unfortunately, the specific origin of this I_D-DLTS peak could not be identified.

4.5 Summary

TDRC and I_D-DLTS experiments were conducted to extract trap bands in 4H-SiC MOS devices and the trap bands correlated with the room temperature performance. With TDRC, two trap distributions were identified: One interface trap band with $E_A - E_C = 0.13\,\text{eV}$ and one NIT distribution with $E_A - E_C \approx 0.3\,\text{eV}$. The first trap band seems to have a weak influence on the room temperature mobility but cannot be the main mobility degrading defect. NITs cannot be studied in detailed with TDRC because this type of defect is barely detectable with this method.

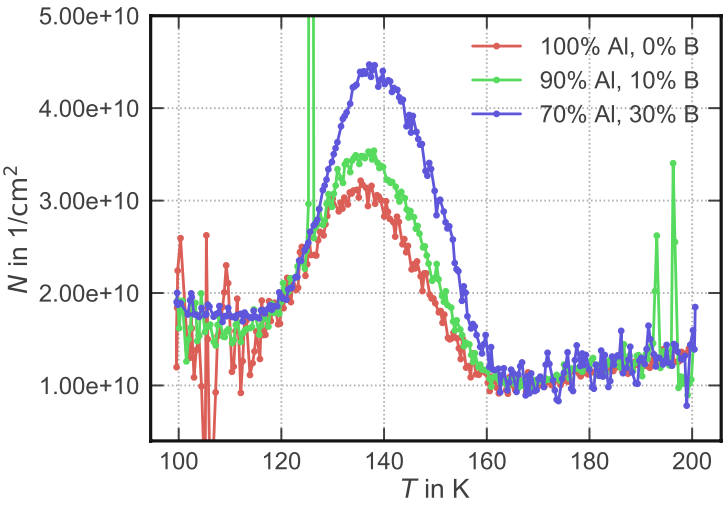


Fig. 4.30 Trap density as a function of the temperature measured with I_D-DLTS for MOSFETs with Al/B co-implantation. A reduction of the trap density with increasing Al dose is observed.

Summarizing the I_D-DLTS results, two trap bands were detected. The first peak in the spectrum occurs at around 70 K and it is most likely in any form related to the Al-doping. This trap band significantly influences the field effect mobility and therefore the drain current at cryogenic temperatures. It can be reduced by decreasing the p-doping concentration and by adjusting the post implantation anneal to the optimal temperatures. At room temperature, however, no direct correlation between the density of these traps and the mobility is detected anymore.

Additionally, a second peak around 125 K was observed whose origin could not be determined. The trap density of the second trap band is around one order of magnitude smaller than that of the first one. It does not seem to have any direct impact on the drain current and the field effect mobility at this temperature. It can be reduced by increasing the Al doping concentration. Therefore, for optimizing both trap bands, a trade-off is necessary in order to determine the optimal doping concentration. One possibility to improve the inversion channel mobility might be replacing the Al doping by B doping.

CHAPTER 5

Conclusion and Outlook

In this thesis, studies on the reliability and charge carrier mobility in 4H-SiC trench MOSFETs were presented. Numerous differently processed MOSFETs were investigated which mainly differ in their post oxidation annealing, oxidation technique and doping procedure. Numerous experiments were conducted in a wide temperature range from close to the absolute zero, over room temperature, up to 200°C in order to asses the device performance and reliability. The characterization at room temperature or above is of special interest for addressing and understanding the device behavior with special focus on its reliability at application-relevant conditions. In contrast, cryogenic temperatures are used to obtain a better understanding of underlying trapping effects. At low temperatures, capture and emission time constants become longer such that trapping-related processes are significantly slowed down and become experimentally accessible. Therefore, it is possible to determine different trap bands and their impact on the device performance and reliability.

The room temperature experiments focus on the full device characterization in form of device reliability and performance studies. The results can be summarized as follows:

- Device performance and reliability studies cannot be separated from each other. It was demonstrated that improved inversion channel mobility may be accompanied with reduced device reliability in form of e.g. bias temperature instability or gate oxide tunneling.
- The promising post oxidation anneals in NH_3 and $NO + NH_3$ were investigated and resulting trench MOSFETs compared to the common NO annealed devices. It was found that NH_3 containing POAs are beneficial for the device performance. Significantly improved inversion channel mobilities, on-resistances and reduced subthreshold sweep hysteresis were found. On the other hand, a higher bias temperature instability was measured and a lower gate oxide reliability detected.
- Trap assisted tunneling in NH_3 annealed trench MOSFETs was studied and explained. For annealing temperatures above a certain temperature threshold, NH_3 containing POAs lead to the formation of hydrogen related defects in significant amounts. These defects enable trap assisted gate oxide tunneling already at rather low gate biases. NO annealed MOSFETs do not show such a behavior.
- Additionally, the gate oxide breakdown was studied. Experimental data were presented supporting theoretical breakdown models from literature.

- MOSCAPs with plasma grown oxides were studied with focus on the distribution of interface traps and compared to thermal oxides. Regarding the interface trap density, no differences were found. Additionally, MOSFETs with CVD oxide and plasma grown oxide show similar device performance.

- The differences and similarities of bias temperature instability in SiC and Si power MOSFETs were studied. An intrinsic trap band in SiO_2 in both technologies causes PBTI. Because of the different band structures, SiC devices drift more than Si devices.

The second part of this thesis deals with the cryogenic characterization of 4H-SiC trench MOSFETs and mainly focuses on the underlying trap distributions in correlation with the inversion channel mobility. The results can be summarized as follows:

- The mobility as a function of the ambient temperature revealed surface roughness, Coulomb scattering and doping as mobility limiting factors.

- With the help of TDRC measurements, an interface trap band and a near interface trap band were identified. The first seems to have a weak impact on the channel mobility at room temperature but cannot explain the large mobility differences between NH_3 and NO annealed MOSFETs.

- I_D-DLTS studies also revealed two trap bands. Both are affected by the Al doping concentration in opposite directions. The first trap band degrades the drain current and the field effect mobility at cryogenic temperatures.

Even though important contributions towards the understanding of mobility and reliability limitations in 4H-SiC trench MOSFETs have been presented, further research is needed in order to make use of the full potential of this material. First of all, other POAs need to be studied and understood in order to further reduce or, in the best case, totally eliminate the trap bands found in this thesis. Additionally, other process optimizations might be needed, especially with regard to the channel doping. It has been found that the Al doping is related to mobility limiting defects. Therefore, methods need to be found to minimize the formation of Al-related and implantation related defects. One possibility, which needs to be studied in detail, might be exchanging the Al dopant by B. At the moment, B doping is quite challenging due to its higher activation and ionization energy and its ability to diffuse in 4H-SiC. Last but not least, it might be beneficial to assess the old cryogenic SRH based measurement techniques with the NMP model. The NMP model is valid for a larger amount of trap types and can therefore give additional valuable information about the defect levels, helping to identify and understand them.

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List of Publications

Journal Contributions

J. Berens, F. Rasinger, T. Aichinger, M. Heuken, M. Krieger, and G. Pobegen. Detection and cryogenic characterization of defects at the SiO_2/4H-SiC interface in trench MOSFET. In: *IEEE Transactions on Electron Devices* (2019), pp. 1–5. ISSN: 00189383. DOI: 10.1109/TED.2019.2891820.

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J. Berens, S. Bichelmaier, N. K. Fernando, P. K. Thakur, T.-L. Lee, M. Mascheck, T. Wiell, S. K. Eriksson, J. M. Kahk, J. Lischner, M. V. Mistry, T. Aichinger, G. Pobegen, and A. Regoutz. Effects of nitridation on SiC/SiO_2 structures studied by hard x-ray photoelectron spectroscopy. In: *Journal of Physics: Energy* 2.3 (May 2020), p. 035001. DOI: 10.1088/2515-7655/ab8c5e. URL: https://doi.org/10.1088%2F2515-7655%2Fab8c5e.

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List of Figures

Symbols

Symbol	Description	Unit
A	constant	V
A	effective area	cm^2
C'_{OX}	oxide capacitance per area	$\mathrm{F\,cm}^{-2}$
C	capacitance	F
D_{it}	density of interface traps	$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$
$E_{\mathrm{A,Al}}$	activation energy of the Al dopant	eV
$E_{\mathrm{A,i}}$	activation energy i	eV
E_{A}	activation energy	eV
E_{B}	band gap energy	eV
$E_{\mathrm{C,SiC}}$	energy at the bottom of the conduction band of SiC	eV
$E_{\mathrm{C,Si}}$	energy at the bottom of the conduction band of Si	eV
E_{C}	energy at the bottom of the conduction band	eV
E_{F}	Fermi energy	eV
E_{OX}	oxide field	$\mathrm{MV\,cm}^{-1}$
E_{T}	trap energy	eV
E_{V}	energy at the top of the valence band	eV
$E_{\mathrm{i,j}}$	transition barrier from state i to state j	eV
I_{TDRC}	TDRC current	A
I_{D}	drain current	A
I_{G}	gate current	A
J	current density	$\mathrm{A\,cm}^{-2}$
L	channel length	m
M	voltage acceleration factor (BTI exponential approach)	V^{-1}
N_{A}	acceptor concentration	cm^{-3}
N_{D}	donor concentration	cm^{-3}
N_{T}	trap density	cm^{-3}
N_{t}	number of trapped charges	cm^{-2}
N	time evolution factor (BTI exponential approach)	s^{-1}
Q	charge	C
R_{on}	on-resistance	Ω
R	ratio of the curvatures of the trap parabolas in the NMP model	1
$S(T)$	DLTS spectrum as a function of the temperature T	
S	relaxation energy in the NMP model	eV
T_{ref}	reference temperature	K
T	temperature	K
V_{DS}	drain-source voltage	V

Symbol	Description	Unit
V_{ch}	charging voltage	V
V_{dis}	discharging voltage	V
V_{p}	DLTS pulse stress bias	V
$V_{\mathrm{th}}^{\mathrm{G}}$	threshold voltage extracted by the method of Ghibaudo	V
V_{th}	threshold voltage	V
V_{D}	drain voltage	V
$V_{\mathrm{G,ref}}$	refrence gate voltage	V
V_{GS}	gate-source voltage	V
V_{Grec}	DLTS recovery bias	V
$V_{\mathrm{G}}^{\mathrm{str}}$	stress voltage	V
V_{G}	gate voltage	V
V	voltage	V
W	channel width	m
ΔC	capacitance shift/transient	F
ΔT_{TDRC}	TDRC half width	K
$\Delta V_{\mathrm{th,\ max}}$	maximum threshold voltage shift	V
ΔV_{th}	threshold voltage shift	V
Φ_{ox}	tunneling barrier height	eV
Θ	mobility reduction factor	V^{-1}
β	temperature ramping rate	$\mathrm{K}/\,\mathrm{min}$
γ	power-law exponent describing the temperature dependence of the field effect mobility	1
$\hbar$	reduced Planck constant (6.58)	$\mathrm{eV\,s}$
μ_{Coulomb}	mobility scattering component of Coulomb scattering	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{ac}	mobility scattering component of surface acoustic phonons	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{bulk}	mobility bulk scattering mechanisms	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{ref}	mobility at a reference point, e.g. at a reference temperature	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{sr}	mobility scattering component of surface roughness	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_n	electron mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ	mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
ν	attempt-to-escape frequency	$\mathrm{s^{-1}}$
σ	standard deviation of the normal distribution	eV
σ	capture cross section	$\mathrm{cm^{-2}}$
τ_0	inverse attempt frequency/effective time constant	s
τ_{i}	time constant of the defect level i	s
τ	time constant	s
ε_0	vacuum permittivity $(88.54 \cdot 10^{-15})$	$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$
$\varepsilon_{\mathrm{r,SiC}}$	relative permittivity of SiC (≈ 10)	1
ε	capture/emission barrier	eV
e	emission rate	$\mathrm{s^{-1}}$
g_{m}	transconductance	$\mathrm{A\,V^{-1}}$
k_{B}	Boltzmann constant $(86.17 \cdot 10^{-6})$	$\mathrm{eV\,K^{-1}}$
$k_{\mathrm{i,j}}$	transition rate from state i to state j	$\mathrm{s^{-1}}$

Symbol	Description	Unit
m^*	effective electron mass (SiC: 0.39 times the electron mass)	kg
m	voltage acceleration exponent (BTI power law appraoch)	1
m	slope of a straight line	
n_i	intrinsic carrier density	cm^{-3}
n	time evolution exponent (BTI power law approach)	1
q	elementary charge ($1.602 \cdot 10^{-19}$)	C
t_mes	DLTS measurement time window length	s
t_ref	reference time	s
t	time	s
$w(t)$	correlation function as a function of the time t	

Acronyms

I_D-DLTS drain current deep level transient spectroscopy.

I_D-V_G transfer characteristic.

AC alternating current.

Al aluminum.

Ar argon.

B boron.

BFOM Baliga figure of merit.

BTI bias temperature instability.

C carbon.

CET capture/emission time.

CTL charge transistion level.

CV capacitance-voltage.

CVD chemical vapor deposition.

DC direct current.

DFT density functional theory.

DLTS deep level transient spectroscopy.

DMOSFET double-diffused metal oxide semiconductor field effect transistor.

DRC dielectric relaxation current.

FET field effect transistor.

FN Fowler-Nordheim.

GaAs gallium arsenide.

GaN gallium nitride.

GOX gate oxide.

H hydrogen.

H-E' hydroxyl-E' center.

H_2 dihydrogen.

HAXPES hard x-ray photoelectron spectroscopy.

HB hydrogen bridge.

HTA high temperature anneal.

IDRC isothermal dielectric relaxation current.

IGBT insulated-gate bipolar transistor.

MOS metal oxide semiconductor.

MOSCAP metal oxide semiconductor capacitor.

MOSFET metal oxide semiconductor field effect transistor.

MSM measure-stress-measure.

N nitrogen.

N_2 dinitrogen.

N_2O nitrous oxide.

NBTI negative bias temperature instability.

NH_3 ammonia.

NIT near interface trap.

NMP non-radiative multi-phonon.

NO nitric oxide.

O oxygen.

OV oxygen vacancy.

PBTI positive bias temperature instability.

PBTS positive bias temperature stress.

PGOX plasma oxide.

PMA post metallization anneal.

POA post oxidation anneal.

$POCl_3$ phosphoryl cloride.

Si silicon.

SiC silicon carbide.

SiO_2 silicon dioxide.

SMU source-measurement unit.

SNR signal-to-noise ratio.

SRH Shockley-Read-Hall.

TAT trap assisted tunneling.

TDDB time dependent dielectric breakdown.

TDRC thermal dielectric relaxation current.

TEOS tetraethylorthosilicat.

Ti titanium.

TiN titanium nitride.

WBG wide band gap.

XPS X-ray photoelectron spectroscopy.

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Language Skills	German: native speaker English: highly fluent speaker (12 years, equivalent to level C1) French: basic working knowledge (7 years, DELF Niveau B1) Spanish: basic command (2 years)
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National Instruments	Basic knowledge of NI Diadem und NI LabVIEW
Programming Languages	C, C++, Python
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