DISSERTATION

Hot-Carrier Degradation in Planar and Trench Si-MOSFETs

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Univ.Prof. Dipl.-Ing. Dr. techn. Tibor GRASSER
Institut für Mikroelektronik

eingereicht an der Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik

von

Dipl.-Ing. Bernhard Ruch

Georgibergstraße 10
A-9122 St. Kanzian am Klopeiner See, Österreich

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To my beloved parents,
Gertraud and Friedrich

Disclaimer

Central findings of this thesis base on material which has been partly published in journal publications and conference proceedings. According to the consensus of several guidelines of Austrian funding agencies and Austrian Universities regarding proper scientific work, the ideas of these publications are re-used with explicit citation at several positions in this thesis. The thesis puts the individual topics of the publications together with unreported topics into a larger context.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

February 4, 2021

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Abstract

As transistor technologies evolve, reliability is, apart from performance, a main driver of development. For the past decades, research on the degradation of the silicon-oxide interface of metal oxide semiconductor (MOS) structures has put a lot of focus on the hot-carrier degradation (HCD) phenomenon. Therefore, a lot of knowledge about this effect has been gathered so far. This work investigates properties of HCD which have so far still not been understood well. One aspect is the temperature dependence in lateral long-channel devices. Although it is known that increasing temperatures suppress hot-carrier stress (HCS), few details about the nature of the defects created at various temperatures are known. Using spectroscopic charge pumping (SPCP), it is shown that the energetic spectra of the traps after HCS are influenced by the stress temperature in the same way as by the stress duration. It is therefore concluded that temperature is only an acceleration factor of HCD and does not influence the types of defects which are created. An efficient measurement strategy is developed in order to minimize and thereby quantify the number of defects which are lost to recovery after stress before they can be characterized. This setup includes the use of poly-silicon heater structures where the device temperature can be changed by up to 200 °C within seconds.

Another little explored detail of HCD is the interplay of border and interface traps, which is investigated on lateral transistors. It is shown that newly created border traps, electrically active defects which are located near the interface in the oxide, have a stronger voltage than time dependence.

Generally, the investigation of defects requires models to describe their interactions with the carriers of the semiconductor. For interface defects, the Shockley Read Hall (SRH) model is usually used to model the defect time constants. Unfortunately, this model disregards reconfigurations in the atomistic structure. In an experimental benchmark, the SRH model is compared to the more complete non-radiative multi-phonon (NMP) model. The latter models the structural relaxations by a relaxation energy. Using this relaxation energy, a bridge between the SRH and NMP models is built. This is realized by modifying the SRH cross sections by an Arrhenius factor which employs the NMP relaxation energy. It is shown that although all models yield slightly different results, interpretations of the data of all models leads to very similar conclusions. This investigation explains why the SRH model has persisted in the description of defect interaction for a long time although it does not consider relaxation energies.

Apart from lateral devices, compensated trench MOSFETs are investigated. So far, few investigations of HCD have focused on these complex two-dimensional structures. Therefore, the charge pumping (CP) method is adapted for these devices first. It is shown that the edges of the structures can distort the measurement results and a model for the removal of these unwanted influences is presented. On the basis of the reverse bias CP method, an experimental approach, which yields localized profiles near the gate base point of trench devices, is developed. Using this new measurement method, different HCS conditions and various geometrical variations of the compensated trench device are investigated. The results are compared to two drift-diffusion quantities, the vertical electrical field and the impact ionization rate, which are obtained from technology computer-aided design (TCAD) investigations of the device. It is shown that these simple TCAD simulations cannot accurately predict the intensity and location of the stress damage.

Kurzfassung

Bei der Entwicklung von neuen Transistortechnologien ist ein Hauptaugenmerk die Verbesserung der Zuverlässigkeit. In den letzten Jahrzehnten hat sich die Erforschung der Degradation an der Silizium-Oxid-Grenzfläche von Metal Oxid Halbleiter (MOS)-Strukturen auf das Hot-Carrier Degradation (HCD)-Phänomen konzentriert. Daher gibt es bisher viel Literatur zu diesem Effekt. Die vorliegende Arbeit konzentriert sich auf Eigenschaften von HCD, die bisher noch nicht gut untersucht sind. Ein Aspekt ist die Temperaturabhängigkeit in lateralen Lang-Kanal Transistoren. Obwohl bekannt ist, dass steigende Temperaturen Hot-Carrier Stress (HCS) unterdrücken, sind nur wenige Details über die Art der Defekte bekannt, die bei verschiedenen Temperaturen entstehen. Mit spektroskopischem Charge Pumping (CP) wird gezeigt, dass die energetischen Spektren der Defekte nach HCS von der Stresstemperatur in gleicher Weise wie von der Stressdauer beeinflusst werden. Daraus kann geschlossen werden, dass die Temperatur nur einen Beschleunigungsfaktor von HCD darstellt und keinen Einfluss auf die durch den Stress entstandenen Defekttypen hat. Es wird eine effiziente Messstrategie entwickelt, um die Anzahl der Defekte zu minimieren und die Anzahl der Defekte zu quantifizieren, die durch die Recovery nach dem Stress verloren gehen, bevor sie charakterisiert werden können. Dieser Aufbau nutzt Polysilizium-Heizstrukturen, bei denen die Bauteiltemperatur innerhalb von Sekunden um bis zu 200 °C verändert werden kann.

Ein weiteres wenig erforschtes Detail von HCD, das an lateralen Transistoren untersucht wird, ist das Zusammenspiel von Border und Interface Traps. Es wird gezeigt, dass durch den Stress erzeugte Border Traps, welche elektrisch aktive Defekte darstellen, die sich in der Nähe der Grenzfläche im Oxid befinden, eine starke Spannungsabhängigkeit aufweisen.

Die Untersuchung von Defekten erfordert Modelle zur Beschreibung ihrer Wechselwirkungen mit den Ladungsträgern des Halbleiters. Für Grenzflächendefekte wird üblicherweise das Shockley Read Hall (SRH)-Modell verwendet, um die Zeitkonstanten der Defekte zu modellieren. Leider vernachlässigt dieses Modell atomare Strukturänderungen. In einem experimentellen Vergleich wird das SRH-Modell dem kompletteren Non-Radiative Multi-Phonon (NMP)-Modell gegenübergestellt. Letzteres modelliert die Strukturrelaxationen durch eine Relaxationsenergie. Mit dieser Relaxationsenergie wird eine Brücke zwischen dem SRH- und dem NMP-Modell geschlagen. Dies wird umgesetzt, indem die SRH-Wirkungsquerschnitte durch einen Arrhenius-Faktor modifiziert werden, der die NMP-Relaxationsenergie enthält. Es wird gezeigt, dass, obwohl alle Modelle leicht unterschiedliche Ergebnisse liefern, Interpretationen der Daten aller Modelle zu ähnlichen Schlussfolgerungen führen. Daher hat sich das SRH-Modell lange Zeit in der Beschreibung der Defektwechselwirkung bewährt, obwohl es die Relaxationsenergie nicht berücksichtigt.

Neben lateralen Bauelementen werden auch kompensierte Trench-MOSFETs untersucht. Bislang haben sich nur wenige Untersuchungen von HCD auf diese komplexen zweidimensionalen Strukturen konzentriert. Daher wird die CP-Methode zunächst für diese Bauelemente angepasst. Es wird gezeigt, dass die Ränder der Strukturen die Messergebnisse verfälschen können und es wird ein Modell zur Beseitigung dieser unerwünschten Einflüsse vorgestellt. Auf der Basis der Reverse-Bias CP-Methode wird ein experimenteller Ansatz entwickelt, der lokale Defektdichten in der Nähe des Gate Fußpunkts von Trench-MOSFETs liefert. Mit dieser neuen Messmethode werden verschiedene HCS-Bedingungen und verschiedene geometrische Variationen des kompensierten Trench-MOSFETs untersucht. Die Ergebnisse werden mit zwei Drift-Diffusionsgrößen verglichen, dem vertikalen elektrischen Feld und der Stoßionisationsrate, die aus Technology Computer-Aided Design (TCAD)-Untersuchungen der Struktur gewonnen werden. Es wird gezeigt, dass diese einfachen TCAD-Simulationen die Intensität und den Ort der Spannungsschädigung nicht genau vorhersagen können.

Contents

CHAPTER 1

Introduction

Chapter Contents

> *And another one gone, and another one gone*
> — Queen, *Another One Bites the Dust*

As in all disciplines of engineering, reliability has always been a main focus in the development of semiconductors. While Queen's John Deacon certainly did not have semiconductors in mind when he wrote the 1980 hit "Another One Bites the Dust", "and another one gone, and another one gone" was what reliability engineers in the late 1970s and early 1980s might have thought when many more devices failed with decreasing size according to Moore's law. A main driver of device failure in this case was certainly hot-carrier degradation (HCD) [1], which has been in the spotlight ever since. This is because the shrinking of cell structures at unchanged operational voltages inevitably leads to increased drain-source fields facilitating HCD. Although countless authors [2]–[7] have investigated HCD in the meantime, some questions have still not been answered. This thesis aims to tackle some major open issues like the amount of border and interface defects generated by HCD and their voltage and time dependence, as well as the general temperature dependence from an experimental perspective. Furthermore, hot-carrier stress

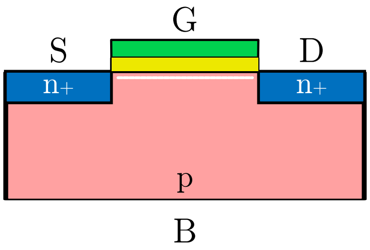

Fig. 1.1. Lateral n-channel MOSFET with a horzontal channel (white) between drain (D) and source (S). The metal gate (G, green) controls the channel by inducing a field by charging the gate capacitance (yellow: oxide). Source is usually tied with body (B).

(HCS) damage in compensated trench devices, complex two-dimensional structures used in low-voltage power electronics, is spatially profiled. The respective stress conditions are then investigated with drift diffusion technology computer-aided design (TCAD) simulations. Over the course of this journey, new measurement concepts have been developed and established methods adapted.

1.1. Power Devices

In the past decades, MOSFETs have dominated the market for switching applications of high power loads along with IGBTs [8]. Especially in scenarios where the required breakdown voltages are low, Silicon MOSFETs prevail, as for example in the power management of computer motherboards or automotive electronics. The main focus of this thesis are low-voltage Silicon n-channel MOSFETs.

1.1.1. Lateral Structures

Lateral MOSFETs are not state-of-the-art transistors for power applications. On the one hand, a lot of wafer area is needed for the MOSFET channel. On the other hand, advanced layouts like compensated trench devices (cf. Section 1.1.3) allow for higher performance. Nevertheless, these simple structures, as shown in Figure 1.1, allow for easier investigation of fundamental physical phenomena like HCD. This is due to their simpler device physics and the fact that a lot of literature is available for most degradation mechanisms. In our case, the metal oxide semiconductor (MOS) stack is comprised of a 30 nm SiO_2 and highly n-doped poly-crystalline silicon. The latter acts as gate electrode.

In order to be able to change device temperatures, poly-silicon heater structures are often used in the experiments described in this work. In principle, a standard MOS structure is embedded between trenches which are filled with highly resistive poly-crystalline silicon and can be contacted on both ends. By forcing a current through these heater structures, the device temperature is increased by Joule heating. Following a calibration procedure [10], [11], well-determined temperature increases up to 200 °C and much more can be achieved. The major advantage of using such structures is that the wafer under test does

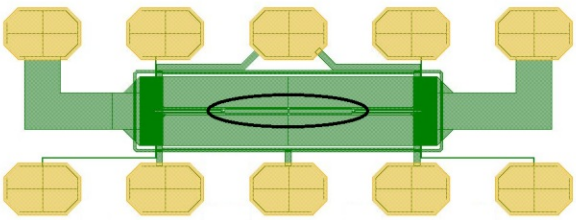

Fig. 1.2. Lateral MOSFET embedded in a poly-silicon heater structure. The MOSFET is shown by the ellipse. Identical devices are used in [9].

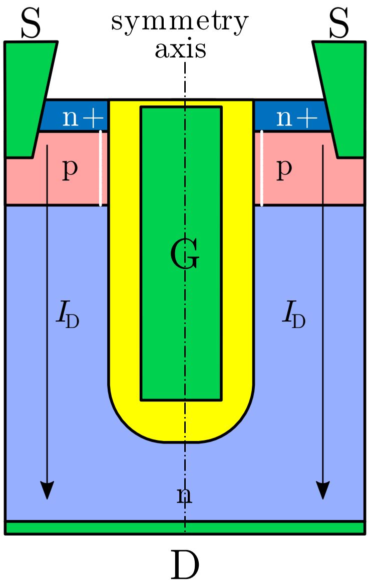

Fig. 1.3. Schematic cross section of a simple trench MOSFET. The current flows between the top and bottom of the chip. In the figure, the inversion channel is marked by a white line.

not have to be heated as a whole. Also, large temperature changes can be achieved within seconds [12], even while electrical measurements are performed simultaneously on the MOSFET itself.

1.1.2. Trench Devices

Trench MOSFETs (often referred to as UMOSFETs) are vertical devices, i.e. the current flow in the on-state is directed between the top and bottom of the die. From a fabrication point of view this means that the device is built starting from the drain. On top, the trenches are etched, respective doping profiles implanted and source contacts added (Figure 1.3). As in all MOSFETs, the gate, embedded in the trench within the gate oxide, opens or closes the channel between source (S) and drain (D) which is shown in Figure 1.3 as a white line in the p-doped body region. The highly doped n-region on top of the device acting as source is shorted with the body region during fabrication with a metal contact.

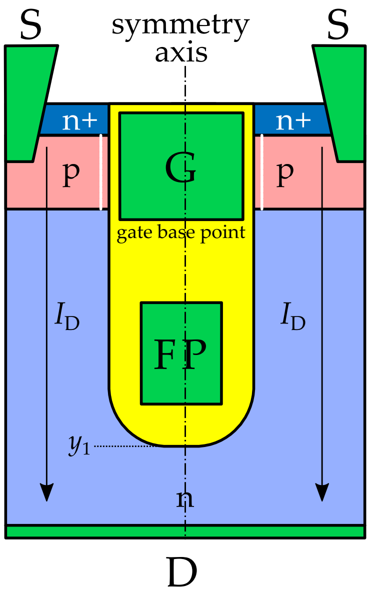

Fig. 1.4. Schematic cross section of the compensated trench MOSFET incorporating a field-plate (FP). In this design, the current flow I_{D} is vertical, with drain on the bottom and source on the top. The channel in the p-doped body region is visualized with a white line and the gate is, like the FP, embedded in the SiO_2 trench. y_1 refers to the y-position of the trench bottom.

Variations of this design exist, where body and source are contacted separately, which can is an advantage for charge pumping (CP) (cf. Section 5.2).

Since the thinning process of wafers is limited to a certain threshold due to mechanical stability of the wafer, the n-doped drift region below the trench is not to scale in Figure 1.4. Generally, the depth of the trench is much smaller than the thickness of the actual n-doped drain drift region. Also, the whole trench structure is symmetrical along the vertical axis. This symmetry can be utilized in simulations where usually only one half of the structure is analyzed. A main advantage of trench devices compared to lateral devices is the tremendously increased packing density of channel area on the wafer, as mentioned in Section 1.1.1. By flipping the channel 90 degrees, it occupies an area within the silicon rather than on its surface. Thus, production costs can be significantly reduced.

1.1.3. Compensated Trench Concept

Compensated trench MOSFETs do not differ from standard trench devices with one exception. Additionally to the gate electrode, a FP electrode is embedded within SiO_2 in the trench. Its purpose is inducing a field into the drain region which compensates the electric field of the body-drain p-n junction during reverse biased operation. Generally, the current flow in a MOSFET is blocked during the off-state by this junction. The design shown in Figure 1.4 incorporates the additional FP which increases the breakdown voltage of the device due to a compensation principle compared to uncompensated designs as described in Section 1.1.2. The compensation principle [13] can be explained by investigating a

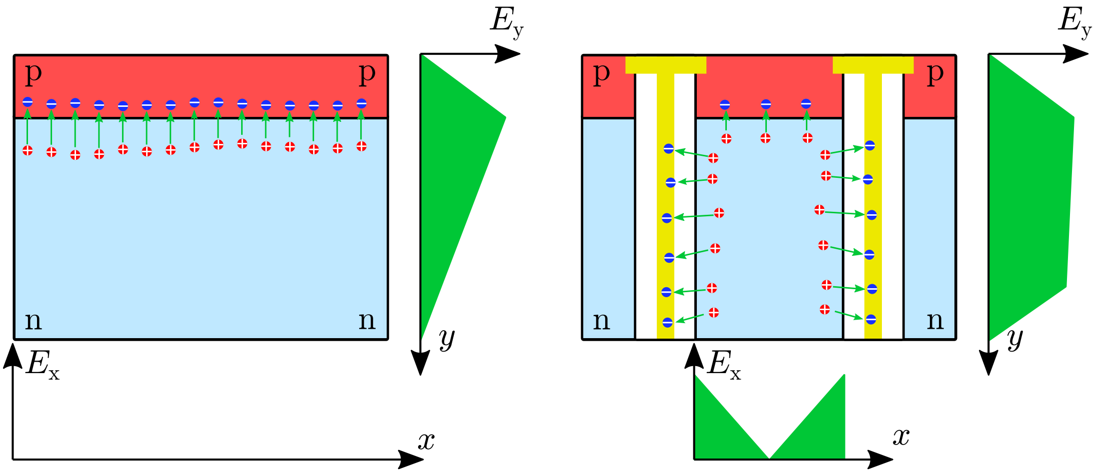

Fig. 1.5. Schematic visualization of the compensation principle on the example of a p-n junction. The x-component of the electric field in uncompensated (left) reverse biased diodes is zero while the compensated (right) structure has a non-zero electric field when reverse-biased. A compensating horizontal field is induced by an electrode (yellow) connected to the p-region potential, which is embedded in an insulator (white). The reverse bias for both structures in this visualization is selected such that the value of the peak y-component of the electric field is equal.

simple p-n junction with constant p- and n-doping concentrations (Figure 1.5): Such an abrupt junction, as known from basic semiconductor literature [14], has a fairly simple electric field behavior when reverse biased. Figure 1.5 (left) assumes a reverse bias just below the breakdown voltage. The vertical y-component of the electric field peaks at the junction where further increasing of the reverse bias would increase this peak which would in turn trigger an avalanche breakdown of the junction. Along the x-axis, the structure is identical at every position. Thus, due to symmetry, no horizontal electric field is expected since the reverse bias is applied vertically. Introducing a field plate Figure 1.5 (right), which is an electrode embedded in an oxide, opens the possibility to induce a horizontal field. The electrode is shorted with the potential of the p-region. Thus, in the reverse bias condition, a negative field is induced. With this additional horizontal field, the spatial carrier distribution during reverse bias is modified. Due to a wider spread of carriers, the vertical electrical field also spreads as dictated by the Poisson equation. In order to reach the peak of the electric field which would cause avalanche, a much higher bias is therefore necessary in the compensated diode compared to the uncompensated structure. Consequently, the compensated structure has a significantly increased breakdown voltage. In the actual MOSFET structure, the FP acts as the compensating electrode. The fields are shown in Figures 1.6 and 1.7.

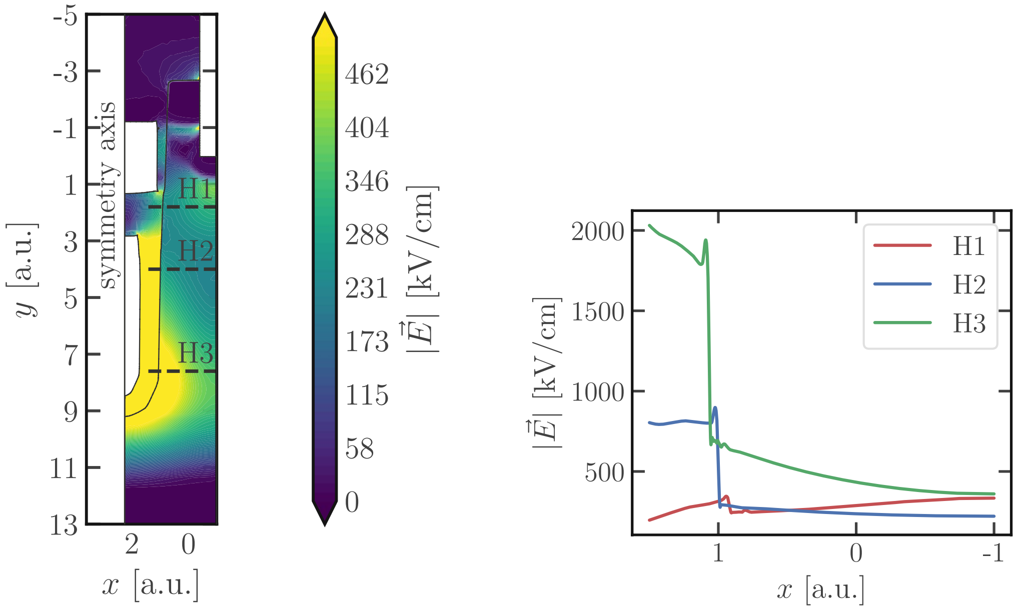

Fig. 1.6. Simulation of the magnitude of the electric field in the compensated trench device at a drain voltage which causes breakdown. All contacts besides drain are grounded. In order to highlight the relevant electric filed range, the color bar in the left figure is capped at 500 kV cm^{-1} and values above this limit are shown in yellow. The electric field in the three horizontal cuts is shown in the right figure.

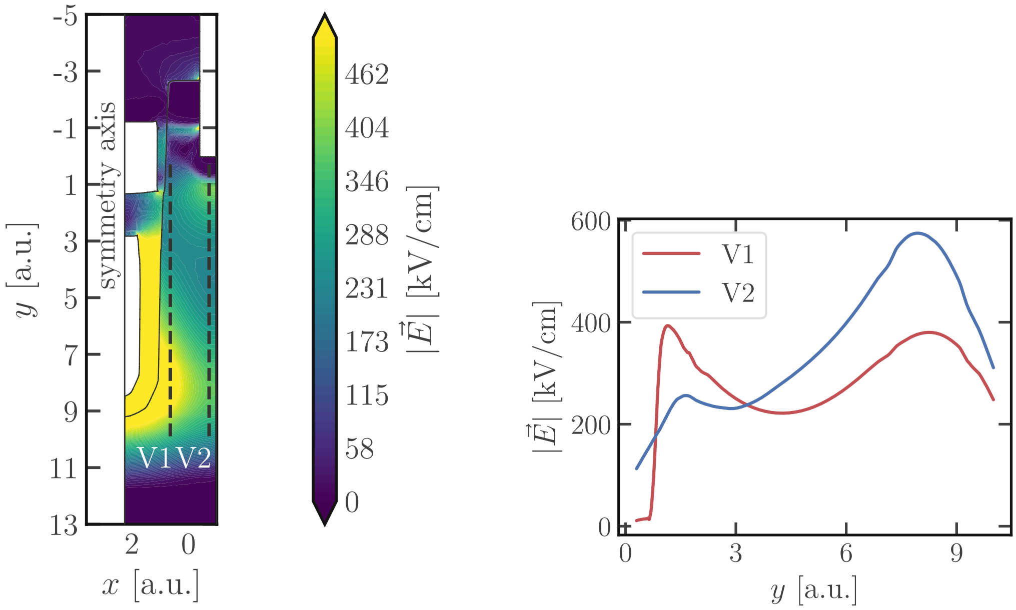

Fig. 1.7. Simulation results from Figure 1.6. The electric field in the two vertical cuts is shown in the right figure.

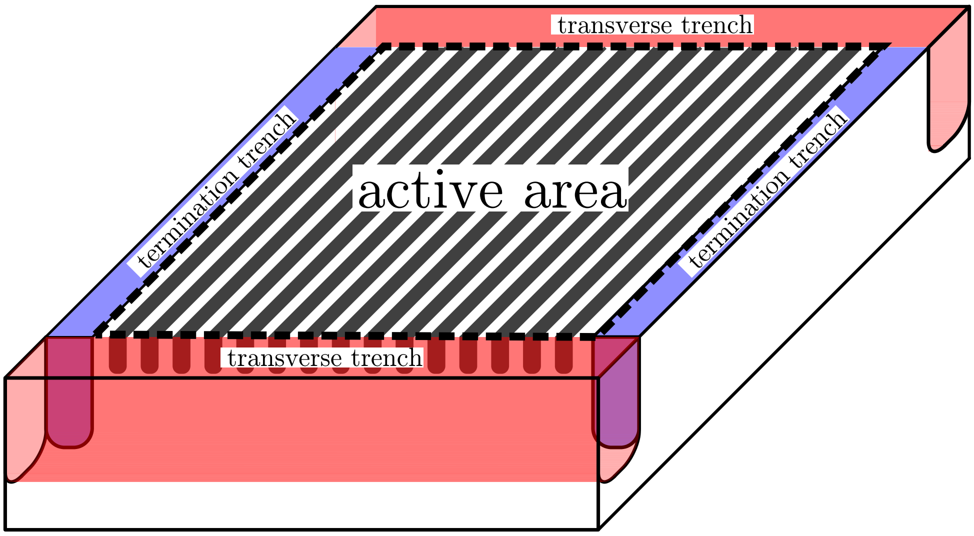

Fig. 1.8. Schematic three-dimensional view of a full trench device. Each grey trench contains a gate and a FP as presented in Figure 1.4. The termination trenches delimit the device along with the transverse trenches. These transverse trenches are also used to connect all gate and FP electrodes. The electrically active device area is represented by the dashed black border and represents the available area for current flow during the on-state.

This compensation concept is only applicable in technologies where the resulting breakdown voltage of the device is below the breakdown field of the oxide between the semiconductor and FP electrode. Otherwise, naturally, the oxide would be destroyed during operation. Suitable technologies are low-voltage silicon power MOSFETs. Higher voltage classes use other methods to increase the breakdown voltage and performance. For silicon, the superjunction principle [15] is well established, where p-doped pillars within the n-doped drain region achieve a similar compensating effect as a FP. Wide band gap semiconductors like SiC and GaN have higher breakdown fields compared to silicon [16], [17] rendering the compensation principle unfavorable.

A full device consists of multiple trenches as shown in Figure 1.8 which are delimited by transverse and termination trenches. The former are also used to contact the electrodes in the trenches and therefore have to be wider than standard trenches. From an electrical point of view, each trench incorporates two MOSFETs, one on the left hand side and a second one on the right hand side. The complete product connects the multiple MOSFETs from all trenches in parallel. The actual number of trenches depends on the final product and its specifications but is usually in the dozens if not hundreds. Generally, a large device allows for a lower overall on-resistance but also increases switching capacitances. Obviously, larger devices are also capable of handling higher current densities. The length of the trenches also depends on the product but should be kept as short as possible. Long gate electrodes within the trenches can lead to a delayed switching of parts of the active area since the charging and discharging of the MOS structure has finite time constants. Regions of the device which are located further away from the external gate contact can therefore follow the signal slightly slower. This effect is especially problematic in high-frequency applications.

1.2. Reliability of Power Devices

This chapter introduces two degradation mechanisms, bias temperature instability (BTI) and HCD, which both impact the oxide of MOS structures during operation. In both cases, chargeable defects near and at the semiconductor-oxide interface are charged and created. These defects stem from the fact that, in the case of Si-SiO_2 interfaces, the amorphous SiO_2 cannot match the Si crystal. Thus, a large number of electrically active defects in the form of unsaturated bonds, i.e. unfilled orbitals, emerge at the Si-SiO_2 interface. For non-passivated interfaces, the trap densities range from $1 \times 10^{12}\,\mathrm{cm}^{-2}$ to $5 \times 10^{12}\,\mathrm{cm}^{-2}$ [18], [19] which are unacceptably high values for modern technologies. These traps have to be passivated by hydrogen during fabrication, thereby being reduced down to between $2 \times 10^{9}\,\mathrm{cm}^{-2}$ and $1 \times 10^{10}\,\mathrm{cm}^{-2}$ under optimal processing conditions [19]. Unfortunately, it is possible to charge the remaining defects or tear the hydrogen bonds and recreate trap states.

These defects impact device performance two-fold: On the one hand, the defects are chargeable, which leads to an increase of the MOS capacitance. Depending on the energetic positioning of these traps, the charge states change when the Fermi level crosses the energy level of the defect. Furthermore, when charged, the defects modify the electrostatics of the device: A change of the threshold voltage is commonly observed [20], [21] since the electric field of the charged states superimposes the gate-induced field. Secondly, the defects are scattering centers which impede carrier mobility [22]. This leads to an increase of the on-resistance of the transistor. The physical nature of these defects is explored in Chapter 2.

1.2.1. Bias Temperature Instability

The generation of traps due to BTI [23] is one of the fundamental degradation mechanisms of MOSFETs which is particularly strong at high temperatures and gate voltages. While the positive bias temperature instability is usually observed in n-channel MOSFETs, negative bias temperature instability (NBTI) is mostly investigated in p-channel MOSFETs. This is because n-channel MOSFETs generally require positive gate biases for on-state operation while their p-channel counterparts are switched on by negative voltages. The latter BTI effect causes more issues than the former which is why most publications focus on NBTI.

The MOS structures investigated for this thesis do not exceed $4\,\mathrm{MV\,cm}^{-1}$ during operation which is far below the fields where significant positive bias temperature instability is observed in p-channel MOSFETs [24]. Therefore this degradation mechanism is not considered.

As for the microscopic mechanism, taking NBTI as an example, positive charges are captured in traps at and near the Si-SiO_2 interface when negative gate biases are applied. Furthermore, additional defects are created during the stress. For the description of the effect two competing models, the reaction-diffusion model and the defect-centric model, have emerged [25]. The reaction-diffusion approach focuses on the kinetics of the interface trap generation. There are issues with its model parameters which are not in agreement with the accepted physical description of hydrogen in Si-SiO$_2$ systems. In the defect-centric approach, on the other hand, the correct physical description of discrete defects is desired. Charge transitions in this approach are described by an non-radiative multi-phonon (NMP) model (cf. Section 2.1.2).

1.2.2. Hot-Carrier Degradation

During the on-state operation of a MOSFET with high gate and drain voltages, charge carriers in the channel are accelerated by the applied electric fields. Thereby the carriers gain enough energy to break the hydrogen bonds of passivated defects on the interface, located in the direct vicinity of the channel, recreating a charge trap.

The bond breakage mechanisms, involved in HCD are so-called single excitation and multi-vibrational excitation (MVE) processes [26] where the bonded and transport states of the passivated defects are modeled as quantum harmonic oscillators. The bonded state refers to the stable state of the hydrogen atom and the defect while the hydrogen is released in the transport state. As for single excitations, a single hot carrier interaction is sufficient to excite the bonded state to the transport state while MVE processes require a large quantity of carriers with medium energies to cause the bond to slowly increase the energy of the harmonic oscillator until the transport state is reached. Single excitation processes are usually dominant in long-channel devices, i.e. when the gate length exceeds approximately 100 nm, MVE processes are mainly found in short-channel devices [7]. The energy density function of carriers, which is responsible for whether single excitations of MVE processes dominate, is dependent on the major scattering mechanisms. Electron-electron scattering, which significantly contributes to HCD, populates the high-energy tail of the carrier density while other mechanisms like scattering at ionized impurities and impact ionization decrease the number of electrons with high energies. In long-channel MOSFET structures, the scattering mechanisms which depopulate the high-energy tail dominate. The different temperature dependences of the various scattering processes cause opposite HCD temperature dependencies in long-channel and short-channel devices.

1.3. Measurement Setup and Experimental Procedure

All measurements are performed on a needle prober on wafer level. For a electrical measurements, a Keysight B1500A semiconductor parameter analyzer with source measurement units and pulse units is used. It is connected to the probe station using a Keithley 708B switching matrix. Capacitance measurements are performed with an Agilent 4294A impedance analyzer which is also connected to the switching matrix.

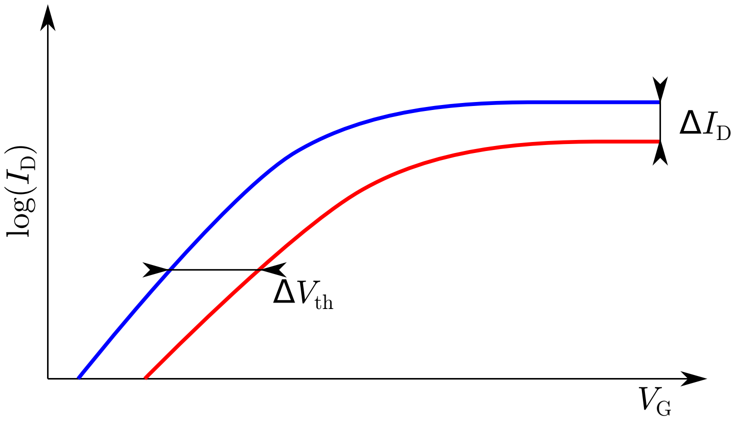

Fig. 1.9. Schematic sketch of the MOSFET transfer characteristics before (blue) and after (red) stress. The change of the threshold voltage V_{th} and drain current I_D allows for drawing conclusions about the stress-induced defects.

1.3.1. I-V Analysis

The degradation of transistor parameters described in Section 1.2 can be exploited for the investigation of the defects causing it. One often characterized parameter is the threshold voltage of the MOSFET which can be extracted by various methods [27]. In the simplest approach, the threshold voltage is defined as the gate bias required to reach an arbitrary drain current for a fixed drain voltage. This defined drain current has to lie in a regime where it increases exponentially with the gate bias. After a stress, the transfer characteristics shift (Figure 1.9) can be calculated to a trap density. Assuming that the charged defects are a sheet charge directly at the interface, the threshold voltage shift can be written as

$$C = \frac{\varepsilon_0 \varepsilon_{\mathrm{SiO_2}} A_{\mathrm{channel}}}{d} = \frac{\Delta Q}{\Delta V_{\mathrm{th}}} = \frac{\Delta N q A_{\mathrm{channel}}}{\Delta V_{\mathrm{th}}} \tag{1.1}$$

which can be rewritten to

$$\Delta N = \frac{\varepsilon_0 \varepsilon_{\mathrm{SiO_2}} A_{\mathrm{channel}} \Delta V_{\mathrm{th}}}{dq}. \tag{1.2}$$

The change of the threshold voltage as a measure for trap densities can be problematic when the slopes of the transfer characteristics changes significantly due to carrier mobility reduction [28]. In this case, the change of threshold voltage becomes dependent on the drain current criteria and thus the calculated trap density is inaccurate. It should be noted that the definition of the threshold voltage at a certain current criterion is different from the physical definition where it is defined as the voltage where the number of minority carriers in the channel is equal to the number of majority carriers.

As for the drain current change, which is associated with a mobility decrease, the quantitative analysis of traps is not straight-forward. A comparison of the drain current change after stress to trap densities obtained from CP is presented in Section 4.2.4.

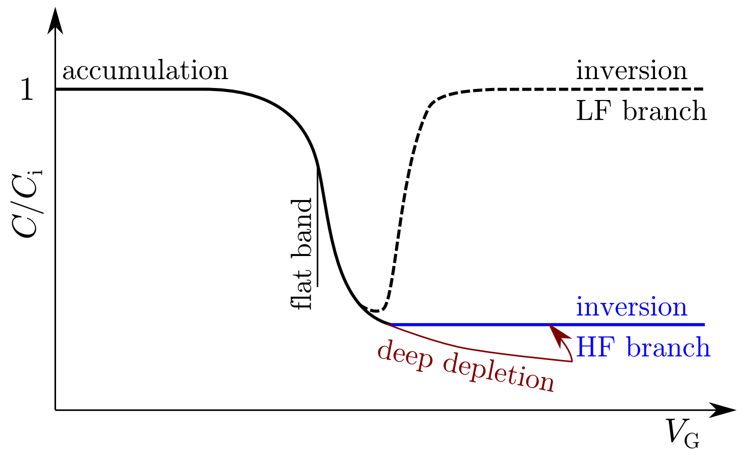

Fig. 1.10. Schematic sketch of the ideal MOS capacitance characteristics assuming that the semiconductor is p-doped. The capacitance is shown with respect to the insulator capacitance C_i. Depending on the measurement frequency, a high frequency or low frequency branch is observed.

1.3.2. Capacitance Measurements

The capacitance-voltage characteristics of ideal MOS structure, as presented in Figure 1.10, have a strong non-linear behavior. This stems from the fact that this system acts like two serial capacitors, the oxide capacitance and the capacitance of the space charge region in the semiconductor. While the oxide capacitance is independent of the voltage, the space charge region is strongly dependent on the surface potential in the semiconductor near the interface. For gate voltages where the semiconductor is in accumulation (negative biases for p-doped semiconductors), a value close to the insulator capacitance is measured. Increasing the gate voltage pushes majority carriers away from the interface and depletes the semiconductor in this region, decreasing the overall capacitance. When inversion is reached, three branches can be observed. At high frequencies, the capacitance stays low because generation and recombination of minority carriers at the oxide-silicon interface cannot follow the measurement signal. When the high frequency C-V characteristics are measured at fast sweep rates, the deep depletion effect is observed. In this case, the depletion region of the MOS structure is wider than at equilibrium for a short time during the sweep which further decreases the capacitance. When the voltage sweep is stopped, a return to the high frequency curve can be observed. The deep depletion effect is again caused by the insufficient supply of minority carriers near the insulator-silicon interface, thereby widening the depletion region as no inversion layer can form at the interface. For low frequencies, sufficient time for the thermal creation and annihilation of minority carriers is available, increasing the capacitance at higher gate voltages again, causing the low frequency branch.

Since defects are usually chargeable, it is obvious that they also impact the CV characteristics of MOS structures. This allows for detecting them after stress. Additional to chargeable defects, fixed oxide charges can be detected in CV measurements since they shift the whole curves.

1.3.3. Charge Pumping

Brugler and Jespers [29] first discovered the CP effect in 1969. More than a decade after its discovery, Groeseneken et al. [30] presented a thorough explanation of the phenomenon. In this measurement method, the chargeable defects on a Si-oxide interface of an MOS structure are investigated. It is necessary to have a p-doped as well as an n-doped region in the direct vicinity of interface to supply the traps with holes and electrons. In the experiment, the metal contact of the MOS structure is pulsed between deep inversion and deep accumulation. The n- and p-doped regions are connected to separate ammeters. In the transition between accumulation and inversion, charges are captured within the traps and recombine with carriers of the other kind during the transition between inversion and accumulation and vice versa. This causes a measurable current I_{CP} on the ammeters as carriers are pumped from the n to the p region, or, in an energetic sense, from the conduction to the valance band (or the other way round). I_{CP} is proportional to the electrically active trap density

$$N_{\mathrm{CP}} = \frac{I_{\mathrm{CP}}}{q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}}}. \tag{1.3}$$

These transition dynamics of CP are typically described with the Shockley Read Hall (SRH) theory (cf. Section 2.1.1). Two common classical CP methods are the constant base and constant high methods where the base or high levels of the pulse are held constant and the high or base levels are swept, respectively. The fixed levels have to fulfill the basic CP condition of being in deep accumulation or deep inversion. As the swept level approaches this condition, the CP current rises abruptly as the CP mechanisms kicks in (Figure 1.11). In this context, the flat-band and threshold voltage of CP ($V_{\mathrm{FP}}^{\mathrm{CP}}$ and $V_{\mathrm{TH}}^{\mathrm{CP}}$) can be defined: In n-channel MOSFETs, the flat-band voltage of CP is the base level voltage during the constant high level experiment where the CP current increases the most. Analogously, the threshold voltage of CP is observed at the maximum increase of the CP current in the constant base level method. In p-channel MOSFETs, these definitions are reversed, i.e. the constant high level CP method is associated with the threshold voltage while the flat-band voltage can be extracted from the constant base level method.

It is noted that the terms ‘flat-band voltage’ and ‘threshold voltage’ in the context of CP [31] differ from their classical textbook definitions. Thus, the values of these voltages may vary slightly from their usual definition in semiconductor physics. In CP, both values are obtained from the constant high and constant base level methods, whereas they are usually defined by surface potentials in semiconductor physics [14]. While these descriptions are not physically equivalent, the CP definition has the advantage of being experimentally accessible.

Besides the constant base and constant high level methods, the constant amplitude method is often employed. As suggested by its name, the amplitude of the CP pulse is kept constant while the base and high levels are swept simultaneously. The resulting CP current is measured over the base level of the pulse and has a bell shape [31]. This method should not be used as it is hard to confirm whether deep accumulation and deep inversion are reached during the sweep of the base and high levels.

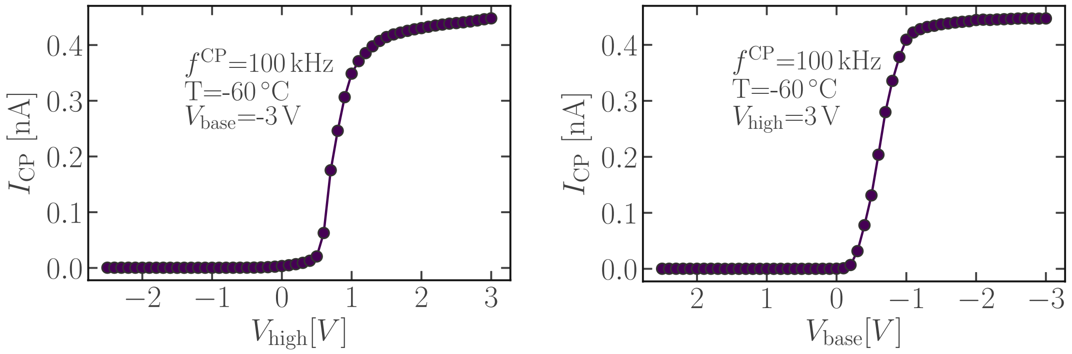

Fig. 1.11. Constant low (left) and constant high (right) signal of the standard CP method on a lateral MOSFET structure.

1.3.4. Spectroscopic Charge Pumping

The spectroscopic charge pumping (SPCP) method [32], [33] allows for the spectral scanning of defects in the band-gap and is an extension of the CP method. SPCP relies on a parasitic effect of CP, namely the re-emission of carriers in the CP pulse transition phase into an inversion or accumulation layer of carriers of the same type before they can recombine with carriers of the opposite charge. Thus, carriers with sufficiently low emission time constants are unable to contribute to the CP current.

In contrast to classical CP, the rise and fall time of the CP pulse are swept at various temperatures to scan the lower and upper half of the band-gap piece by piece at various temperature steps. The rise time variation scans the lower half, the fall time variation the upper half of the band gap at each measured temperature (Figure 1.12). Taking the rise time as an example, holes are captured in traps as the pulse bias level is initially at its minimum. If these hole traps are energetically located near the valence band, the captured holes can be emitted before a recombination with electrons is possible as the electrons can only reach the interface after the pulse level has increased to a certain level. Without the recombination with electrons, the holes are flushed away from the interface as if they had never been captured by a trap. Thus, they do not contribute to the overall CP current. Increasing the rise time causes selective deactivation of defects towards mid-gap since the slower transitions allow for the escape of deeper traps from the CP process. The fall time variation is completely analogous. Since these emission processes are only possible during the transitions between accumulation and inversion as carriers are pinned to the defects due to the position of the Fermi-level otherwise, the relation between the emission times and the CP pulse rise and fall times is described as

$$\tau_{\mathrm{emi}}^{\mathrm{h}^+} = \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{rise}} \tag{1.4a}$$

$$\tau_{\mathrm{emi}}^{\mathrm{e}^-} = \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{fall}}. \tag{1.4b}$$

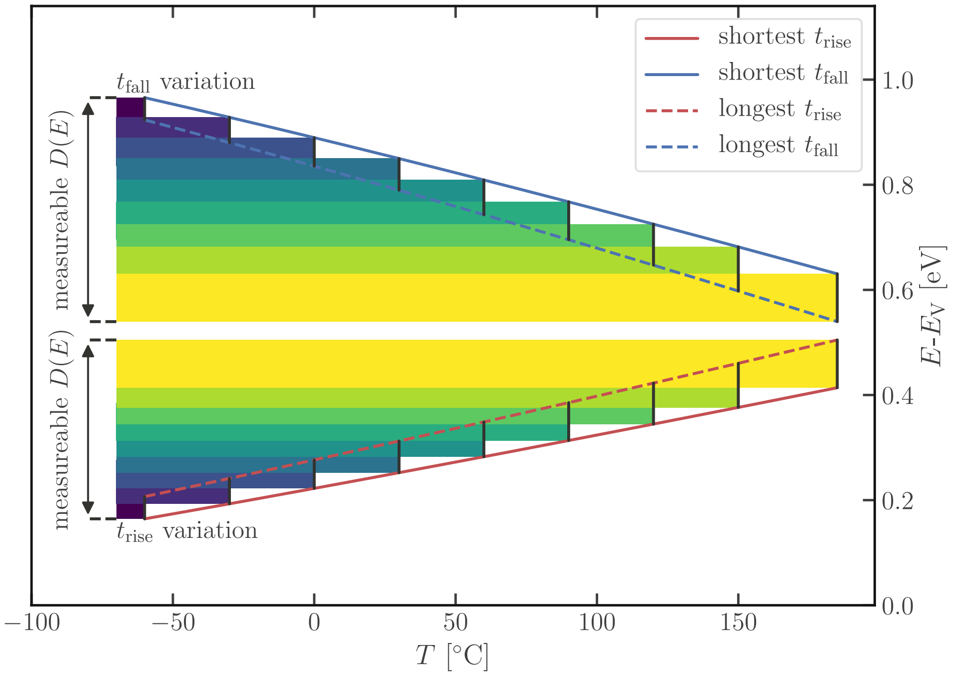

Fig. 1.12. Visualization of the sampled energy window of SPCP in the band-gap. Rise and fall time sweeps, indicated by vertical black lines, scan a small fraction of the lower and upper half of the band-gap (calculated assuming SRH dynamics, very similar picture in non-radiative multi-phonon (NMP) dynamics). Performed at various temperatures, they are combined to obtain a spectrum of traps within the band-gap.

By varying the measurement temperature, it is possible to further modify the emission time constants and shift the energy window scanned by the transition time variations, thereby scanning a large portion of the band gap. As previously mentioned, the universally accepted interpretation of CP is based on SRH statistics. For SPCP, the variations of the rise and fall times of the pulse at multiple temperatures are therefore usually transformed into respective trap energies by this model. The main idea behind this transformation is that for a certain transition time, the profiled energy must correspond to the emission time constant of a trap of this very energy. Using Equation (1.4) and SRH emission rates (Equation (2.2)), the energy transformation of SPCP can be written as

$$-E_{21}^{\mathrm{h}^+} = E_{\mathrm{t}} - E_{\mathrm{V}} = k_{\mathrm{B}}T \ln\left(N_{\mathrm{V}} v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{rise}}\right) \tag{1.5a}$$

$$-E_{21}^{\mathrm{e}^-} = E_{\mathrm{C}} - E_{\mathrm{t}} = k_{\mathrm{B}}T \ln\left(N_{\mathrm{C}} v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{fall}}\right). \tag{1.5b}$$

In order to obtain the respective density of states, the definition

$$I_{\mathrm{CP}} := q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}} \underbrace{\int_{\mathrm{E_t(t_{rise},T)}}^{\mathrm{E_t(t_{fall},T)}} D(E_{\mathrm{t}})\mathrm{d}E_{\mathrm{t}}}_{\mathrm{N_{CP}(t_{rise},t_{fall},T)}} \tag{1.6}$$

is used. Quite intuitively, the trap density obtained by a CP measurement, which is proportional to the CP current (cf. (1.3)), can be defined as the integrated density of states. The boundaries of the integral stem from the parasitic emission which limits the active energy window of CP which can be observed at a given rise and fall time, as well as temperature. Equation (1.6) finally yields the transformation of the transition times to the density of states

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}t_{\mathrm{rise}}} = -q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}} D(E_{\mathrm{t}}) \frac{\mathrm{d}E_{\mathrm{t}}}{\mathrm{d}t_{\mathrm{rise}}} \tag{1.7a}$$

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}t_{\mathrm{fall}}} = q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}} D(E_{\mathrm{t}}) \frac{\mathrm{d}E_{\mathrm{t}}}{\mathrm{d}t_{\mathrm{fall}}} \tag{1.7b}$$

which can be rewritten to

$$D^{\mathrm{h}^+}(E_{\mathrm{t}}) = -\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}t_{\mathrm{rise}}} \frac{t_{\mathrm{rise}}}{q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}}} \frac{1}{k_{\mathrm{B}}T} \tag{1.8a}$$

$$D^{\mathrm{e}^-}(E_{\mathrm{t}}) = -\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}t_{\mathrm{fall}}} \frac{t_{\mathrm{fall}}}{q f^{\mathrm{CP}} A_{\mathrm{eff}}^{\mathrm{CP}}} \frac{1}{k_{\mathrm{B}}T} \tag{1.8b}$$

using the SRH energy transformations (1.5), where $D^{\mathrm{h}^+}(E_{\mathrm{t}})$ represents the hole contribution to the density of states and $D^{\mathrm{e}^-}(E_{\mathrm{t}})$ the electron contribution. The mathematical framework presented in this section is based on the work of Van den Bosch et al. [32] which has since been established SPCP theory.

It is worth taking a closer look at the thermal carrier velocity v_{th}, introduced in several equations above. Although some authors (e.g. [31]) assume v_{th} to be constant, with $1 \times 10^{7}\,\mathrm{cm\,s^{-1}}$ being usually cited for Si, it is advisable to use a temperature dependent model instead. A commonly used description [14] is

$$v_{\mathrm{th}} = \sqrt{\frac{3k_{\mathrm{B}}T}{m^*}}. \tag{1.9}$$

This CP method will be used in a case study in Chapter 3 where the well-established SRH model [34], [35] will be benchmarked against the more complete NMP model [36].

1.3.5. Frequency Dependent Charge Pumping

The classic approach of separating interface and spatially deeper border traps with the CP method involves varying the pulse frequency [33]. In this procedure, it is assumed that defects which are located deeper in the oxide have higher capture and emission times and are therefore only detected at sufficiently low frequencies during which enough time for charging and discharging is available. Therefore, by gradually lowering the CP frequency, more and more traps are activated for the CP mechanism. Comparing actual trap densities for various frequencies, where the frequency dependence of the CP current is removed (cf. Equation (1.3)), allows for the detection of frequency dependent border traps.

There were also unsuccessful attempts to map the trap density changes over the CP frequency to the depth of defects in the oxide [37]. These ideas failed as the energy distributions of oxide defects are not known and can clearly not be assumed constant. Since only one variable, the frequency, is varied, it is impossible to separate the contribution of the border trap energy and depth distributions as spatially deep traps near the band gap edges can have the same time constants as traps near mid-gap which are located near the interface. Also, the Boltzmann factor of time constants associated with the relaxation energies of traps (cf. Equations (2.6) and (2.7)) generally trumps the depth dependent quantum-mechanical tunneling factor [36], [37] $\exp(-x/x_0)$. This renders the correct depth mapping even more difficult, if not impossible.

CHAPTER 2

Defects in MOS Structures

Chapter Contents

> *Not all those who wander are lost*
> — J. R. R. Tolkien, *The Fellowship of the Ring*

A critical part of understanding degradation mechanism in silicon MOSFETs is the investigation of the underlaying defects. There are four types of defects which impede the reliability of MOSFETs [38]. Fixed oxide charges and mobile ions do not change their charge state and add additional electric fields to the device. The fixed oxide charges neither change their positions while mobile ions can be moved within the oxide by electric fields and therefore introduce time dependent changes of the oxide field. Interface traps, which are located directly on the interface of the insulator and the semiconductor, as well as border traps in the insulator generally have more than one charge state. They are most prominently created by HCS and are presented in this chapter.

2.1. Modeling of Defect Dynamics

The modeling of the interaction of traps and charge carriers is important for the characterization of the defects and allows for a description of the temperature and energy dependence. Two prominent models are discussed in this section.

2.1.1. Shockley Read Hall Model

The SRH model [34]–[36], developed in the early 1950s, is the most popular model for the description of charge transitions to and from trap states. Originally developed for doping

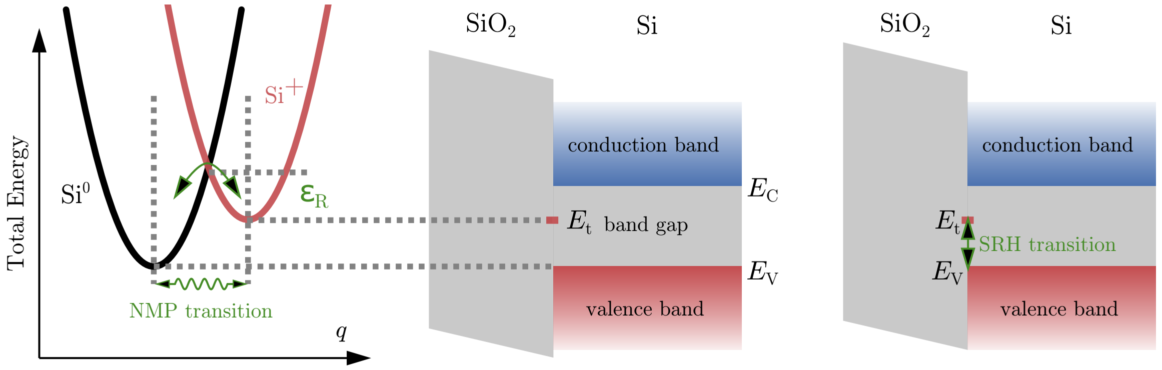

Fig. 2.1. Physical description of transitions in the NMP (left) and SRH (right) model. The SRH model lacks barriers introduced by structural changes.

impurities, this theory was later adapted for many types of defects in the semiconductor band-gap. The capture and emission times of holes are calculated without the consideration of structural changes of the molecular structure of the defects' surroundings due to its charge. The core element of the model are capture rates

$$k_{12}^{\mathrm{h}^+} = \frac{1}{\tau_{\mathrm{cap}}^{\mathrm{h}^+}} = p v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \exp\left(-\frac{\varepsilon_{12}^{\mathrm{SRH}}}{k_{\mathrm{B}}T}\right) \tag{2.1a}$$

$$k_{12}^{\mathrm{e}^-} = \frac{1}{\tau_{\mathrm{cap}}^{\mathrm{e}^-}} = n v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \exp\left(-\frac{\varepsilon_{12}^{\mathrm{SRH}}}{k_{\mathrm{B}}T}\right) \tag{2.1b}$$

and emission transition rates

$$k_{21}^{\mathrm{h}^+} = \frac{1}{\tau_{\mathrm{emi}}^{\mathrm{h}^+}} = N_{\mathrm{V}} v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \exp\left(-\frac{\varepsilon_{21}^{\mathrm{SRH}}}{k_{\mathrm{B}}T}\right) \tag{2.2a}$$

$$k_{21}^{\mathrm{e}^-} = \frac{1}{\tau_{\mathrm{emi}}^{\mathrm{e}^-}} = N_{\mathrm{C}} v_{\mathrm{th}} \sigma^{\mathrm{SRH}} \exp\left(-\frac{\varepsilon_{21}^{\mathrm{SRH}}}{k_{\mathrm{B}}T}\right) \tag{2.2b}$$

which are obtained using the requirement of detailed balance in thermal equilibrium [36] and are the inverse of the respective capture and emission times. The transition energies for the capture process (ε_{12}) and emission process (ε_{21}) are related as

$$\varepsilon_{12} = \varepsilon_{21} + E_{21} \tag{2.3}$$

where E_{21} is the energy difference between the trap state 2 and the reservoir 1. In the SRH model, the transition energy $\varepsilon_{21}^{\mathrm{SRH}}$ is equal to the energy difference between the trap state and the valence $E_{21}^{\mathrm{h}^+}$ or conduction band $E_{21}^{\mathrm{e}^-}$, depending on whether valance or conduction band interactions are investigated.

2.1.2. Non-Radiative Multi-Phonon Theory

The NMP description of trap transitions includes the modeling of reconfigurations of the molecular structure upon charge capture and emission. This is achieved by approximating the total energy of the system by parabolic potentials over the reaction coordinate. This reaction coordinate reduces the complex 3N-dimensional molecular configuration of a system, where N is the number of atoms, to a single dimension. Each charge state is modeled by its respective parabola (Figure 2.1 left). These parabolic potentials are described as

$$V_\mathrm{i} = \frac{1}{2} M {\omega_\mathrm{i}}^2 \Delta q^2 + E_\mathrm{i}^\mathrm{NMP} \tag{2.4}$$

and allow for the extraction of a relaxation energy

$$\varepsilon_\mathrm{R} = \frac{1}{2} M {\omega_\mathrm{i}}^2 \Delta q^2. \tag{2.5}$$

In a classical approximation, transitions in the NMP model are only possible when the parabolas intersect, i.e. when the respective state receives enough phononic energy due to thermal vibrations to overcome this relaxation barrier. In the SRH model, such an energy is not present, thus all transitions are direct (Figure 2.1).

The transition rates of the NMP theory remain analogous to the SRH model. Capture processes

$$k_{12}^{\mathrm{h}^+} = \frac{1}{\tau_\mathrm{cap}^{\mathrm{h}^+}} = p v_\mathrm{th} \sigma^\mathrm{NMP} \exp\left(-\frac{\varepsilon_{12}^\mathrm{NMP}}{k_\mathrm{B} T}\right) \tag{2.6a}$$

$$k_{12}^{\mathrm{e}^-} = \frac{1}{\tau_\mathrm{cap}^{\mathrm{e}^-}} = n v_\mathrm{th} \sigma^\mathrm{NMP} \exp\left(-\frac{\varepsilon_{12}^\mathrm{NMP}}{k_\mathrm{B} T}\right) \tag{2.6b}$$

and emission processes

$$k_{21}^{\mathrm{h}^+} = \frac{1}{\tau_\mathrm{emi}^{\mathrm{h}^+}} = N_\mathrm{V} v_\mathrm{th} \sigma^\mathrm{NMP} \exp\left(-\frac{\varepsilon_{21}^\mathrm{NMP}}{k_\mathrm{B} T}\right) \tag{2.7a}$$

$$k_{21}^{\mathrm{e}^-} = \frac{1}{\tau_\mathrm{emi}^{\mathrm{e}^-}} = N_\mathrm{C} v_\mathrm{th} \sigma^\mathrm{NMP} \exp\left(-\frac{\varepsilon_{21}^\mathrm{NMP}}{k_\mathrm{B} T}\right) \tag{2.7b}$$

only differ in the transition energy. Assuming linear electron-phonon coupling [36], the transition energy is written as

$$\varepsilon_{21}^\mathrm{NMP} = \frac{(\varepsilon_\mathrm{R} - E_{21})^2}{4 \varepsilon_\mathrm{R}}. \tag{2.8}$$

The relationship (2.3) also holds true for the NMP model.

2.2. Interface Traps

The most well-known candidate for interface defects in Si devices is the $\mathrm{P_b}$ center [39]–[41]. As mentioned in Chapter 1, the Si-$\mathrm{SiO_2}$ interface has structural imperfections due to the mismatch of the Si-crystal and the amorphous $\mathrm{SiO_2}$ structure. Within the Si-$\mathrm{SiO_2}$ interface, some silicon atoms miss one of the four covalently bonded partner atoms. Dangling bonds remain, which can be passivated by atomic hydrogen but are sometimes broken again due to HCS (cf. Section 1.2.2). It is agreed upon that the $\mathrm{P_b}$ center is of amphoteric nature. This means that it has a positive and negative charge state additionally to the neutral configuration, i.e. it can capture a hole or an electron.

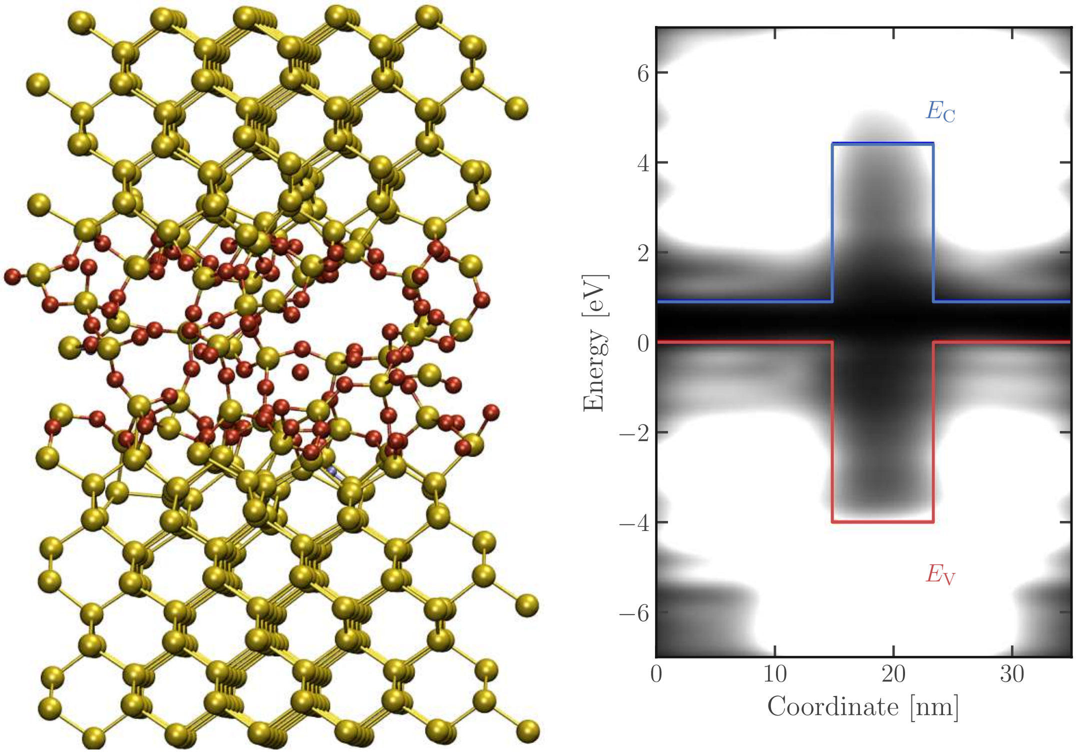

Fig. 2.2. Left: Interface model used in DFT simulations. Right: Band structure of said model with Si and SiO_2 band gaps of 1.0 eV and 8.7 eV. Figures from [43].

2.2.1. Density Functional Theory Investigation

Using density functional theory (DFT) simulations, Jech et al. [42] were able to identify defects at the Si-SiO_2 interface which closely resemble the properties of the P_b center. Based on this work, three probable configuration of the P_b center are analyzed based on the data of Jech [43].

In order to find a suitable lattice with which the defects itself could be simulated, an Si-SiO_2-Si geometry was used (Figure 2.2). The three most promising candidates for P_b centers were chosen from over 100 periodic Si-SiO_2 interface models (Figure 2.3). In this process, the two interface regions were modeled using a melt and quench procedure in molecular dynamics simulations. These three candidates show geometrical properties and formation energies (Figure 2.4) which fit well to P_b centers [39]. The first defect, defect A, is a Si atom one layer below the interface, trivalently bonded to three other Si atoms. The missing fourth bond causes the well-known DB configuration [6]. Defect B, being located close to an O atom, is otherwise very similar to defect A. The third defect, C, is another DB, bonded to one O and two Si atoms. The spin density of the defects, visualized in Figure 2.3 shows the location of the DB. In the DFT simulations, the positive and negative charge states are also calculated and are shown in Figure 2.5 depicting the structural changes of the lattice due to being positively or negatively charged with respect to the neutral state. From these charge states, the parabolas described in the NMP model can be obtained (Figure 2.6). As defect A is the most likely candidate of a P_b center, it

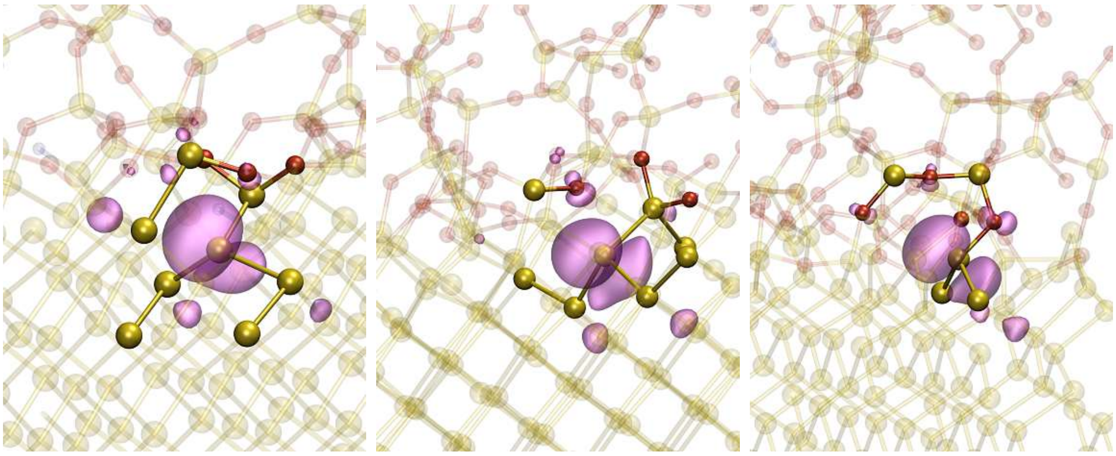

Fig. 2.3. Spin densities of defects A, B and C (left to right). Si atoms are represented in a yellow color, spin density isosurfaces of 0.01 are shown in magenta. Defect A and B are typical dangling bond (DB), with defect B having an O atom in its vicinity. Defect C is represented by a Si atom bonded to two other Si atoms and one O atom. Figures from [43].

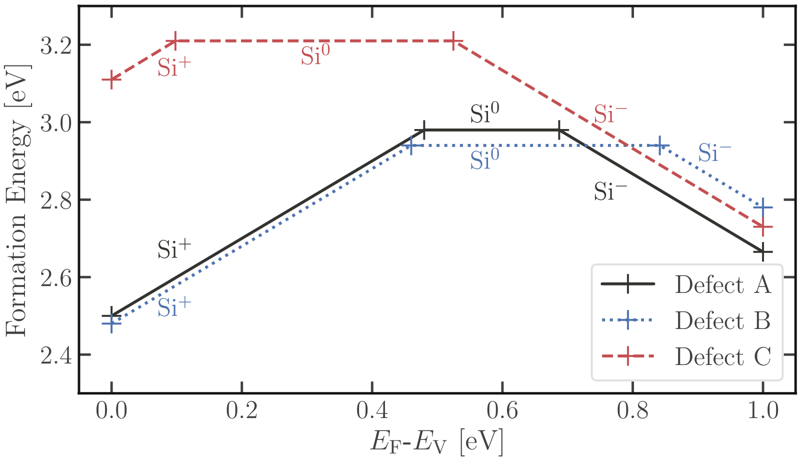

Fig. 2.4. Formation energies of the three defects used in DFT simulations plotted against the Fermi level with respect to the valence band energy. Figure from [43].

will be used for further analysis. The relaxation energies for the respective charge state are revealed by a quadratic fit of the potentials shown in Figure 2.6 (Equation (2.5)). This yields a relaxation energy of 0.22 eV for the positively charged state and 0.18 eV for the negatively charged state.

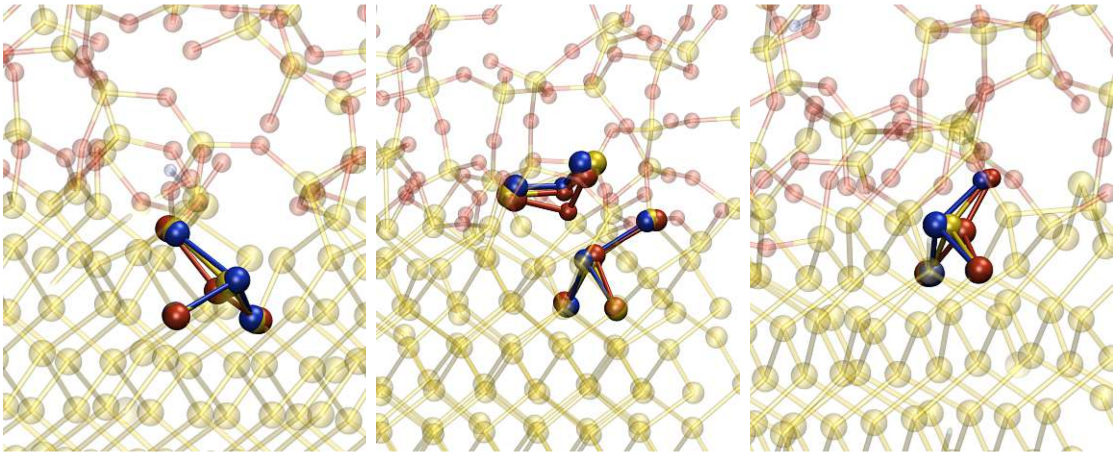

Fig. 2.5. Structural changes of defects A, B and C (left to right) due to transitions into the positive, neutral and negative charge states. The positive charge state is colored red, the neutral yellow and the negative blue. Figures from [43].

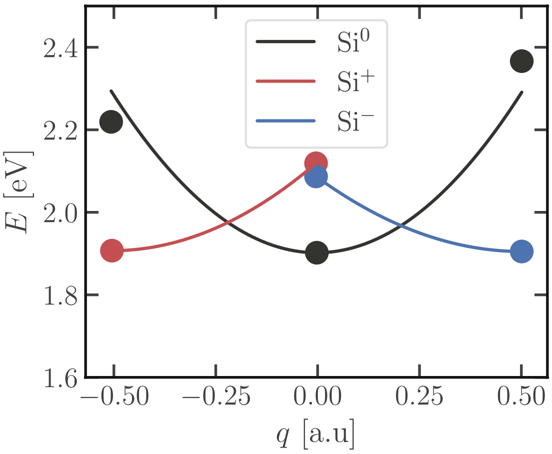

Fig. 2.6. Total energies of the positive, neutral and negative charge states for defect A plotted against the reaction coordinate of the DFT simulation. The data was fitted with parabolas according to the NMP model. Figure from [43].

2.3. Border Traps

In contrast to interface traps, border traps are located in the oxide of MOS structures rather than the insulator-semiconductor interface. As such, they differ at a microscopic level. While interface defects are typically associated with P_b centers [39], typical candidates for border traps are the hydroxyl E' center [44], [45], the oxygen vacancy [46] and the hydrogen bridge [47]. As already mentioned, border traps can interact with the semiconductor electrically in a similar way as interface traps. From an experimental point of view, the distinction between interface and border traps is somewhat arbitrary since both types of defects behave very similarly even though their physical origin is different.

Generally, border traps can have higher capture and emission times as interface traps due to the additional tunneling processes of carriers between insulator and semiconductor. Furthermore, relaxation energies are typically significantly larger in border traps [48]. Also, a bias dependence of border traps can be observed and is thoroughly discussed in Section 4.3.

CHAPTER 3

Benchmarking Recombination Models

Chapter Contents

> *We are not to tell nature what she's gotta be. … She's always got better imagination than we have.*
>
> — Richard Feynman

Whenever defects are studied, whether in experiments or simulations, it is necessary to find a way to model their capture and emission dynamics. For interface defects, the SRH model (cf. Section 2.1.1) is usually used to model the interaction of carriers with the defects. As stated by Richard Feynman in his Sir Douglas Robb Lectures in 1979 at the University of Auckland, nature's imagination is significantly more refined than mathematical models may imply. This is also true for the dynamics of traps. In this chapter, which is based on the findings in [49], [50], this will be explored in greater detail by replacing the SRH model by NMP dynamics in an experimental study of the SPCP method which has so far always employed the SRH model [32], [33]. The NMP model, in contrast, considers structural relaxations by quadratic quantum mechanical potential wells (cf. Section 2.1.2) and thus offers a more complete description of the actual dynamics. The inclusion of structural changes in the NMP model, which are not accounted for in the SRH model, is a major advantage of the former theory and brings results closer to physical reality. To achieve this, the NMP equations need an additional parameter: the relaxation energy, which adds a barrier to the capture and emission processes (cf. Section 2.1.2). This parameter depends on the atomistic lattice of the materials and can be extracted from DFT simulations as presented in Section 2.2.1.

Furthermore, this chapter introduces an approximated NMP framework which yields a modified SRH model. In these adapted SRH equations, the capture cross section is Arrhenius activated, which has already been proposed earlier [51], also based on arguments derived from NMP theory [52]. This work of Henry and Lang [52] is lacking modern DFT simulations which, though, give more insight into the possible molecular structure of interface traps.

3.1. Recombination Models and Spectroscopic Charge Pumping

In order to apply the NMP model to SPCP, the mathematical framework presented in Section 2.1.1 has to be adapted. More specifically, the emission transition energy of the SRH model has to be replaced by the transition energy of the NMP model. Plugging (2.8) into (2.2) along with (1.4) yields the NMP energy transformations of the CP rise and fall times.

$$-E_{21}^{\mathrm{h}^+} = E_\mathrm{t} - E_\mathrm{V} = \sqrt{4\varepsilon_\mathrm{R}^{\mathrm{h}^+} k_\mathrm{B} T \ln\left(N_\mathrm{V} v_\mathrm{th} \sigma^\mathrm{NMP} \frac{|V_\mathrm{TH}^\mathrm{CP} - V_\mathrm{FP}^\mathrm{CP}|}{\Delta V_\mathrm{G}} t_\mathrm{rise}\right)} - \varepsilon_\mathrm{R}^{\mathrm{h}^+} \tag{3.1a}$$

$$-E_{21}^{\mathrm{e}^-} = E_\mathrm{C} - E_\mathrm{t} = \sqrt{4\varepsilon_\mathrm{R}^{\mathrm{e}^-} k_\mathrm{B} T \ln\left(N_\mathrm{C} v_\mathrm{th} \sigma^\mathrm{NMP} \frac{|V_\mathrm{TH}^\mathrm{CP} - V_\mathrm{FP}^\mathrm{CP}|}{\Delta V_\mathrm{G}} t_\mathrm{fall}\right)} - \varepsilon_\mathrm{R}^{\mathrm{e}^-} \tag{3.1b}$$

Analogously to the derivation in the SRH model, the transformation of the CP current to the density of states is obtained from Equation (1.7).

$$D^{\mathrm{h}^+}(E_\mathrm{t}) = -\frac{\mathrm{d}I_\mathrm{CP}}{\mathrm{d}t_\mathrm{rise}} \frac{t_\mathrm{rise}}{q f^\mathrm{CP} A_\mathrm{eff}^\mathrm{CP}} \sqrt{\frac{\ln\left(N_\mathrm{V} v_\mathrm{th} \sigma^\mathrm{NMP} \frac{|V_\mathrm{TH}^\mathrm{CP} - V_\mathrm{FP}^\mathrm{CP}|}{\Delta V_\mathrm{G}} t_\mathrm{rise}\right)}{\varepsilon_\mathrm{R}^{\mathrm{h}^+} k_\mathrm{B} T}} \tag{3.2a}$$

$$D^{\mathrm{e}^-}(E_\mathrm{t}) = -\frac{\mathrm{d}I_\mathrm{CP}}{\mathrm{d}t_\mathrm{fall}} \frac{t_\mathrm{fall}}{q f^\mathrm{CP} A_\mathrm{eff}^\mathrm{CP}} \sqrt{\frac{\ln\left(N_\mathrm{C} v_\mathrm{th} \sigma^\mathrm{NMP} \frac{|V_\mathrm{TH}^\mathrm{CP} - V_\mathrm{FP}^\mathrm{CP}|}{\Delta V_\mathrm{G}} t_\mathrm{fall}\right)}{\varepsilon_\mathrm{R}^{\mathrm{e}^-} k_\mathrm{B} T}} \tag{3.2b}$$

Equation (3.2) completes the derivation of transformations for SPCP.

3.2. Extension of the Shockley Read Hall Theory

Since the NMP model can be considered an extension of the SRH model, as only the transition energy is updated by a more realistic term, the question arises whether an approximation of the SRH to the NMP model is possible. One way to approach this is to approximate the NMP transition energy.

$$\varepsilon_{21}^\mathrm{NMP} = \frac{\varepsilon_\mathrm{R}}{4} + \frac{{E_{21}}^2}{4\varepsilon_\mathrm{R}} - \frac{E_{21}}{2} \approx \frac{\varepsilon_\mathrm{R}}{4} + E_{21} = \frac{\varepsilon_\mathrm{R}}{4} + \varepsilon_{21}^\mathrm{SRH} \tag{3.3}$$

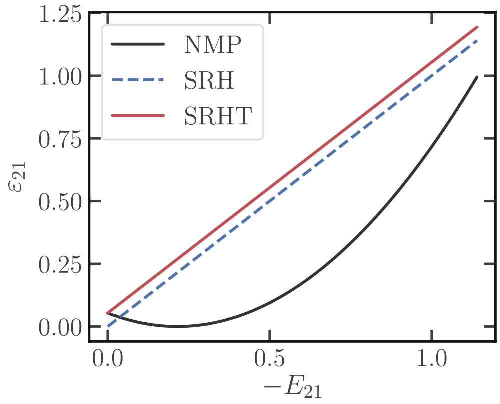

Fig. 3.1. Comparison of exact NMP transition energy and the approximation in Equation (3.3), as well as the SRH transition energy.

This approximation (SRHT) is compared to the exact calculation in Figure 3.1. The reason for choosing this rather rough approximation is that a transition from the NMP to the SRH model is only possible when the transition energy is linearly dependent on the energy difference between traps and reservoir. In this case, comparing (2.2) to (2.7) considering (3.3) yields the often used empirical Arrhenius correction [52]

$$\sigma^{\mathrm{NMP}} \approx \sigma^{\mathrm{SRHT}} \exp\left(-\frac{\varepsilon_{\mathrm{R}}}{4k_{\mathrm{B}}T}\right) \tag{3.4}$$

for capture cross sections. Using the same approach as in the previous sections, the energy transformation of SPCP can be written as:

$$-E_{21}^{\mathrm{h}^+} = E_{\mathrm{t}} - E_{\mathrm{V}} = k_{\mathrm{B}}T \ln\left(N_{\mathrm{V}} v_{\mathrm{th}} \sigma^{\mathrm{SRHT}} \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{rise}}\right) - \frac{\varepsilon_{\mathrm{R}}^{\mathrm{h}^+}}{4} \tag{3.5a}$$

$$-E_{21}^{\mathrm{e}^-} = E_{\mathrm{C}} - E_{\mathrm{t}} = k_{\mathrm{B}}T \ln\left(N_{\mathrm{C}} v_{\mathrm{th}} \sigma^{\mathrm{SRHT}} \frac{\left|V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FP}}^{\mathrm{CP}}\right|}{\Delta V_{\mathrm{G}}} t_{\mathrm{fall}}\right) - \frac{\varepsilon_{\mathrm{R}}^{\mathrm{e}^-}}{4} \tag{3.5b}$$

These equations differ from the respective SRH equations (Equation (1.5)) only by the offset of a quarter of the relaxation energy. The transformation from the CP current to the density of states remains the same as in the SRH model (Equation (1.8)) as the relaxation energy offset vanishes in the derivative of (1.7). This Arrhenius activated SRH model will be referred to as Shockley Read Hall - temperature activated (SRHT) model.

3.3. Comparison of the Models

Without investigating actual measurement data, taking a closer look at the three introduced models reveals interesting properties. In the simple SRH and SRHT density of states transformations (Equation (1.8) for both theories), a dependence of the capture cross

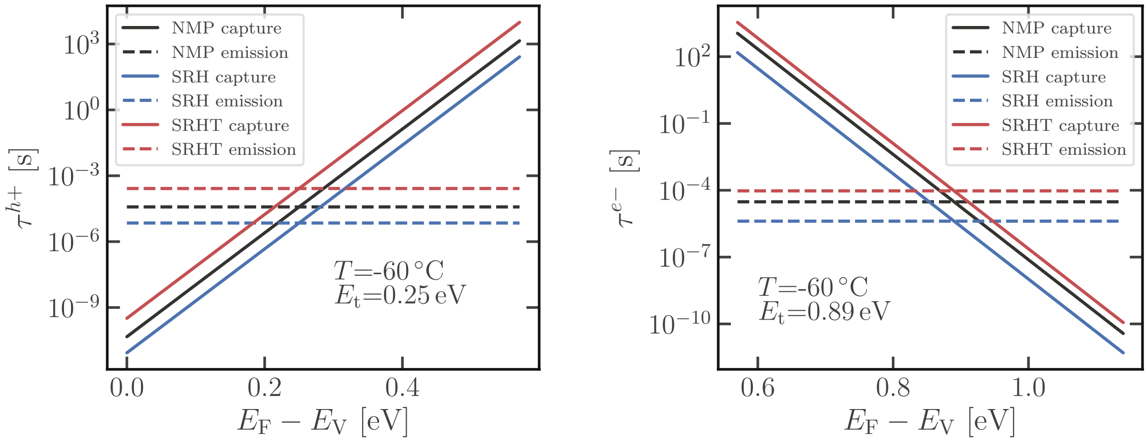

Fig. 3.2. Capture and emission time constants comparison of SRH, NMP and SRHT models. Left: Holes. Right: Electrons.

section is missing. This means that in these models, the capture cross section can only stretch or compress the spectrum but has no impact on the absolute values. This shortcoming is corrected in the NMP model (Equation (3.2)).

Focusing on the energy transformations, introducing Arrhenius activated capture cross sections in the SRHT model (Equation (3.5)) creates a constant offset by a quarter of the NMP relaxation energy to the energies in the SRH model (Equation (1.5)). This offset is also found in the NMP framework (Equation (3.1)), but to the full extend of the relaxation energy. Thus, these relaxation energies cause an additional barrier for the emission processes, which is expected since this is a basic premise of the NMP theory. Generally, temperature and emission times play a less dominant role in the NMP energy transformations, reflected in the square-root dependence which is neither present in SRH nor SRHT equations.

Before directly comparing the models' behavior from an energetic point of view, it is important to investigate the capture and emission time dependencies on the Fermi level since the latter directly dictates the trap occupation. It is noted that the respective capture cross sections have been adjusted to fit experimental data as will be explained in Section 3.5.

Again, the correct transition energy for emission (ε_{21}) is to be used. Using Equations (2.1), (2.2), (2.7) and (3.4) the capture and emission dependencies can be calculated (Figure 3.2). The dependency of capture time constants on the Fermi level stem from the availability of carriers with the energy needed for transitioning into traps. For a similar reason the emission times show no dependence on the Fermi level: The emission process is exothermic, not in need of external carriers to emit the captured traps. Due to the presence of relaxation energies in the SRHT and NMP models, both the capture and emission time constants of these models are higher than in the SRH model. This is a result of the added barrier in all transition processes.

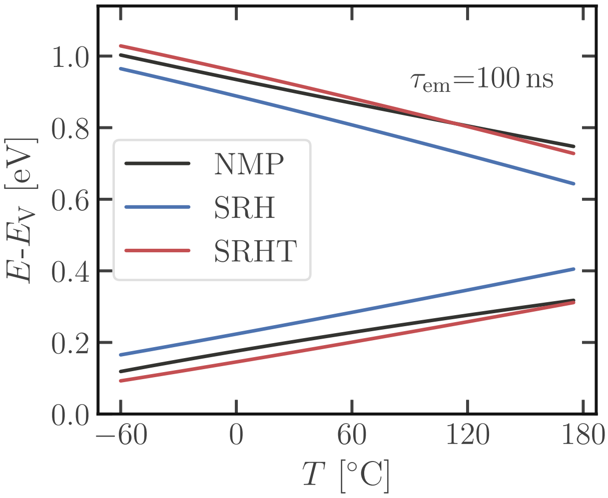

Fig. 3.3. Energy boundaries of CP for the SRH, NMP and SRHT models at a constant emission time.

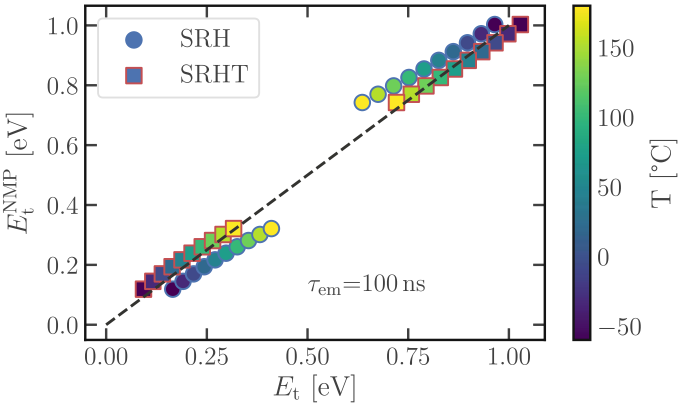

Fig. 3.4. Benchmark of energy dependence of the SRH and SRHT models against the NMP models on the temperature dimension.

The impact of these dynamics on the temperature dependence of energy scales in CP is shown in Figure 3.3 where the energy boundaries of CP, the active energy window, are plotted for all models at a given emission time constant dictated by the transition times of the CP pulse (1.4) similar to Figure 1.12. This analysis is based on Equations (1.5), (3.1) and (3.5). Although the SRH based energy windows is smaller than predicted by NMP theory, the corrected SRHT model is able to yield results very similar to the NMP description due to the inclusion of the temperature dependent capture cross section (3.4). A direct comparison of SRH and SRHT to the NMP model (Figure 3.4) reveals this clearly: The SRHT model hardly deviates from the NMP counterpart while the SRH approach drastically loses precision with increasing temperature.

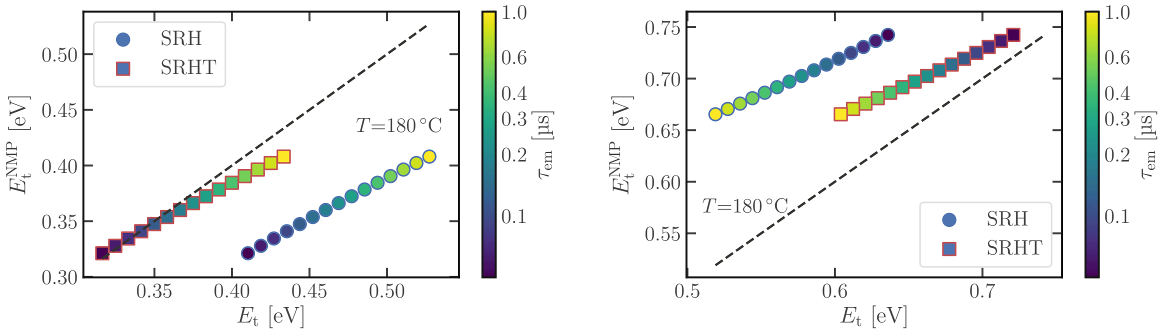

Fig. 3.5. Benchmark of energy dependence of the SRH and SRHT models against the NMP models on the emission time dimension. Left: Holes. Right: Electrons.

On the time dimension (Figure 3.5), the deviation at high temperatures is more apparent, showing that the models match better for shorter emission times. The conformity of the models is thus improved when the investigated traps are located near the band gap edges or when the measurement temperature is low, both cases in which the emission times are short. A possible interpretation lies in the exponential dependence of the emission time on temperature and trap level: Adding an additional barrier slows down emission exponentially. For low barriers, i.e. traps near the band edges, the added barrier does not significantly change the dynamics while it decelerates emission more prominently at already high barriers. Since the relaxation energy is only considered by a quarter of its value compared to the NMP model in the SRHT model (Equation (3.5)), the aforementioned interpretation is also true for this Arrhenius corrected version of the SRH model which still deviates from the NMP model towards mid-gap albeit much less than the classic SRH model.

3.4. Experimental Results

In order to correctly asses the quantitative impact of the models on the calculation of density of states, actual measurement data have to be investigated. A thorough discussion of the nature of the HCS generating the defects which are to be analyzed in this section, is found in Chapter 4. The transformations of CP current to density of states (3.2) and (1.8) for the NMP and SRH model yield comparable spectra for the three models as shown in Figure 3.6.

A high level of noise in the spectra stems from the numerical derivation of the raw data, i.e. the CP current, which amplifies the various noise sources in the experiment. Although it is possible to measure the CP current itself with high precision, the rise and fall times of the CP pulse, which are varied in this kind of measurement, cannot be adjusted with an arbitrarily high precision since the cable inductances and capacitances impact the transition rates. Thus, longer averaging during the digitalization of the CP current cannot significantly decrease noise in the final spectrum. In order to improve the comparability of

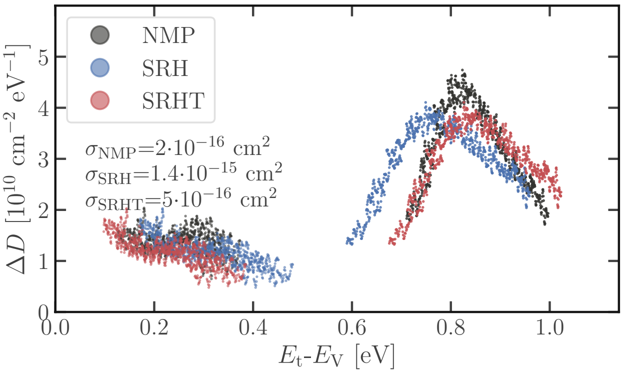

Fig. 3.6. SPCP spectra after HCS at −60 °C for 20 ks for all three models. Drain and gate voltages of 8 V and 4 V are applied during stress. It is noted that Equations (1.8) and (3.2) require a numerical derivative of the CP current leading to noisy data.

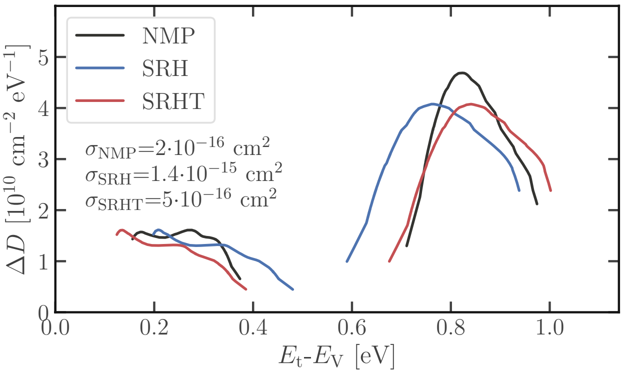

Fig. 3.7. Correction of the fluctuations in the data of Figure 3.6 using a moving average filter with Gaussian weights.

the spectra, they are smoothed using a moving average filter with Gaussian weights, as shown in Figure 3.7.

For the energy axis of the calculated spectra the conclusions from the previous section are shown in practice: In its corrected SRHT form, the SRH model shows very similar results while the data obtained from the SRH model without Arrhenius correction is shifted towards the middle of the band gap. Both SRH models use the same transformation for the density of states axis, thus the structural relaxations are only considered in the NMP model for this dimension.

From the density of states spectra, the actual numbers of traps N_{CP} can be extracted with Equation (1.6) and compared to N_{CP} obtained by the standard CP method, where the CP current is proportional to the trap density (Equation (1.3)). This comparison is presented in Figure 3.8. The integrated spectra for the various models are plotted as shaded areas rather than lines as the capture cross sections are determined experimentally (see Section 3.5) and thus have a variance. The respective areas are obtained by integrating over

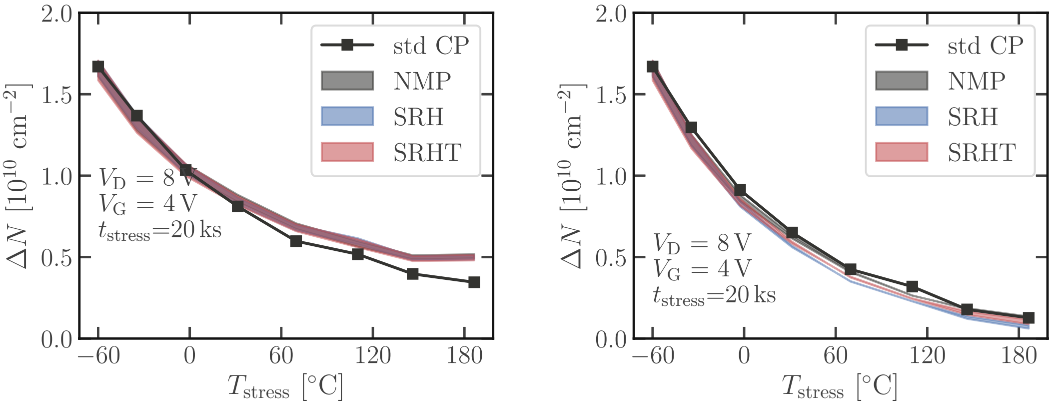

Fig. 3.8. Integrated SPCP spectra after HCS at various temperatures compared for all three models and standard CP. Left: Trap densities at a measurement temperature of −60 °C. Right: Trap densities measured at the stress temperature.

the active energy window corresponding to the pulse in the standard CP measurement as the latter is always performed at fixed rise and fall slopes as well as constant temperatures. Thus, data from integrated density of states spectra is directly comparable to trap densities calculated from the CP current in the standard CP experiment. Two major conclusions can be drawn from these comparisons: At first, the integration obfuscates the differences between the different models almost completely as the shaded areas for all models overlap very well. Thus, the impact of molecular relaxations is averaged out in the process of integrating the spectra. The second major learning is that the spectra become inaccurate when defect densities are small, i.e. for HCS at high temperatures, and near the band edges. This second conclusion is not obvious at a first glance but explains why the data of standard CP at low measurement temperatures (Figure 3.8 left) deviate from the integrated spectra, which is not the case when the readouts are done at the respective stress temperature (Figure 3.8 right): When a standard CP measurement is performed at a low temperature, the comparable trap density is obtained from the spectrum by integrating it over a large fraction of the band gap, including the density of states data near the band edges. This is due to the large active CP window at low temperatures (cf. Figures 1.12 and 3.3). When the CP measurements are performed at higher temperatures, the borders of the equivalent integration of the density of states from SPCP move towards mid gap. Therefore, the less precise fractions of the band edges are not considered when readouts are made at higher temperatures. The cause of this discrepancy near the band edges is twofold: On the one hand, the absolute number of defects created at these high stress temperatures are very low making it more difficult to obtain SPCP signals with sufficient quality. On the other hand, in the SPCP method the spectra are obtained by performing pulse rise and fall time sweeps at multiple temperatures where the investigated energy ranges overlap for all but the highest and lowest temperature (cf. Figure 1.12). Thus, at the band edges, the signals may be less precise due to missing additional data from other temperatures where the investigated energy ranges overlap.

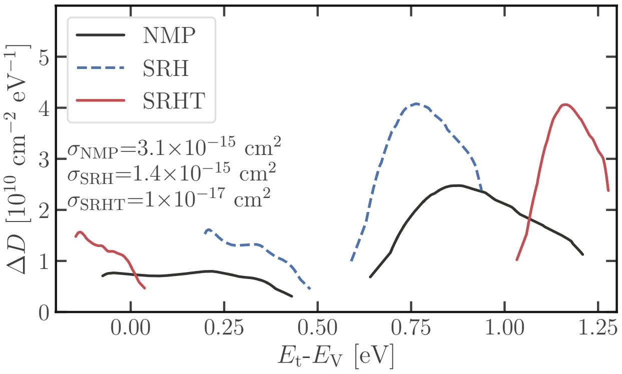

Fig. 3.9. Evaluation of the data of Figure 3.6 using a relaxation energy of 1 eV for electrons and holes.

Border traps typically show relaxation energies beyond 1 eV [48]. When the data from Figure 3.7 is recalculated with a relaxation energy of 1 eV, neither the SRH nor the SRHT model can approximate the NMP spectra (Figure 3.9). As for the SRHT model, the approximation of the transition energy (Figure 3.1) becomes invalid for the increased relaxation energies. As a consequence, models employing the Arrhenius modification of the capture cross section yield incorrect values for the relaxation energy when experimental data is fitted to them.

3.5. Determination of Capture Cross Section

The value of the capture cross section of interface traps has always been controversial as it is hard to directly obtain from simulations or experiments. Authors found values between $1.4 \times 10^{-25}\,\mathrm{cm}^2$ in random telegraph noise measurements [51] and $4 \times 10^{-13}\,\mathrm{cm}^2$ in deep level transient spectroscopy investigations [53]. For CP, literature suggests values between $1 \times 10^{-15}\,\mathrm{cm}^2$ and $1 \times 10^{-16}\,\mathrm{cm}^2$ [9]. In order to determine the capture cross section for the models used in SPCP, a new method based on the comparison of trap densities obtained from integration of spectra and standard CP is developed.

The basic premise of the method is that the trap densities obtained from any approach must be equal. In the standard CP method the calculation of N_{CP} is trivial (Equation (1.3)) as the CP current is proportional to the trap density, electron charge, interface area and CP frequency but not dependent on the capture cross section. As all these parameters are well known or adjusted during the experiment, the method of integrating the SPCP spectrum (Equation (1.6)), which is, contrary to the standard CP method, dependent on the capture cross section, can be used as a comparison to determine σ. First, the spectra have to be calculated for a variety of plausible capture cross sections. Then, these densities of states are integrated over the energy window which fits to the respective standard CP measurement in terms of CP pulse transition times and temperature. At this point, the value of sigma can be extracted from the intersection of SPCP and standard

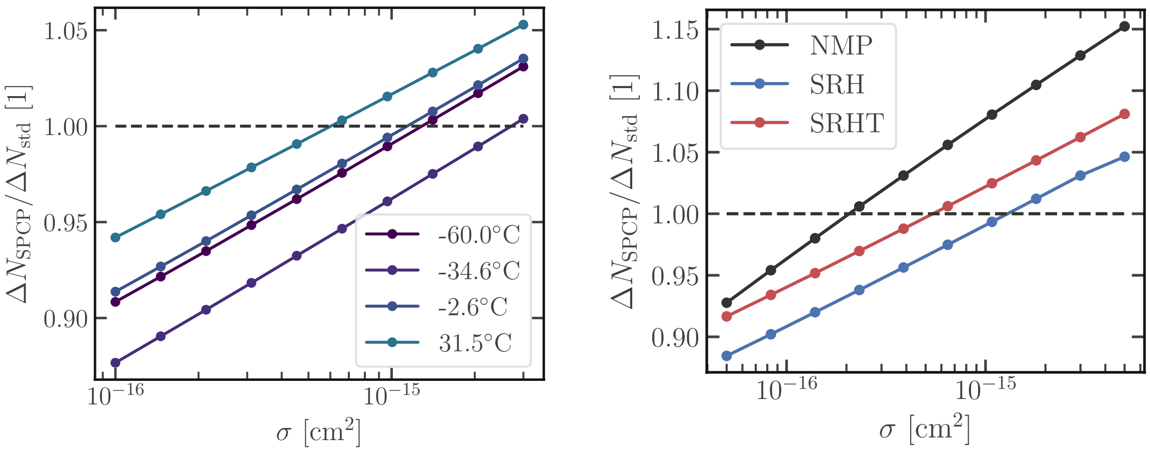

Fig. 3.10. Determination of the capture cross section by comparison of integrated spectra to the trap density of standard CP at varying capture cross sections. On the y-axis, the ratio N_{CP} from SPCP to N_{CP} of standard CP is plotted. Left: Data after HCS, evaluated with the SRH model. Temperatures in the legend are referring to the stress during HCS. Right: Data for the three models after a HCS at $-60\,°\mathrm{C}$

CP data when the trap densities are set in relation to the capture cross section. This is shown in Figure 3.10 where the trap densities are normalized to the respective trap densities of standard CP. Only the data from the four lowest temperatures in the HCS are considered at a measurement temperature of $-60\,°\mathrm{C}$. The four higher stress temperature data points are omitted due to their deviation explained in Section 3.4. From these data, the capture cross sections result to σ^{NMP}=2.0 ± 1.3 × $10^{-16}\,\mathrm{cm}^2$ for the NMP model, σ^{SRH}=14 ± 9 × $10^{-16}\,\mathrm{cm}^2$ for the SRH model and σ^{SRHT}=5.7 ± 4.3 × $10^{-16}\,\mathrm{cm}^2$ for the SRHT model. Consistently, the capture cross sections of the SRH and SRHT model lie within the same range. Generally, it would also be possible to investigate the capture cross section of the defects in the virgin device which are present after the fabrication process. Unfortunately, the trap densities and densities of states of the investigated technology are too low for an analysis with sufficient precision.

CHAPTER 4

Hot-Carrier Degradation Revisited

Chapter Contents

> *If you want to make a bond, you are to take the risk of tearing.*
>
> — Antoine de Saint Exupéry, *Le Petit Prince*

Although HCD on Si MOS structures has already been investigated for over three decades, two major questions have still not been answered satisfactorily. On the one hand, the temperature dependence of HCS, although often discussed in literature [4], [7], [54], [55], has not been investigated thoroughly on an experimental basis. On the other hand, the relationship of interface and border traps is often examined on the basis of time constants but not with regard to voltage dependencies. The failure to consider these voltage dependencies sometimes leads to the incorrect mapping of trap capture and emission time constants to defect depths [37]. The focus of this chapter are long-channel devices, in which lower temperatures facilitate HCD, as the power transistors investigated in Chapter 5 usually have a gate length above 100 nm (cf. Section 1.2.2).

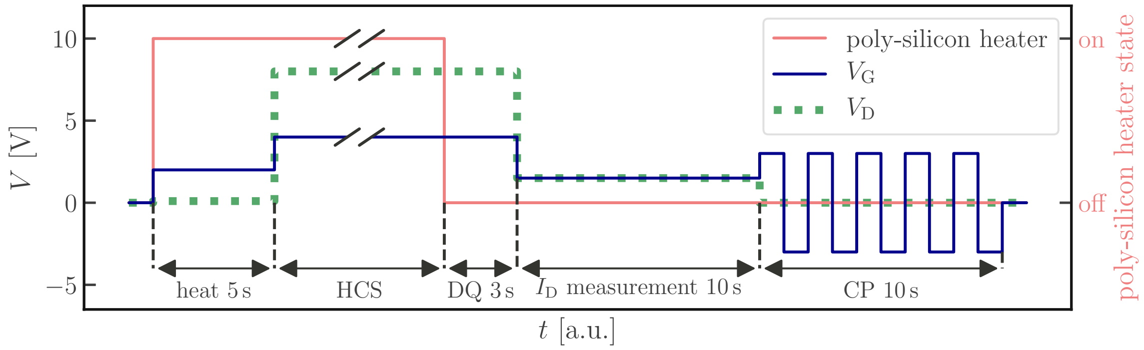

Fig. 4.1. Sequence of a HCS experiment with degradation quenching (DQ). Device temperatures are adjusted with a poly-heater. Directly after the HCS, the DQ step ensures that no traps are lost to recovery. The stress time is variable.

4.1. Design of the Hot-Carrier Stress Experiment

Whenever a CP experiment is performed at various stress temperatures, one faces two major problems which may lead to a wrong interpretation of the obtained data [56]:

(i) The active CP window in the Si band gap is strongly temperature dependent (Figure 1.12). Based on SRH statistics, 83% of the band gap are covered by the CP experiment at −60 °C while this number drops to only 63% at 125 °C. Although the models presented in Chapter 3 allow for a precise determination of the energy boundaries, the traps outside the active CP energy window are lost at increased temperatures. This may distort the overall result.

(ii) The removal of the stress condition may initiate recovery which is not understood completely. It is certain though that increased temperatures foster recovery [57]. Thus, the reduction of trap densities due to recovery is more pronounced at higher temperatures rendering it impossible to obtain comparable data sets as the varying impact of the recovery cannot precisely be determined.

So far, HCD measurements have been conducted at the same stress and measurement temperature. Considering the aforementioned points, the defect densities should always be analyzed at the same temperature, independent of the stress temperature, to allow for comparison of the results. Only if the aforementioned conditions are fulfilled, the true temperature dependence of HCD can be determined.

All of these issues can be tackled by degradation quenching (DQ) which has been implemented in a similar way for NBTI by Aichinger et al. [9]. DQ is incorporated into the five-step HCS measurement procedure (Figure 4.1) where all temperatures are adjusted using the poly-heater [56]:

1. The device is first heated to the desired stress temperature for 5 s before the HCS commences. During this preheating step, a slightly positive drain voltage of 0.1 V

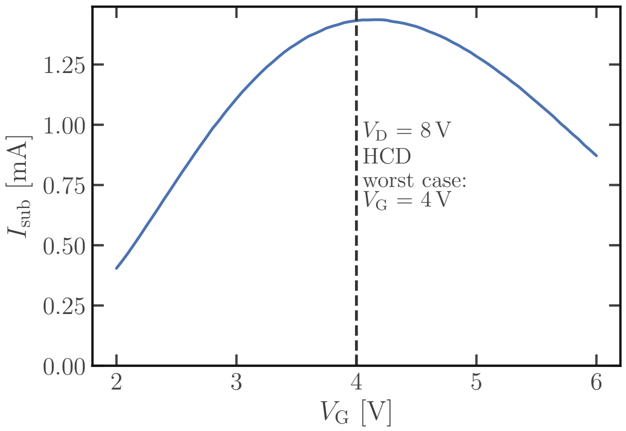

Fig. 4.2. Substrate current dependence on the gate voltage at a drain voltage near breakdown. The gate voltage at the highest substrate current reflects the worst-case scenario for HCD.

and a gate voltage of 2 V are applied. This ensures a drain current which is strongly temperature dependent in order to monitor whether the poly-heater successfully heats the device.

2. Following the heating step, the stress conditions are applied. For the lateral devices used in these investigations, 8 V at the drain and 4 V at the gate while body and source are grounded is the worst-case HCS condition. No higher drain voltage can be applied as the body-drain diode would otherwise break down. The gate voltage is obtained from maximizing the substrate current at the respective maximum drain voltage (Figure 4.2) which stems from carriers created by impact ionization in the channel [3]. This is a good indirect predictor for the magnitude of the stress impact.

3. During the DQ step, launched directly after the HCS for 3 s, the stress conditions remain applied while the poly-heater is switched off. This causes the device to cool down to the base temperature of the experiment, in our case −60 °C, which freezes possible fast recovery of traps. Unfortunately, the decrease of temperature accelerates HCD, thus the DQ causes additional unwanted stress unrelated to the preceding HCS. This additional stress is negligible, as will be shown in section Section 4.1.1.

4. After the DQ, the drain current, which is sensitive to interface defects, is measured at a operating point of 1.5 V at the drain and gate. While it does not allow for an exact quantitative evaluation of trap densities, it is used as a qualitative indicator whether traps recover directly after the stress, even after the DQ step which cools the transistor to a very low base temperature. This step lasts for 3 s.

5. Finally, 10 s of standard CP are applied to ensure that even after measurement of the drain current no fast recovery is observed. The advantage of using CP at this point is the possible quantification of loss of generated defects due to recovery. The

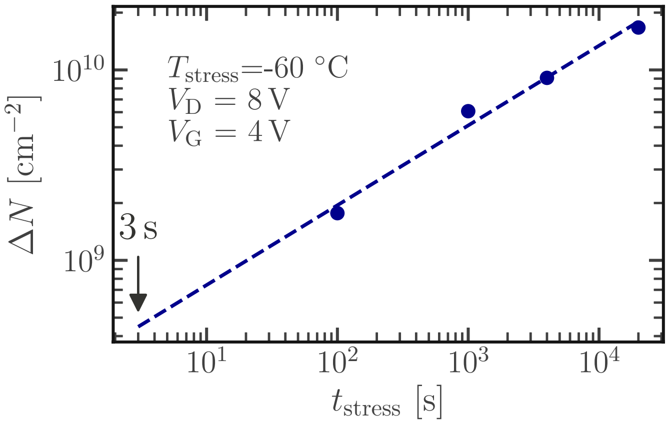

Fig. 4.3. Time dependence of trap generation during HCS, extrapolated to 3 s which corresponds to the duration of DQ. Data are fit to a power law using an exponent of 0.42.

reason why this step is not employed directly after DQ is that switching from the stress conditions to CP requires a rewiring of the contacts since drain and source are tied in the CP measurement. Leaving drain and source separated during CP would cause an unwanted current flow which interferes with the actual CP current. This parasitic current is caused by the ground potentials which have to be applied on both drain and source during CP. They may be shifted within the specifications of the source-measuring instrument, thereby causing an compensating current during the on-state of the transistor. Although the rewiring is done automatically via a switching matrix, it cannot be guaranteed that no traps are lost very rapidly due to the rewiring procedure which leaves some the contacts in a undefined floating state for few tens of milliseconds. However, the switching from DQ to step 4 is possible without issues.

Before and after this procedure, arbitrary measurements and readouts like SPCP can be performed.

4.1.1. Possible Measurement Errors

As already insinuated, the design of the HCS experiment is prone to errors. Two major sources of problems can be identified. The first possible error has already been discussed in step four and five of the measurement sequence: Recovery of defects after stress. While traps which recover directly after turning off the HCS can only be qualitatively identified, the CP method in step five offers a quantitative estimation of recovery.

The second major issue in the hot-carrier measurement setup is the added stress during the DQ step. An estimation of its impact on the trap density is easily possible: Since DQ lasts for 3 s, the traps generated after a HCS of this duration set an upper limit for the deviation. This is still a very pessimistic estimate since HCD does not accumulate in a linear but rather logarithmic fashion. Thus, the stress added during DQ on top of the regular HCS is certainly a lot less severe than a 3 s stress on a virgin device. Practically, it is not even easily possible to perform a CP readout after a 3 s HCS on the devices investigated in this chapter because the trap density increase is too small to resolve with the available measurement equipment. In order to still be able to estimate the impact, measurements at varying stress durations are performed (Figure 4.3). From these data, the stress impact after a 3 s stress can be extrapolated by a power law [58], [59]. For the lateral structures investigated in this chapter, this extrapolation yields a trap density of $4.5 \times 10^8\,\mathrm{cm}^{-2}$ which is beyond the detection limit of the CP measurement.

4.2. Temperature Dependence of Hot-Carrier Degradation

Using the experimental procedure described in Section 4.1, the temperature dependence of HCD is investigated as in [56]. Ranging from −60 °C to 186 °C, HCS experiments at eight different stress temperatures are performed to obtain the density of trap states and their spectra. In order to interpret the outcomes properly, the data from steps 1, 4 and 5 of the HCS experiment have to investigated thoroughly first. These results show whether the poly-heater worked as intended as well as if and how severe recovery of defects manifests itself.

4.2.1. Heating Step of the Hot-Carrier Stress Experiments

Investigating the drain current during step 1, the heating step, allows for taking a closer look on the progression of the temperature increase of the transistor due to the temperature dependence of the drain current. As shown in the saturation of the drain current in Figure 4.4, the 5 s of this step are sufficient to bring the devices to the target temperature for the subsequent HCS. The currents are normalized to the initial current at the base temperature of −60 °C and the operating point of 0.1 V at the drain and 2 V at the gate shows a negative temperature coefficient for the drain current. Naturally, the lower the desired stress temperature, the lower the absolute change of the drain current. Thus, noise increases with decreasing target HCS temperatures. As expected for the experiment at the base temperature, where no bias was applied to the poly-heater showing, only noise but no change of the drain current is observed.

4.2.2. Investigation of Post-Stress Recovery

Steps 4 and 5 of the HCS measurement procedure determine the fast recovery of defects after the stress. The experiments reveal no recovery (Figure 4.5). Neither the drain current change nor the trap density obtained from CP after stress measured in step 4 and step 5, respectively, show any signs of recovery and stay constant over the measured interval after stress. This leads to the conclusion that the low readout temperature of −60 °C renders the loss of defects after stress negligibly small. Both parameters increase in value

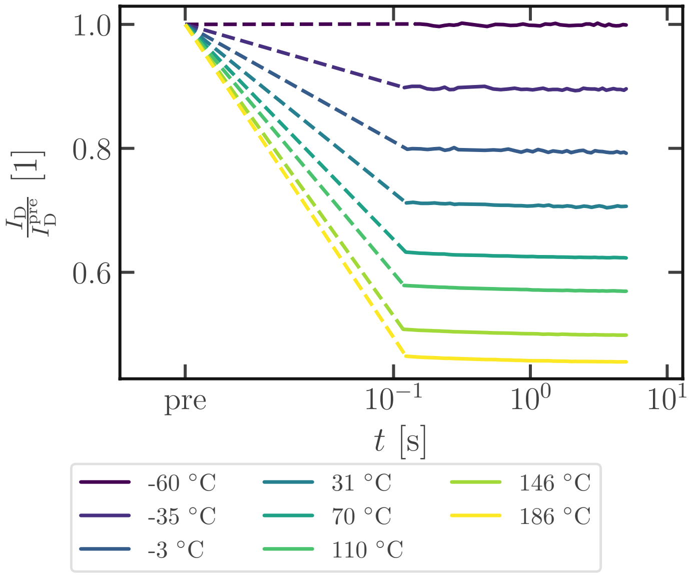

Fig. 4.4. Drain current during the heating step of the HCS measurement sequence presented in Figure 4.1 with 'pre' referring to a measurement before the heating step at the temperature of −60 °C. Temperatures indicated in the legend refer to the stress temperature.

for decreasing stress temperatures consistent with the well-known behavior of HCD in long-channel devices.

4.2.3. Charge Pumping Analysis

In order to get a clear picture of the temperature dependence of HCD, not only the number of defects is analyzed, but also their density of states. This allows for a more precise picture of the actual microscopic nature of the traps generated at various temperatures. Conveniently, as shown in Section 4.2.2, there is no fast recovery of degradation after stress at cold temperatures. Thus, it is possible to investigate spectra and numbers of traps without further consideration of possibly recovering defects.

Figure 4.6 depicts the trap spectra generated at various stress temperatures after HCS. Without checking the actual number of traps, these densities of states already indicate the well-known behavior of HCD in long-channel MOSFETs: Increasing stress temperatures suppress degradation. This is apparent due to the steady decrease of the spectra at all energies which show a peak in the upper and lower half of the band gap. Two peaks are expected for P_b centers [39] although they should have similar heights which is clearly not the case in these data and is a peculiarity which will be discussed in Section 4.3.

The steady decrease of the spectra raises the question whether various types of defects are generated at different stress temperatures or if the temperature rather acts as a deceleration factor for the creation of the same kinds of defects. This issue can be tackled by comparing the density of states after stresses at different temperature to the ones generated at various

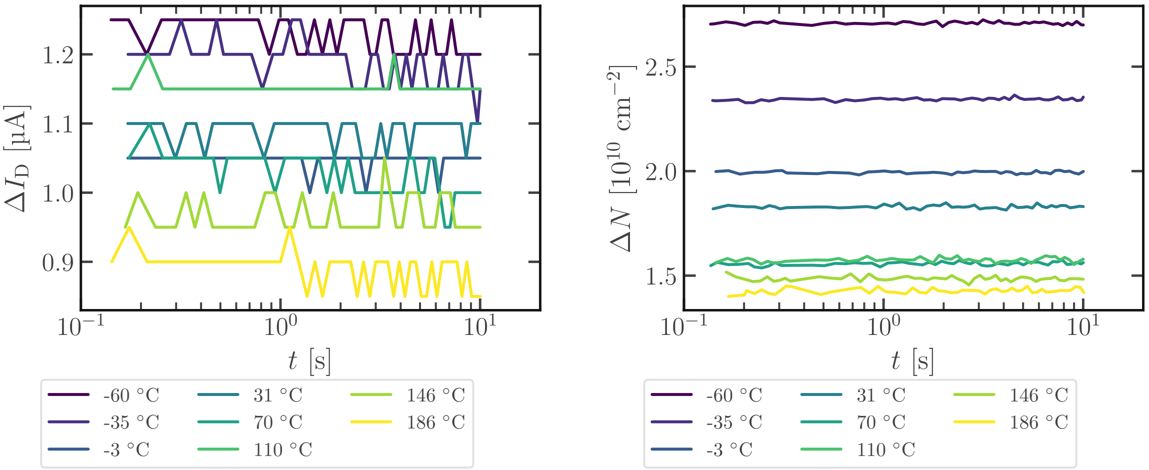

Fig. 4.5. Change of drain current (left) and change of the trap density from the CP current (right, using Equation (1.3)), both due to HCS, during the recovery steps of the HCS measurement sequence presented in Figure 4.1 at the temperature of −60 °C. Temperatures indicated in the legend refer to the stress temperature.

stress durations at the lowest temperature where most defects are generated. Such a comparison is shown in Figure 4.7 where the HCS experiments performed at the base temperature (−60 °C) and 186 °C for 20 ks are compared to three spectra after a 4 ks, a 1 ks and a 100 s stress at the base temperature. These additional data sets fit perfectly to the long stress tests and are indistinguishable from spectra generated at varying temperatures for 20 ks.

Thus, unless *different* defects with *identical* densities of states are generated at varying stress temperatures - which is highly unlikely, temperature only acts as a deceleration factor in long-channel devices without impacting the types of microscopic traps generated.

The two available methods of SPCP and standard CP open the possibility to investigate the numbers of traps generated after HCS twofold. The integration of spectra, discussed in detail in Chapter 3, requires a model for the calculation of the trap spectra while the standard CP method allows for a straight-forward analysis of the CP current (Equation (1.3)). Results of these approaches are depicted in Figure 4.8 which is a more thorough visualization of Figure 3.8. Additionally to trap densities measured at the base temperature of the experiment and trap densities obtained at their respective HCS temperatures, three special data points are added: At 30 °C, 100 °C and 175 °C, the HCD experiment was performed without the use of the poly-heater. Instead, the conventional method of adjusting the wafer temperature with the chuck was used. These data points fit very well to the trap densities obtained by using the poly-heater justifying that it can indeed be used to regulate the device temperature and that it does not influence the HCS.

The data presented in Figure 4.8 show clearly why performing readouts at the stress temperature instead of a common base temperature fails to unveil the full picture of stress damage. Due to the change of the active energy window of defects, a significant fraction of the traps are not detected at elevated temperatures. Since the spectra within the band

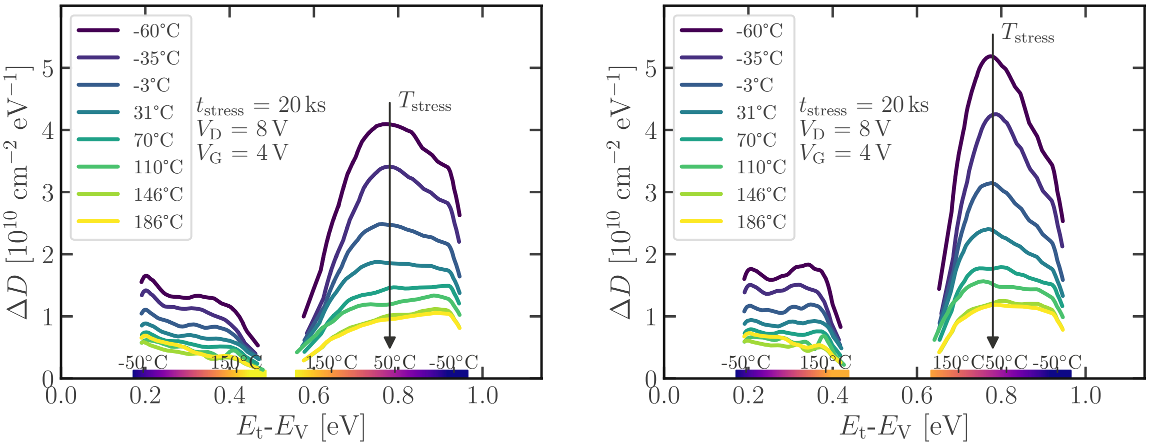

Fig. 4.6. SPCP performed before and after HCS to obtain the stress-generated density of states using capture cross sections selected according to investigations from Chapter 3. The color bar on the x-axis represents the readout temperature for the respective energies assuming an emission time of 200 ns. Temperatures in the legend refer to the temperature of the HCS. Left: Analysis using the SRH model. Right: Analysis using the NMP model.

gap are clearly not constant, the impact of this loss of traps cannot be quantified in any meaningful way unless these spectra are known. Even if an estimation of the trap profiles was possible in some way, a model for the change of the active energy window is still needed. Unfortunately, these issues are not limited to the CP evaluation but are found for any measurement method since the defect dynamic is always temperature dependent.

It is noted that all presented spectra in this subsection lead to the same conclusions, no matter if evaluated with the SRH or NMP model. Of course, the shapes of the energetic trap profiles vary, but no doubt about the interpretations of the data is left. This can be seen as another clue why the SRH model has held up so long for interface defects. Although missing a key element of the physics of these traps, the structural relaxation, SRH may very well predict a lot of aspects of the dynamics of interface defects correctly, most likely due to the low values of their relaxation energy. Especially when the energetic spectra are integrated, as shown in Figure 4.8, the data are almost identical besides for a slight deviation around 70 °C.

4.2.4. Temperature Dependence of the Drain Current Change

Many investigations of HCD such as [55], [60]–[62] use the drain current or related parameters like the transconductance as a measure for trap induced damage. This subsection aims at benchmarking the quality of the drain current as a qualitative and quantitative parameter for the investigation of trap densities. The drain current change for HCS tests at different temperatures, Figure 4.9, reveals a similar behavior as the analogous CP measurement presented in Figure 4.8. Due to the small recorded trap

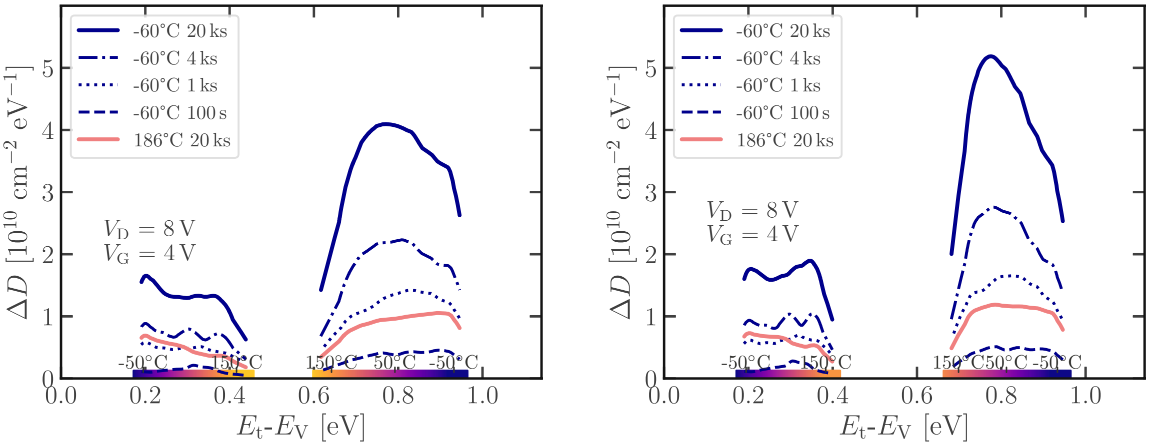

Fig. 4.7. SPCP performed before and after HCS to obtain the stress-generated density of states using capture cross sections selected according to investigations from Chapter 3. The color bar on the x-axis represents the readout temperature for the respective energies assuming an emission time of 200 ns. In contrast to Figure 4.6, the stress durations are varied additionally to the HCS temperatures. Both parameters are found in the legend. Left: Analysis using the SRH model. Right: Analysis using the NMP model.

densities, the drain current is a lot more noisy though. Except for a data point at around 0 °C, the drain current changes obtained at the base temperature of the experiment are always higher than their respective counterparts measured at the stress temperature. This confirms the conclusion of Section 4.2.3, which states that a common low base temperature for all measurements should always be preferred if HCD is analyzed at multiple stress temperatures. In other words, potential traps are lost for the further analysis when readouts are performed at the same temperature as the stress test.

Comparing the drain current changes to the trap densities obtained from CP reveals some interesting features of the trap dependence of the drain current (Figure 4.10). For the drain current changes, a surprisingly good correlation is found with CP trap densities measured at the same respective measurement temperatures, even though the drain current change shows significant noise. Since the measurement temperature dictates the active energy window of the trap dynamics, this is certainly expected. As the trap densities and drain current changes are fairly small, these interpretations could lack information about the relationship of drain currents and actual numbers of traps and should therefore only be considered for such small defect densities. There is the possibility that these correlations cannot be observed for devices with significantly more degradation. In order to obtain a useful model of the relationship of trap densities and the drain current, a well calibrated TCAD model might be useful. It is though questionable if this is worth the afford when methods like CP are available.

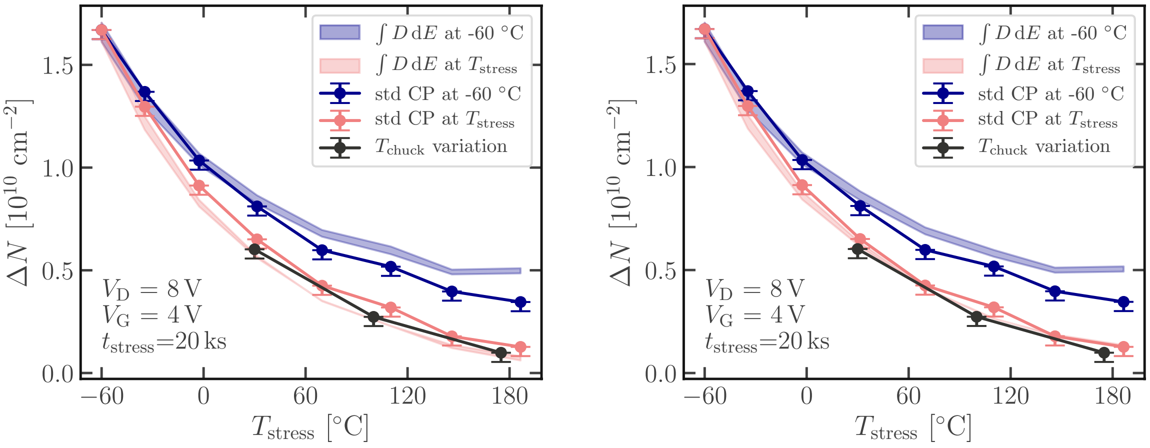

Fig. 4.8. Number of traps obtained from the integration of defect spectra (Equation (1.6)) and standard CP (Equation (1.3)) at the base measurement temperature of −60 °C and the stress temperature. The ranges of the integrated spectra reflect the variation of the respective capture cross sections and the error bars are based on the additional stress induced during the DQ step. Left: Analysis using the SRH model. Right: Analysis using the NMP model. For both models the data is almost identical except for the stress temperature readout around 70 °C.

4.3. Interface and Border Traps

So far, the previous chapters focus on the discussion of interface defects. However, it is known that HCD also creates border traps, i.e. defects in the oxide which are located in the direct vicinity of the interface but not directly on the interface itself [63] (cf. Section 2.3). Obviously, among other things, time constants for capture and emission increase with the depth of the defect in the oxide which is the most obvious observed effect. Another less reported feature of border traps in the context of HCD is their voltage dependence. The influence of both the time and voltage dependence of border traps is discussed in this section. These findings are based on Ruch et al. [11].

4.3.1. Detection of Interface and Border Traps

Applying the universally accepted CP method, frequency dependent CP (cf. Section 1.3.5), before and after HCS (Figure 4.11), reveals very little border trap densities. Due to the energy distribution of border traps, the gate voltage also plays a major role in whether they can be detected. Increasing the absolute value of base or high level of CP beyond inversion and accumulation causes an increase of the oxide field since the surface potential on the interface does not change significantly anymore at this point. Thus, the energy bands in the oxide change, thereby enlarging the active energy window of CP. In Figure 4.12, which uses NMP dynamics, the observable traps are shown within the salmon-colored area. At a pulse base level of −1.1 V less traps are visible than at −3 V. For a fixed energetic trap

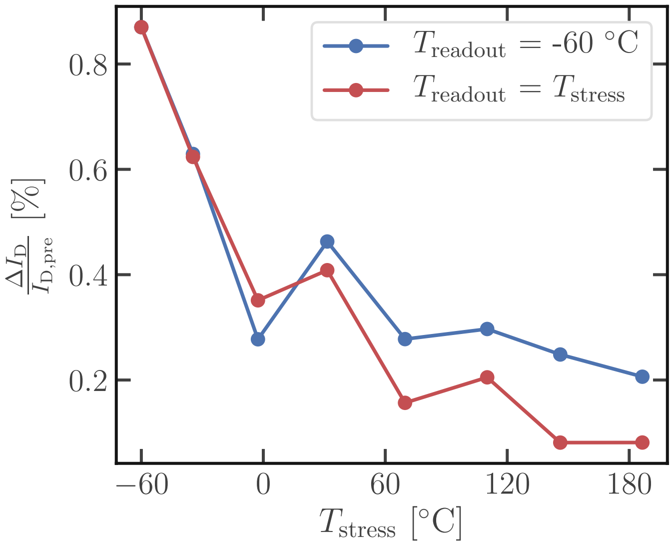

Fig. 4.9. Change of the drain current at the operating point of V_D=V_G=1.5 V due to HCS at varying stress temperatures. Readouts performed at the base temperature of the experiment and at the respective stress temperatures.

level, deeper areas can be accessed with decreasing frequencies while for a fixed position a wider spectrum of traps becomes active in CP. The caveat of the simulation presented in Figure 4.12 is that the occupancy, visualized by a gradually darker blue shade for increased probability, is calculated for equilibrium conditions. Thus, the frequency dependent depth of occupation observed in CP cannot be depicted and defects at all depths are occupied in the simulation which is clearly not possible for all CP frequencies.

The voltage dependent active energy window motivates a different approach for the characterization of border traps. After a HCS, the saturation behavior of the constant high CP method is observed to change as shown in Figure 4.13. Although the virgin device saturates very well at approximately −1.1 V, saturation only starts at 3 V after the stress. Thus, assuming only insignificant numbers of detectable border traps in the virgin device, the gate voltage of −1.1 V is defined as the (arbitrary) cut-off point between border and interface traps. The stress-induced further increase of the CP current at lower CP base levels is attributed to voltage-dependent border traps. The basic equation of CP, Equation (1.3), is split into

$$N_\mathrm{it} = \frac{I_\mathrm{CPit}}{q f^\mathrm{CP} A_\mathrm{eff}^\mathrm{CP}} \tag{4.1a}$$

$$N_\mathrm{bt} = \frac{I_\mathrm{CPbt}}{q f^\mathrm{CP} A_\mathrm{eff}^\mathrm{CP}} \tag{4.1b}$$

for interface and border traps which allows for a voltage dependent separation of interface and border traps.

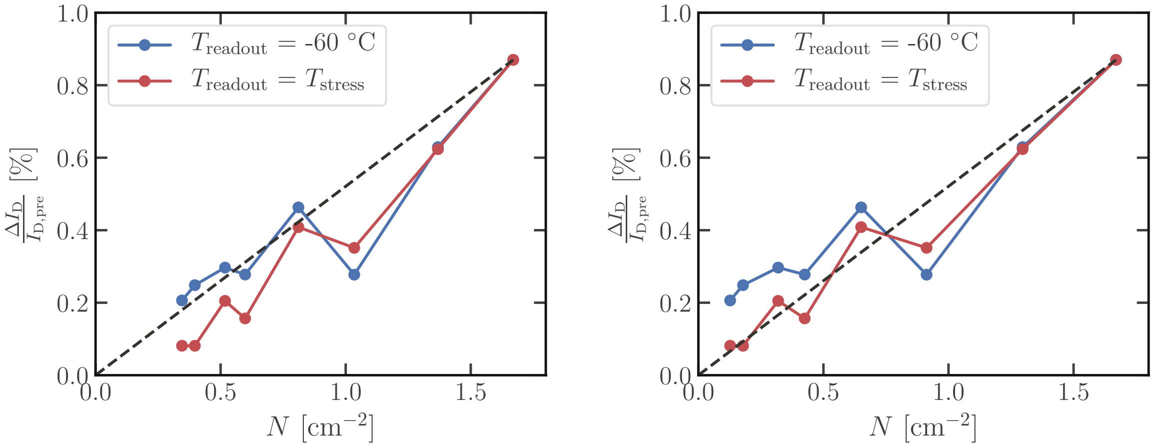

Fig. 4.10. Change of the drain current at the operating point of V_D=V_G=1.5 V in the saturation regime due to HCS compared to trap density measured with CP. Readouts of I_D performed at the base temperature of the experiment and at the respective stress temperatures. Left: CP trap density on the x-axis measured at the base temperature. Right: CP trap density on the x-axis measured at stress temperature.

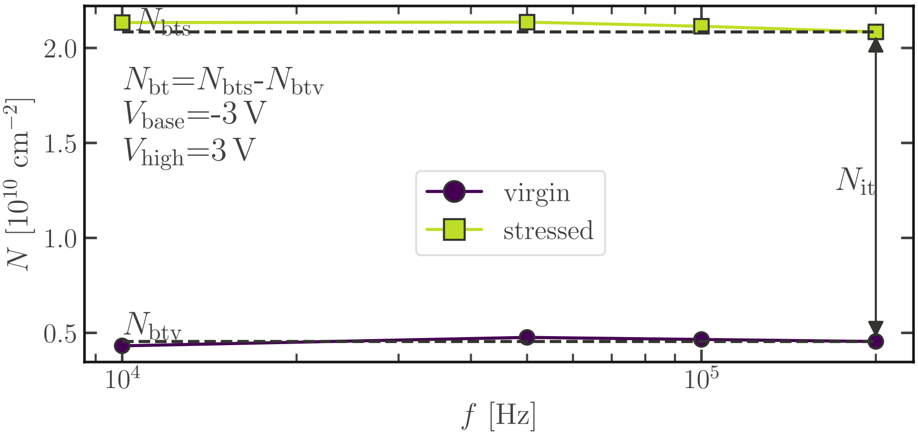

Fig. 4.11. CP at varying frequency before and after a HCS for 20 ks at −60 °C.

When investigating the frequency dependence of the traps at an increased CP base level of −1.1 V instead of −3 V, significantly more frequency dependent border traps are observed as shown in Figure 4.14. This is expected as the smaller CP pulse amplitude activates less border traps at high frequencies. Traps which would normally be activated at the base level of −3 V are visible at decreased frequencies when the CP base level is set to −1.1 V as this gives them enough time to capture and emit charges from the channel. These defects have slower time constants at the increased CP base level because their energetic position must lie below the valance band (Figure 4.12) for this voltage. At

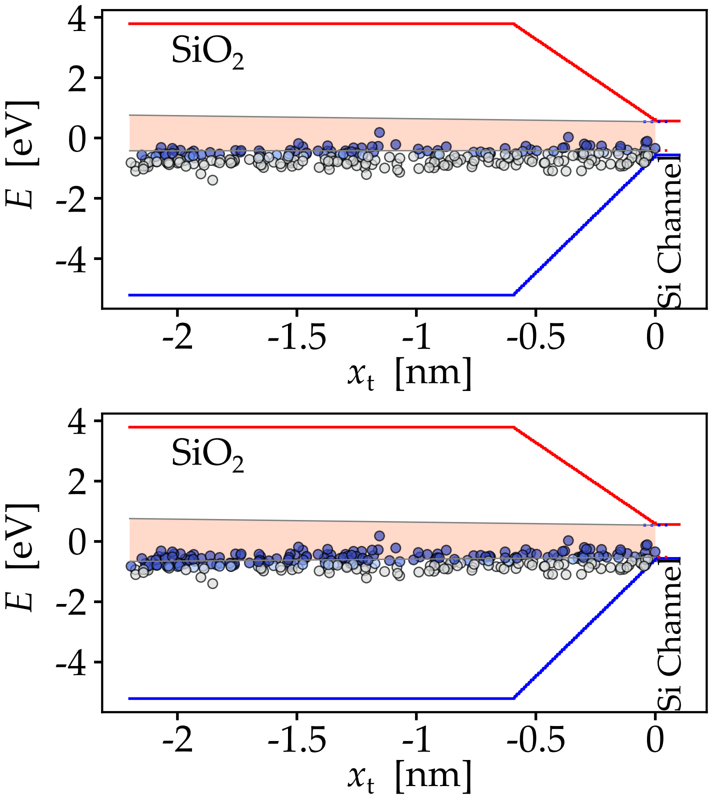

Fig. 4.12. Qualitative representation of the energy region scanned by CP in a MOS structure. Simulated with the tool Comphy [64], [65]. Top: Active energy window for traps at CP base and high levels of −1.1 V and 3 V, respectively. Bottom: Increased active energy window for traps at CP base and high levels of −3 V and 3 V, respectively.

increased CP amplitudes, the valence band position is shifted down, such that the border trap energies are shifted to higher levels (in relation to the valence band energy) causing them to be fast enough to be accessed even at high CP frequencies. Thus, border traps below the Si valence band are either accessed by lowering the CP base level or frequency. This observation is consistent with literature, where border traps are actually found to be below the Si valance band edge [48].

4.3.2. Quantitative Comparison of Interface and Border Traps after Hot-Carrier Stress

Due to the complex interplay of voltage and time dependence of border traps, which was explored in Section 4.3.1, quantifying the number of interface and border traps proves to be difficult. For example, the sweep of the CP frequency at a pulse base level of −3 V (Figure 4.11) would have suggested that hardly any border traps were created during stress while at a pulse level of −1.1 V, a clear increase of trap densities for lower frequencies is observed, albeit still insignificant compared to the increase of interface traps. The

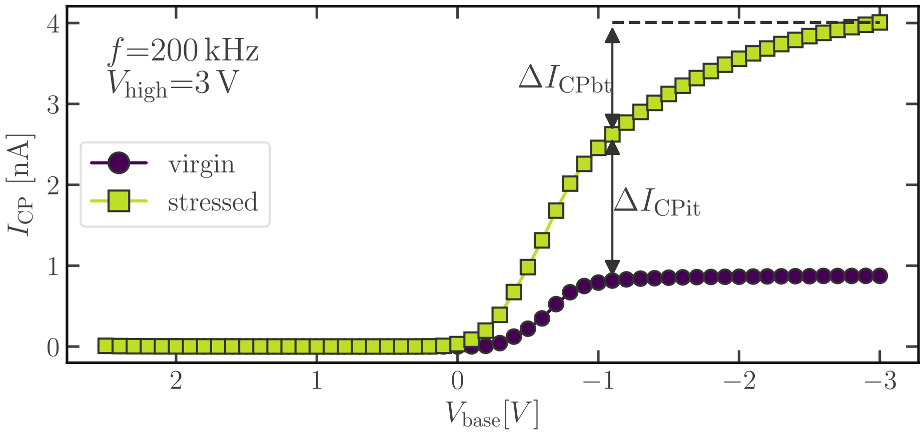

Fig. 4.13. Constant high CP measurement. Interface and border traps are separated at a pulse base level of −1.1 V.

whole picture is different when border and interface traps are separated by two CP pulse base levels as depicted in Figure 4.13 where the increase of border traps is of the same magnitude as the increase of interface defects. The two CP approaches are compared in Figure 4.15, where a frequency of 200 kHz and a pulse base level of −1.1 V were chosen for constant high and frequency dependent CP, respectively. For these parameters, the interface trap density is equal by definition in both cases since interface traps are separated in the voltage dependent CP method at −1.1 V and in the frequency dependent CP method at the highest frequency, 200 kHz. This allows for a direct comparison of border traps analyzed by frequency and voltage. Clearly, the voltage dependence trumps the time dependence of border traps for HCD presented in this chapter.

A further analysis of the voltage dependent border traps reveals how they are created by HCD along with interface states. As shown in Figure 4.16, where stress experiments with varying severity of degradation are shown, border traps are generated at the same rate as interface traps for low stress intensities. When the HCS temperature decreases, which causes an increase of traps, interface traps take the upper hand. A probable explanation for this observation lies in the microscopic mechanism of HCD. During a HCS, hydrogen is released as its covalent Si-H bonds are broken by hot carriers, thereby creating interface defects. The atomic hydrogen then may go on to create border traps [66]. Thus, interface and border traps could be created at the same rate. At some point, the atomic hydrogen dimerizes to molecular hydrogen before it can create further border traps causing a saturation of their generation. Then, the interface traps dominate the HCD process.

4.3.3. Spectral Impact of Border Traps

As observed in Figures 3.6, 4.6 and 4.7, the density of states spectra obtained after HCS do not show the characteristic two humps of equal height which are expected for P_b centers [39], which are most the likely candidate for interface defects. Since, as shown in

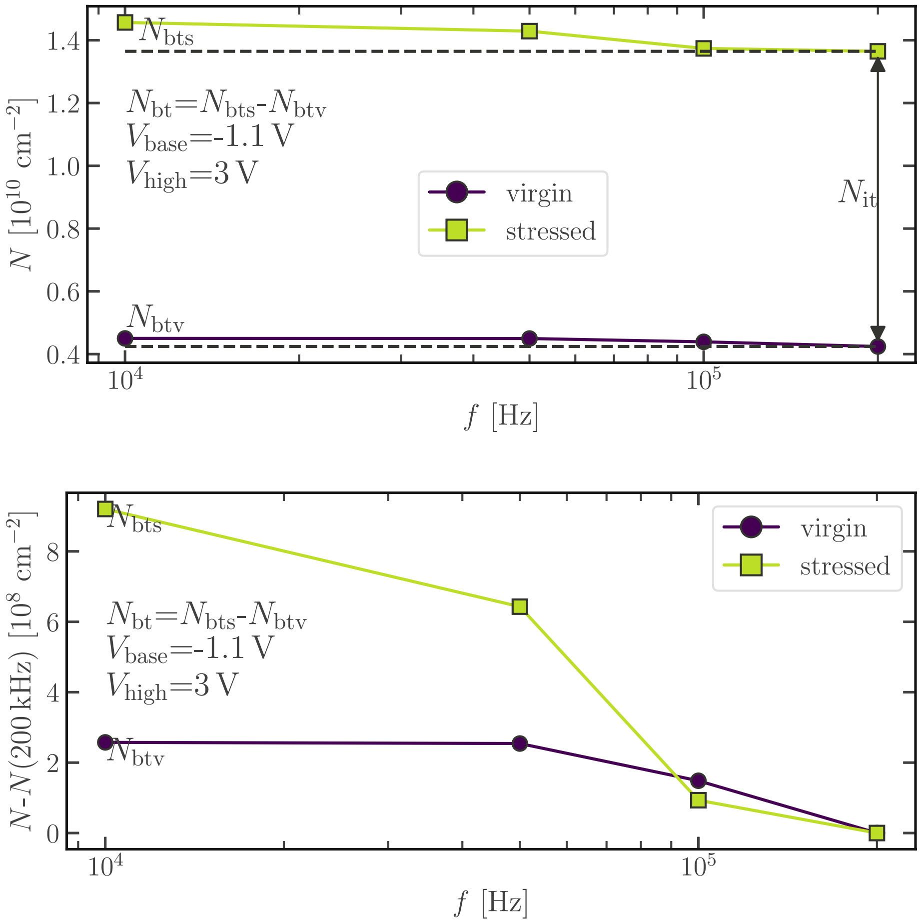

Fig. 4.14. CP at varying frequency before and after a HCS for 20 ks at −60 °C with a reduced CP amplitude, i.e a pulse base level of 1.1 V instead of 3 V. Bottom: Data from top figure, but plotted with respect to the trap density at the highest measured frequency.

Section 4.3.2, substantial amounts of border traps are observed after HCS, the densities of states have to adapt accordingly. Thus, the deviation from the typical P_b spectrum after HCS likely stems from border traps. Further evidence for this assumption is shown in Figure 4.17: Density of states spectra are shown for various stress durations. For the longest HCS, a spectrum after a long recovery, where the device was heated for 13 h, is added. Near the valence band, the post-recovery densities of states show a behavior different from the spectra after shorter stress durations: For these lower trap energies less recovery seems to be observed. Thus, different kinds of defects must be involved after stress and recovery. These different recovery mechanisms of traps have been documented before [63] and offer a plausible explanation for the presented data.

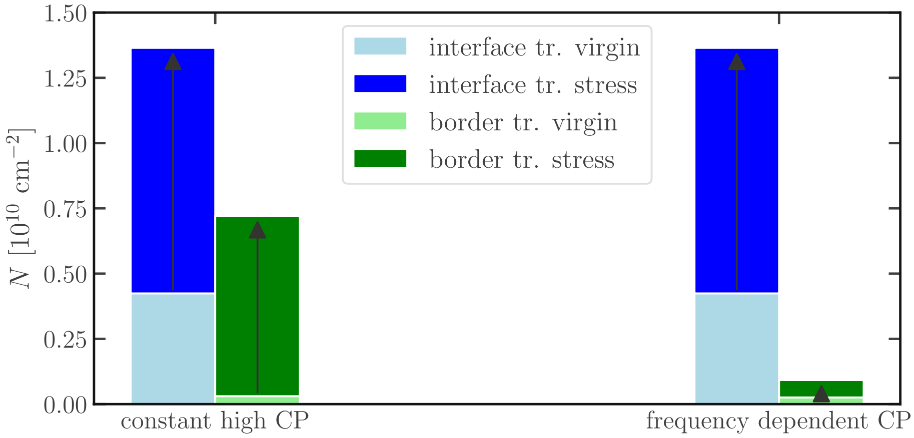

Fig. 4.15. Comparison of interface and border traps detected by the constant high and frequency dependent CP methods after a 20 ks stress at −60 °C. The constant high CP frequency was set to 200 kHz, the base level of the frequency dependent CP pulse was set to −1.1 V.

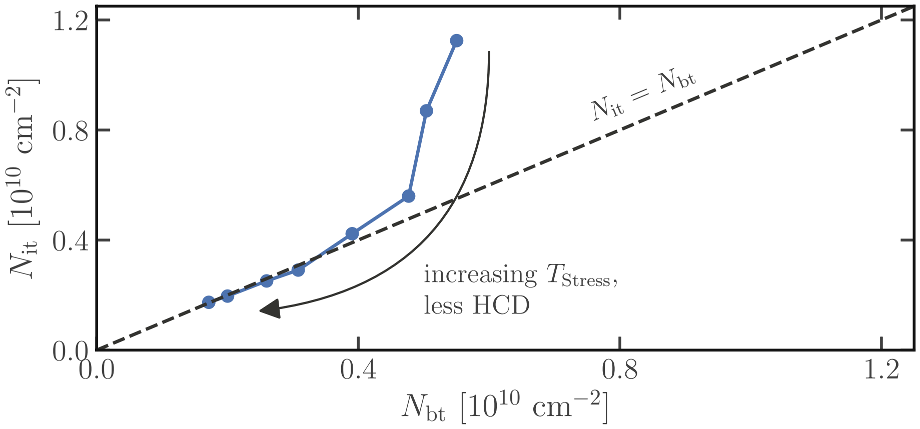

Fig. 4.16. Correlation of border and interface traps after 20 ks of HCS at different stress temperatures. The variation of the stress temperature allows for dosing the trap generation (cf. Section 4.2). Traps are separated at different CP pulse base levels as explained in Figure 4.13.

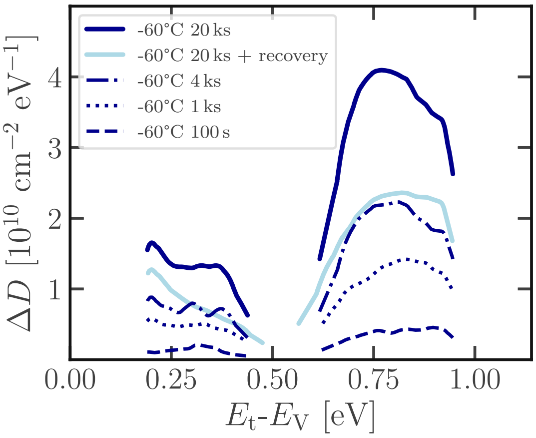

Fig. 4.17. Density of states of HCD induced damage for varying stress times. The light blue data set represents the 20 ks stress after a 46.8 ks recovery at 185 °C. Spectra are analyzed with the SRH model.

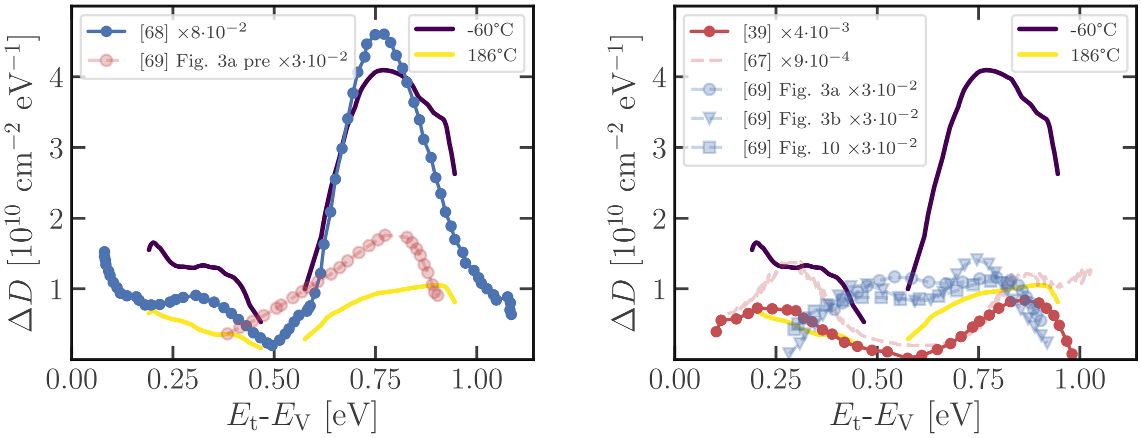

Fig. 4.18. Spectra of HCS after 20 ks stress experiments at −60 °C and 186 °C compared to densities of trap states from literature. The cited values are scaled by a factor indicated in the legend.

4.3.4. Densities of States of Traps in Literature

A great variety of authors have analyzed traps in oxides of MOS structures [39], [67]–[69] and found many seemingly unrelated trap spectra.

A few examples of such densities of states are depicted in Figure 4.18. A very interesting spectrum was measured by Devine et al. [68], also after HCD (Figure 4.18 left, blue). Like for the stress at −60 °C, two peaks are observed. The peak in the upper half of the band gap is also increased compared to the counterpart in the lower half of the band gap. It is therefore likely that Devine et al. [68] also observed border trap behavior. Similarly, Ma [69] (Figure 4.18 left, red) observed a significant peak in the upper half of the band gap after irradiation. Following recovery, these irradiation damage spectra (Figure 4.18 right, blue circles and triangles) resemble P_b centers characterized by Ragnarsson and Lundgren [39] (Figure 4.18 right, red circles). In the same publication [69], HCD was also investigated (Figure 4.18 right, blue squares). Additionally to Ragnarsson and Lundgren [39], Uren et al. [67] also investigated P_b centers and obtained very similar results. It is noted that the HCD spectra after weak HCS presented in this thesis fit very well to the P_b center spectra. Only after more severe stress conditions, an increase of the peak in the upper half of the band gap is observed. In any case, the energetic positions of the peaks never deviate significantly from what is usually observed for P_b centers.

CHAPTER 5

Investigation of Trench Devices

Chapter Contents

> *It seems that perfection is attained not when there is nothing more to add, but when there is nothing more to remove.*
>
> — Antoine de Saint Exupéry

Modern power MOSFET technologies have seen an evolution to extremely high levels of performance. Advancements in manufacturing have led to densely packed trench concepts minimizing necessary wafer real-estate driving down production costs (cf. Section 1.1). Further improvements of the technologies are only possible using sophisticated designs like compensated trench devices as presented in Section 1.1.3. Feasible shrinking of the geometries at this point is limited as they are designed near electrical and thermal boundaries for their rated data sheet specifications. Thus, in order to further increase performance and robustness, it is crucial to understand the physics of degradation well

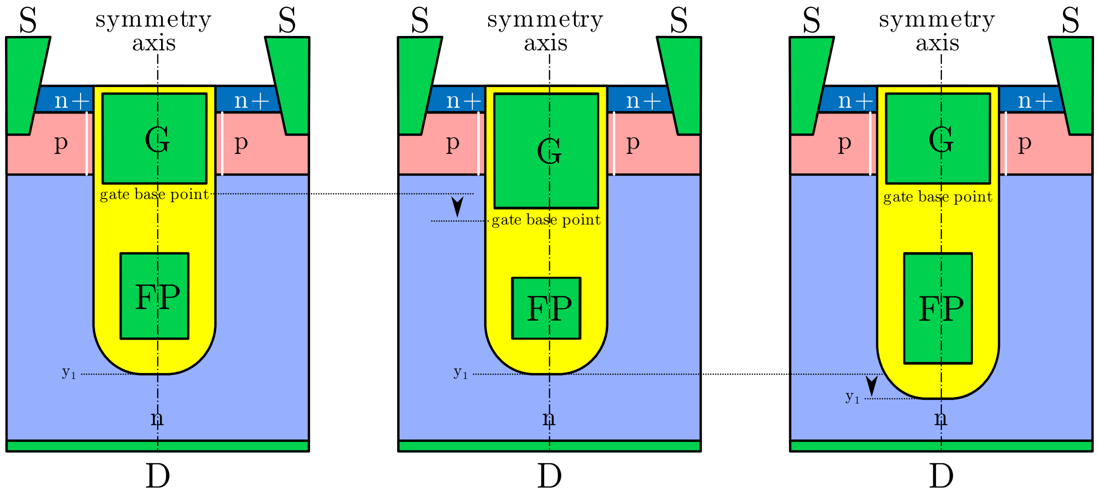

Fig. 5.1. Geometrical process splits of the compensated trench MOSFET. The left structure acts as the reference structure. In the middle figure, the shift of the gate base point is depicted while the right shows the variation of the trench depth. The function of the FP is explained in Section 1.1.3.

in these devices. So far, there is little knowledge about the impact of HCD on trench devices, especially compensated technologies. The intention of this chapter, which is based on [70], [71], is to shed more light on the poorly understood behavior of HCD in these compensated trench MOSFETs.

5.1. Process Splits

A thorough investigation of HCD in complex structures like the compensated trench device (Figure 1.4) requires a variation of the geometry as it has a major impact on the field and carrier distributions of the devices. For this, certain parameters of production processes of an existing technology are varied during fabrication of the devices. This is referred to as a process split. The biggest impact for the FP compensated trench MOSFETs is expected for two splits in particular which are depicted in Figure 5.1: The variation of the gate base point (Figure 5.1 middle) lowers the bottom point of the gate electrode which then increases in size. Thus, more Si-SiO$_2$ interface area in the n-doped drain drift region is exposed to the gate potential during stress. Furthermore, the size of the FP decreases because the thickness of the oxide between gate and FP has to remain constant due to fabrication process constraints. The second process split is the trench depth variation (Figure 5.1 right) where the trench is deeper than in the reference structure. As a consequence the FP increases in size while the geometry of the gate electrode is not influenced. This leads to a variety of a total of four process splits, as shown in Table 5.1, which are investigated in more detail.

Table 5.1. Explanation and nomenclature of the four process splits of the compensated trench device.

Name of split	Description
P1	standard structure
P2	deeper gate base point
P3	deeper trench
P4	combination of P2 and P3

5.1.1. TCAD Investigation of Trench Devices

The correct modeling of the physics of the investigated trench structures is crucial for the accurate interpretation of experimental data. The quality of the simulation of electrical behavior of devices depends strongly on the availability of device models which represent the geometry and doping profiles of real structures acceptably well. To achieve this, process simulations of all process splits are performed before the electrical simulations. Generally, it is sufficient to perform two-dimensional simulations to emulate the electrical behavior of trench devices. Although there are certainly edge effects at the trench terminations (Figure 1.8), they can be neglected in most cases. Electrical simulations are performed using Sentaurus SDevice by Synopsys Inc. [72].

5.2. Charge Pumping of Trench Devices

CP is not limited to planar devices but can also be adapted for any MOS structure where holes and electrons of a p- and n-doped region, respectively, are accessible separately. These contacts are grounded in the CP experiment and the CP current is measured on them [30]. It was shown that the CP experiment can also be performed on trench MOSFETs [73], [74]. For the technology depicted in Figure 1.4 the CP pulse can be applied on the FP electrode while the combined source/body contact acts as a reservoir for holes and the drain contact supplies electrons. In this configuration, it is possible to investigate a large fraction of the trench, mainly the lower part. The upper accessible region is thoroughly discussed in Section 5.3.2. Many findings of this section are based on [70].

Applying CP on the gate on the other hand allows for the investigation of the gate oxide in the body region of the device. Again, the drain region supplies the electrons. Unfortunately, there are possible issues: Since the source contact shorts the body and source doping regions by design, there is the possibility of carrier annihilation of CP carriers in the p-doped region due to the presence of the n-doped source region. Furthermore, when the CP pulse transitions to positive voltage, the inversion channel between source and drain is opened. Due the low resistance between drain and source, any noise between drain and source will superimpose the very low CP currents. As mentioned earlier, in a CP experiment contacts of the p- and n-doped areas have to be contacted and grounded separately. Since ground potentials may vary slightly within a measurement system, equalizing currents between the contacts will flow and distort the CP experiment during the inversion phase of the CP pulse where the channel is open. If it is necessary to apply

CP on the gate, the source implantation has to be omitted during fabrication or a separate body contact is needed [75]. In any case, a contact, where holes are supplied has to be established.

5.2.1. Impact of Device Edges

The complex design of a trench device, where terminating and transverse trenches are needed (cf. Section 1.1.3 and Figure 1.8), raises the question if these edge trenches have different defect densities than the active area which is of major interest for the investigation of degradation. It is possible that the edges of a trench device behave differently from the active area since their trenches are wider than the trenches in the active area. This is investigated using three devices with differing areas and aspect ratios of process variation P1. It is noted that all devices investigated in this subsection are unstressed. Thus, all defects have already been present after fabrication.

For this CP investigation, the CP pulse is applied to the FP electrode and not to the gate electrode. This is due to the larger area which can be scanned by the FP during CP. Also, the issues described in Section 5.2 do not have to be considered when using the FP. Furthermore, as will be shown in Section 5.3.2, the FP can be utilized for spatial profiling of defects after HCS.

In the following, the frequency dependent border traps and total trap concentrations $N_\mathrm{tot} = N_\mathrm{bt} + N_\mathrm{it}$ of the geometric variations of the trench devices are investigated with frequency dependent CP. The voltage dependent components of the border traps (cf. Section 4.3.1) are included in the total trap concentrations as the pulse amplitude during the experiments is chosen sufficiently high.

Since all geometric variations are of the same technology and fabricated on the same wafer, it is expected that they show similar trap densities at all frequencies if the impact of the edge of the device was negligible. It is shown in Figure 5.2 that this is clearly not the case: The smaller the device, the bigger the trap densities. Thus, a major impact of traps on the edges of the devices causes an increase of the overall trap densities in small devices. Since the slopes of the frequency dependent CP also increase with decreasing device sizes, it can be concluded that the device edges are affected by slower traps than the active area. In order to quantify the impact of the edges on the overall trap densities, the frequency dependent trap densities are fit to a logarithmic model

$$N_\mathrm{CP}(f^\mathrm{CP}) = N_\mathrm{tot} - N_\mathrm{bt} \log\left(f^\mathrm{CP}/1\,\mathrm{Hz}\right). \tag{5.1}$$

This logarithmic approximation is introduced because border traps are known to have a large variance of time constants [76]. Therefore, these time constants can be assumed uniformly distributed over the small investigated frequency range of the data presented in Figure 5.2. Generally, the probability that a border trap contributes to the trap density N_CP measured by CP, is exponentially dependent on its respective time constant. As demonstrated by Lagger et al. [77], the sum of a large number of such exponentially dependent contributions to a signal can be approximated very well by a logarithm. The values for N_tot and N_bt extracted from the measurement data depicted in Figure 5.2 is shown in Figure 5.3.

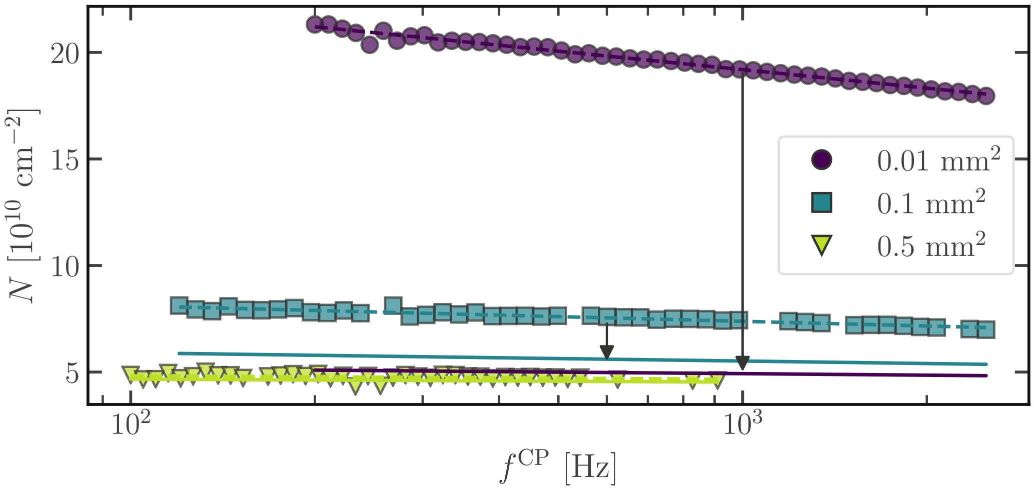

Fig. 5.2. Frequency dependent CP of trench devices as depicted in Figure 1.4 (process variation P1). The areas in the legend refer to the total die areas of the devices while the dashed lines with markers represent the original CP data (including edge contributions) while the solid lines represent the calculated active area contributions (Equation (5.3)).

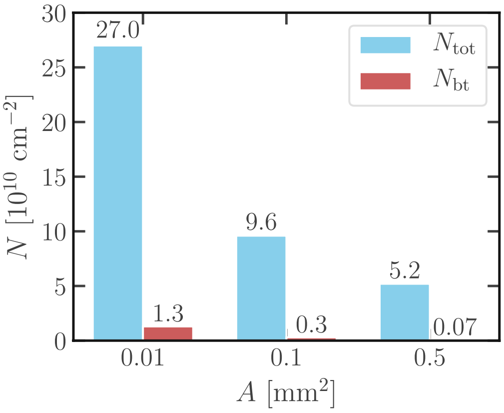

Fig. 5.3. Fit parameter of experimental data (Figure 5.2) fit to Equation (5.1) for the three investigated geometrical variations of the device.

The validity of this model can easily be checked by normalizing the data from Figure 5.2 to an arbitrary frequency f_0^{CP}

$$N_{norm} = \frac{N_{CP}(f^{CP}) - N_{tot}}{N_{CP}(f_0^{CP}) - N_{tot}} = \frac{\log(f^{CP})}{\log(f_0^{CP})}. \tag{5.2}$$

As shown in Figure 5.4, the CP data from Figure 5.2 follows the trend predicted in Equation (5.2) very well. The noise increases with increasing device areas since bigger

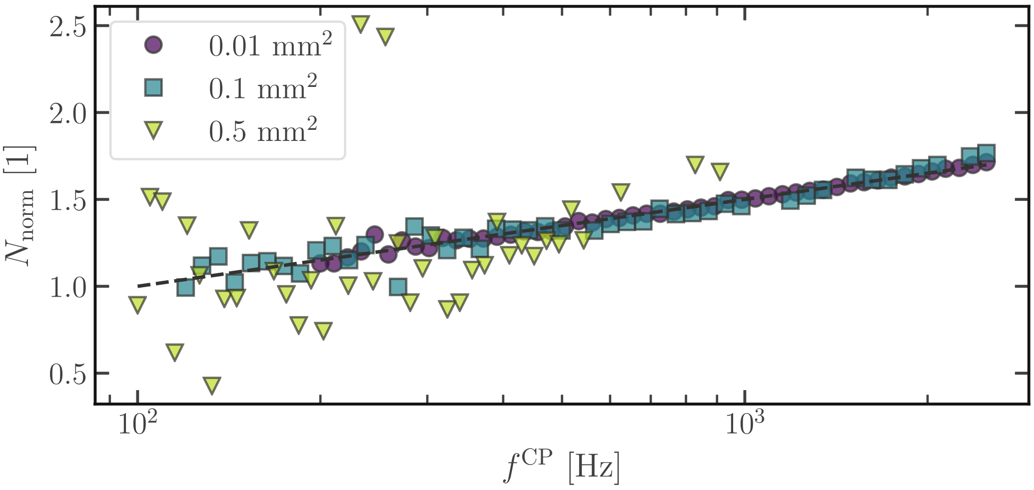

Fig. 5.4. Normalization of the CP data from Figure 5.2 according to Equation (5.2). The black dashed line represents $\log(f^{\text{CP}})/\log(f_0^{\text{CP}})$ with f_0^{CP}=100 Hz.

devices have less border traps. Thus, both the numerator $N_{\text{CP}}(f^{\text{CP}}) - N_{\text{tot}}$ and dominator $N_{\text{CP}}(f_0^{\text{CP}}) - N_{\text{tot}}$ in Equation (5.2) are smaller for devices with less border traps causing an amplification of noise.

In order to separate the edge and active area contributions for the total and border trap concentration, a model for the geometrical influence is proposed. In the following, the lengths of the transverse and termination trench in Figure 1.8 is referred to as L_{trans} and W_{term}, respectively.

$$N_{\text{tot}} = N_{\text{tot}}^{\text{act}} + \underbrace{C_{\text{tot}}^{\text{edge}} \frac{W_{\text{term}}/L_{\text{trans}}}{A_{\text{die}}}}_{N_{\text{tot}}^{\text{edge}}} \tag{5.3a}$$

$$N_{\text{bt}} = N_{\text{bt}}^{\text{act}} + \underbrace{C_{\text{bt}}^{\text{edge}} \frac{W_{\text{term}}/L_{\text{trans}}}{A_{\text{die}}}}_{N_{\text{bt}}^{\text{edge}}} \tag{5.3b}$$

This model is based on the following assumptions: Contributions of the active area to the total and border trap concentration must be independent of any geometrical properties of the device. Therefore, they are simply added as a constant factor. Secondly, the total amount of traps and the amount of border traps have the same geometrical dependencies. Furthermore, the number of traps on the edges scales with the inverse of the die area as bigger devices have relatively less edge area. Lastly, the aspect ratio is considered: The termination trench (cf. Figure 1.8) plays a more dominant role than the transverse trench. Devices with a longer termination trenches show more traps in CP. Therefore, the aspect ratio is considered with a $W_{\text{term}}/L_{\text{trans}}$ factor in Equation (5.3). Using Equation (5.3) to fit the total trap and border trap concentrations extracted from the experimental data by Equation (5.1) reveals that the model is in good agreement with the experiment. This is

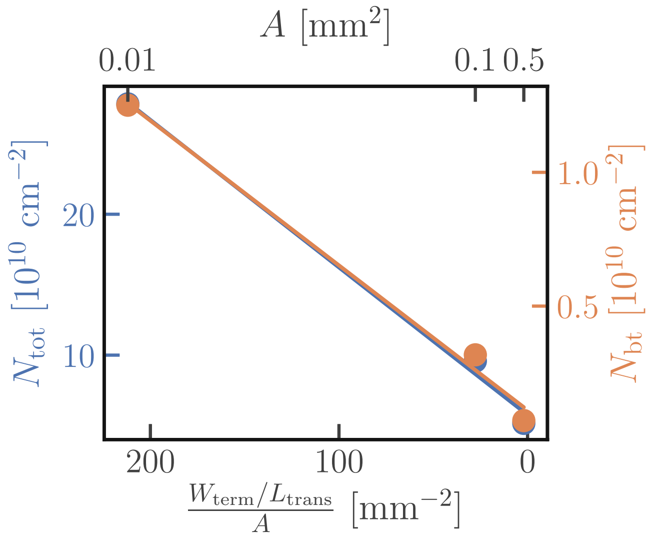

Fig. 5.5. Fit of total trap densities and border trap densities extracted from Equation (5.1) using the data presented in Figure 5.2 to Equation (5.3).

Table 5.2. Values of border and total trap contributions for edges and active area according to Equation (5.3) along with the geometrical parameters of the devices.

A_die [mm^2]	$W_\mathrm{term}/L_\mathrm{trans}$ [1]	$N_\mathrm{tot}^\mathrm{act}$ [10^{10}cm^{-2}]	$N_\mathrm{bt}^\mathrm{act}$ [10^{10}cm^{-2}]	$N_\mathrm{tot}^\mathrm{edge}$ [10^{10}cm^{-2}]	$N_\mathrm{bt}^\mathrm{edge}$ [10^{10}cm^{-2}]
0.01	2.12	5.8	0.1	22.2	1.1
0.1	2.77	5.8	0.1	2.9	0.1
0.5	1.00	5.8	0.1	0.2	0.01

shown in Figure 5.5, where an interesting detail about the data becomes apparent: The total number of traps on the devices' edges scale with the edge border traps by a factor of approximately 20. Thus, the ratio of border and interface traps on the device edges is constant for all sizes which suggests that the scaling of the structures has no impact on the border trap generation during fabrication on the device edges. This is also reflected in the resulting values for the fit parameters, which are presented in Table 5.2. Surprisingly, the active device area does not seem to be as affected by border traps as the edges of the structures, where the total trap density is 60 times higher than the border trap density.

For easier comparison of the contributions of the edges to both the total and border trap densities, Figure 5.6 depicts those relative components. As for the smallest structure, the impact of the edge is massive while the total contribution of the edge shrinks to only 4% for the device with a die area of 0.5 mm^2. Although even for this biggest structure the border trap contribution is 15%, the overall contribution of the edge is only at 4%. Thus, the edge of trench devices may distort results of other experiments and should therefore always be investigated in the first place.

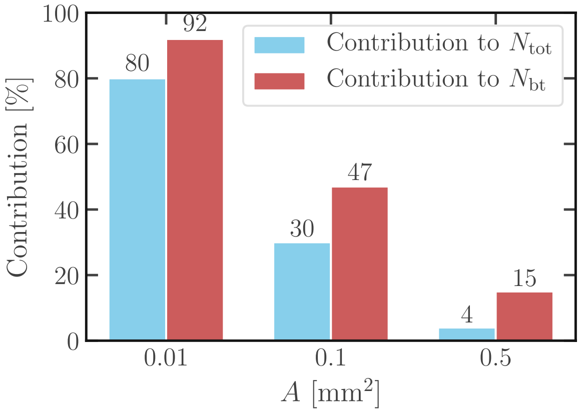

Fig. 5.6. Contributions of the edges to the total amounts of traps and to the overall border trap concentration, i.e. $N_{\mathrm{tot}}^{\mathrm{edge}}/N_{\mathrm{tot}}$ and $N_{\mathrm{bt}}^{\mathrm{edge}}/N_{\mathrm{bt}}$.

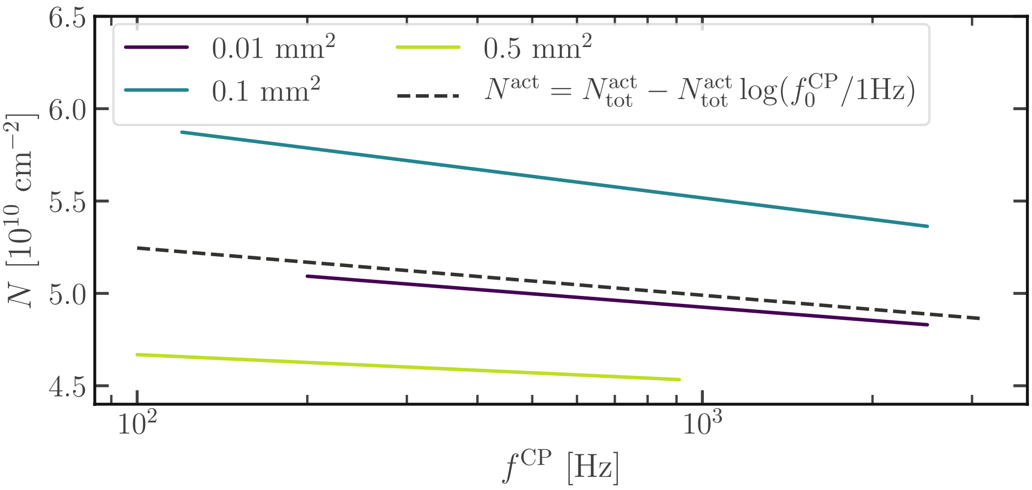

Fig. 5.7. Active area contribution of traps calculated from Equation (5.4) using the data depicted in Figure 5.2 along with the direct calculation with Equation (5.5)

The actual contribution of the active area, which is of most interest for the investigation of degradation in trench devices after electrical stress, can be calculated from the aforementioned parameters. This is achieved by subtracting $N_{\mathrm{tot}}^{\mathrm{edge}}$ and $N_{\mathrm{bt}}^{\mathrm{edge}}$ from Equation (5.3) from the measurement data.

$$N^{\mathrm{act}} = (N_{\mathrm{tot}} - N_{\mathrm{tot}}^{\mathrm{edge}}) - (N_{\mathrm{bt}} - N_{\mathrm{bt}}^{\mathrm{edge}}) \log\left(f^{\mathrm{CP}}/1\,\mathrm{Hz}\right) \tag{5.4}$$

Alternatively, instead of using the measurement data, $N_{\mathrm{tot}}^{\mathrm{act}}$ and $N_{\mathrm{bt}}^{\mathrm{act}}$ can be used directly.

$$N^{\mathrm{act}} = N_{\mathrm{tot}}^{\mathrm{act}} - N_{\mathrm{bt}}^{\mathrm{act}} \log\left(f^{\mathrm{CP}}/1\,\mathrm{Hz}\right) \tag{5.5}$$

In Figure 5.2, the reduction of the total trap densities to the active area trap densities using Equation (5.4) is shown by solid lines. Both variants of active area contribution estimations (Equations (5.4) and (5.5)) are depicted in Figure 5.7 which shows that both approaches yield similar results.

5.2.2. Other Plausible Models for Edge Trap Density Contribution

Generally, other models are plausible candidates for the modeling of the contribution of device edges to the total and border trap density. The two most obvious models are presented in the following.

One of the simplest possible assumption is that both the transverse and termination trench have equal influence on the edge contribution, i.e. either edge trench has the same trap density for both border and interface traps. In this case, the aspect ratio would not be a contributing factor in the model. Thus, the edge contributions would only depend on the inverse of the die area.

$$N_{\mathrm{tot}} = N_{\mathrm{tot}}^{\mathrm{act}} + \underbrace{C_{\mathrm{tot}}^{\mathrm{edge}} \frac{1}{A_{\mathrm{die}}}}_{N_{\mathrm{tot}}^{\mathrm{edge}}} \tag{5.6a}$$

$$N_{\mathrm{bt}} = N_{\mathrm{bt}}^{\mathrm{act}} + \underbrace{C_{\mathrm{bt}}^{\mathrm{edge}} \frac{1}{A_{\mathrm{die}}}}_{N_{\mathrm{bt}}^{\mathrm{edge}}} \tag{5.6b}$$

Of course, the termination trenches could be prone to more defects than the transverse trenches, unlike the opposite situation described in Equation (5.3). In this case, their reciprocal length ratios are considered in the model, i.e. $L_{\mathrm{trans}}/W_{\mathrm{term}}$ instead of $W_{\mathrm{term}}/L_{\mathrm{trans}}$.

$$N_{\mathrm{tot}} = N_{\mathrm{tot}}^{\mathrm{act}} + \underbrace{C_{\mathrm{tot}}^{\mathrm{edge}} \frac{L_{\mathrm{trans}}/W_{\mathrm{term}}}{A_{\mathrm{die}}}}_{N_{\mathrm{tot}}^{\mathrm{edge}}} \tag{5.7a}$$

$$N_{\mathrm{bt}} = N_{\mathrm{bt}}^{\mathrm{act}} + \underbrace{C_{\mathrm{bt}}^{\mathrm{edge}} \frac{L_{\mathrm{trans}}/W_{\mathrm{term}}}{A_{\mathrm{die}}}}_{N_{\mathrm{bt}}^{\mathrm{edge}}} \tag{5.7b}$$

The two models can easily be tested on the existing data of the three differently sized structures. As shown in Figure 5.8, the simple model which does not consider the aspect ratio (Equation (5.6)) does not successfully reduce the measured trap densities to similar values. This is neither the case for the model where the termination trench is assumed to be more defect-prone than the transverse trench (Equation (5.7)).

This is also reflected in the fits to the models depicted in Figure 5.9 compared to Figure 5.5. Therefore it can be ruled out that the models (5.6) and (5.7) reflect the trap distributions between edge and active area of the devices for the investigated technologies well. As suggested by Equation (5.3), the termination trench has higher defect densities.

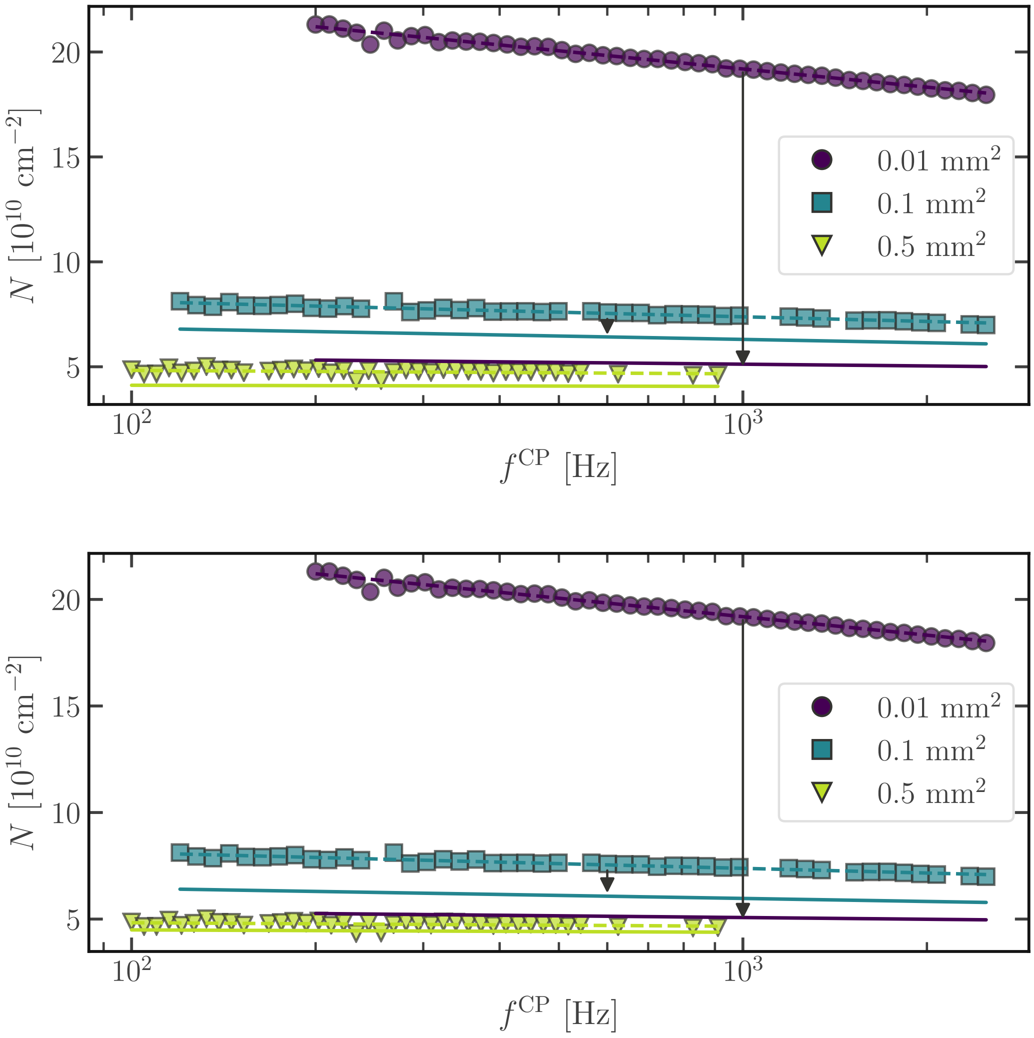

Fig. 5.8. Data from Figure 5.2. The solid lines represent the calculated active area contributions according to Equation (5.6) (top) and Equation (5.7) (bottom).

5.3. Spatial Profiling of Defects by Charge Pumping

Due to the sophisticated geometries of trench devices, localizing defects is a complex task which can in turn yield valuable insights for technology development. As complex electric fields, compared to lateral devices, are present in these structures the prediction of degradation of any kind, not just HCD, is not straight forward. Knowledge about the positions of defects not only allows for estimating any eventual impact of the degradation on device operation but can also help improving future technologies. This can be achieved by benchmarking different process variations of the same technology and selecting the optimal process settings. In this section, two methods are presented. While they are presented and discussed in the context of trench MOSFETs, they can in principal be adapted to other technologies as well.

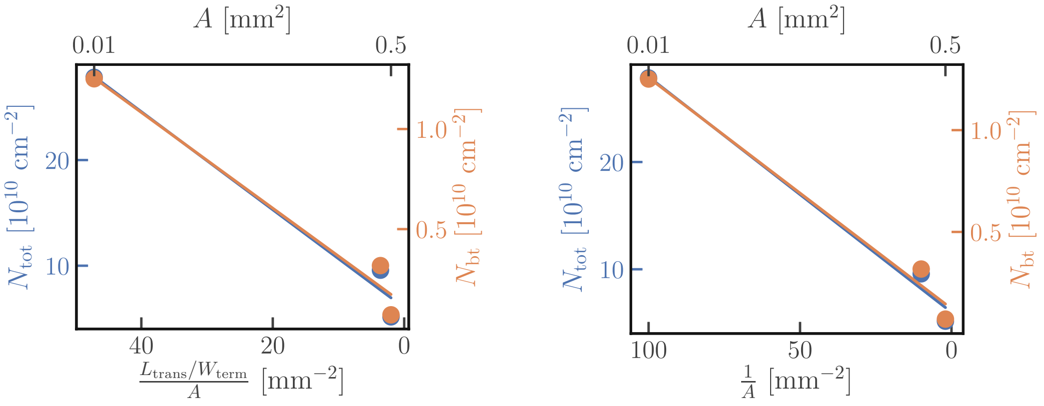

Fig. 5.9. Fit of total trap densities and border trap densities extracted from Equation (5.1) using the data presented in Figure 5.2 to Equation (5.6) (left) and Equation (5.7) (right).

5.3.1. Spatial Profiling by Doping Variation

The first presented spatial profiling CP method makes use of differently doped semiconductor areas within a device. After stress, it is possible to detect which interface areas degraded based on the type of doping of the semiconductor bordering the interface.

In order to demonstrate this method by means of a case study, trench MOSFETs without a compensating FP are fabricated. As mentioned in Section 5.2, devices without source implantation are required to investigate the p-doped body region. A cross section of these special structure is shown in Figure 5.10. The additional characterization of the defects in the n-doped drain region is performed simultaneously in one CP measurement. This is based on the following consideration: The increase of the CP current during the constant high level and constant base level measurements, where pulse base and high levels are swept, respectively, (cf. Section 1.3.3) causes a peak in the derivative of the CP current with respect to the base and high levels. These peaks are called *doping-induced peaks* and are observed when the semiconductor under a MOS structure reaches the important condition of CP which states that the pulse base and high levels have to cause accumulation and inversion in the semiconductor, respectively (or vice versa, depending on the doping type). If differently doped regions are present under a MOS structure, this condition is fulfilled successively during a constant base level or constant high level measurement as the pulse amplitude rises, thereby resulting in the observation of multiple doping-induced peaks – one for each distinct doping region. This requires that each doping region is supplied by both carrier types and that the flat-band and threshold voltages of the regions are sufficiently different from each other such that the peaks do not overlap.

In order to quantify the impact of the different doping areas, basic CP theory has to be revisited [33]. Generally, the number of traps involved in a CP experiment $N_{\mathrm{CP}}A_{\mathrm{eff}}^{\mathrm{CP}} =$

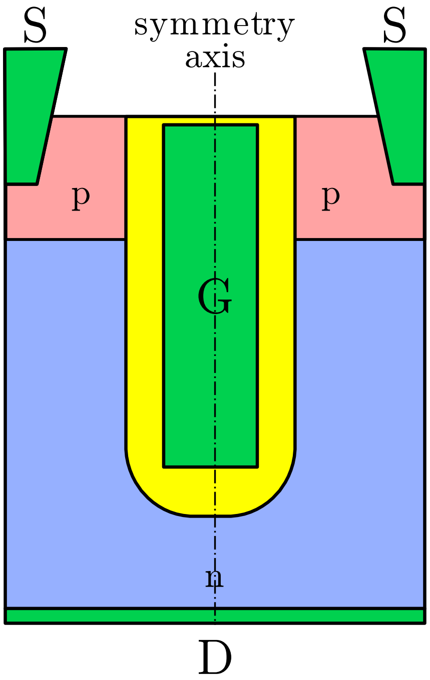

Fig. 5.10. Schematic cross section of a simple trench MOSFET without compensating FP and without source implantation for CP.

$I_{\mathrm{CP}}/qf^{\mathrm{CP}}$ can be written as

$$\frac{I_{\mathrm{CP}}(V_{\mathrm{base}}, V_{\mathrm{high}})}{qf^{\mathrm{CP}}} = W_{\mathrm{term}} \int_0^{L_{\mathrm{eff}}(V_{\mathrm{base}}, V_{\mathrm{high}})} n_{\mathrm{CP}}(y)\,\mathrm{d}y. \tag{5.8}$$

The effective length of CP, L_{eff}, should not be confused with the length of the transverse trench L_{trans}. The former refers to one side of the effective CP area, $A_{\mathrm{eff}}^{\mathrm{CP}} = L_{\mathrm{eff}} W_{\mathrm{term}}$, and increases rapidly with the amplitude of the CP pulse when full inversion or full accumulation of the semiconductor at the oxide interface are reached. When I_{CP} is differentiated with respect to V_{base} or V_{high}, two kinds of peaks can be identified [33].

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{base}}} = qf^{\mathrm{CP}} n_{\mathrm{CP}}(L_{\mathrm{eff}}) W_{\mathrm{term}} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{base}}} \tag{5.9a}$$

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{high}}} = qf^{\mathrm{CP}} n_{\mathrm{CP}}(L_{\mathrm{eff}}) W_{\mathrm{term}} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{high}}} \tag{5.9b}$$

As evident from Equation (5.9), on the one hand, strongly localized degradation anywhere on the scan-able semiconductor-oxide interface will cause a peak in the CP current derivative. This is because $n_{\mathrm{CP}}(L_{\mathrm{eff}})$ will also increase as soon as the base or high level of the CP pulse reaches a level which causes L_{eff} to extend to the the position of high degradation. The resulting peak is referred to as *degradation-induced peak*. It will be discussed in more detail in Section 5.3.2. As already mentioned before, the *doping-induced peak* is observed when the effective length of CP increases rapidly, as hinted by the factor $\mathrm{d}L_{\mathrm{eff}}/\mathrm{d}V_{\mathrm{high}}$ in Equation (5.9). Such a doping-induced peak is observed for every doping region.

Since the effective CP length is dependent on the base and high level of the CP pulse and therefore distinct doping-induced peaks appear, localized profiling of defect densities on the semiconductor-oxide interface adjacent to the respective doping regions is possible. This is achieved by integration over the respective doping-induced peak corresponding to the doping region under investigation.

$$\int_{V_1}^{V_2} \frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{base}}}\,\mathrm{d}V_{\mathrm{base}} = qf^{\mathrm{CP}}\overline{N}_{\mathrm{dop}}W_{\mathrm{term}} \int_{V_1}^{V_2} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{base}}}\,\mathrm{d}V_{\mathrm{base}} \tag{5.10a}$$

$$\int_{V_1}^{V_2} \frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{high}}}\,\mathrm{d}V_{\mathrm{high}} = qf^{\mathrm{CP}}\overline{N}_{\mathrm{dop}}W_{\mathrm{term}} \int_{V_1}^{V_2} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{high}}}\,\mathrm{d}V_{\mathrm{high}} \tag{5.10b}$$

This assumes that $n_{\mathrm{CP}}(L_{\mathrm{eff}})$ is constant in the respective doping region which is spatially delimited by $L_{\mathrm{eff}}(V_1)$ and $L_{\mathrm{eff}}(V_2)$. Therefore $n_{\mathrm{CP}}(L_{\mathrm{eff}})$ is replaced by the average trap density of the oxide adjacent to the respective doping region $\overline{N}_{\mathrm{dop}}$. In a final step, the area of the interface adjacent to the respective doping region can be associated by

$$A_{\mathrm{dop}} = W_{\mathrm{term}} \int_{V_1}^{V_2} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{base}}}\,\mathrm{d}V_{\mathrm{base}} \tag{5.11a}$$

$$A_{\mathrm{dop}} = W_{\mathrm{term}} \int_{V_1}^{V_2} \frac{\mathrm{d}L_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{high}}}\,\mathrm{d}V_{\mathrm{high}}. \tag{5.11b}$$

$\overline{N}_{\mathrm{dop}}$ can now be evaluated using Equation (5.10) and Equation (5.11):

$$\overline{N}_{\mathrm{dop}} = \frac{I_{\mathrm{CP}}(V_2) - I_{\mathrm{CP}}(V_1)}{qf^{\mathrm{CP}}A_{\mathrm{dop}}} \tag{5.12}$$

The result is intuitive: The change of the CP current between the integration boundaries is proportional to the trap density in the investigated region. It is noted that these bounds of integration (V_1 and V_2) used in Equations (5.10) and (5.11) are generally different for the constant base level and constant high level CP methods as the investigated doping-induced peak stems from reaching accumulation in one case and from reaching inversion in the other case. Whether reaching accumulation or inversion is associated with constant high level or constant low CP depends on the doping type of the investigated region.

For the case study demonstrating this method, trench MOSFETs without FP compensation and without source implantation (Figure 5.10 right) are stressed similarly as in a HCS: For 14 h, a gate voltage of 6.8 V and a drain voltage of 20 V was applied. The CP measurements of the virgin and stressed device are presented in Figures 5.11 and 5.12. Before the data can be analyzed quantitatively, the doping-induced peaks have to be identified correctly.

In the constant base level CP measurement, depicted in Figure 5.11, the high level is swept. Thus, a peak in the derivative of the CP current is expected at the threshold voltage of the p-doped region (body). Furthermore, this peak must be located at a positive high level voltage. Therefore, the right doping-induced peak is associated with the body region. This means that the remaining left doping-induced peak can only stem from the drain region and corresponds to its flat-band voltage. An analogous argument can be made for the constant high level CP measurement: Since the base level of the CP pulse

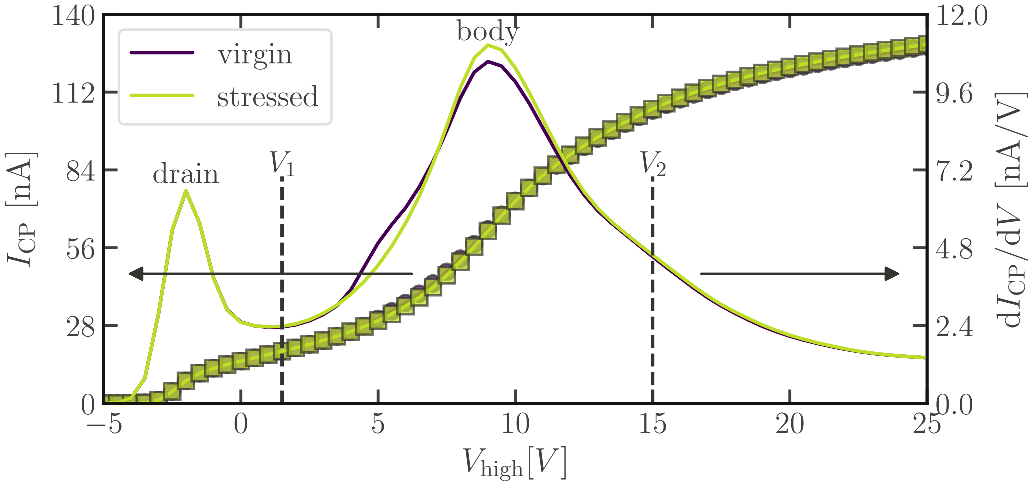

Fig. 5.11. Constant base level CP signal at a pulse base level of −6 V at a CP frequency of 100 kHz and transition slopes of $12.5\,\mathrm{V\,\mu s^{-1}}$ before and after a HCS on a trench MOSFET without compensating FP and without source implantation as depicted in Figure 5.10 right. HCS was applied for 14 h at a gate voltage of 6.8 V and a drain voltage of 20 V. The derivative of the CP current is plotted on the right axis in solid lines without markers. Upper and lower integration limits for the evaluation of the body doping-induced peak (Equation (5.12)) are marked with V_1 and V_2.

is swept while the high level kept constant, a peak in the derivative of the CP current is expected at the threshold voltage of the n-doped region (drain). Furthermore, this peak must be located at the negative base level voltage. Thus, the right doping-induced peak is associated with the flat-band voltage of the drain region and the left doping-induced peak can only stem from the body region.

After the stress, only the body doping-induced peak changes, as can be observed in both constant base level and constant high level CP (Figures 5.11 and 5.12). This implies that the stress only degraded the interface in the body region since the doping profiles cannot change due to stress. Also, no additional degradation-induced peak is observed suggesting that the degradation in the body region was uniform. By setting V_1 and V_2 around the body peak, the degradation in this region can be calculated. The selection of these voltages results from the following considerations: One integration border is set at the minimum between the drain and body peak while the second integration border is placed where no more change between virgin and stress measurement can be observed. More precise allocations of this voltages can be achieved by TCAD simulations if necessary. Using Equation (5.12) finally allows for the extraction of the degradation in the body region: For the constant base level method, a value of $3 \times 10^8\,\mathrm{cm^{-2}}$ and for the constant high level method, a value of $3.5 \times 10^8\,\mathrm{cm^{-2}}$ is found. Given the very low trap densities, the two values match remarkably well. This shows how sensitive CP measurements can be.

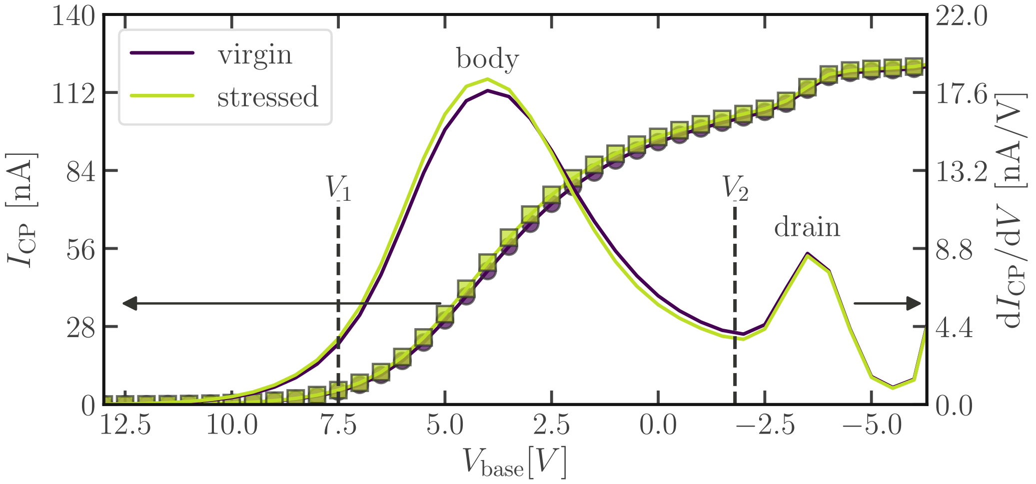

Fig. 5.12. Constant high level CP signal at a pulse high level of 20 V for the same conditions as in Figure 5.11.

In order to verify the drain doping-induced peaks of CP in the uncompensated device, constant base level and constant high level CP measurements are performed on a compensated device, where the CP pulse is applied to the FP. Both the uncompensated and compensated device are identical in geometry and doping profiles. The only difference is the absence of a FP in the trench of the uncompensated device. As expected, only one doping-induced peak is observed in the constant high level and constant base level measurements, depicted in Figures 5.13 and 5.14. As for the constant high level measurement (Figure 5.13), mainly the n-doped drain region adjacent to the FP is charge-pumped, therefore the doping-induced peak can be associated with the drain region and its threshold voltage is, as expected, negative. Remarkably, a second small doping-induced peak is observed in the constant high level CP measurement at approximately −7 V. It is caused by oxide thickness variations at the bottom of the trench where the oxide is slightly thicker for processing reasons. Due to a thicker oxide, higher amplitudes are needed to cause inversion at the interface. Thus, a second increase is observed. Also the peak in the constant high level measurement is not as wide as in the constant base level measurement. The FP, where the pulse is applied covers only the n-doped region of the device, therefore the hole-supplying p-doped body region is pinched off until sufficiently low voltages in the constant high level measurement are reached. At the point where a hole connection is established, holes are swept to the interface, thereby creating a much narrower peak. For the constant base measurement, the p-region is already able to constantly supply the holes for the CP mechanism. Therefore, accumulation stets in steadily, rendering the doping-induced peak wider. Also, the peak in this CP measurement has a fairly long tail. This is caused by activation of some fractions of the adjacent p-doped body region which can be fully inverted and accumulated in the vicinity of the junction. In case of the uncompensated trench, hole and electron supplies are always available. Therefore observed peaks are never extremely narrow and conceal the second small doping-induced

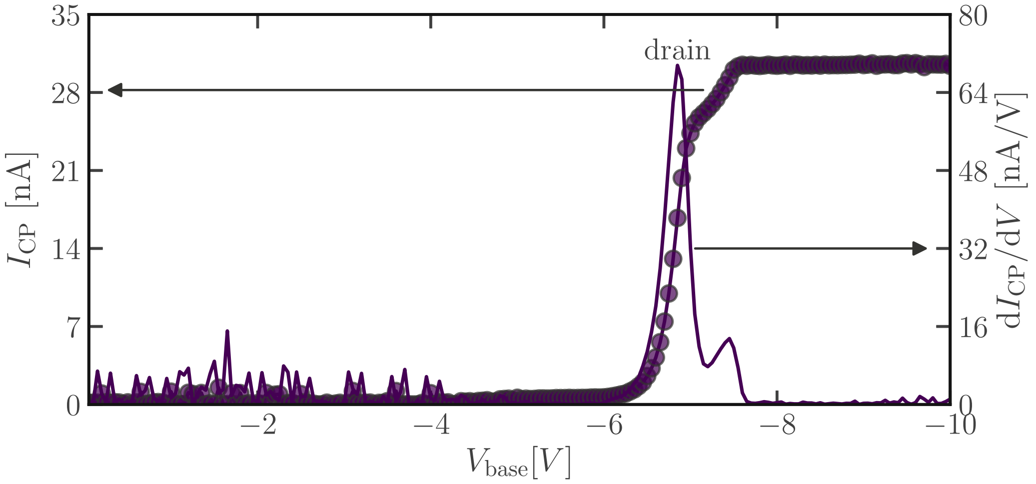

Fig. 5.13. Constant high level CP measurement on a FP compensated structure (Figure 1.4) with a high level of 15 V, a CP frequency of 500 Hz and transition slopes of 26.3 V ms^{-1}. A constant offset correction as described in Appendix A was performed. For the CP measurement, the FP electrode is used for applying the pulse while the gate is grounded. The derivative of the CP current is plotted on the right axis in a solid line without markers.

peak observed in the constant high level CP measurement of the compensated trench device.

5.3.2. Spatial Profiling by Reverse Drain Bias

The reverse bias CP method [33], [78] has been established for the localization of defects near the drain and source region in lateral devices. It is based on the idea that applying a reverse bias on a p-n junction deactivates the CP effect on the interface in the vicinity of the junction. This is because a space charge region (SCR) is introduced by the reverse bias. During the accumulation phase of the CP pulse, no full accumulation of the interface is possible within the SCR, hence violating the fundamental CP condition. Thus, by gradually increasing the junction reverse bias during the CP experiment, an increasing area of the interface can be selectively deactivated for the CP effect. The established reverse bias CP method generally relies on the presence of a degradation-induced peak (cf. Equation (5.9)) which is expected to disappear as soon as the SCR covers the interface area which is considerably degraded. In the interpretation of the results, a qualitative assertion is often made, namely whether the doping-induced peak after stress could be suppressed by the reverse bias. This only allows for an approximate localization of the defects, and this only when the increased degradation is present near the junction. For simple lateral structures, analytical solutions for the reverse bias dependence are available, allowing for more precise localization. Of course, for complex structures, no analytical

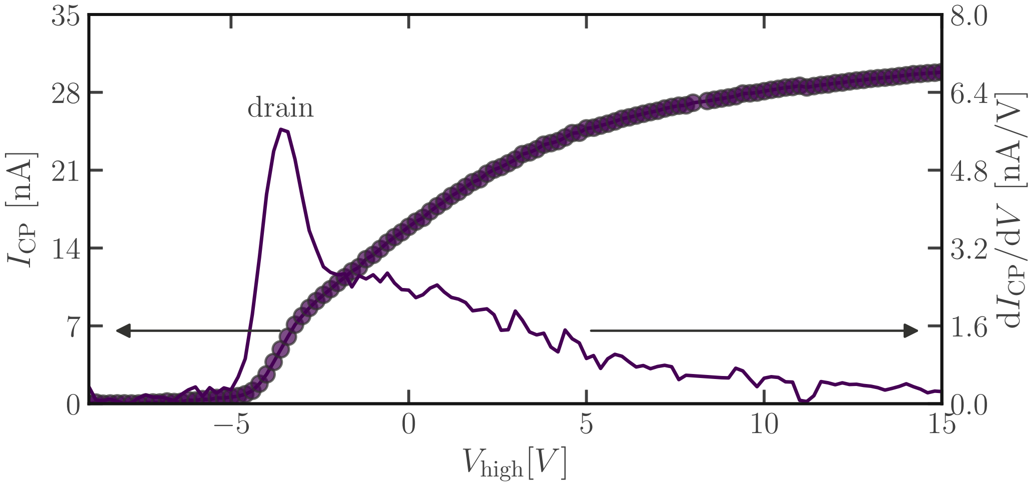

Fig. 5.14. Constant base level CP measurement on a FP compensated structure with a base level of -10 V for the same conditions as in Figure 5.13.

solutions exist. Also, a quantitative spatial profiling of the defect density is not possible with this method. Furthermore, the presence of a degradation-induced peak is crucial.

In this section, a more sophisticated extension of the reverse bias CP method is presented [71]. Supported by TCAD simulations, spatial profiling of the absolute values of the defect densities is possible, even without requiring the presence of a degradation-induced peak. Thus, virgin devices can also be investigated.

For the compensated trench device specifically, the borders of the SCR are shown for the four process variations for various drain voltages in Figure 5.15. They were calculated with the help of TCAD simulations. In this case, the drain voltage is used as a means of reverse bias. Thus, a SCR around the body-drain p-n junction is induced. Due to the higher body doping, compared to the drain doping, the borders of the SCR mainly change in the drain region, therefore only the SCR border in the drain region is shown. It is noted that different geometries, i.e. process splits, will have slightly different mappings of their SCR to the drain bias. In order to investigate the defects on the trench interface near the gate base point, the FP is used as the CP electrode. Using the FP instead of the gate reduces the aforementioned issues, like the mandatory omission of the source implantation, and also allows for the investigation of deeper areas of the trench interface. The calculation of the SCR in Figure 5.15 is performed at a FP bias which is equal to the high level of the CP pulse in the experiment since a positive FP bias causes accumulation at the interface. Of course, the FP bias in the simulation must always match the respective CP high level (or low level if doping types are switched) used in the experiment. For the compensated trench technologies, a high level of 20 V is used. Also, all drain bias steps of the experiment must be simulated separately to obtain the corresponding SCR positions. A maximum drain voltage of 4 V is applied at the body-drain diode during CP, as leakage currents between the body/source and the drain contact distort the CP signal at higher

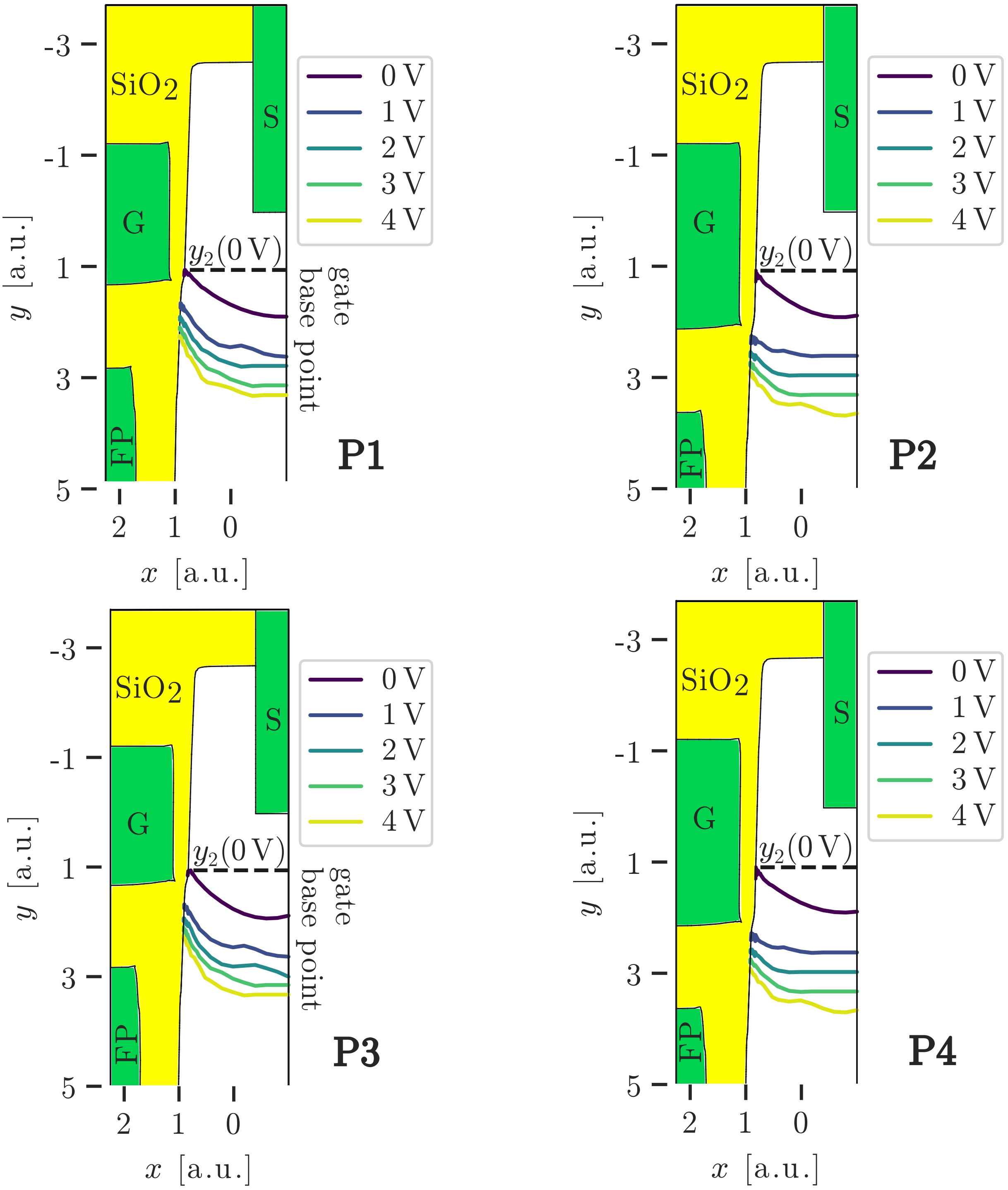

Fig. 5.15. TCAD simulation of the lower borders of the SCR at the body-drain junction for the four process variations (Table 5.1) at various drain biases. A FP bias of 20 V is applied in the simulation while gate and source are grounded. The legend refers to the drain biases.

reverse biases. As mentioned before, the CP current is measured at the source/body and the drain contact.

Regarding the mathematical framework, the definition of the amount of defects after CP $N_{\mathrm{CP}}A_{\mathrm{eff}}^{\mathrm{CP}} = I_{\mathrm{CP}}/qf^{\mathrm{CP}}$, analogously to Equation (5.8), is revisited.

$$\frac{I_{\mathrm{CP}}(V_{\mathrm{D}})}{qf^{\mathrm{CP}}} = W_{\mathrm{term}} \int_{z_1}^{z_2} \int_{y_1}^{y_2(V_{\mathrm{D}})} n_{\mathrm{CP}}(y)\,\mathrm{d}y\mathrm{d}z \tag{5.13}$$

Since the pulse base and high levels are not varied in the reverse bias CP method, the integration borders of the y-coordinate vary from the ones introduced in Section 5.3.1 in this derivation. When different reverse biases V_{D} are applied to a p-n junction, the effective length of CP of an MOS structure changes with the position of the SCR near the gate base point as shown in Figure 5.15. The y-position y_1, which is the lower integration boundary, is always at the trench bottom (shown in Figure 1.4) while the upper integration boundary, y_2, reflects the intersection of the interface of the trench and the SCR at the respective drain bias. Trap densities in the trench device cannot be dependent on the z-coordinate, which is the dimension along W_{term}, because it is a symmetry axis. Therefore, the integration over this z-coordinate is constant with a value of W_{term}. Thus, Equation (5.13) can be rewritten to

$$W_{\mathrm{term}} \int_{y_1}^{y_2(V_{\mathrm{D}})} n_{\mathrm{CP}}(y)\,\mathrm{d}y = \frac{I_{\mathrm{CP}}(V_{\mathrm{D}})}{qf^{\mathrm{CP}}}. \tag{5.14}$$

From this equation, the trap density can be extracted from the derivative with respect to y_2.

$$n_{\mathrm{CP}}(y_2) = \frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}y_2}\frac{1}{qf^{\mathrm{CP}}W_{\mathrm{term}}} \tag{5.15}$$

For a successful extraction of the trap densities, the SCR for each drain voltage step in the experiment has to be calculated in order to be able to map the positions y_2 to the respective reverse biases. The drain voltage dependent CP current $I_{\mathrm{CP}}(V_{\mathrm{D}})$ is thereby transformed into a spatially dependent CP current $I_{\mathrm{CP}}(y_2)$. Similarly to the transformations in SPCP, a numerical derivative $\mathrm{d}I_{\mathrm{CP}}/\mathrm{d}y_2$ of the data has to be obtained in Equation (5.15) which can for example be achieved by a Savitzky-Golay filter. Analogously to Equation (5.12), a mean trap density for spatial CP can be defined.

$$\overline{N}(y_2(V_{\mathrm{D}})) = \frac{I_{\mathrm{CP}}(V_{\mathrm{D}})}{qf^{\mathrm{CP}}W_{\mathrm{term}}(y_1 - y_2(V_{\mathrm{D}}))} \tag{5.16}$$

The quantity defined in Equation (5.16) describes the average trap density of the trench in the spatial interval $[y_1,y_2(V_{\mathrm{D}})]$ with an active CP area of

$$A_{\mathrm{eff}}^{\mathrm{CP}} = W_{\mathrm{term}}(y_1 - y_2(V_{\mathrm{D}})). \tag{5.17}$$

It is (incorrectly) assumed for this quantity that traps are uniformly distributed in the active CP area within this interval. Although the assumption is incorrect, this quantity can be used to quantify the uniform part of the total degradation in the device. In other words, after stress, a constant offset of this quantity for all position indicates that degradation has been uniform. Therefore, devices which generally have uniform trap densities will not show significant changes of this quantity over y_2.

Since the SCR induced by the reverse bias is also influenced by the FP voltage, the latter can theoretically also be used to modulate the position y_2. For the compensated trench device with a n-doped drain region, the constant base level CP signal first has to be examined thoroughly. The variation of the pulse high level on the FP will shift the active CP area by pushing the SCR in the accumulation phase of the CP pulse further towards the body region of the device. Thus, instead of a saturation of the constant base level method, a slight increase of the CP current would be expected. For an unstressed device where the trap densities within this change of active CP area can be assumed approximately constant, this change of CP current must scale with the simulated change of the active CP area (Equation (5.17)) due to the shift of the SCR. If this is not the case, voltage dependent border traps (cf. Section 4.3) are observed. Another obvious issue might be the oxide thickness and its associated breakdown voltage: If full inversion and accumulation of the semiconductor are only reached near the the oxide breakdown voltages, the possible extended range of y_2 is most likely very limited. Generally, in this more advanced method, the CP current and position y_2 are not only dependent on the reverse bias V_D but also the high level of the CP pulse on the FP.

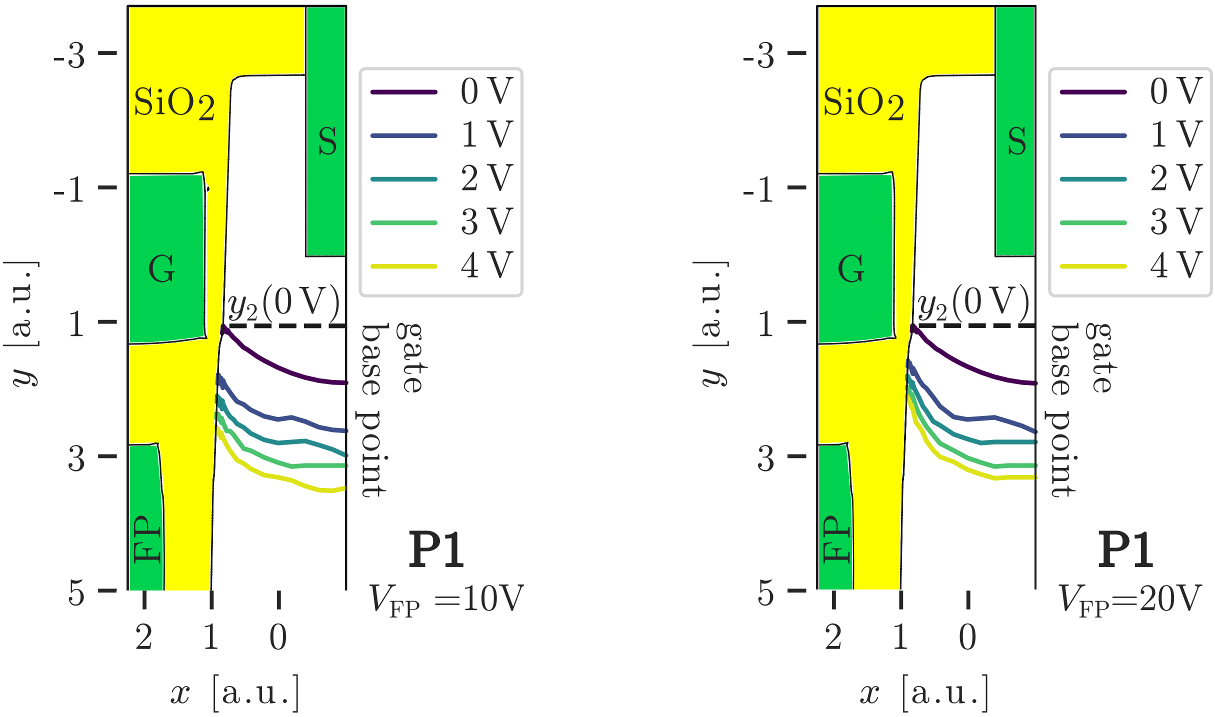

Fig. 5.16. TCAD simulation of the lower borders of the SCR at the body-drain junction as depicted in Figure 5.15. Only process variation P1 is shown, but for two different FP biases. A lower FP bias allows for an investigation of a larger area towards the trench bottom.

For the specific technology investigated in this chapter, the FP bias hardly influences the borders of the SCR for low reverse bias voltages as shown in Figure 5.16. Even when the FP bias is increased by 10 V, only negligible change of the SCR border is observed when no reverse bias is applied. When the reverse bias, i.e. the drain voltage is increased, the FP bias influence on the SCR positions becomes more dominant. Thus, this method may be applicable in principle for the investigated technology.

It is noted that the application of a pulsed instead of constant reverse bias is mentioned in literature [33] for the reverse bias CP method. This is based on a twofold idea: On the one hand, a reverse bias on a lateral structure will inevitably cause a drain-source current during the inversion phase of the CP pulse. This would render the measurement of the CP current complicated. Secondly, a change of the CP threshold voltage is observed. Both of these issues can be prevented by synchronizing the CP pulse to the reverse bias. In this case, the reverse bias is only applied during the accumulation phase of the CP pulse.

In the experimental setup described in this section, a constant instead of pulsed reverse bias is preferred. On the one hand, the two aforementioned issues are not bothersome for trench devices. Also, the FP cannot open a channel between drain and source at any voltage. Thus, the CP current is neither influenced during accumulation nor during the inversion phase. Furthermore, the shift of the threshold voltage does not matter when it is possible to set the CP base level to a bias where full inversion can be achieved for all reverse bias levels in the experiment. This is the case in all our investigations.

The spatial CP method presented in this section, which employs a reverse bias, is not applicable in the case presented in Section 5.3.1. For this method to work, it must be possible to cover the area under investigation with a SCR. Since the body area is much higher doped than the drain region of the junction, no meaningful changes of the SCR can be achieved in the body region. Another condition which has always been crucial for reverse bias CP was the presence of a degradation-induced peak after stress [33] which was not observed in the measurements discussed in Section 5.3.1. Such a degradation-induced peak is caused by strong localized degradation as discussed earlier. As shown earlier though, this condition becomes obsolete when the measurement is supported by TCAD simulations.

5.4. Hot-Carrier Degradation in Trench Devices

Investigations of HCD in compensated trench devices (Figure 1.4) are relatively sparse in literature. Existing papers [79], [80] tend to focus on the symptoms rather than the microscopic nature of HCD in these technologies. As such, a thorough investigation of the traps generated by HCS [71] has long been overdue. For all HCD experiments in this section, structures with an active area of 0.03 mm^2 have been chosen. Due to improved edges, edge trap contributions as described in Section 5.2.1, are not an issue in these devices. Since the investigated technology is optimized for low-voltage power applications, the bias conditions leading to HCD are fairly different from conventional lateral MOSFETs. For long-channel transistors, a drain bias to gate bias ratio of of 2:1 is generally regarded as worst-case condition for HCD [4]. This is an unrealistic configuration for power transistors.

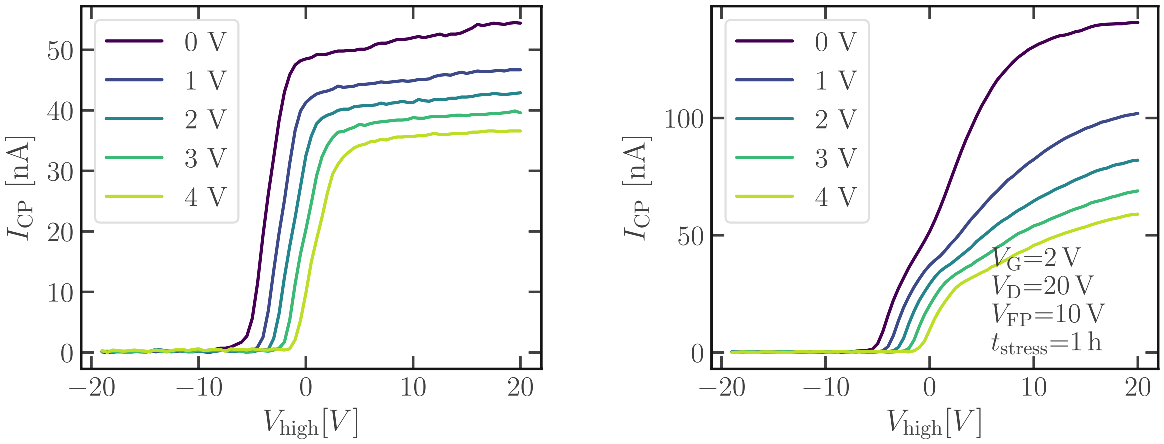

Fig. 5.17. Constant base level CP current of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

The following experiments are carried out at drain biases near the nominal breakdown voltage of 25 V. These drain voltages can only be sustained at gate voltages at which the channel resistance is sufficiently high. Therefore, for all experiments a gate bias of 2 V is chosen.

Although the FP bias is kept at the source bias (typically 0 V) during normal operation, HCD is investigated at higher FP biases in the following. This way, a less optimal design, in which more hot carriers and higher fields are present near the gate base point, can be emulated. Three distinctive FP biases have been chosen for a more detailed analysis: 10 V, 0 V and 5 V. While this order may seem odd at first, the configuration with the most degradation is investigated first. Subsequently, the bias condition representative for the on-state of the device during operation is investigated. Lastly, the transition between those two extremes is presented.

5.4.1. Field-plate Potential 10 V

An initial approach to study the impact of HCD on trench devices is to investigate the CP currents as presented in Figure 5.17 for process variation P1. Before thoroughly discussing the stress impact, the virgin CP current already provides a few very interesting insights on the behavior of the device itself. Initially, the CP current increases for all reverse biases approximately 2 % to 4 % between a FP pulse high level of 10 V and 20 V. The active CP area, on the other hand, rises only 0.6 % between those high levels at a drain voltage of 0 V while it increases by 9 % at 4 V. This indicates that the device either has a non-uniform trap density within the active CP areas which are accessed by the varying CP pulse high levels or that voltage dependent border traps as described in Section 4.3 are present. Either way, the advanced spatial profiling method which takes varying FP

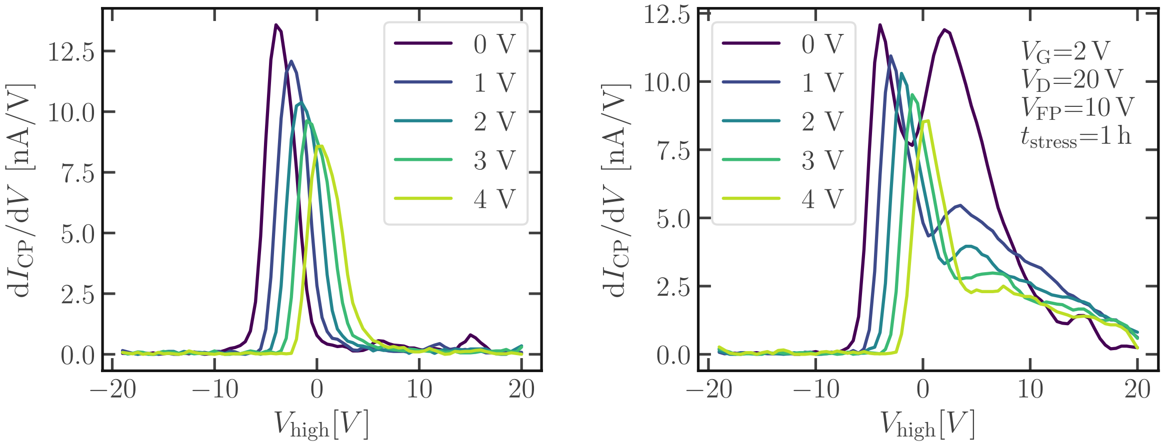

Fig. 5.18. Derivative of the constant base level CP current with respect to the high level voltage of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

accumulation levels, additionally to reverse biases, into account is not suitable for these devices. Whether the culprits are voltage dependent border traps or areas with increased degradation is addressed later.

The CP measurement after stress (Figure 5.17 right) clearly shows that the number of defects must have more than doubled. Without further analysis, very few definite conclusions can be drawn about the spatial distribution. Indeed, kinks around a CP pulse high level of 0 V are visible for reverse biases of 0 V and 1 V.

These kinks are transformed into degradation-induced peaks by calculating the numerical derivatives of the CP currents. These derivatives are plotted in Figure 5.18. It becomes apparent that, after stress, a major localized degradation was caused by the HCS. This can be concluded from the large new peak which is observed after stress at V_D=0 V. The peak fades away rather quickly as the drain bias during CP is increased. This clearly points to a degradation near the gate base point where the SCR can deactivate the CP mechanism locally. How much uniform degradation was added by the stress additionally cannot be concluded yet. Although a qualitative statement about localized degradation due to HCD is already possible at this point, the virgin data shows no sign of additional localized degradation.

In process variation P2, the virgin device, as well as the stressed device show an interesting behavior of the CP pulse high level sweep (Figure 5.19): At zero drain bias, the CP current starts to increase slowly already for very low high levels before the typical rapid increase due to expansion of the active CP area takes place. This can easily be explained by the nature of this process variation. The gate electrode in this geometry is stretched to a lower position of the trench compared to the earlier discussed variation P2. Since the gate potential in this CP setup is set to 0 V, the gate induces a more positive

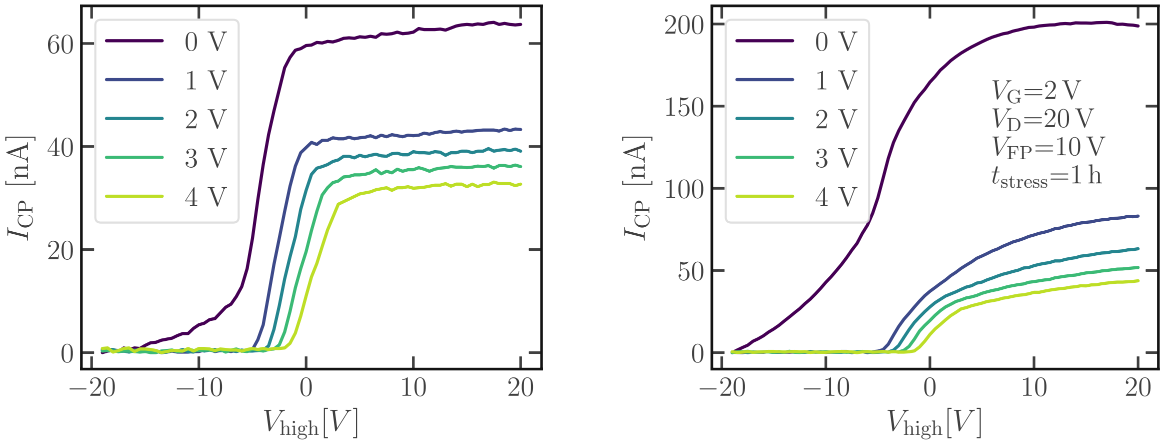

Fig. 5.19. Constant base level CP current of the process split P2 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

potential than the FP at CP pulse high levels below 0 V. In the area around the gate base point in the n-doped drain region, this is, for process variation P2, sufficient to cause accumulation, thereby activating the CP mechanism. Thus, the premature increase of the CP current is caused by a gate-induced extension of the active CP area. When the reverse bias on the drain electrode is increased, this effect is suppressed very rapidly. The superimposed drain bias can easily increase the potential around the gate base point to levels which do not allow for accumulation at the interface. This is shown in a simulation of the electron density in Figure 5.20 for both drain biases. At 0 V, an area of accumulation is clearly observed near the gate base point but completely vanishes at 1 V. Generally, the drain reverse bias seems to impact the CP current at most at levels between 0 V and 1 V. This indicates that the active CP area is impacted at most in this reverse bias range for this specific process variation which fits to the TCAD simulations of the SCR shown in Figure 5.15. After stress, the spread between these two reverse bias voltages becomes even higher as in the virgin device. A possible explanation for this are high and strongly localized defect densities around the gate base point, as already observed in split P1.

Such a strongly localized degradation would be expected to be visible in the form of an additional degradation peak in the derivative of the CP current as shown in Figure 5.21. While after stress no additional peaks are observed, the values of the CP current derivative for a reverse bias of 0 V increase at the lowest pulse high level values. A high defect density near the gate base point would explain this very well since the active CP area slowly increases in exactly this area at these low high level values as discussed earlier for the CP current. For anyone trained to interpret the doping-induced and degradation-induced peaks of CP current derivatives of constant base level measurements, this may seem odd though. Usually, distinctive new peaks for localized degradation after stress, as observed in the split P1, would be expected.

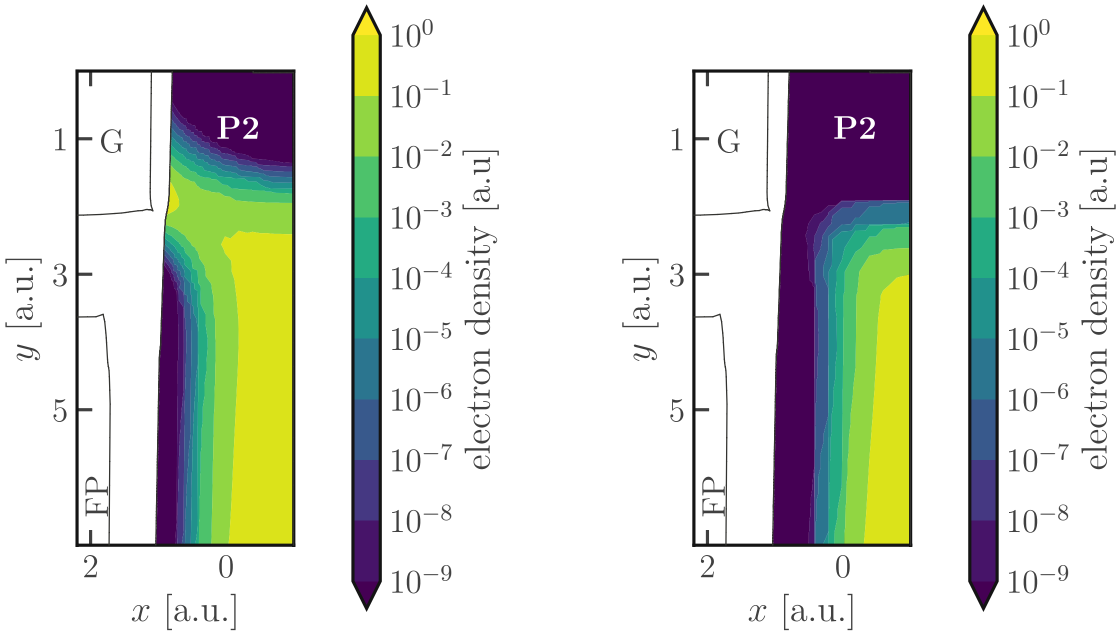

Fig. 5.20. TCAD simulation of the electron density of process variation P2 at a FP voltage of $-10\,\mathrm{V}$ with grounded gate and source contacts. Left: No drain bias. Right: Drain bias of $1\,\mathrm{V}$.

For process variation P3 (Figure 5.22), where the trench is deeper compared to P1, very similar results as in P1 are found for the CP current. This implies that this geometric variation has little impact on the generation of defects due to HCS.

The derivative of the CP current signal (Figure 5.23) reveals one difference compared to structure P1. As for P1, a degradation-induced peak is observed after stress. It seems significantly less pronounced. For this, there are two possible explanations. On the one hand, increasing the trench depth might lead to milder stress conditions. On the other hand, the strongly localized degradation near the gate base point may be overall broadened due to the increased interface area. A conclusive decision which of these possibilities is true can only be made when the trap densities are calculated.

The process variation P4, which is a combination of splits P2 and P3, incorporates properties observed in both these variations. For one, the CP current starts to rise at very low CP pulse high level voltages which is caused by the same mechanism observed in split P2 (Figure 5.24).

Secondly, in the derivative of the CP current, as depicted in Figure 5.25, the signal increases slightly less after stress at low CP pulse high level voltages than in variation P2. Again, whether this can be interpreted as absolute or relative lower localized trap densities can only be answered by checking the evaluated trap densities.

The localized trap densities before and after stress near the gate base point, calculated by Equation (5.15), are shown in Figure 5.26. Earlier interpretations of the constant base

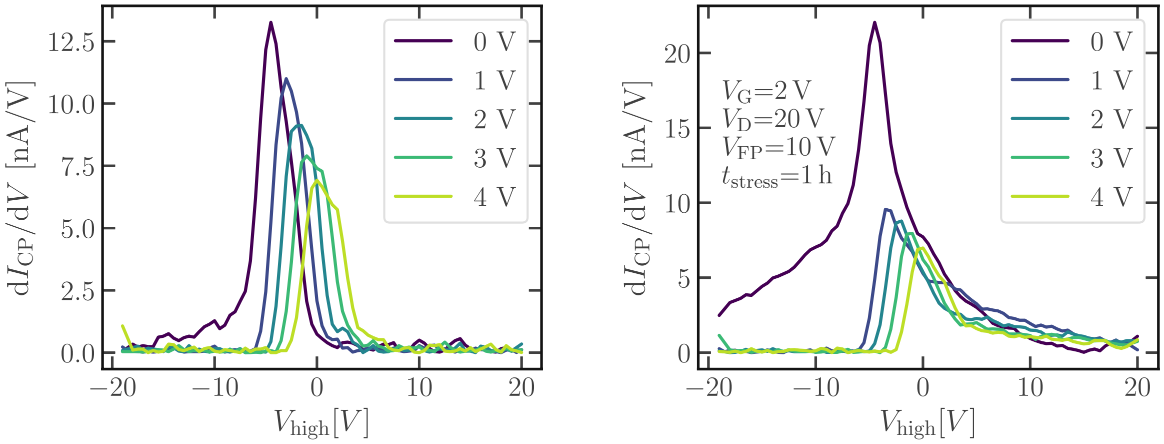

Fig. 5.21. Derivative of the constant base level CP current with respect to the high level voltage of the process split P2 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

level CP are confirmed. Regarding the virgin device of the split P1, the trap density is indeed not constant for the investigated area. In the CP current data, a smaller than expected increase with the CP pulse high level was observed. As a possible explanation, non-uniform degradation within the active area which changes due to the pulse high level was offered. This is confirmed by the calculated localized trap density of this split. At higher trench positions, which are reached by increasing CP high levels, the trap density decreases. Thus, although the active CP area increases, the CP current does not increase by the same factor as less defects contribute to the CP mechanism. After stress, a significant increase of the localized trap densities is observed, especially for the process variations with a lower gate base point (P2 and P4). It is noted that these process variations did not show distinctive doping-induced peaks in the derivative of the CP current signal.

The mean trap densities, depicted in Figure 5.27, show that, even before stress, the average trap densities are lower than the corresponding localized densities near the gate base point. One has to keep in mind that the mean trap density, as defined in Equation (5.16), averages the number of traps between the trench bottom position y_1 and the SCR position y_2. Since this quantity decreases with increasing y_2, it can even be deduced from these data alone that the localized trap density increases towards the top of the trench, even without directly comparing it to the localized trap density in Figure 5.26. The reason for the increased degradation in the virgin device is most likely due to a kink in the trench geometry near the gate base point. During the fabrication of the structure, this imperfection is created and prone to higher defect densities. A similar, albeit more pronounced, behavior is observed after stress. As already concluded from the localized trap density, the stress damaged the oxide near the gate base point severely. Remarkably,

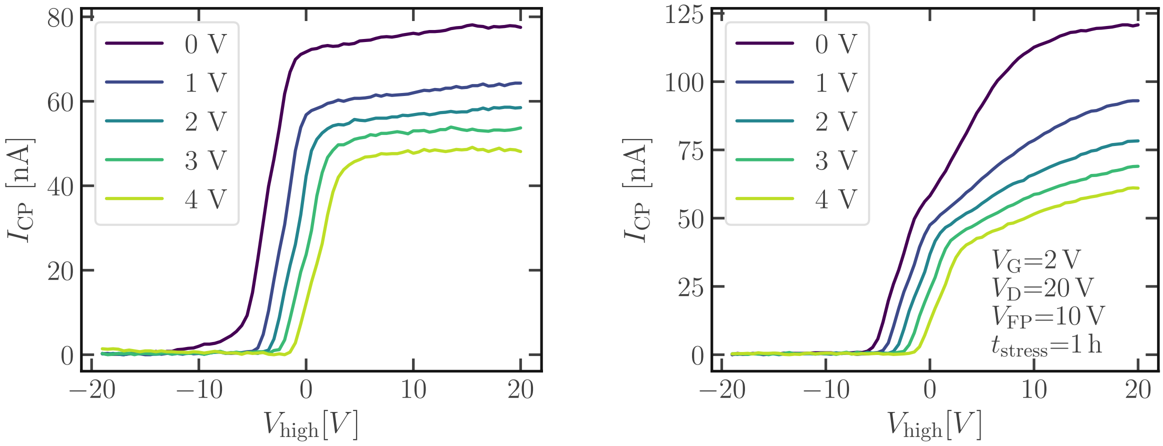

Fig. 5.22. Constant base level CP current of the process split P3 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

areas near the trench bottom have hardly increased in the mean trap density. Thus, almost the whole stress damage is concentrated near the gate base point for this stress condition.

As a qualitative indication for stress damage due to creation of traps, capacitance measurements can be used. The FP capacitance is measured for various biases at the electrode while all other contacts, including the gate electrode are grounded. The results, plotted in Figure 5.28, show a change after stress. Since defects can be detected by CP, where the FP is pulsed between the bias levels reached in the capacitance measurement, this is expected. Unfortunately, the data allows for no easy quantitative extraction of trap densities as the structures are geometrically very complex. For example, although the splits P2 and P4 show higher trap densities than P1 and P3 in CP, the capacitance changes are smaller. This can be explained by the lower positioning of the FP, further away from the generated defects in this case.

In a similar manner, the gate capacitance before and after stress can be considered. Analogously, all contacts except for the gate electrode are grounded while the gate bias is swept and the small-signal capacitance is recorded. As shown in Figure 5.29, changes are observed, similar to the FP capacitance data. In contrast to the measurement of capacitance on the FP, these results are not necessarily expected. They confirm the CP spatial profiling results which clearly showed a high defect concentration after stress near the gate base point. Had the defects been located further towards the trench bottom, no changes of the gate capacitance would have been expected due to the positioning of the gate electrode in the upper part of the trench.

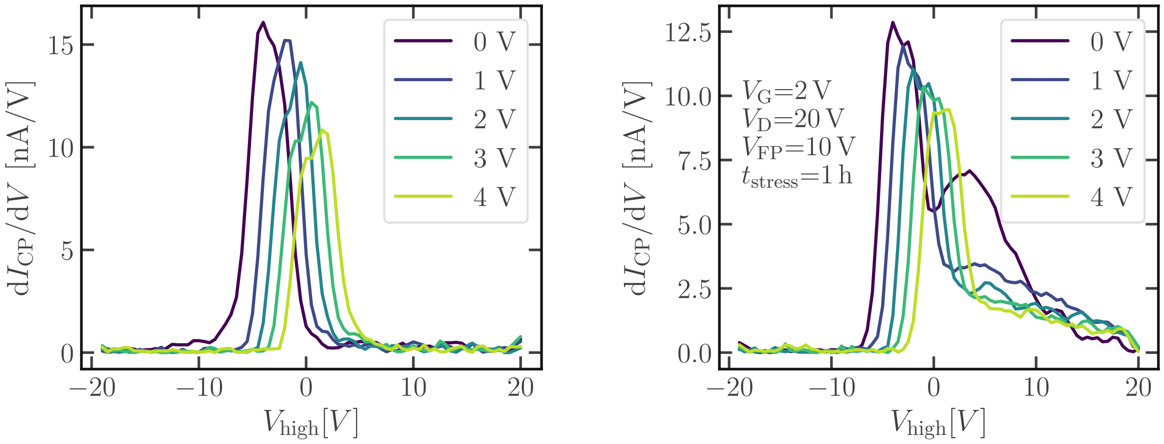

Fig. 5.23. Derivative of the constant base level CP current with respect to the high level voltage of the process split P3 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

5.4.2. Impact of the drain voltage

Since the geometries investigated in this chapter have high breakdown voltages, it is worth characterizing the impact of the drain bias on HCD. For this comparison, drain voltages of 17 V, 20 V and 22 V have been chosen. The respective localized trap densities before and after stress are shown in Figure 5.30. As known from lateral devices, increasing the drain bias also leads to defect generation – higher electric fields increase the population of the high-energy tail of the carrier density functions, thereby increasing the number of carriers which can break bonds and cause HCD [81]. Also, the peak of the localized degradation moves towards the source region.

The mean trap densities (Figure 5.31) reveal that increasing the drain bias adds a spatially constant component to the overall degradation of the device. While the mean trap densities hardly differ at stress drain voltages of 17 V and 20 V between the trench bottom and the lowest measured position y_2 (highest absolute value of y_2), an offset is observed at a drain voltage of 22 V. At the same time, the mean trap density between the trench bottom and the highest measured position y_1 increases less from 20 V and 22 V than from 17 V to 20 V. Thus, although certainly more defects are created at higher stress drain biases, the spatial distribution seems to become more uniform.

5.4.3. Field-plate Potential 0 V

Constant base level CP currents (Figure 5.32) show the same behavior before and after stress when the FP potential during stress is reduced to 0 V. The only most obvious difference between the pre and post stress behavior is the magnitude of the signal. This points towards spatially uniform degradation. The aforementioned figure shows process

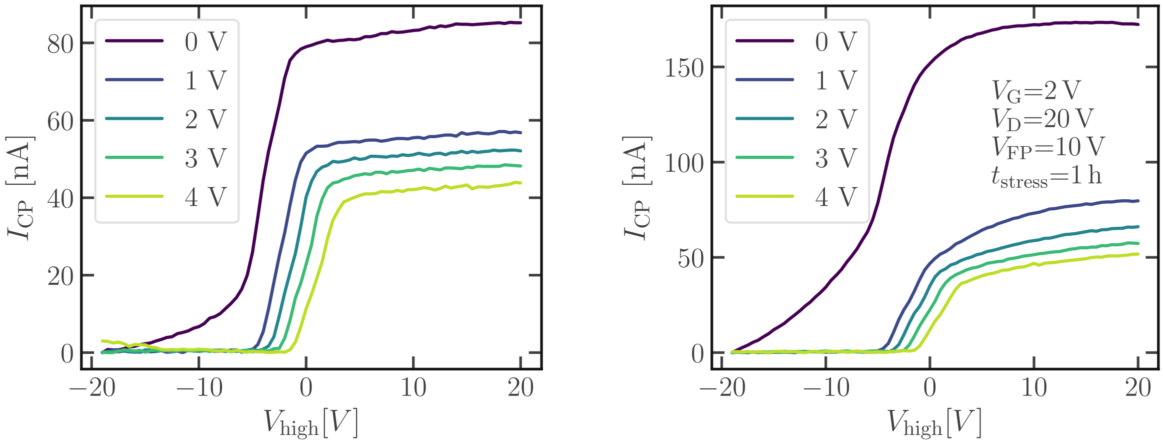

Fig. 5.24. Constant base level CP current of the process split P4 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

variation P1 which will be the only split where the CP current and its derivatives will be discussed in the following. All other process variations behave analogously and are therefore not plotted explicitly.

The derivatives of the CP signal, depicted in Figure 5.33, seemingly confirm this behavior. No additional degradation-induced peaks are observed and, except for a change of the absolute values, no significant new features arise after stress. As mentioned earlier, one would interpret these results as spatially uniform HCS degradation without further data. This argument must be taken with care though. Although it is known from previous measurements that the presence of a degradation-induced peak most likely points to a high localized degradation, the inversion of this argument is not possible. The absence of such a peak does not naturally mean that no locations of strongly localized degradation exist.

This interpretation seems to hold true though for the data of localized degradation, as shown in Figure 5.34. For all process variations, the localized trap density increases approximately by $8 \times 10^9\,\mathrm{cm}^{-2}$ to $1 \times 10^{10}\,\mathrm{cm}^{-2}$. A deeper trench, as in P3 and P4, suppresses the localized degradation more than a more shallow trench.

Generally, a similar interpretation can also be drawn from the mean trap densities, plotted in Figure 5.35. It seems that, in good approximation, a constant offset is caused by the stress. A closer look at the data reveals though that this offset is in the range of $5 \times 10^9\,\mathrm{cm}^{-2}$ to $8 \times 10^9\,\mathrm{cm}^{-2}$, smaller than the offset in the localized trap densities. Thus, at least for shallow trench splits P1 and P2, the localized trench density near the gate base point rises slightly more than the mean trap density. Therefore, even though constant base level CP shows no hints of non-uniform degradation, there are very fine differences in the local trap densities between the gate base point and trench bottom in these process variations. A possible explanation why the splits P3 and P4 are less affected

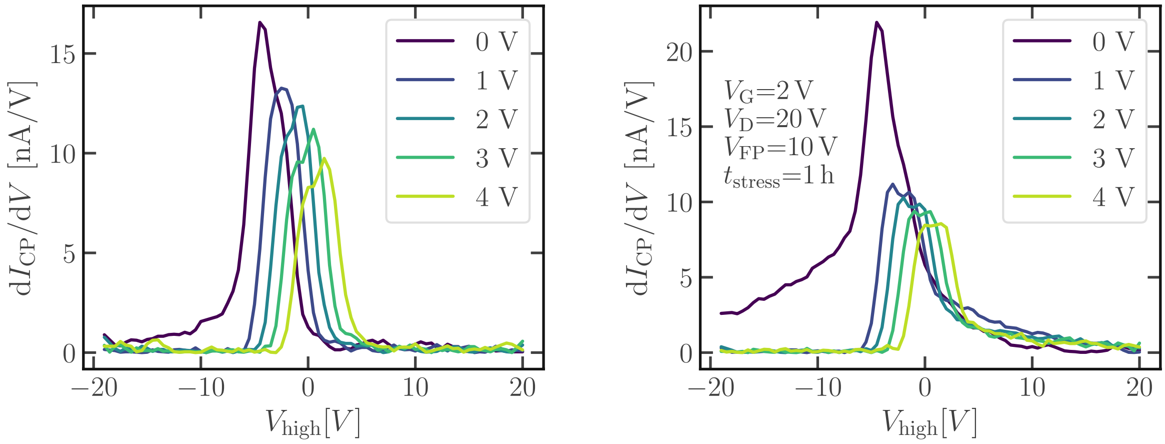

Fig. 5.25. Derivative of the constant base level CP current with respect to the high level voltage of the process split P4 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

by localized degradation near the the gate base point lies in the geometry. Due to their deeper trenches the, relative to the drain bias, negative potential of the FP distributes the electric fields at stress conditions over a larger volume. Thus, carriers with sufficient energies to cause hot-carrier induced damage are not as concentrated at the gate base point. That, however, also means that less HCD should be observed at the splits P3 and P4 as less pronounced field peaks generally result in lower population of high-energy tails of carrier energy distribution functions. The comparison of previous data (Figures 5.26, 5.27, 5.34 and 5.35) consistently confirms this hypothesis.

Although the total number of traps is smaller after the HCS at a FP bias of 0 V than after the 10 V stress, the FP capacitance shows more absolute change at the lower FP bias (Figure 5.36). Again, the geometric complexity of the structures obfuscates the quantitative impact of the traps on the FP capacitance.

Since only an insignificant change of the trap density near the gate base point was observed, the gate capacitance also hardly changes in any process variation (Figure 5.37).

5.4.4. Field-plate Potential 5 V

When a FP voltage of 5 V is applied during the HCS, a much smaller increase of the CP current is observed than for the FP biases of 0 V and 10 V, as shown in Figure 5.38. This is an interesting behavior since one might expect that the trap density change would correlate with the applied FP bias during stress. It was observed for all process splits in a similar manner. As in the previous subsection, only CP constant base level measurements for variation P1 are therefore shown.

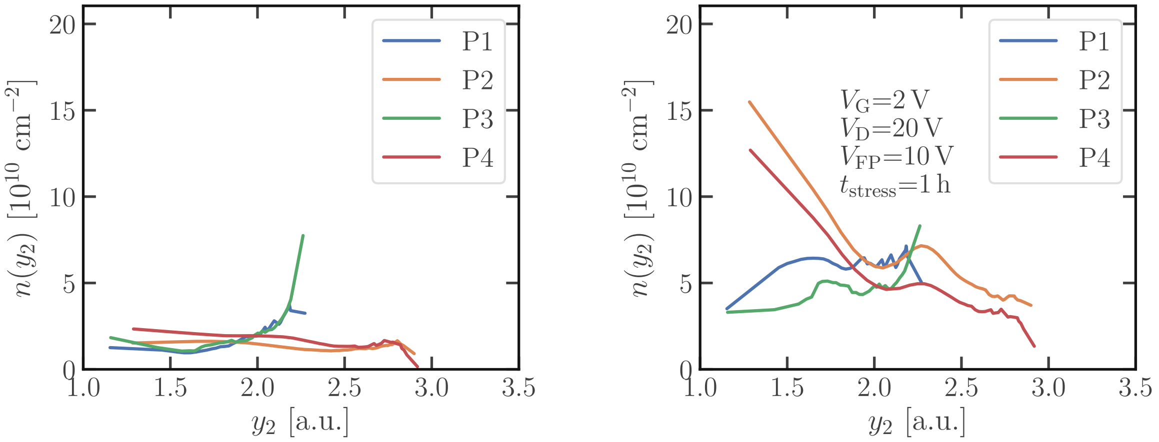

Fig. 5.26. Localized trap densities of the four process splits around the gate base point, calculated by Equation (5.15). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

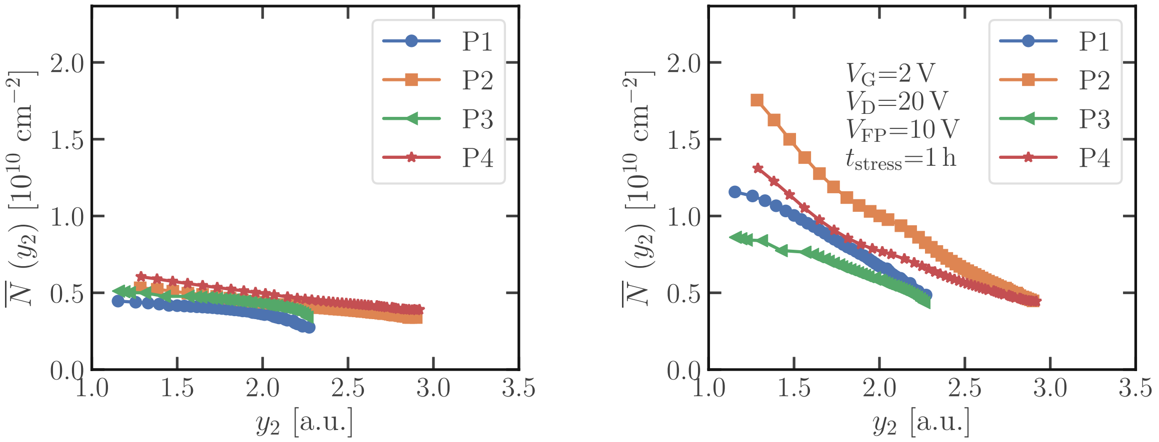

Fig. 5.27. Mean trap densities of the four process splits, calculated by Equation (5.16). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 10 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

The derivative of the aforementioned constant base level measurement (Figure 5.39) indicates an additional degradation-induced peak after stress. It is almost masked by the doping-induced peak but can still be identified, at least at reverse biases between 1 V to 3 V. As in the HCD experiment at a FP bias of 10 V, this can be interpreted as the presence of a high localized degradation after stress. In contrast to this earlier measurement, it is hard to distinguish the doping-induced peak from the degradation-induced peak, though. Also, it is not clear from the data whether the reverse bias can successfully suppress the

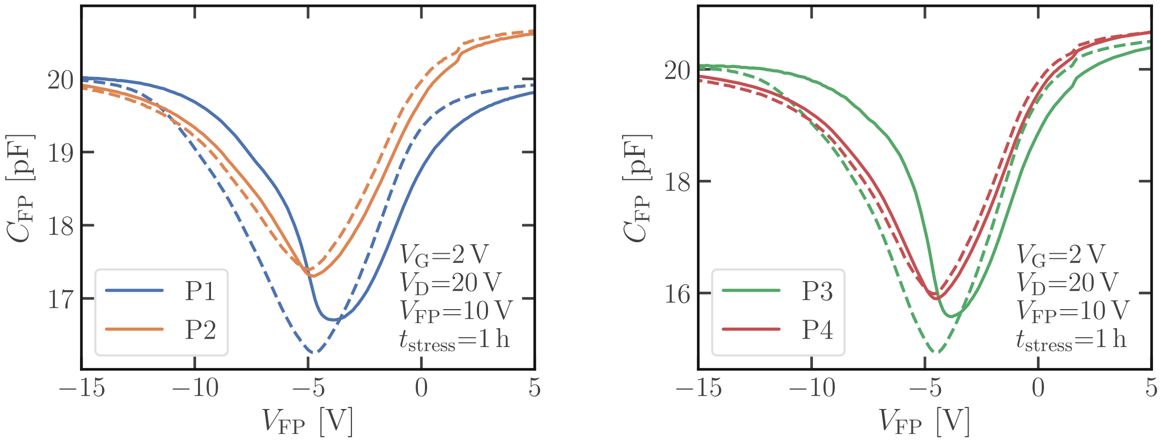

Fig. 5.28. FP capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 10 V was applied. The detailed HCS conditions are given in the figure.

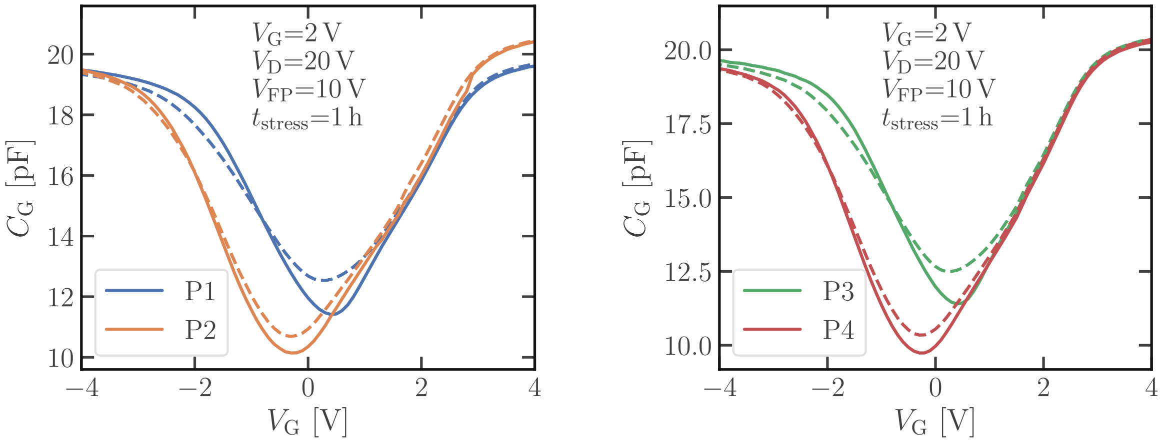

Fig. 5.29. Gate capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 10 V was applied. The detailed HCS conditions are given in the figure.

degradation-induced peak. Therefore, no information about the position of the degradation causing the degradation-induced peak can be drawn.

The localized trap density depicted in Figure 5.40 shows an increase after stress for all process variations. This increase does not correspond to a constant offset.

A clearer picture of the degradation can be obtained from the mean trap density (Figure 5.41). It shows what can be suspected from the constant base level CP data. In comparison to the other stress conditions, the HCS at a FP bias of 5 V shows the lowest increase of the average trap density. Although it only increases by $2 \times 10^9\,\mathrm{cm}^{-2}$ to $5 \times 10^9\,\mathrm{cm}^{-2}$, the localized trap densities still increase by more than $1 \times 10^{10}\,\mathrm{cm}^{-2}$ at some

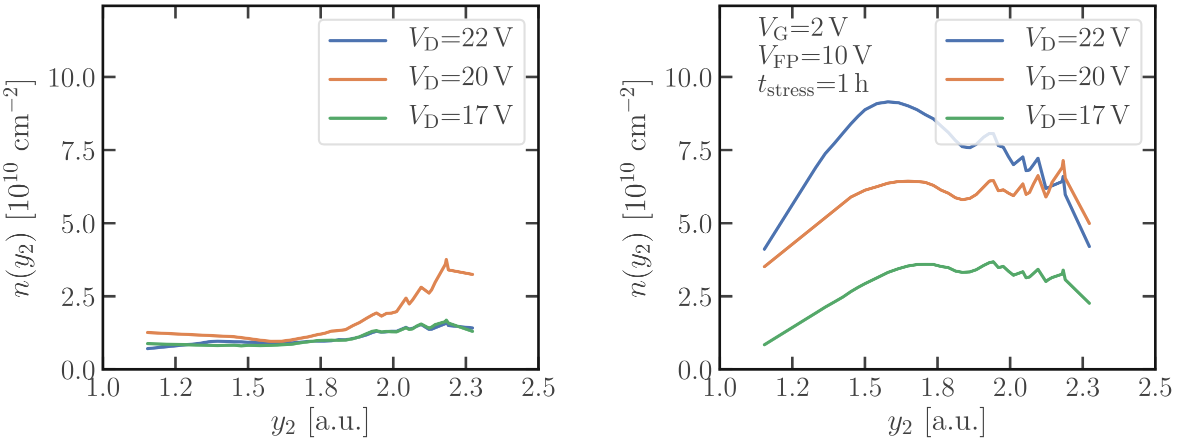

Fig. 5.30. Localized trap densities of process split P1 around the gate base point for various drain biases during stress, calculated by Equation (5.15). The units of y_2 correspond to the y-axis in Figure 5.15. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

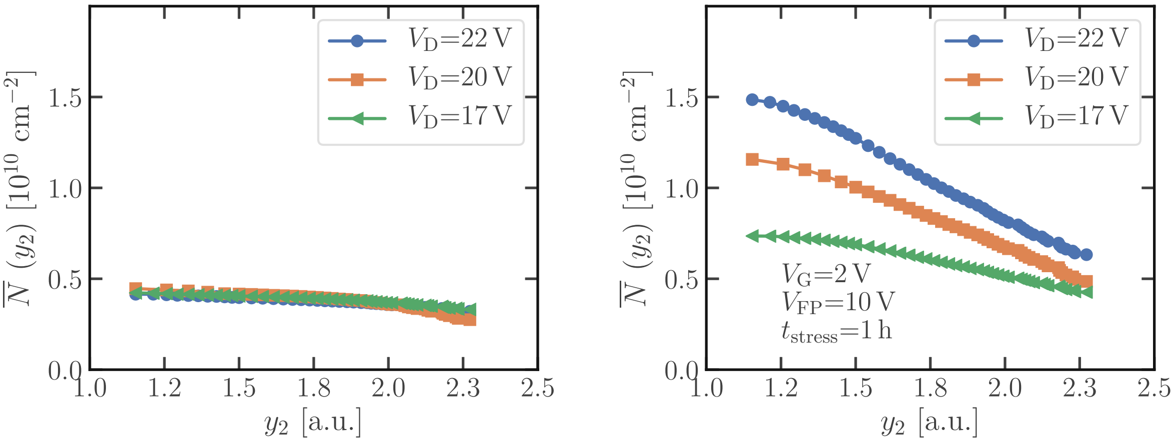

Fig. 5.31. Mean trap densities of process split P1 for various drain biases during stress, calculated by Equation (5.16). The units of y_2 correspond to the y-axis in Figure 5.15. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

positions. This explains the degradation-induced peak of the derivative of the constant base level CP signal.

Due to the insignificant change of the mean trap densities, the FP capacitances (Figure 5.42) also barely change. Again, the structures with lower gate base points show less significant changes due to the positioning of the FP further away from the intensely affected interface areas.

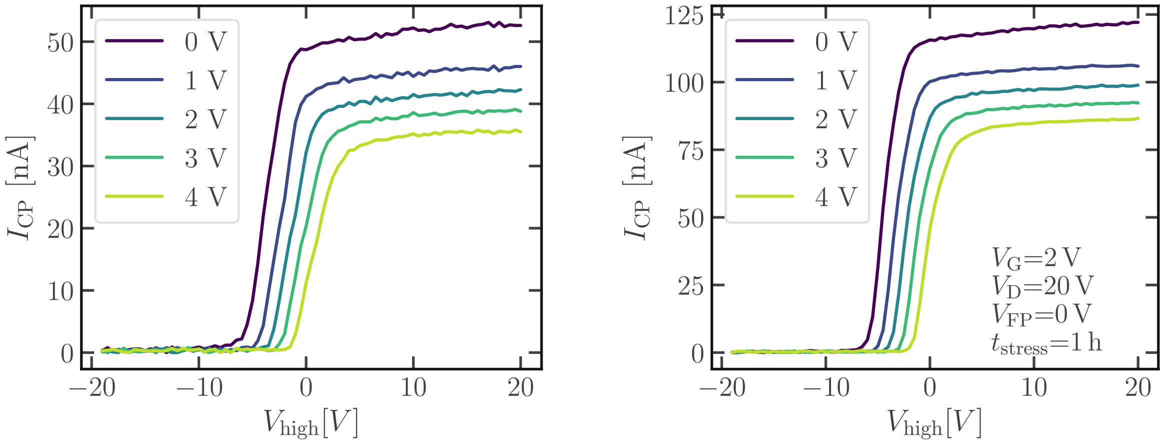

Fig. 5.32. Constant base level CP current of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 0 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

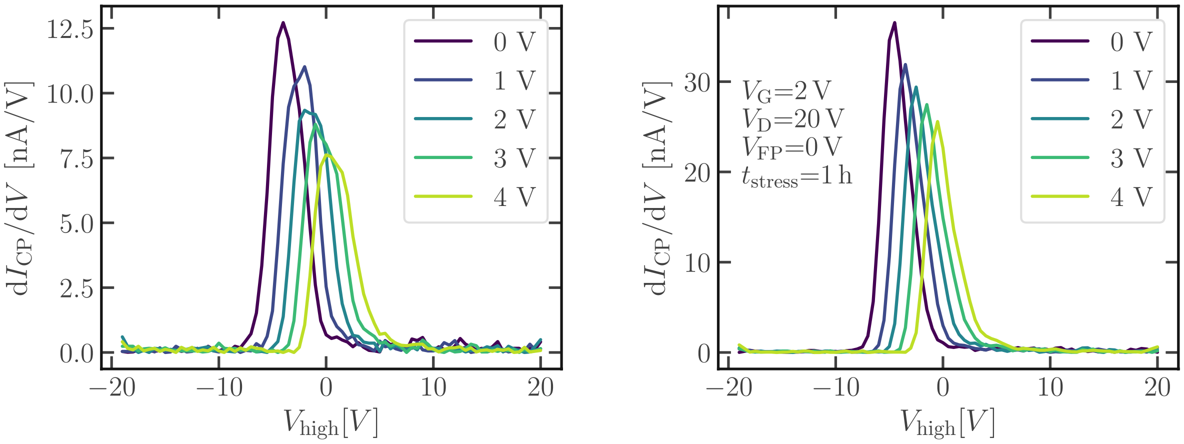

Fig. 5.33. Derivative of the constant base level CP current with respect to the high level voltage of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

Although a very minor impact on the FP capacitances by the stress is observed, the gate capacitances (Figure 5.43) still show a measurable change. This underlines the observed degradation near the gate base point.

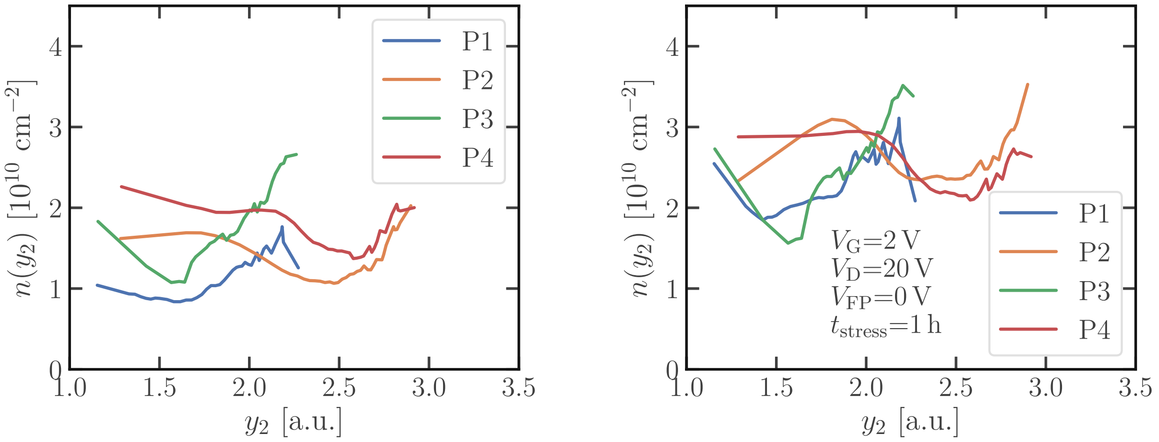

Fig. 5.34. Localized trap densities of the four process splits around the gate base point, calculated by Equation (5.15). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 0 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

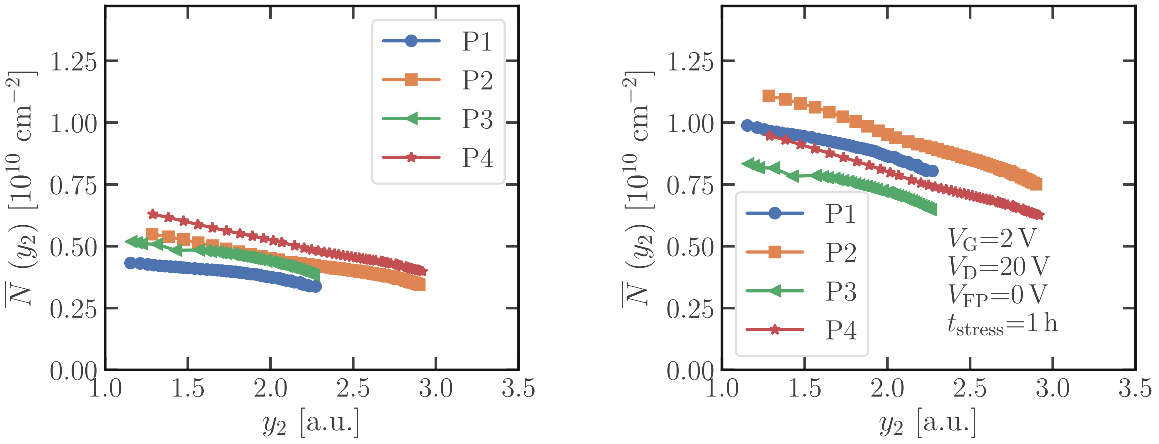

Fig. 5.35. Mean trap densities of the four process splits, calculated by Equation (5.16). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 0 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

5.4.5. Summary

The studies of the various stress conditions of the compensated trench structures have not only revealed new insights on HCD in these devices but also showed new perspectives of the evaluation of CP data. Due to the geometrical peculiarities, new effects, which have not been known from lateral structures, were observed. On the one hand, the increase of the active CP area with the CP pulse amplitude is not as trivial as in lateral devices.

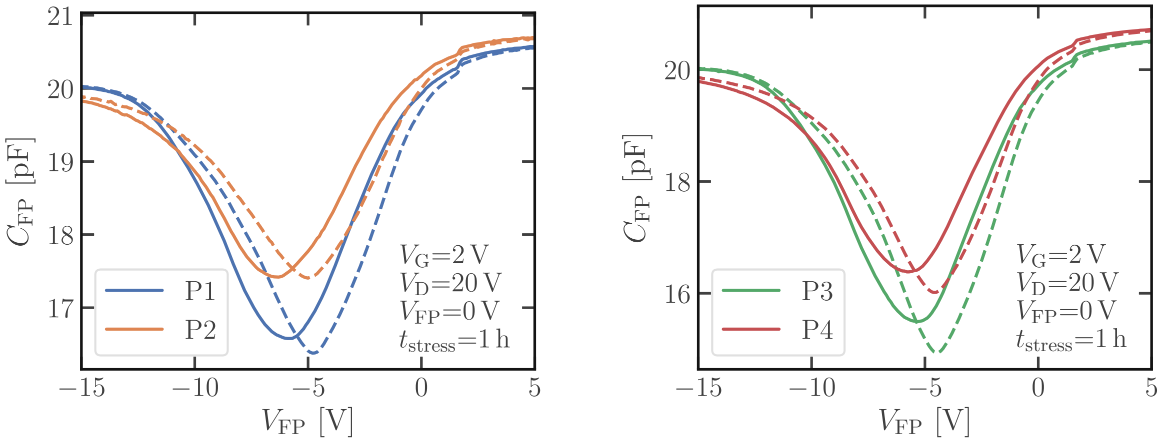

Fig. 5.36. FP capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 0 V was applied. The detailed HCS conditions are given in the figure.

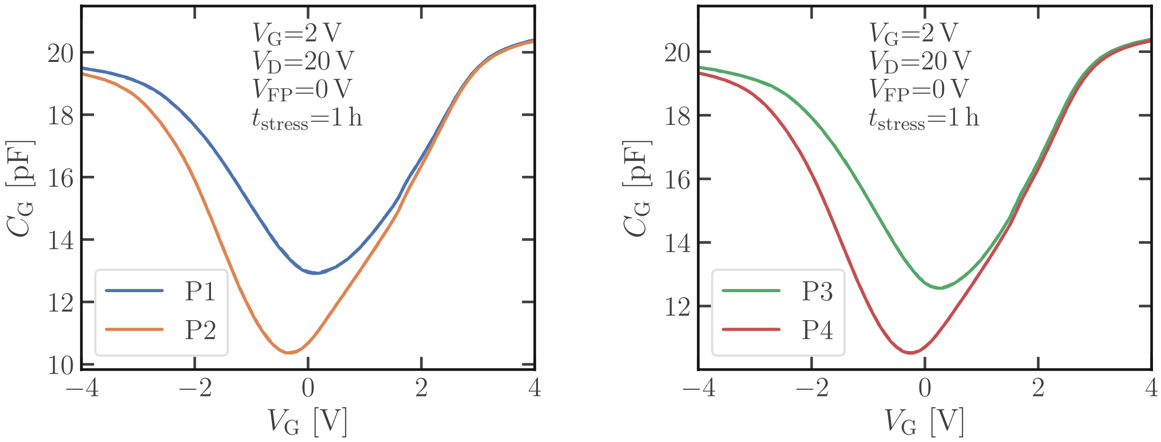

Fig. 5.37. Gate capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 0 V was applied. The detailed HCS conditions are given in the figure.

Even after most of the interface area, which can be investigated in CP by pulsing the FP, reaches accumulation, the SCR in the drain area can be pushed further towards the body region. This causes the aforementioned increase of active CP area (explained in detail in Section 5.3.2). On the other hand, the field constellations in devices with a FP electrode which is positioned deep in the trench cause the premature activation of the CP effect observed in the process variations P2 and P4. These effects should be considered in any complex structures with non-trivial geometries and could cause incorrect interpretations of simple constant base level or constant high level CP measurements. While, for example, the absence of saturation of these signals can be interpreted as presence of voltage dependent

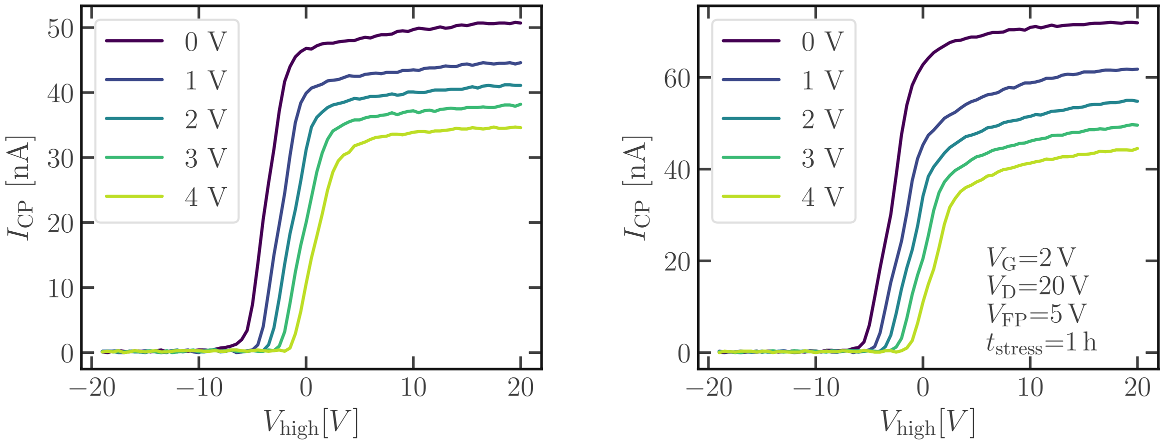

Fig. 5.38. Constant base level CP current of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. During HCS a FP bias of 5 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

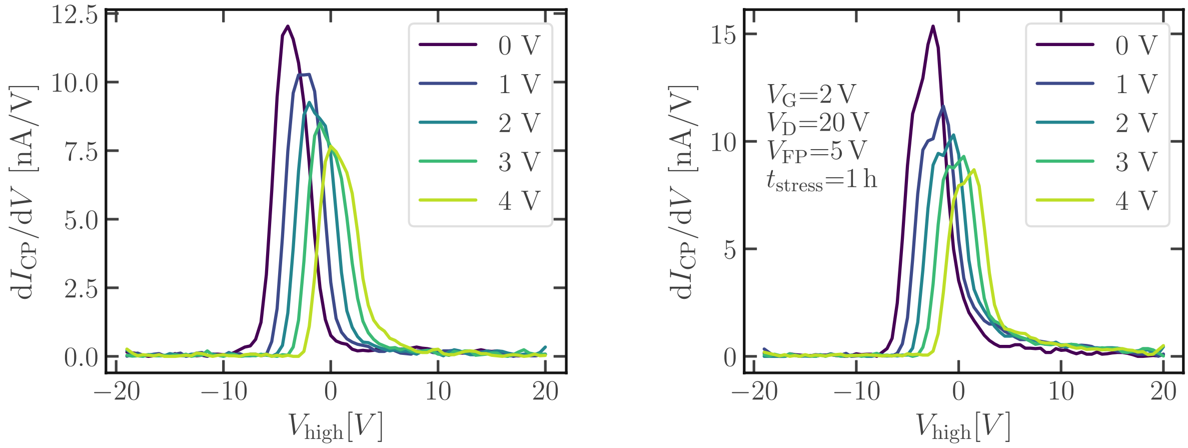

Fig. 5.39. Derivative of the constant base level CP current with respect to the high level voltage of the process split P1 at various drain reverse biases (labeled in legend) at a CP frequency of 100 kHz and a pulse base level of −30 V. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

border traps (cf. Section 4.3), it could also be associated with the aforementioned increase of the active CP area. Additionally, a non-uniform spatial degradation in the added active CP areas may further impact the saturation behavior. Thus, while one possible influence of this saturation behavior is identified for lateral devices (border traps), three parameters can be plausible causes in more complex devices (border traps, increase of active CP area, non-uniform degradation).

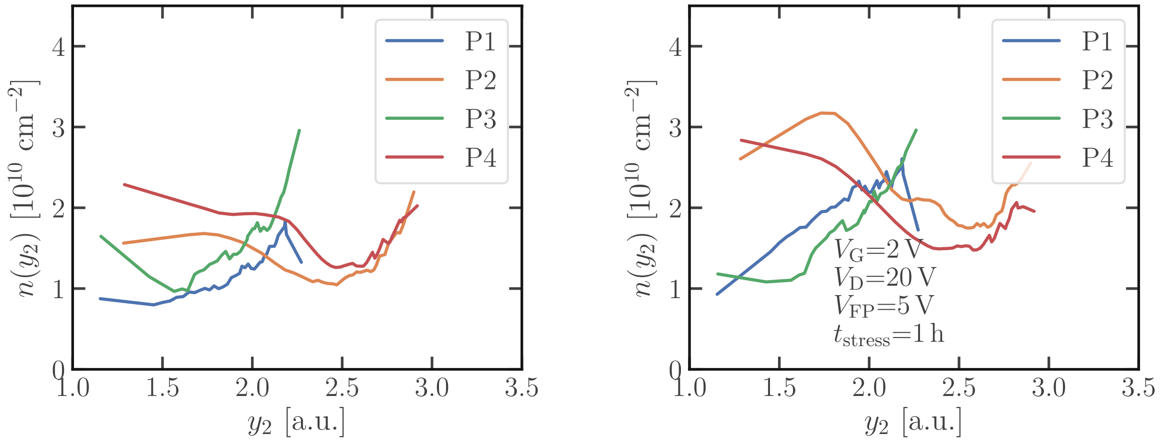

Fig. 5.40. Localized trap densities of the four process splits around the gate base point, calculated by Equation (5.15). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 5 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

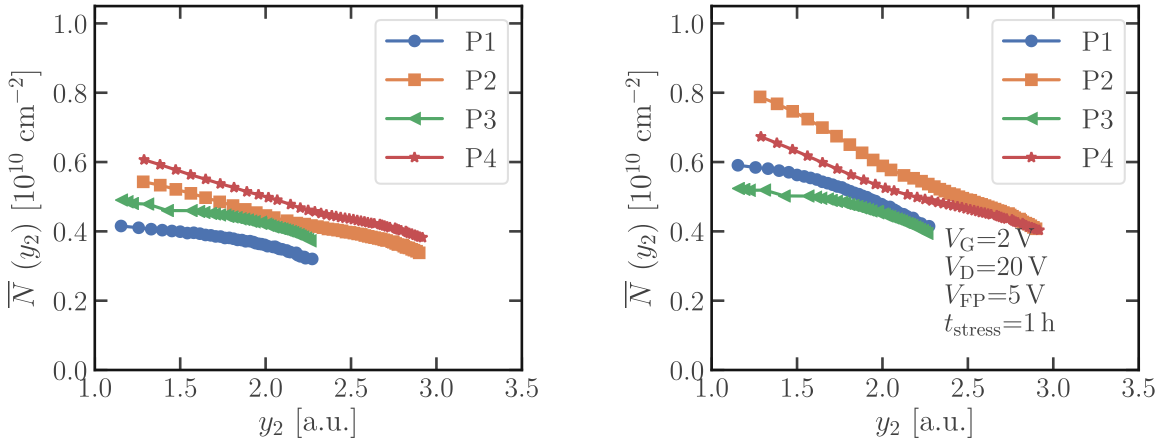

Fig. 5.41. Mean trap densities of the four process splits, calculated by Equation (5.16). The units of y_2 correspond to the y-axis in Figure 5.15. During HCS a FP bias of 5 V was applied. Left: Virgin device. Right: Stressed device, detailed HCS conditions in the figure.

Regarding HCD, it was shown that technological changes of the compensation principle, emulated by the variation of the FP bias during HCS, have a massive impact on the quantitative damage caused by the stress as well as the location of degradation. A medium FP voltage of 5 V causes the smallest number of defects although the localized degradation concentrated near the gate base point is higher than when no bias is applied to the FP during the stress. Furthermore, the higher local degradation near the gate is not immediately evident from constant base level CP measurements after the stress at a FP

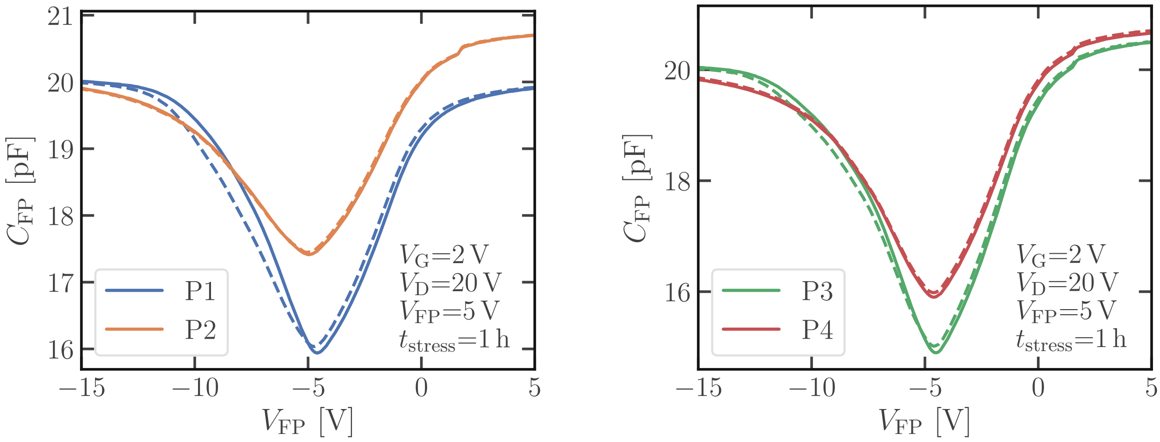

Fig. 5.42. FP capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 5 V was applied. The detailed HCS conditions are given in the figure.

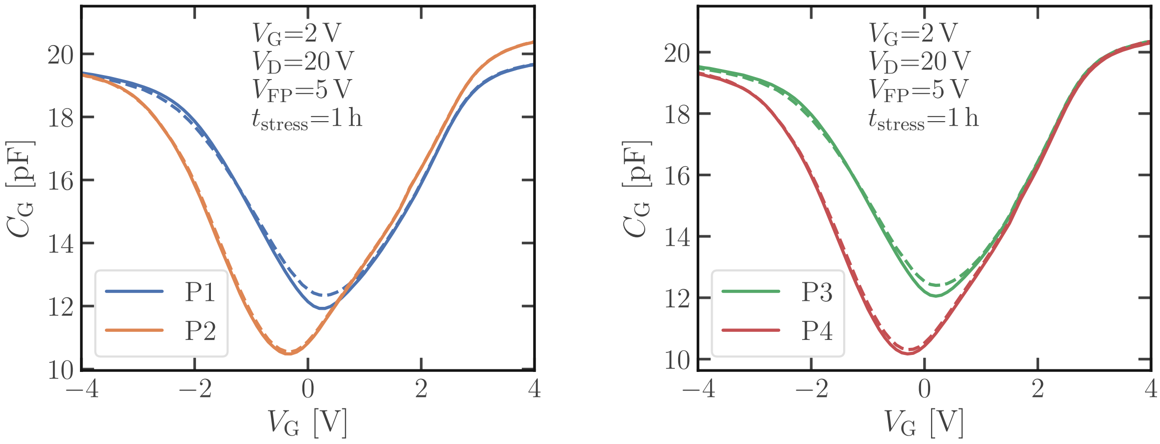

Fig. 5.43. Gate capacitance measurements of the four process splits. Dashed lines represent the virgin device, solid lines the stressed device. During HCS a FP bias of 5 V was applied. The detailed HCS conditions are given in the figure.

voltage of 5 V. Although the derivative of this CP current signal suggests an additional degradation-induced peak after stress, this peak may be obfuscated by the doping-induced peak which is always present. Therefore, it is advisable to aways check and compare the localized and mean trap density of all vertical positions of the device as sensitive differences of localized trap densities can be observed by these two quantities.

The measurements of the gate and FP capacitances of the devices before and after stress may be indicators of the location of the degradation. This measurement method fails in predicting the magnitudes of localized and mean trap densities of the device though.

Therefore, these capacitance methods can be used as a last resort for qualitative defect characterization in measurement setups where CP is not possible.

5.5. Drift-Diffusion Simulation of Hot-Carrier Degradation

TCAD simulations are a significant element of technology development since the fabrication of actual devices is extremely time consuming. With the help of TCAD, it is possible to shape new technologies before the production of actual designs is launched. Therefore, it would be a major advantage to be able to predict the location and severity of HCD during this concept phase. In this section, two drift-diffusion quantities, the vertical electric field and the impact ionization rate, are investigated as potential candidates for such a prediction.

5.5.1. Vertical Electric Field

The vertical electric field has long been suspected to predict the location of HCD. Thorough studies [82] show that it is not an accurate predictor but yields a good estimation of the location of the degradation. At first, its applicability is checked on process variation P1, where local trap density profiles are available for different stress conditions. The comparison for the three drain voltages is shown in Figure 5.44. Due to the compensation principle, the different drain biases do not impact the vertical component of the electric field as much as in a lateral or uncompensated device. A cut through the simulation data is depicted in the bottom right corner of Figure 5.44. In this area, close to the investigated oxide, the change of the vertical electrical field is negligibly small although a clear trend from low to high drain potentials is visible. No shift of the position of the electric fields can be observed either. Although, as in previous literature, the approximate position of the increased localized degradation is certainly correct, this simulation quantity fails to predict details about the position and intensity of the HCS damage. As discussed in Section 5.4.2, increased drain voltages during stress shift the degradation towards the body area. Also, higher trap densities are caused (cf. Figure 5.30).

A similar interpretation can be drawn from the localized trap data of the four process variations when compared to the simulation (Figure 5.45). Again, the vertical electric field fails to predict the magnitudes. A closer look at the data from the cut of the simulation (Figure 5.46) reveals that for process variation P2 and P4 (where the gate base point is located further towards the trench bottom) the localization is even worse than for P1 and P3. At a FP bias of 10 V during stress, splits P2 and P4 show a distinctive increase of degradation near the body region while the change of localized trap density is not as pronounced for P1 and P3 (Figures 5.26 and 5.40).

5.5.2. Impact Ionization Rate

As a second possible candidate, the impact ionization rate is investigated. It seems to predict the location very well for process variation P1, which was stressed at various drain biases (Figure 5.47). Also, it increases with the drain voltage as well as the resulting degradation. Unfortunately, when the other three process variations are compared, as depicted in Figure 5.48, the magnitudes are incorrect. The cuts of the 2D simulation (Figure 5.49), which were always made at the same position, show that for process splits P2 and P4 the maxima of the impact ionization rate move further away from the interface. Thus, one could speculate that although less carriers are created by impact ionization, the distance over which they can be accelerated towards the interface is greater, thereby resulting in more damage.

In any case, neither the impact ionization rate nor the electric field can reliably predict HCD. The complex physics of this degradation mechanism [26] with many non local influences can therefore not approximated by a drift-diffusion approach with enough precision.

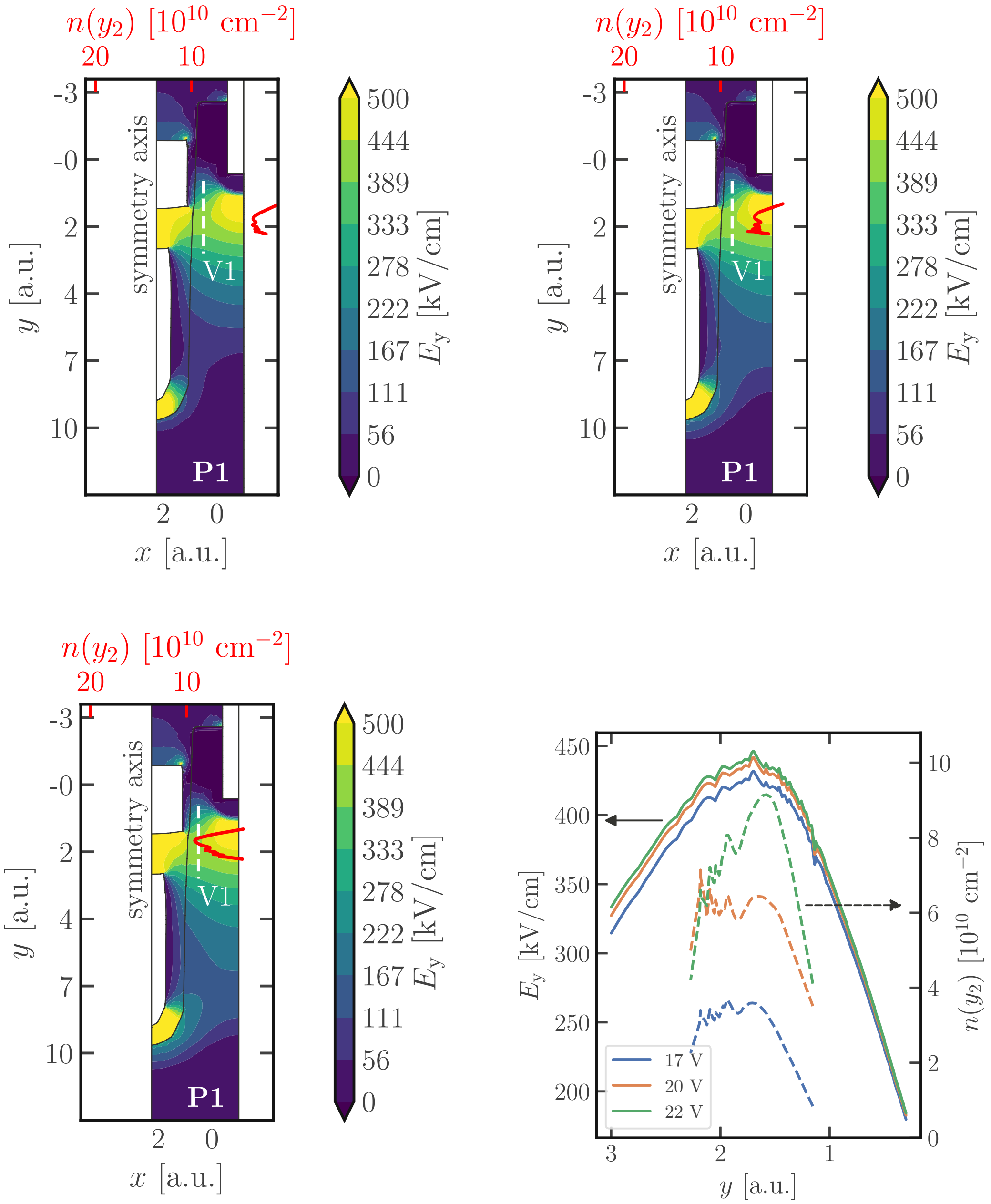

Fig. 5.44. TCAD simulation of the y-component of the electric field during HCS (gate and FP voltages of 2 V and 10 V, respectively) for process variation P1. The drain voltage of the HCS condition is varied (top left: 17 V, top right: 20 V, bottom left: 22 V, bottom right: vertical cuts (V1)). The top axis (red) shows the measured trap density (data from Figure 5.30) for a HCS with a duration of 1 h. Dashed lines (right axis) represent the localized trap density from Figure 5.30.

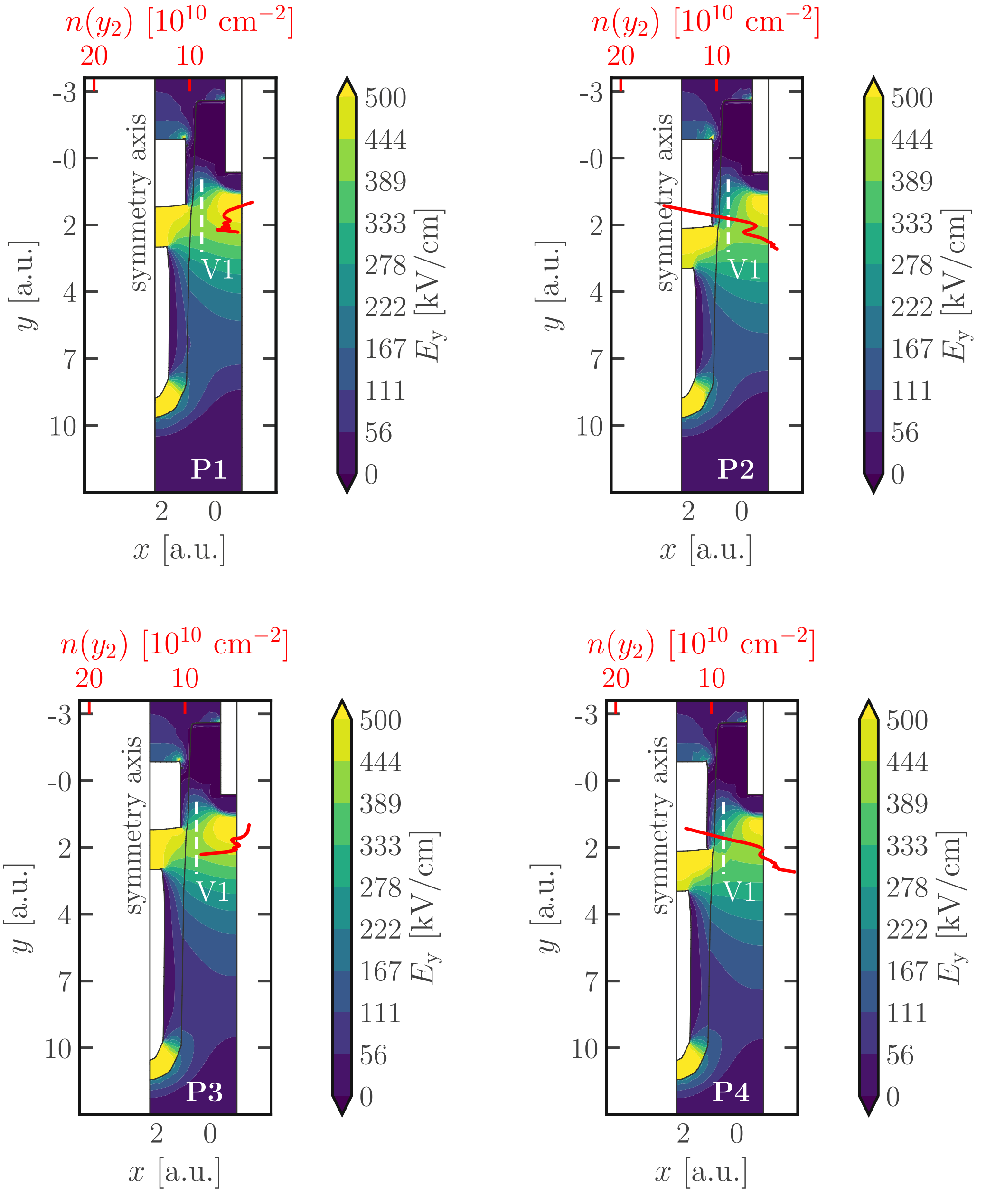

Fig. 5.45. TCAD simulation of the y-component of the electric field during HCS (gate, drain and FP voltages of 2 V, 20 V, 10 V, respectively) for all four process variations. The top axis (red) shows the measured trap density (data from Figure 5.26) for a HCS with a duration of 1 h.

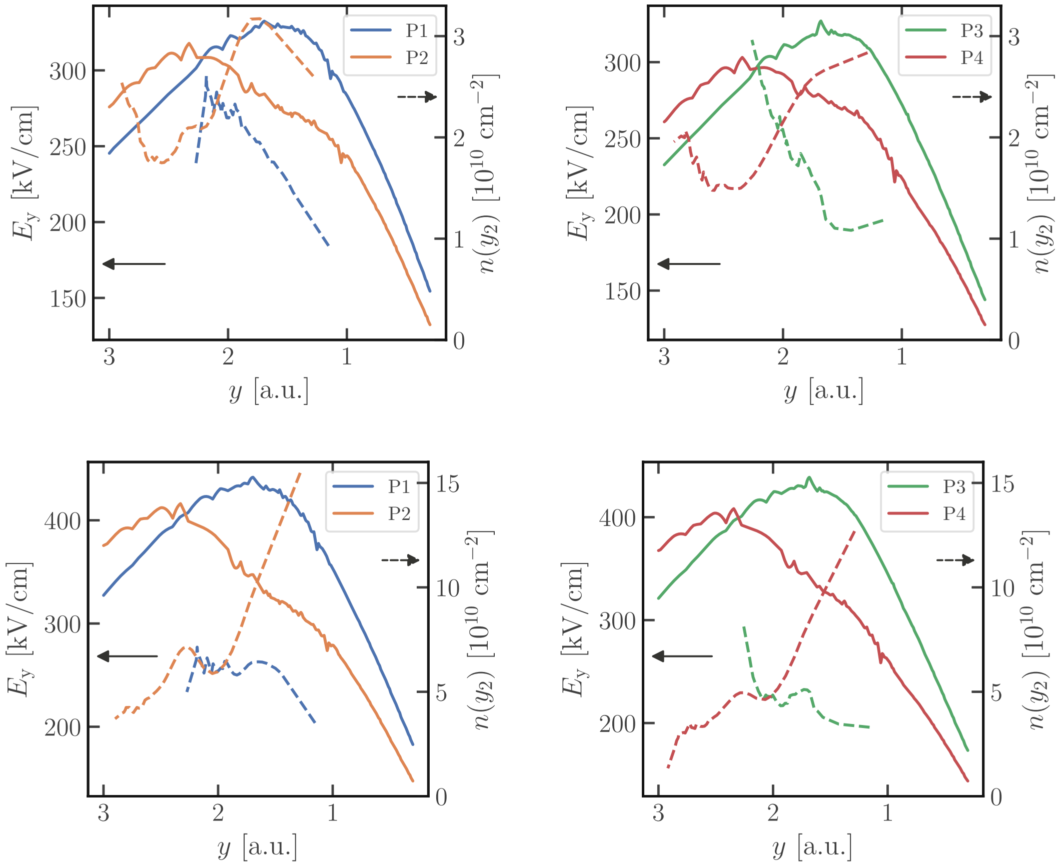

Fig. 5.46. Vertical cuts (V1) of the simulation of the y-component of the electric field for all process variations. Top: HCS conditions at a FP voltage of 5 V. Bottom: FP voltage of 10 V as depicted in Figure 5.45. Dashed lines (right axis) represent the localized trap density from Figures 5.26 and 5.40.

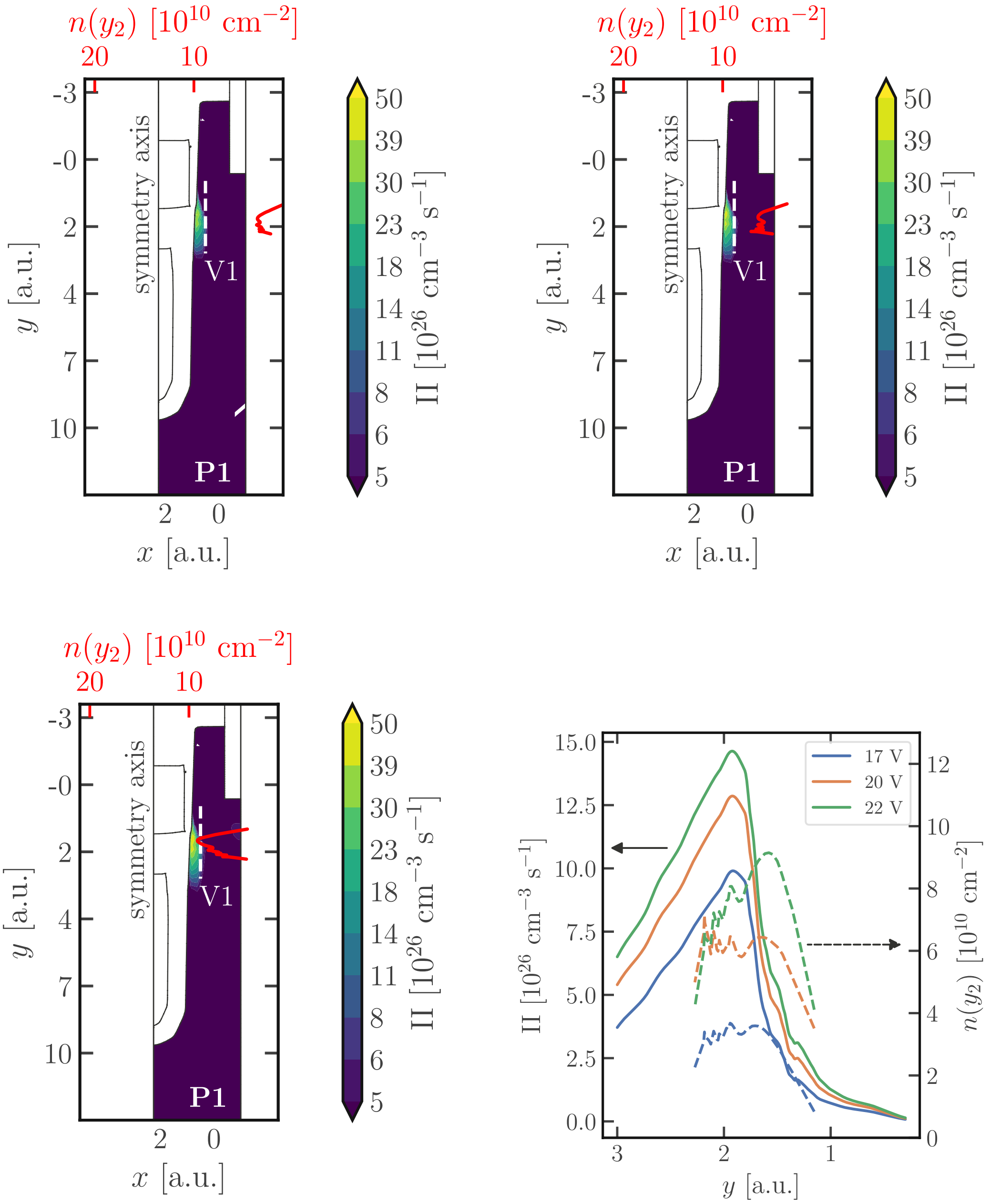

Fig. 5.47. TCAD simulation of the impact ionization rate during HCS (gate and FP voltages of 2 V and 10 V, respectively) for process variation P1. The drain voltage of the HCS condition is varied (top left: 17 V, top right: 20 V, bottom left: 22 V, bottom right: vertical cuts (V1)). The top axis (red) shows the measured trap density (data from Figure 5.30) for a HCS with a duration of 1 h. Dashed lines (right axis) represent the localized trap density from Figure 5.30.

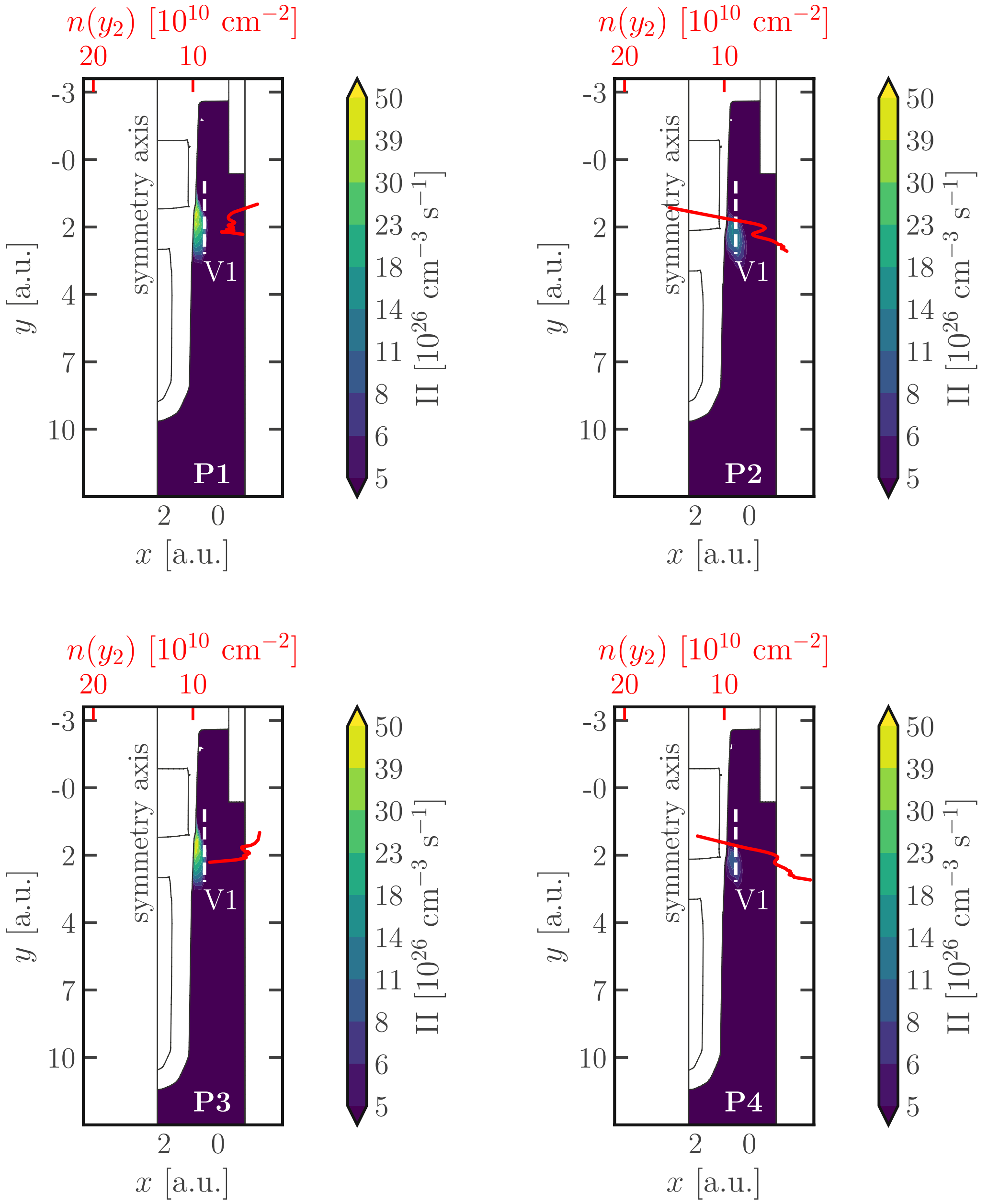

Fig. 5.48. TCAD simulation of the impact ionization rate during HCS (gate, drain and FP voltages of 2 V, 20 V, 10 V, respectively) for all four process variations. The top axis (red) shows the measured trap density (data from Figure 5.26) for a HCS with a duration of 1 h.

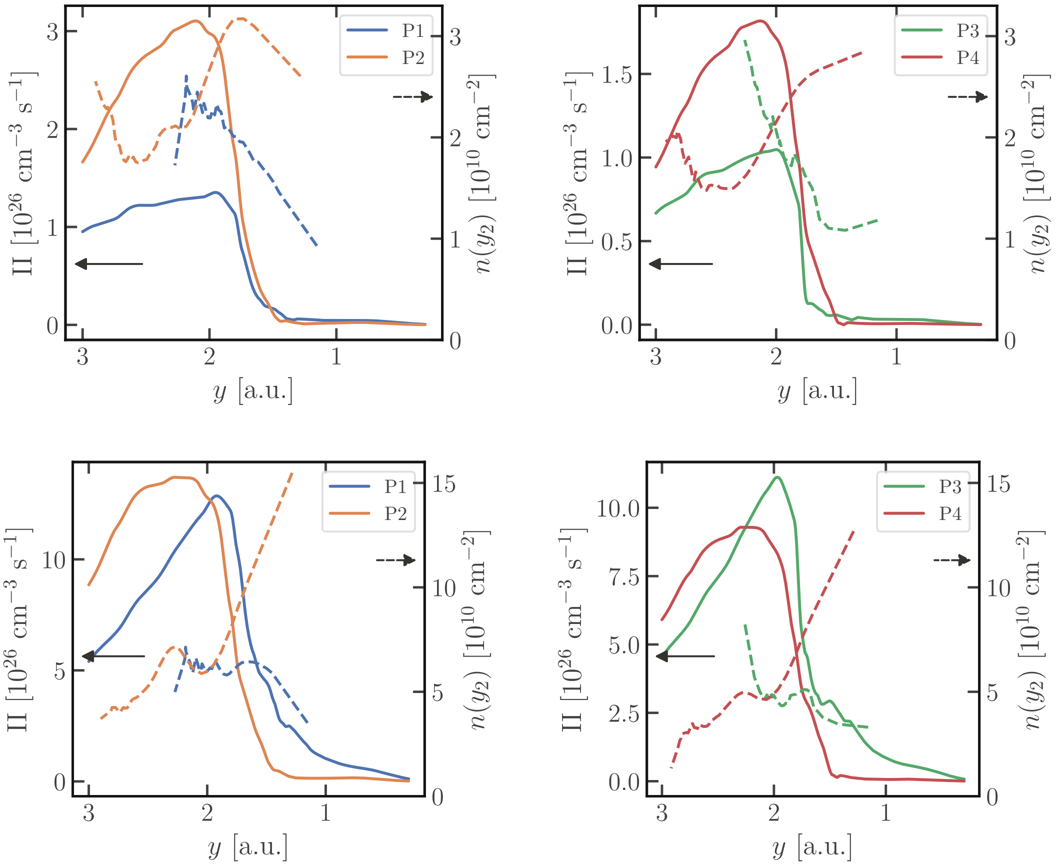

Fig. 5.49. Vertical cuts (V1) of the simulation of the impact ionization rate for all process variations. Top: HCS conditions at a FP voltage of 5 V, bottom: FP voltage of 10 V as depicted in Figure 5.48. Dashed lines (right axis) represent the localized trap density from Figures 5.26 and 5.40.

CHAPTER 6

Conclusion and Outlook

Fast is fine but accuracy is final.
— Wyatt Earp

The first chapters of this work present new perspectives of the well-known hot-carrier degradation (HCD) phenomenon and the associated defects, even though it has already been thoroughly investigated in the past decades. New insights into the fundamental dynamics of the interaction of silicon-oxide interface defects with charge carriers were gathered in a comparison of the well-established Shockley Read Hall (SRH) model with the improved non-radiative multi-phonon (NMP) model. The latter introduces a relaxation energy which models the atomic reconfiguration of the interface due to the change of charge states, which is missing in the SRH model. By modifying the capture cross section of the SRH theory by an Arrhenius factor, this NMP relaxation energy could be added 'through the back door', thereby creating the Shockley Read Hall - temperature activated (SRHT) model. Using experimental data, these three theoretical models could be compared. It was shown that, although the SRH model completely omits the structural relaxation, all models yield similar results. While the newly introduced hybrid model results in better agreement with the NMP model than the SRH model, the practical uses are limited. Since the SRHT model also requires the knowledge of a correct NMP relaxation energy, the NMP model should always be preferred. The SRHT theory is rather a theoretical study which explores the transition from SRH to NMP by applying temperature dependent cross sections, which itself is not a new concept. It was found in the study of the SRH, SRHT and NMP theories that, even though they yield differing data, the same final conclusions can be drawn from either approach. This explains why the SRH model, albeit being introduced in the beginning of the 1950s, is still frequently used in modern literature. Due to its simplicity it can be implemented rather quickly as no thoughts about the relaxation energy have to be wasted, but its accuracy may very well be limited.

With these results in mind, two unsolved problems of HCD are tackled. On the one hand, its temperature dependence had never been fully investigated. It had been clear, that long-channel devices showed worse degradation after hot-carrier stress (HCS) at low temperatures but systematic analyses of the phenomenon had been rare. Using a specially designed HCS experiment, this behavior was confirmed. Furthermore, the energetic defect spectra showed that the same types of defects were created at all temperatures. This allows for a more simplified view of the effect for future investigations. It would be a rather simple and fruitful exercise to repeat those experiments for short-channel structures as the developed HCS experiment can be adopted easily. In these devices, the temperature dependence of HCD is inverse, i.e the temperature fosters degradation.

The second issue with HCD which has been investigated was the nature of the created border traps. Usually, the border traps are separated from interface traps by their time constants. Due to additional quantum-mechanical tunneling, the dynamics are usually slowed down compared to interface traps. While this is true, another facet of border traps, their voltage dependence, is often disregarded. It could be shown that, for the technologies used in these experiments, the voltage dependence is by far more significant than the time dependence. Such being the case, there is a risk that border traps are overlooked in HCD studies. Therefore, voltage dependent border traps should always be considered.

After the investigation of defect physics and general peculiarities of HCD, the phenomenon was explored on complex trench structures. At first, common measurement methods had to be adapted and established for these devices. With the development of a new localization technique for charge pumping (CP), it was possible to pinpoint areas of high degradation in the oxide of the trenches for different HCS bias conditions and various geometric variations of the technology. In a drift-diffusion simulation approach, it was attempted to predict the intensity and location of the degradation. It was shown that these models are too simple to model the complex physics of HCD. Thus, a more sophisticated approach for a more reliable prediction of HCD is needed. A promising solution might be the application of the Boltzmann transport equation for carriers. It yields the carrier energy distribution functions which ultimately allows the modeling of HCD. Such a model has already been successfully implemented for trench structures [83]. As these devices are often used in fast switching applications, the investigation of pulsed as opposed to constant voltage HCD may also be interesting.

APPENDIX A

Measurement Challenges of Charge Pumping

Generally, the currents in the CP measurement are very small and depend on defect densities and structure sizes, in the range of nanoamperes. Thus, noise suppression of the whole setup of the experiment must be optimized as much as possible. As the slopes of the CP pulse dictate the active energy window of the experiment, the generated pulse should be as little distorted as possible when applied at the gate. Therefore, it is advisable to keep the wiring connection of the pulse generator and the device under test as short as possible. This means that switching matrices, which are popular in setups with many different measurement devices, should be bypassed for the pulse generator.

What makes the CP measurement even more delicate is that the CP current itself stems from the quick charging and discharging of the defects. The measured CP current is an average of the charging and discharging processes during thousands of CP pulses. An example of the transient progress of the current which – when averaged – results in the CP current is given in Figure A.1. The investigated oxide in this example has a defect density of $1 \times 10^{10}\,\mathrm{cm}^{-2}$. This translates to a CP current of only $4.2\,\mathrm{nA}$ at a CP frequency of $10\,\mathrm{kHz}$. For the transition time of $10\,\mathrm{\mu s}$, peak currents of almost $75\,\mathrm{\mu A}$ are observed. Thus, the actual CP signal is a factor of over 17000 smaller than the charging and discharging current. With this current, mainly the MOS capacity and the semiconductor space charge region are charged. The charging of the interface traps is, as mentioned, only a tiny fraction of the total current. Mainly, the charging and discharging of the SCR of the investigated device and the MOS structure are observed. Although all currents except for the defect charging currents cancel each other out when hundreds of periods are averaged for the CP experiment, the peak currents still have to be captured by the measurement units. Most amperemeters have a fixed set of ranges in which the currents may not be exceeded at any times. Otherwise wrong results are obtained. Some advanced amperemeters support auto-ranging which chooses the respective range for the measurement automatically. Theses systems are usually not designed for fast current changes as in CP and may fail to adjust the correct range. Thus, whenever CP measurements are performed, it is advisable to use fixed ranges which are definitely within the peak currents which occur during the experiment. As an approximate guide for the lowest possible boundary of the current

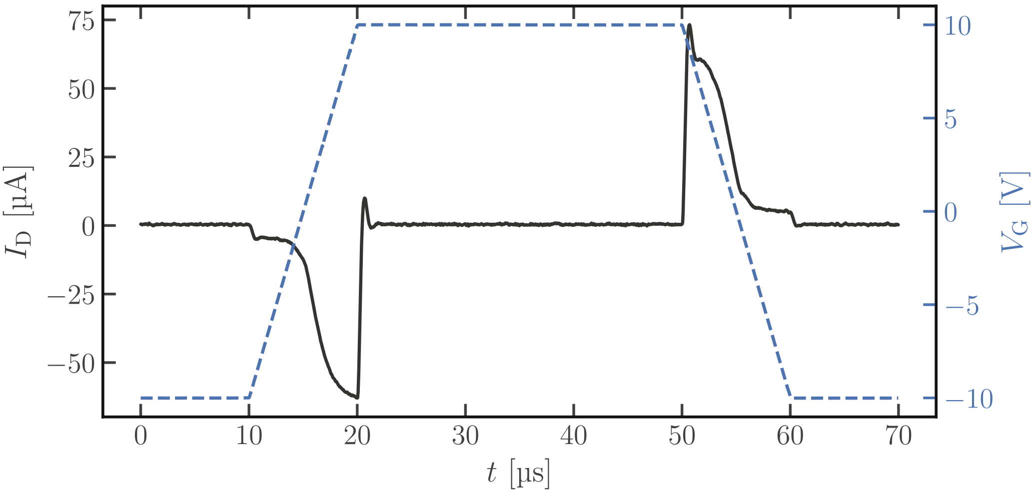

Fig. A.1. Experimental transient signal of the drain current during a typical CP pulse. For a defect density of $1 \times 10^{10}\,\mathrm{cm}^{-2}$, the CP current for this specific structure would only amount to 4.2 nA at a CP frequency of 10 kHz.

range selection, the capacitance of the investigated MOS structure can be used:

$$I_\mathrm{range} > C_\mathrm{MOS}\frac{\Delta V_\mathrm{G}}{t_\mathrm{rf}} \tag{A.1}$$

This equation stems from the fact that the (dis)charging currents are approximately proportional to the transition slopes of the CP pulse. It is noted that too high current ranges may not be able to resolve the much smaller CP current anymore. For big discrepancies between the peak current and the actual CP current, the signal will therefore probably get very noisy. Therefore, increasing the CP frequencies may be helpful in getting better signals. Also, if the drawback of measuring a smaller CP energy window can be accepted, longer transition times of the pulses should be considered. This may be an acceptable compromise, since the active energy window of CP is only logarithmically dependent on the transition times (cf. Equations (1.8) and (3.2)) while the peak current is linearly dependent on them.

In ranges of the amperemeters which are large compared to the CP current signal, offset errors may also cause issues in the experiment. It may be possible to remove this offset by performing the CP experiment while leaving the contact of either the electron or hole source floating. In this case, one of the charge carriers is missing in the CP effect which means that the overall CP is disabled. Therefore, the net current on the remaining contact can stem from CP. Thus, if any non-zero current is measured, it can be seen as an offset and can therefore be subtracted from the data of the actual CP experiment. Contents of this section have been adapted from [70].

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List of Publications

B. Ruch, G. Pobegen, M. Rösch, R. K. Vytla, and T. Grasser, “Charge pumping of low-voltage silicon trench power MOSFETs”, *IEEE Transactions on Device and Materials Reliability*, vol. 19, pp. 133–139, 1 Mar. 2019. DOI: `10.1109/TDMR.2019.2891794`.

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List of Figures

Symbols

Symbol	Description	Unit
A_{channel}	channel area	cm^2
A_{die}	die area	mm^2
A_{dop}	area of the semiconductor-oxide interface adjacent to a specific doping region	cm^2
$A_{\mathrm{eff}}^{\mathrm{CP}}$	active area of CP	cm^2
C_{MOS}	capacitance of an MOS structure	F
$C_{\mathrm{bt}}^{\mathrm{edge}}$	number of border traps obtained by CP for the edge of a device	1
$C_{\mathrm{tot}}^{\mathrm{edge}}$	total number of traps (border and interface traps) obtained by CP for the edge of a device	1
C	Capacitance	F
D	density of states	cm^{-2} eV^{-1}
E_{C}	conduction band energy	eV
E_{V}	valence band energy	eV
E_{t}	trap energy	eV
$E_{21}^{\mathrm{e}^-}$	energy difference between electron traps and conduction band	eV
$E_{21}^{\mathrm{h}^+}$	energy difference between hole traps and valence band	eV
E_{21}	energy difference between traps and reservoir	eV
$E_{\mathrm{i}}^{\mathrm{NMP}}$	potential energy in the minimum of the NMP parabolas	eV
I_{CPbt}	CP current	A
I_{CPit}	CP current	A
I_{CP}	CP current	A
I_{D}	drain current	A
I_{range}	maximum possible current which can be measured in a specific range of an ammeter	A
L_{eff}	effective length of CP	µm
L_{trans}	length of the transverse trench	µm
M	effective mass of the defect molecule in the NMP model	kg
N^{act}	trap density obtained by CP for the active area of a device	cm^{-2}

Symbol	**Description**	**Unit**
N_{C}	number of states in the conduction band	m^{-3}
N_{V}	number of states in the valance band	m^{-3}
N_{CP}	trap density obtained by CP	cm^{-2}
$N_{\mathrm{bt}}^{\mathrm{act}}$	border trap density obtained by CP for the active area of a device	cm^{-2}
$N_{\mathrm{bt}}^{\mathrm{edge}}$	border trap density obtained by CP for the edge of a device	cm^{-2}
N_{bt}	trap density obtained by CP	cm^{-2}
$\overline{N}_{\mathrm{dop}}$	average trap density of an oxide adjacent to a specific doping region	cm^{-2}
N_{it}	trap density obtained by CP	cm^{-2}
N_{norm}	normalized trap density of border and interface traps obtained by CP	cm^{-2}
$N_{\mathrm{tot}}^{\mathrm{act}}$	total trap density (border and interface traps) obtained by CP for the active area of a device	cm^{-2}
$N_{\mathrm{tot}}^{\mathrm{edge}}$	total trap density (border and interface traps) obtained by CP for the edge of a device	cm^{-2}
N_{tot}	total trap density (border and interface traps) obtained by CP	cm^{-2}
$\overline{N}$	average trap density of an oxide in a specific interval	cm^{-2}
N	trap density	cm^{-2}
Q	Charge	C
T	temperature	K or °C
V_1	lower integration limit for the evaluation of a doping-induced peak of CP	V
V_2	upper integration limit for the evaluation of a doping-induced peak of CP	V
V_{D}	drain voltage	V
$V_{\mathrm{FP}}^{\mathrm{CP}}$	flat-band voltage of CP	V
V_{G}	gate voltage	V
$V_{\mathrm{TH}}^{\mathrm{CP}}$	threshold voltage of CP	V
V_{base}	base level of the CP pulse	V
V_{high}	high level of the CP pulse	V
V_{i}	NMP potential	eV
V_{th}	threshold voltage a MOSFET	V
W_{term}	length of the termination trench	µm
ΔV_{G}	amplitude of the CP pulse	V
Δq	difference between the reaction coordinate and the local equilibrium position in the NMP model	m
ω_{i}	vibrational NMP frequency in the minimum i	Hz
σ^{NMP}	capture cross section in the NMP model	cm^2
σ^{SRHT}	capture cross section in the SRHT model	cm^2

Symbol	Description	Unit
σ^{SRH}	capture cross section in the SRH model	cm^2
σ	capture cross section	cm^2
$\tau_{\mathrm{cap}}^{\mathrm{e}^-}$	electron caputure time constant	s
$\tau_{\mathrm{cap}}^{\mathrm{h}^+}$	hole capture time constant	s
$\tau_{\mathrm{emi}}^{\mathrm{e}^-}$	electron emission time constant	s
$\tau_{\mathrm{emi}}^{\mathrm{h}^+}$	hole emission time constant	s
ε_0	vacuum permittivity ($8.854\,187\,817 \times 10^{-14}$)	$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$
$\varepsilon_{12}^{\mathrm{NMP}}$	transition barrier from a reservoir to a trap (caputure) in the NMP model	eV
$\varepsilon_{12}^{\mathrm{SRH}}$	transition barrier from a reservoir to a trap (caputure) in the SRH model	eV
ε_{12}	transition barrier from a reservoir to a trap (caputure)	eV
$\varepsilon_{21}^{\mathrm{NMP}}$	transition barrier from a trap to a reservoir in the NMP model (emission)	eV
$\varepsilon_{21}^{\mathrm{SRH}}$	transition barrier from a trap to a reservoir in the SRH model (emission)	eV
ε_{21}	transition barrier from a trap to a reservoir (emission)	eV
$\varepsilon_{\mathrm{R}}^{\mathrm{e}^-}$	relaxation energy of negatively charged defects in the NMP model	eV
$\varepsilon_{\mathrm{R}}^{\mathrm{h}^+}$	relaxation energy of positively charged defects in the NMP model	eV
ε_{R}	relaxation energy in the NMP model	eV
$\varepsilon_{\mathrm{SiO_2}}$	permittivity of $\mathrm{SIO_2}$ (3.9)	1
d	oxide thickness	nm
f_0^{CP}	normalization frequency for CP (100)	Hz
f^{CP}	frequency of CP	Hz
k_{B}	Boltzmann constant (8.617×10^{-5})	$\mathrm{eV\,K^{-1}}$
$k_{12}^{\mathrm{e}^-}$	transition rate for electron capture	s^{-1}
$k_{12}^{\mathrm{h}^+}$	transition rate for hole capture	s^{-1}
$k_{21}^{\mathrm{e}^-}$	transition rate for electron emission	s^{-1}
$k_{21}^{\mathrm{h}^+}$	transition rate for hole emission	s^{-1}
m^*	effective electron mass	kg
n_{CP}	differential trap density obtained by CP	cm^{-2}
n	electron concentration	m^{-3}
p	hole concentration	m^{-3}
q	elementary charge (1.602×10^{-19})	C
t_{fall}	fall time of the CP pulse	s
t_{rf}	rise or time of the CP pulse	s
t_{rise}	rise time of the CP pulse	s

Symbol	Description	Unit
v_{th}	thermal velocity of carriers	$\mathrm{cm\,s^{-1}}$
y_1	vertical position of the trench bottom	m
y_2	vertical position of the SCR of the body-drain junction at the trench interface.	m

Acronyms

BTI bias temperature instability.

CP charge pumping.

DB dangling bond.
DFT density functional theory.
DQ degradation quenching.

FP field-plate.

HCD hot-carrier degradation.
HCS hot-carrier stress.

MOS metal oxide semiconductor.
MVE multi-vibrational excitation.

NBTI negative bias temperature instability.
NMP non-radiative multi-phonon.

SCR space charge region.
SPCP spectroscopic charge pumping.
SRH Shockley Read Hall.
SRHT Shockley Read Hall - temperature activated.

TCAD technology computer-aided design.