TECHNISCHE UNIVERSITÄT WIEN
Vienna University of Technology

Master Thesis

Electric Characterization of SiC Trench MOSFETs with DLTS and Admittance Spectroscopy

Magdalena Weger BSc

01402990

Supervisor:
Univ. Prof. Dipl.-Ing. Dr. techn. Tibor Grasser
Institute for Microelectronics

KAI-Supervisor:
Dr. Judith Berens

Villach, May 2021

ABSTRACT

SiC trench MOSFETs aim to meet the need for efficient power transistors in our modern technology based society. State of the art are devices with aluminum (Al) as dopant in the inversion channel area. However, previous studies have shown an Al-related defect that might cause a channel mobility reduction. To overcome this SiC MOSFETs with boron (B)-implanted inversion channels are fabricated and electrically investigated. Devices with 10% B, 30% B and 100% B channel implantation are compared to the reference sample implanted with 100% Al. Basic measurement techniques as well as cryogenic characterizations such as DLTS and admittance spectroscopy are used to characterize the samples. A comparison between the latter two is drawn. Furthermore, results from an admittance spectroscopy simulation are shown in relation to the actual measurement. Since the analyzed B samples were annealed at low temperatures in order to prevent B out-diffusion, a non negligible amount of B can be found in the channel area by admittance spectroscopy. However, the measurement results indicate a B concentration that is too low to ensure a working metal oxide semiconductor field effect transistor (MOSFET) device. An outlook for further implantation dosages and annealing temperatures is given, which might lead to functioning MOSFETs with B as a channel implant.

This thesis was written in cooperation with KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH. This work was funded by the Austrian Research Promotion Agency (FFG, Project No. 881110).

ACKNOWLEDGMENT

I wish to express my sincere thanks to my supervisor Dr. Judith Berens and the members of KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH for providing me such a wonderful working atmosphere and a constant support with my master thesis.
Further I would like to thank Univ.-Prof. Tibor Grasser, who thoroughly corrected my work and made it possible for me to write this thesis in cooperation with KAI. His kind and motivating words inspired me. By giving me his trust I had the chance to further develop my research skills at a non-university research institution.
I am also using this opportunity to express my gratitude to my family and my friends for their understanding, support and thoughtfulness while I was working on this thesis.

Eideststattliche Erklärung

Hiermit erkläre ich, dass ich die vorliegende Arbeit eigenständig und ohne fremde Hilfe angefertigt habe. Textpassagen, die wörtlich oder dem Sinn nach auf Publikationen oder Vorträgen anderer Autoren beruhen, sind als solche kenntlich gemacht. Die Arbeit wurde bisher keiner anderen Prüfungsbehörde vorgelegt und auch noch nicht veröffentlicht.

Villach, 28.2.2021

.....
Magdalena Weger BSc

Contents

1 Introduction

SiC as a wide band gap semiconductor used in a MOSFET shows promising properties, which might allow for applications in a variety of new conditions. This fairly new technology based on SiC needs to be investigated and understood in more detail in order to produce high quality devices.

For fast switching and efficient devices, it is essential that the carrier mobility in the bulk as well as in the channel is high. The bulk electron mobility has a satisfying level of about $40\,\mathrm{cm}^2/\mathrm{Vs}$ [1, 2], whereas the channel electron mobility can be sometimes orders of magnitudes smaller and allows thus room for improvement. Ideally, for high channel mobility there are no traps in the channel area and electrons can pass through without getting trapped. Not only interface defects reduce the channel mobility, but also doping atoms act as scattering centers, which impact the carrier mobility. This process among others lowers the efficiency of a MOSFET significantly [1, 3].

The goal of this thesis is to study different trap levels in the band gap and their origin. In previous studies, an Al-related defect has been identified [4]. In this thesis, an alternative p-dopant for SiC (B instead of by Al) and its impact on the aforementioned trap level is investigated. It is known that the diffusion of B in the SiC lattice is high compared to the one of Al, which makes B doping challenging. In addition to that the lattice is damaged and new traps might be created during the implantation process.

The DLTS measurement is state of the art to characterize deep levels in the band gap. A second option to characterize deep traps is a method known as the admittance spectroscopy. DLTS as well as admittance spectroscopy require cryogenic temperatures during the measurement procedure. The goal is to establish the admittance spectroscopy at the measurement setup and compare it to the DLTS measurement. Basic measurement techniques to electrically characterize MOSFETs such as transfer characteristics and mobility measurements will help to further understand the effect of Al/B doping on the trap states.

2 Fundamentals

Power MOSFETs have a wide range of applications. They must function under harsh conditions and at high temperatures while standing strong mechanical and chemical impacts [5]. SiC as a bulk material for a MOSFET seems to meet all these needs. In addition to that the crystal growth technique for SiC has reached a level, at which mass production of SiC MOSFETs is possible. Via sublimation of silicon (Si) and carbon (C) and the combined deposition of these two, a high quality SiC-crystal is grown and then processed to result in a MOSFET structure. In some of the processing steps the SiC lattice might get damaged, which can lead to performance loss. Hence, it is important to understand, which defects exist and how they must be treated in order to produce a high-performant and reliable device.

2.1 Properties of Silicon Carbide

SiC is very suitable for the application in a power electronics since it shows outstanding mechanical, thermal and electrical properties. Its mechanical hardness, for example, ensures long time mechanical robustness. Further advantages of SiC are the wide band gap, which correlates with the intrinsic carrier density, the high electric break down field and the high thermal conductivity. Even at high temperatures the intrinsic carrier concentration remains small. Furthermore, SiC in high power devices allows faster switching than previously used Si, since the produced SiC-MOSFETs are unipolar transistors. In Addition the minority carrier lifetime in a SiC device is magnitudes smaller than in Si.

In SiC the stacking of Si and C layers can vary and form different polytypes. A polytype is a particular case of polymorphs, where closed-packed planes are identical in two dimensions, but differ in the third dimension regarding the stacking sequence. There are a number of different SiC polytypes. Not all of them are stable and are therefore not relevant for the semiconductor industry. One of the stable ones is 4H-SiC, which is the polytype with the widest band gap (E_{gap}= 3.26 eV) and a high electron mobility, which makes it very attractive for n-MOSFETs. In this crystal configuration, Si and C

layers are alternately stacked in a hexagonal arrangement (H). Each Si atom is covalently bonded to four C atoms with a binding energy $E_B = 4.6$ eV. This hexagonal stacking of SiC is shown in Figure 2.1.1. There are two different stacking possibilities: ABCB or ABAC. Both start to repeat after four layers (4), hence it is called 4H-SiC.

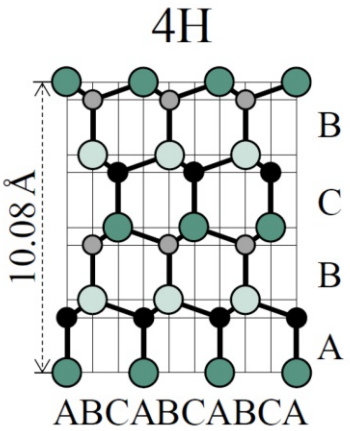


Figure 2.1.1: Stacking order of 4H-SiC. Si-atoms are depicted in green and light green, whereas C-atoms are shown in black and grey [6]

.

The electric band structure depends on the periodicity of the atoms in the lattice. Since the periodicity changes with different polytypes, their band structure differs as well. This leads to different properties in the electric device behavior.

Table I compares 4H-SiC to Si regarding band gap, electron and hole mobility, critical field and thermal conductivity.

Table I: Key constants of 4H-SiC and silicon [7, 8, 9].

Quantity	**4H-SiC**	**Silicon**
band gap E_G (eV)	3.26	1.12
electron mobility μ_e ($cm^2\ V^{-1}\ s^{-1}$)	1000	1400
hole mobility μ_h ($cm^2\ V^{-1}\ s^{-1}$)	115	471
critical field ξ_c ($MV\ cm^{-1}$)	2.2	0.3
thermal conductivity Θ ($W\ cm^{-1}\ K^{-1}$)	3.7	1.5
intrinsic carrier concentration n_i ($cm^{-}3$)	5×10^{-9}	1.8×10^{10}

2.1.1 Native Oxide of SiC

When producing a MOSFET it is essential to isolate the gate contact from the substrate to prevent leakage currents. Silicon dioxide (SiO_2) takes on this role as an dielectric layer between gate and bulk. In Figure 2.1.2 the band structure of SiO_2, which is the native oxide of SiC, is shown in relation to the band structure of SiC. Since the band gap of SiO_2 reaches 9 eV it is a gate insulator in a MOSFET.

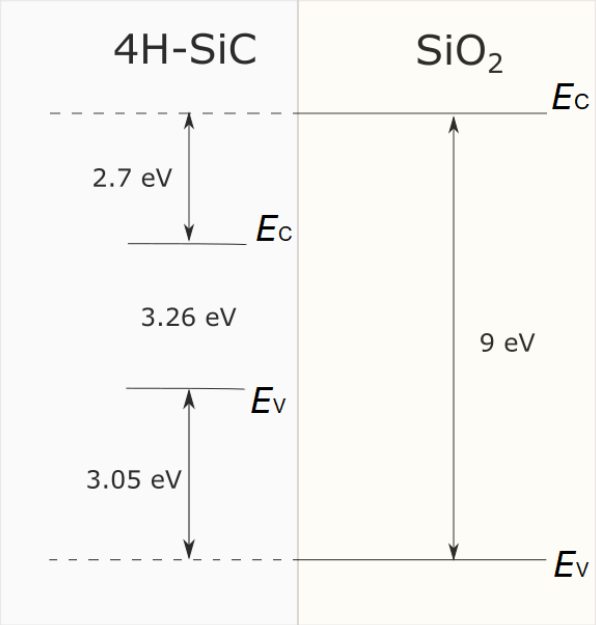


Figure 2.1.2: Band gap of SiC and SiO_2. The band gap width of SiC is 3.26 eV, whereas SiO_2 has a band gap of 9 eV. The band gap of SiC lies 3.05 eV above the bound state and 2.7 eV below the vacuum level.

2.2 Defect States

In an ideal crystal every atom sits perfectly on one lattice site. In case there is a deviation from the perfect crystal lattice, one talks about a defect. During MOSFET production, point defects dominate. They cause localized perturbations, which might lead to undesired electric behavior in the device. As shown in Figure 2.2.1, there are intrinsic point defects such as vacancies or self-interstitials and also extrinsic point defects, where impurities sit on interstitial sites or occupy substitutional lattice sites.

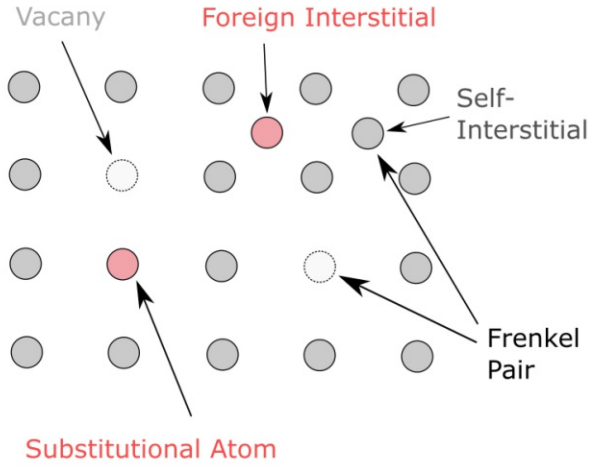


Figure 2.2.1: Point defects such as vacancies, self-interstitials, foreign-interstitials and substitutional atoms. If an interstitial defect and a vacancy are close to each other, they are called a Frenkel pair.

These imperfections in the crystal lattice can introduce additional electric energy states that might lie in the semiconductor's band gap. Depending on their energetic position defects can be subdivided into two categories: shallow levels and deep levels. Shallow levels lie close to the band edges (valence band or conduction band) and can be ionized easily, whereas deep levels are positioned in the middle of the band gap, trapping carriers in compact, localized states [10].

2.2.1 Shallow and Deep Levels

Shallow levels are located close to the valence band (acceptor states) and the conduction band (donor states). The vicinity to the band edges causes them to be ionized at room temperature, which leads to a generation of free carriers. When doping a semiconductor with impurities, usually shallow levels are created to form n-doped and p-doped areas [10].

Compared to the above mentioned dopant levels, one refers to deep traps when the energy of the traps lies in the middle of the band gap and therefore their binding energy for holes and electrons is fairly high. These deep traps can be created by dislocations in the lattice or by the implantation of donor and acceptor atoms on interstitial sites in the lattice. Deep traps can assist in the recombination process of electrons and holes in a semiconductor. Transitions from the conduction band E_C to the valence band E_V and vice versa are more efficient via the deep trap levels. They have a higher ionization

energy and hardly contribute to the free charge carriers.

2.3 Doping in SiC

Since a MOSFET consists of a number of pn-junctions to manipulate the current flow through the device, creating these n- and p-conducting areas is essential. This is realized by doping, where atoms that have a different number of valence electrons compared to the atoms in the MOSFET bulk are implanted. During this process there are some collateral effects induced, that can have a negative impact on the device performance. Hence, it is very important to investigate the quality and quantity of the defects created during implantation and whether it is possible to reduce their amount. In literature [11, 12] there are many suggestions on how to measure and eliminate these defect states, that lie in the band gap of SiC. Some of them will be discussed in the following sections.

2.3.1 Devices under Doping

During the MOSFET production the implantation takes place via a mask, hence, it is unavoidable to have under mask depth profiles of implanted dopants, instead of sharp edges between doped and undoped areas. Furthermore, it is possible that not only the implanted regions contain defects, but also the surrounding area might be affected by defect states. Nipoti and Sasaki [13, 14] suggest that with increasing dopant concentration the local planar stacking fault can extend over a major fraction of implanted thickness, when annealing the device.

2.3.2 Post Implantation Annealing

When implanting ions, lattice damage is unavoidable and increases with the implanted number of dopants. Post implantation thermal treatment seems to be an effective method to reduce the lattice damage, since more thermal energy is available to the lattice to reorder itself and increase its lattice periodicity. Furthermore, post implantation thermal treatment can enhance the diffusion of lattice vacancies as well as interstitial atoms and enable them to recombine. This leads to a reduction in trap states that might limit the device performance [15, 16].
Only with post implantation thermal treatment it is possible to electrically activate the

dopant species. The efficiency of this process is enhanced by increasing annealing time and temperature.

However, these temperature treatments provoke collateral effects, like the thermal generation of intrinsic defects (e.g. carbon vacancies v_C and interstitial carbon atoms – also called Frenkel pairs). A carbon rich surface can counteract this process by recombination of these thermally injected carbon atoms with the carbon vacancies. This creates a number of v_C that stays in equilibrium. At high temperatures v_C formation dominates, while at lower temperatures the annihilation of v_C prevails [15, 16].

2.3.3 Doping atoms

A number of atoms is suitable to be placed in substitutional sites in order to change the conductivity in the area around them. For example the implantation of phosphorous (P), nitrogen (N) or arsenic (As) atoms can lead to n-type conductivity, while gallium (Ga), Al or B force p-type conductivity.
Previous studies have shown [12] N and Al to be the most favorable dopants concerning their high solubility limit, low thermal ionization energy and absence of diffusion during post implantation annealing. In addition to that defects related to N and Al implantation barley have an impact on the device performance. In contrast, B as an alternative p-dopant has a higher diffusion constant compared to Al, which can lead to an B escape from the lattice or to an accumulation in undesired areas. Volakov et. al. show that the diffusion constant of B is one magnitude higher than the one of Al at 1700 °C (B: $8 * 10^{-13}$cm/s, Al: $6 * 10^{-14}$cm/s) [17].

2.3.4 Boron and Aluminum as Dopants in SiC

As mentioned, Al can be used as a p-dopant in SiC. Lately, also B was used as a dopant in SiC, which leads to new challenges but also shows advantages compared to Al. B and Al have different physical properties when implanted into SiC. For example, the solubility of Al in SiC is much higher compared to B, which is favorable when a high doping level is desired. However, an advantage of B is its low mass, allowing it to penetrate deeper in the SiC lattice with less damage to the lattice.

Troffer et al. [11] show that less B atoms are incorporated in the SiC lattice due to outdiffusion of B. This is enhanced by elevated temperatures above 1750 °C, which are used to anneal devices in order to heal lattice damages caused during implantation. The diffusion of Al during annealing is much weaker according to Ryu et al. [18]. However, as

Troffer and others show [11, 19, 20, 21], there is a pile up of Al and B at the surface, that might be attributed to the high number of Si and C vacancies near the surface, which are created during the implantation. This vacancy gradient might cause the dopants to migrate to the surface, especially at higher temperatures.

A further aspect to consider is the electrical activity of implanted dopants. The electrical activation of dopants is essential for a high device performance. It strongly depends on annealing temperature, implantation parameters (sample temperature) and outdiffusion of dopants. As B has a higher ionization energy (around 1800 °C [11]) compared to Al, a hot temperature anneal activates more Al than B. As a consequence, to reach the same activation level in B as in Al, higher temperatures are needed. This comes along with an enhanced outdiffusion, as mentioned above. It is desired to find an optimum between out-diffusion and electrical activity.

2.4 SiC Trench MOSFET

An advanced version of a planar MOSFET is the so called trench MOSFET. The cross section of the investigated n-channel SiC trench MOSFET is depicted in Figure 2.4.1. Compared to the planar structure, the gate is inside a trench. Blue areas indicate p-doped regions, while n-doped areas are depicted in yellow/orange. The electrodes are shown in black and gray. Red arrows indicate the n-channel of the device, which is formed when the gate voltage bias is high enough. The trench structure has certain advantages over a planar MOSFET, such as increased channel mobility, as the channel of the trench MOSFET forms along the a-face of the SiC crystal, which reduces conduction losses due to its lattice structure. Further, the gate oxide stress is significantly reduced, which enhances reliability [22].

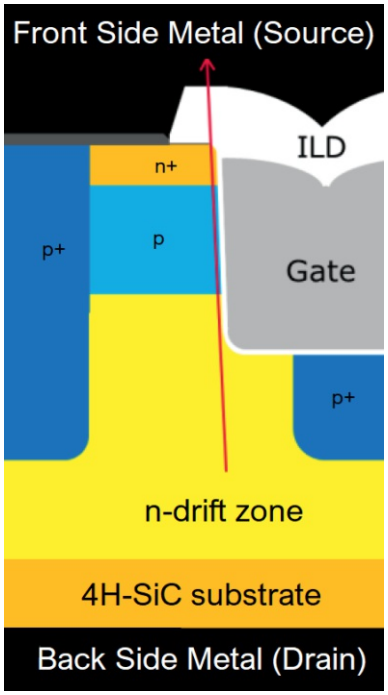


Figure 2.4.1: The cross section of a SiC trench MOSFETs produced by *Infineon Technologies Austria AG* is shown [22]. Black/gray represent electrodes, yellow/orange show n-doped areas and p-doped areas are depicted in blue.

The p-body area, where the n-channel forms, is usually implanted with Al to ensure p-conductivity. The charge behavior of such a MOSFET is explained in Figure 2.4.2 for positive and negative gate voltages. As this thesis investigates the impact of B channel implantation on the device, the Al atoms in the channel area are substituted by B atoms. The tested B implanted devices are not yet technically mature, which might cause an incomplete channel implantation. The result is assumed to be a parasitic junction gate field effect transistor (JFET) without a p-body area, as shown in Figure 2.4.3.

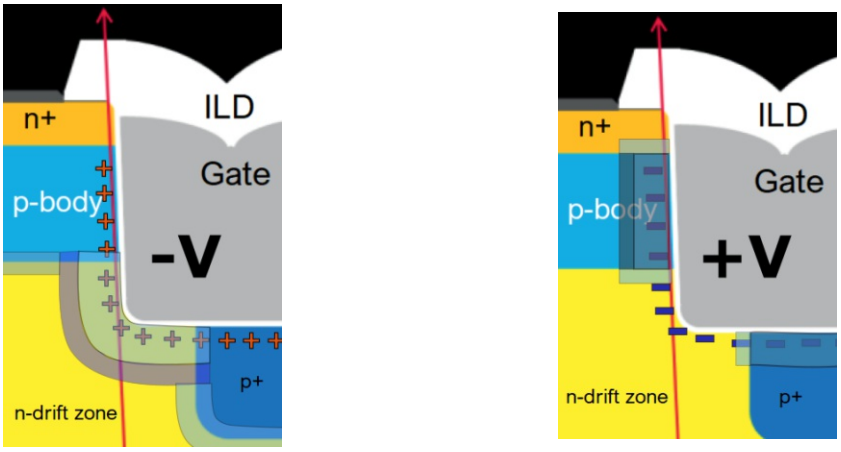


Figure 2.4.2: Zoom of Figure 2.4.1: Cross section of trench area with Al channel implantation. Left: negative gate voltages. Right: positive gate voltages. The transparent blue areas symbolize the space charge region, the transparent dark blue areas show the regions where the space charge region extends, during DLTS or admittance spectroscopy.

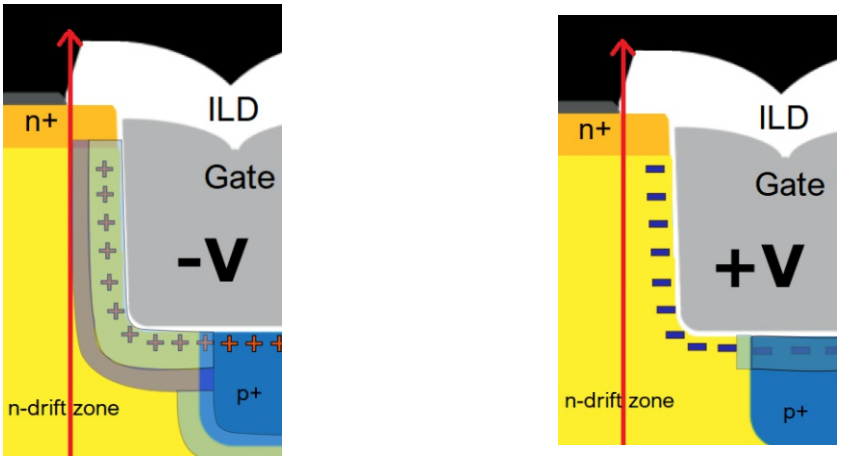


Figure 2.4.3: Zoom of Figure 2.4.1: Cross section of trench area with B channel implantation. It is assumed that the B channel dosage is too low in order to create a p-body area, but rather behaves like the n-drift zone- Left: negative gate voltages. Right: positive gate voltages. The transparent blue areas symbolize the space charge region, the transparent dark blue areas show the regions where the space charge region extends, during DLTS or admittance spectroscopy.

3 Device Characteristics and Room Temperature Measurement Approaches

The following section explains different facets of the MOSFET behavior and the possibilities for device characterization. It might even be possible to deduce facts about defect states.

3.1 Current Voltage Characteristics

The current voltage characteristics can be considered a basic electric characterization of a MOSFET. The drain current is measured while gate or drain voltages are varied. This leads to the transfer characteristics (I_D versus V_G) and the output characteristics (I_D versus V_D).

3.1.1 Transfer Characteristic

When recording a transfer characteristic the gate is swept from accumulation to inversion and vice versa. During this measurement the drain voltage is kept constant at V_D=0.1 V. The threshold voltage V_{th} is extracted when the drain current reaches a certain value (current criterion).
A transfer characteristic can be subdivided into three regimes:

1. $\mathbf{V_G < V_{th}}$**:**
   When the applied gate voltage V_G is smaller than the threshold voltage V_{th}, no current (appart from the diffusion current) flows.

2. $\mathbf{V_G = V_{th}}$**:**
   Only when V_G reaches the threshold voltage V_{th} an inversion layer appears, that is large enough for a significant number of electrons to flow from source S to drain D. In this state the MOSFET is turned on.

3. $V_{\mathbf{G}} > V_{\mathbf{th}}$**:**
   With increasing V_{G}, I_{D} grows as well. If the gate voltage V_{G} is much higher than V_{th}, the drain current saturates.

Figure 7.1.1 illustrates the dependence of I_{D} on V_{G}. The three different regimes accumulation ($V_{\mathrm{G}} < V_{\mathrm{th}}$), depletion ($V_{\mathrm{G}} = V_{\mathrm{th}}$) and inversion ($V_{\mathrm{G}} > V_{\mathrm{th}}$) are depicted. The difference between up and down sweep in Figure 3.1.1 is caused by trapped carriers, that act as additional gate potential. This leads to a small shift in the I_{D}-curve towards more positive gate voltages V_{G}.

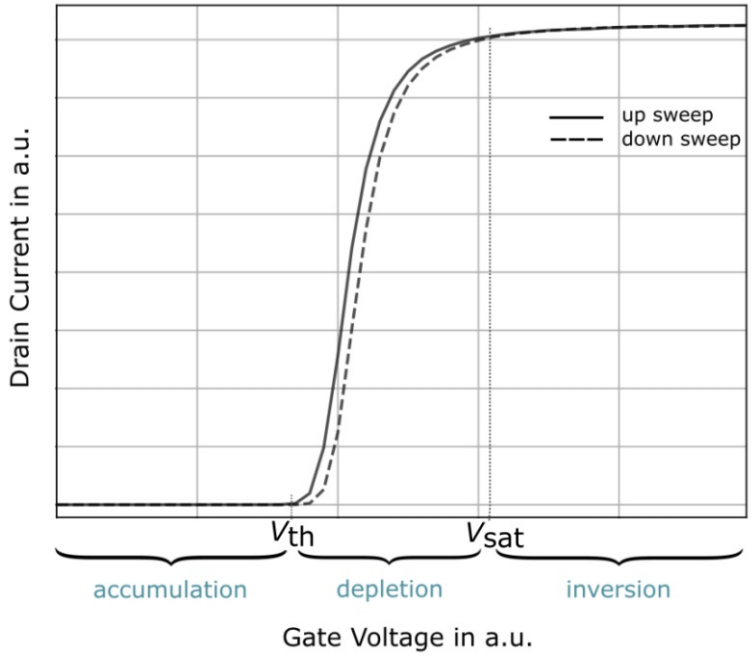


Figure 3.1.1: Transfer characteristic: accumulation ($V_{\mathrm{G}} < V_{\mathrm{th}}$), depletion ($V_{\mathrm{G}} = V_{\mathrm{th}}$) and inversion ($V_{\mathrm{G}} > V_{\mathrm{th}}$)

3.1.2 Temperature dependence of the Threshold Voltage

The threshold voltage V_{th} is a characteristic parameter of a MOSFET that depends on the Fermi level E_{F} in the semiconductor. Since the position of E_{F} is influenced by the temperature T and the number of dopants N_{A}, it directly causes a change in the threshold voltage V_{th}. Sze and Ng [23] provide the necessary formulas to calculate the correlation between the threshold voltage V_{th} and the temperature T for different doping concentrations N_{A}.

The later needed energy difference between E_F and E_i, called ψ_{Bp}, is calculated through

$$\psi_{Bp} = E_F - E_i = kT \ln(n_i/N_A) \tag{3.1.2.1}$$

with n_i being the intrinsic carrier concentration calculated with the standard model for the carrier density of an intrinsic semiconductor.

$$n_i = \sqrt{N_C N_V} \exp(-E_{gap}/2kT) \tag{3.1.2.2}$$

N_C and N_V represent the effective density of states in the conduction and valence band. E_{gap} stands for the energy gap between those two bands. The Fermi energy E_F is determined via

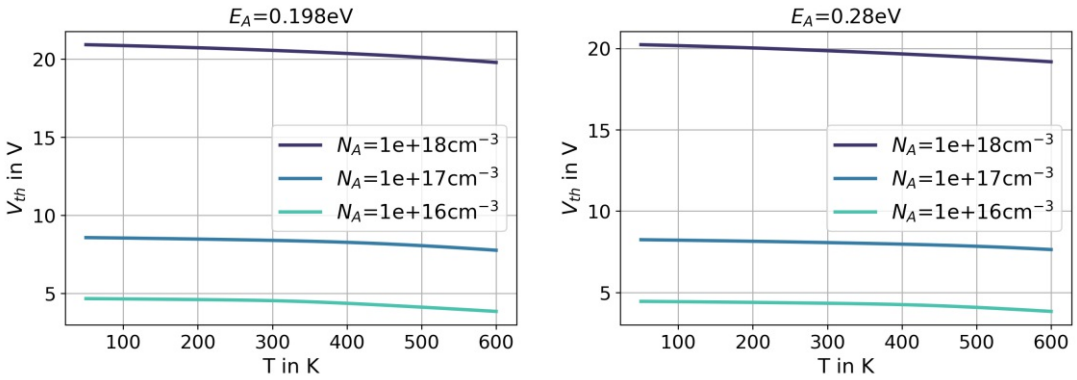
$$E_F = kT \ln(N_V/N_d) \tag{3.1.2.3}$$

where N_d is assumed to be 1×10^{16}. The threshold voltage for a MOSFET is then given by:

$$V_{th} = \frac{\sqrt{4q\epsilon_S \psi_{Bp} N_A}}{C_{ox}} + 2\psi_{Bp} + V_{FB} \tag{3.1.2.4}$$

ϵ_S represents the permitivity of the semiconductor and C_{ox} stands for the oxide capacitance. V_{FB} is the flat band voltage and q symbolizes the elementary charge. N_A and n_i have the following temperature dependency:

The theoretical curves for $V_{th}(T)$ look as shown in Figure 3.1.2 for the case of $E_A = 0.126\,\text{eV}$ (Al) and $E_A = 0.28\,\text{eV}$ (B) [6]. In both cases the threshold voltage decreases over temperature. The higher the doping concentration N_A the higher the threshold voltage. The higher activation energy E_A of B lowers the treshold voltage slightly compared to Al. Since all dopants are already ionized by the applied gate voltage, incomplete ionized dopants do not matter.



(a) $V_{\mathrm{th}}(T)$ for Al

(b) $V_{\mathrm{th}}(T)$ for B

Figure 3.1.2: Calculated $V_{\mathrm{th}}(T)$ for three different doping concentrations N_{A}

.

3.2 Effect of Subthreshold Hysteresis

When sweeping the gate of a MOSFET at a fixed drain current V_{D}=0.1 V from accumulation to inversion and vice versa, a hysteresis in the drain current between up and down sweep can be observed [24]. This hysteresis effect appears due to hole capture in fast trapping interface states during accumulation, which act as additional potential (see Figure 3.2.1). As the gate voltage approaches inversion, captured holes recombine with incoming electrons and the hysteresis effect vanishes.

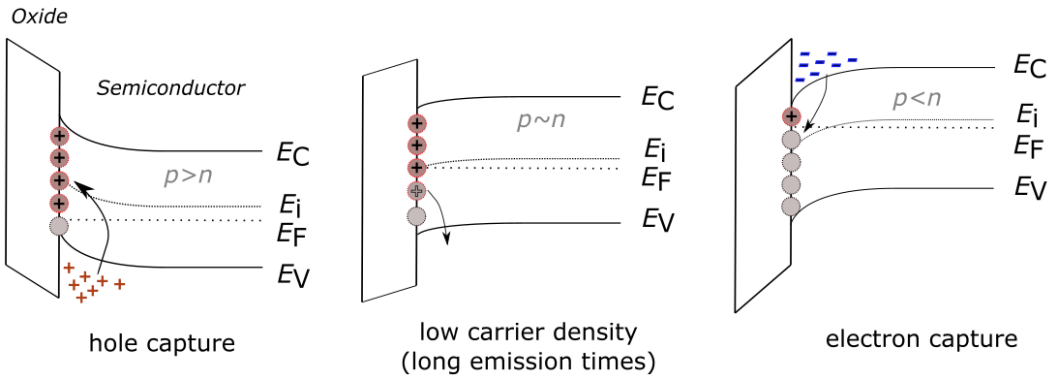


Figure 3.2.1: Mechanism causing subthreshold sweep hysteresis explained with a schematic band diagram. Left: Accumulation leads to hole capture at the interface. Middle: Slow recovery of trapped holes due to few carriers available at the interface. Right: Inversion provides high electron density for recombination process.

The extent of the hysteresis depends on the number of interface states in the inversion channel area and can therefore be taken as a measurement technique to quantify trap states in the channel area. Furthermore, it is to mention that the number of interface states also depends on the relative orientation of the crystal plane to the electron channel. In the subthreshold regime the on-resistance is still in the range of megaohms and the hysteresis effect is most pronounced. As soon as the gate voltage approaches the threshold voltage V_{th}, the hysteresis disappears due to recombination of trapped holes with incoming electrons (see Figure 3.2.2). Even after multiple charging and discharging of the defect states the hysteresis effect remains unchanged and vanishes as soon as V_{th} is reached, which means the hysteresis effect is reversible. Hence, it is harmless to the device performance. It has been suggested that carbon dangling bonds could cause these interface traps, where charges get captured during accumulation [25, 26].

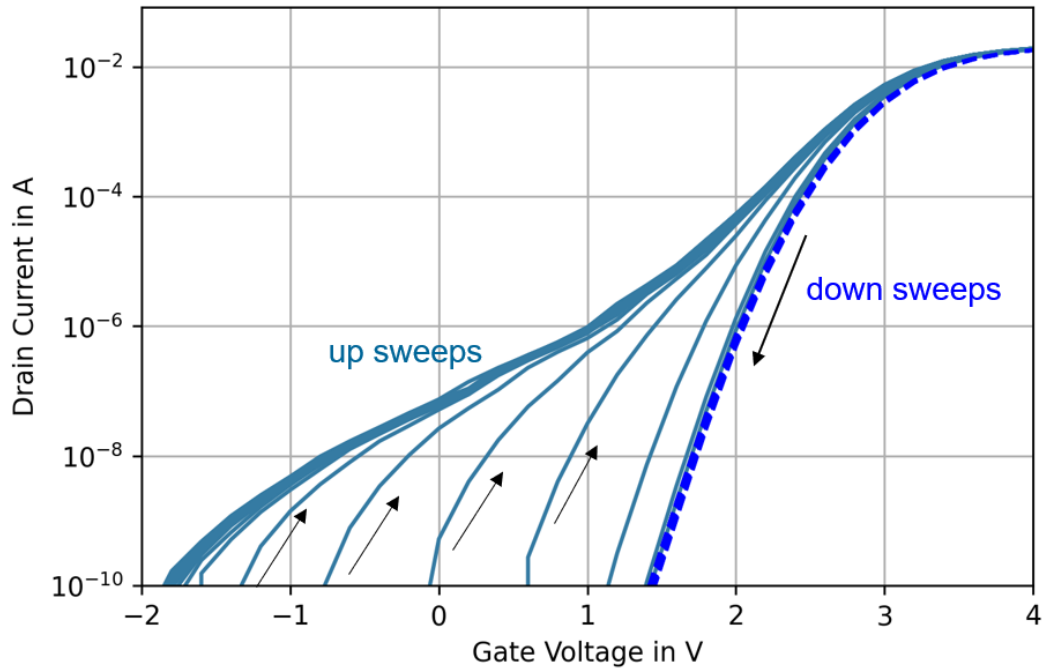


Figure 3.2.2: The subthreshold sweep hysteresis caused by holes trapped in fast interface states during accumulation.

3.3 Determination of Mobility by Ghibaudo Method

The channel mobility in a MOSFET is an important parameter for the device performance. If the carrier mobility in the channel is high, the device can work at a satisfying level.

However, there are defects in or near the channel area, which act as traps or scattering centers for the carriers flowing through. Consequently the mobility in the devices never reaches the bulk electron mobility. This leads to a decrease in the drain current I_D and increased losses.
Hence, it is of considerable interest to determine the carrier mobility in a MOSFET. One method, which is commonly used, was first introduced by Ghibaudo [27]. He suggested to extract the low field carrier mobility μ_0 from the transfer characteristic. In this calculation it is necessary to know the oxide capacitance C_{ox}, the channel width W and the channel length L of the measured MOSFET.
In Ghibaudo's method the drain current I_D in long channel field effect transistor (FET) is assumed as

$$I_D = \frac{W}{L} \cdot C_{ox} \cdot \mu \cdot \left((V_G - V_{th}) V_D - \frac{{V_D}^2}{2} \right) \tag{3.3.0.1}$$

Since the applied drain current I_D is in the range of mA, the last term in Equation 3.3.0.1 becomes negligible. Further it is necessary to replace the mobility μ with a gate voltage independent mobility μ_0, the low field channel mobility. This leads to

$$I_D = \frac{W C_{ox}}{L} \frac{\mu_0}{[1 + \Theta(V_G - V_{th})]} (V_G - V_{th}) V_D, \tag{3.3.0.2}$$

with Θ being the mobility reduction coefficient. Equation 3.3.0.2 can be derived with respect to V_G in order to determine the transconductance g, as shown in Equation 3.3.0.3.

$$g = \frac{W C_{ox}}{L} \frac{\mu_0}{[1 + \Theta(V_G - V_{th})]^2} V_D. \tag{3.3.0.3}$$

When the drain current I_D (Equation 3.3.0.2) is divided by the square root of the transconductance $\sqrt{g}$ (Equation 3.3.0.3) the mobility reduction coefficient Θ can be eliminated and the following relation is obtained:

$$\frac{I_D}{g^{1/2}} = \left(\frac{W C_{ox} \mu_0 V_D}{L} \right)^{1/2} (V_G - V_{th}). \tag{3.3.0.4}$$

From a linear fit of Equation 3.3.0.4 it is possible to extract the low field carrier mobility μ_0 as the slope of a linear fit, which is single valued and V_G independent. The benefits of Ghibaudo's method include the correction for series resistances which can be in the order of ~2 Ω and the consideration of the geometrical components (W and L) of the channel area.

3.4 Capacitance Voltage Characteristics

Capacitance voltage curves ($C(V)$-curves) can be another option to determine the device behavior. Since, trap states in the depletion region of a MOSFET have an impact on the capacitance they become visible in the $C(V)$-curves. The following chapters are based on the works of Sze and Nicollian [23, 28].

3.4.1 MOS Capacitance

Considering a MOS structure, as depicted in Figure 3.4.1, one can understand this structure as a capacitance with the metal and the semiconductor as the two electrical conductors with the oxide in between as the dielectric. The band diagram of such a MOS structure is depicted in Figure 3.4.2.

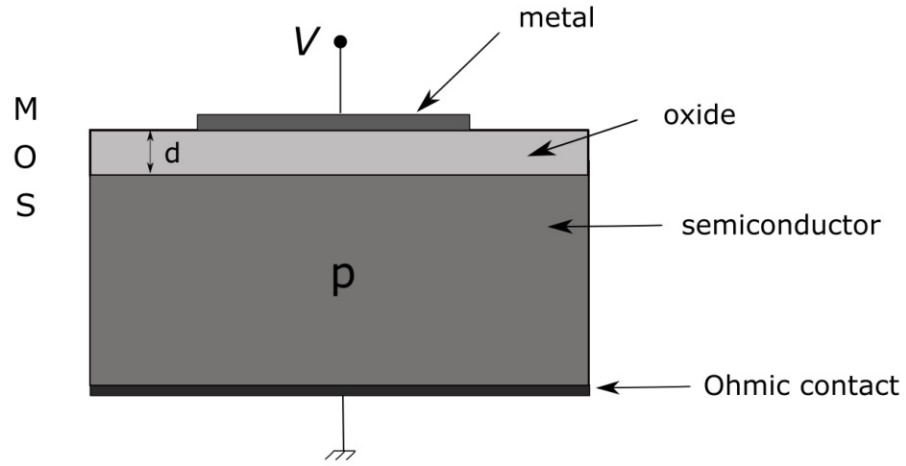


Figure 3.4.1: MOS structure as a capacitor with the metal contact, the oxide as a dielectric with the thickness d and the p-semiconductor.

The potential $\Phi_{\mathrm{p}}(x)$ is assumed as the potential $E_{\mathrm{i}}(x)/q$ in reference to the bulk of the semiconductor.

$$\Phi_{\mathrm{p}}(x) = -\frac{E_{\mathrm{i}}(x) - E_{\mathrm{i}}(\infty)}{q} \tag{3.4.1.1}$$

$E_{\mathrm{i}}(x)$ describes the intrinsic Fermi level at the distance x from the interface and $E_{\mathrm{i}}(\infty)$ at infinity. The surface potential Φ_{S} is defined as $\Phi_{\mathrm{p}}(0)$, as shown in Figure 3.4.2. Φ_{Bp} can be determined by $\Phi_{\mathrm{Bp}} = E_{\mathrm{i}} - E_{\mathrm{F}}$. There are different regions of the surface potential that can be subdivided into:

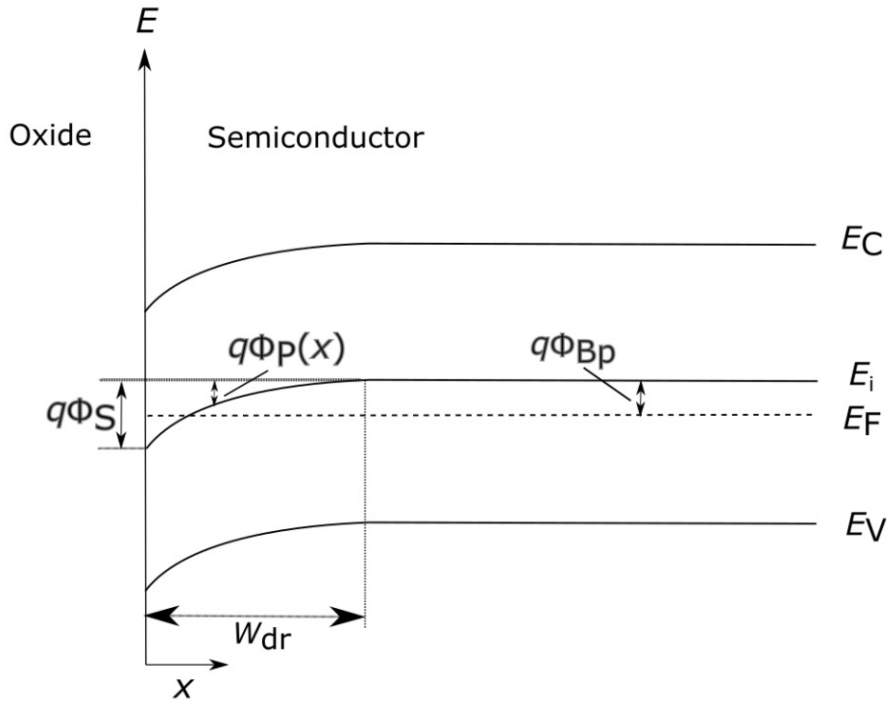


Figure 3.4.2: Band diagram with the surface potential Φ_S, Φ_p and Φ_{Bp}.

$\Phi_S < 0$:	accumulation
$\Phi_S = 0$:	flat-band
$\Phi_{Bp} > \Phi_S > 0$:	depletion
$\Phi_{Bp} = \Phi_S$:	$E_F = E_i(0)$ (Fermi-level at midgap)
$2\Phi_{Bp} > \Phi_S > \Phi_{Bp}$:	weak inversion
$\Phi_S > 2\Phi_{Bp}$:	strong inversion

Another important parameter, when talking about a MOS capacitance, is the space-charge density Q_S. It correlates with the surface potential. Hence, when $\Phi_S = 0$ also $Q_S = 0$. In strong inversion $Q_S \propto e^{q\Phi_S/(2kT)}$ and the surface potential results in:

$$\Phi_S \propto 2\Phi_{Bp} \propto 2\frac{kT}{q}\ln(N_A/n_i) \tag{3.4.1.2}$$

Figure 3.4.3 shows the variation of the space-charge density Q_S in dependence on the surface potential $\Phi_S(V)$.

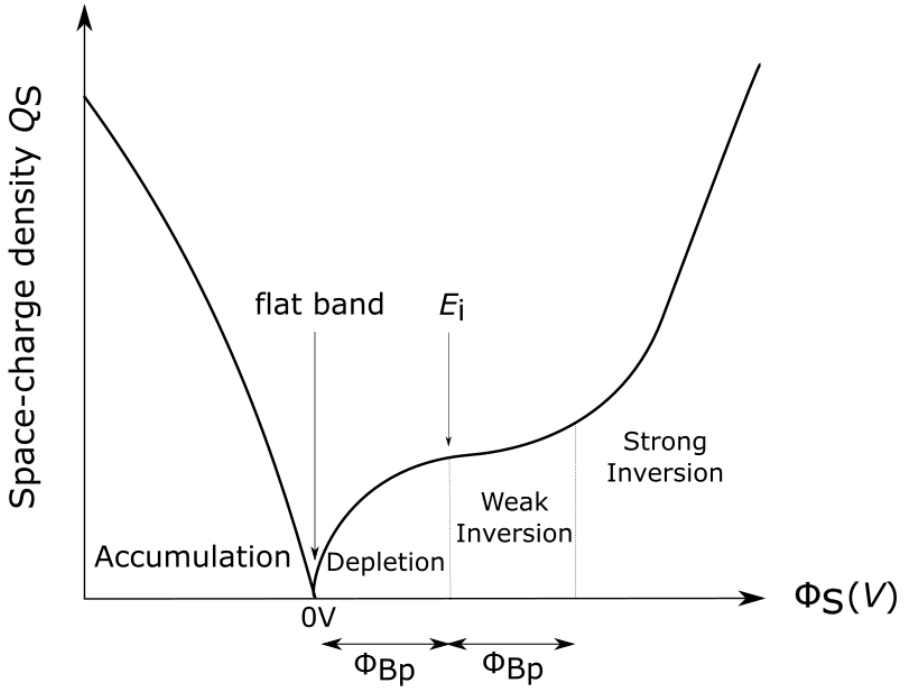


Figure 3.4.3: Space-charge density Q_S depending on the surface potential $\Phi_S(V)$. With increasing bias voltage Q_S decreases until a minimum is hit at V_{FB}. At this point the space-charge density Q_S equals zero. From there on Q_S starts to increase again.

Figure 3.4.4 shows the ideal band diagram when in strong inversion. The correlating charge distribution is also shown. The electric field as well as the potential can be calculated using the Poisson equation. They are also depicted here. The total potential consists of the voltage across the oxide with the thickness d and the surface potential: $V = V_{ox} + \Phi_S$.

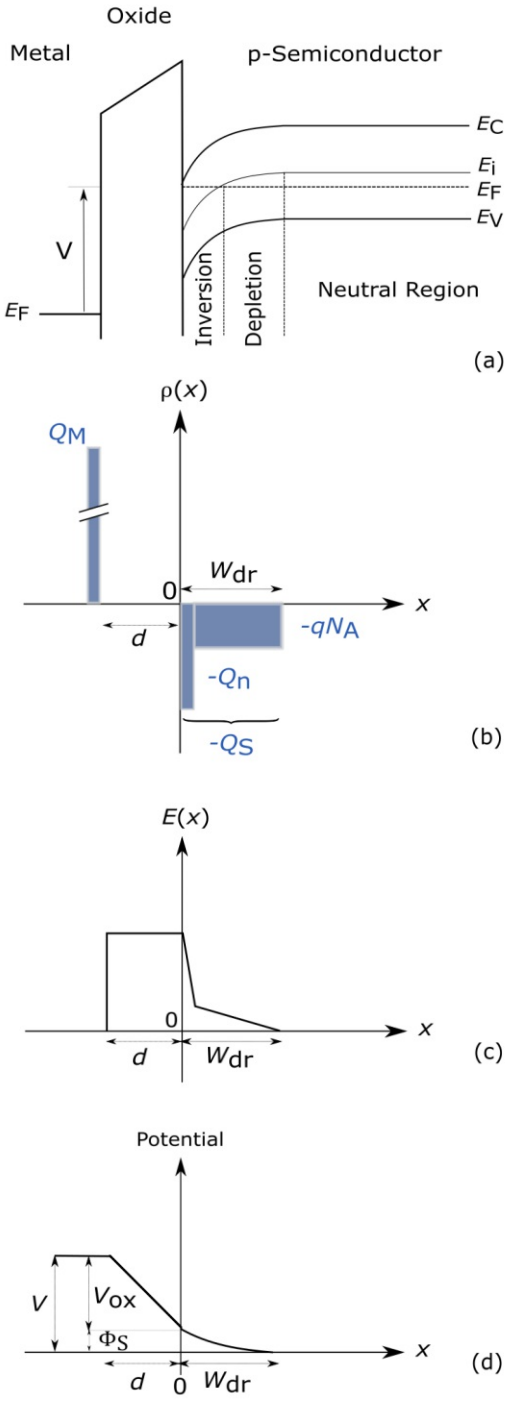


Figure 3.4.4: MOS behavior: (a) shows the band diagram of a MOS structure in strong inversion, (b) visualizes the corresponding space-charge density over the distance x from the interface, (c) depicts the electric field distribution and (d) shows the potential distribution.

When looking at the total capacitance of the system one observes that it is a series combination of the insulator capacitance C_{ox} and the depletion-layer capacitance C_{dr}.

$$C = \frac{C_{\mathrm{ox}} C_{\mathrm{dr}}}{C_{\mathrm{ox}} + C_{\mathrm{dr}}} \tag{3.4.1.3}$$

While C_{ox} is constant, the semiconductor capacitance C_{dr} is a function of the bias voltage as well as the measurement frequency. The biggest difference occurs at high frequencies, since the charge carriers cannot follow the measurement signal anymore. This is discussed in greater detail later on. As Figure 3.4.5 shows, in accumulation the normalized capacitance is high and almost reaches the level of the oxide capacitance C_{ox}. When increasing the applied voltage to the flat-band voltage ($V = 0$), the capacitance decreases. With increasing bias voltage the capacitance decreases further since the depletion region width grows.

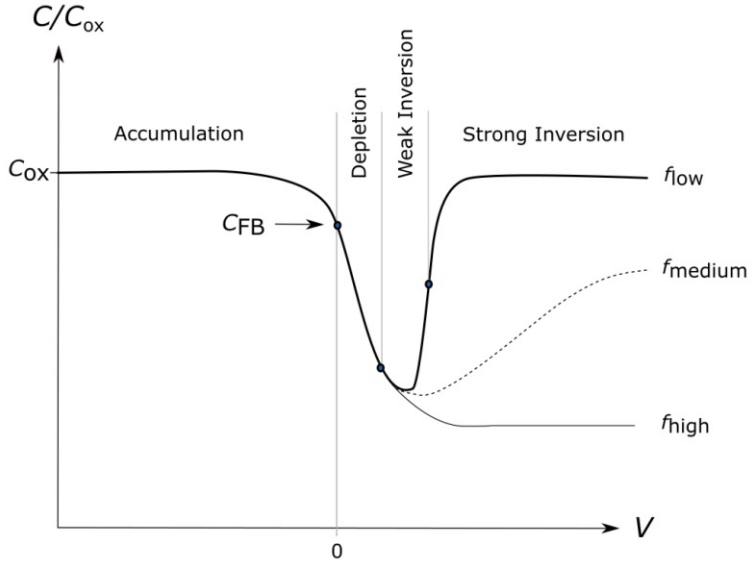


Figure 3.4.5: Ideal Capacitance-Voltage-curves: The CV-curve varies depending on the measurement frequency of the signal.

3.4.2 Frequency Dependence of the Capacitance Voltage Curve

The depletion width widens with rising positive voltages, which reduces the capacitance until a minimum is reached. At that point the previously formed inversion layer stops the electric field from penetrating further into the semiconductor. If a high frequency signal is used, the generation and recombination of minority carriers cannot follow the

fast signal anymore and the capacitance remains at that level even when the bias voltage is increased. In this case the incremental charge is added at the depletion region edge. When applying a low frequency signal the capacitance starts rising again with higher voltages. The incremental charge is no longer added at the depletion region edge but at the inversion layer leading to a capacitance increase. Figure 3.4.6 depicts the charge density in a MOS structure for low and high frequencies, as well as for high frequencies with a fast sweep rate.

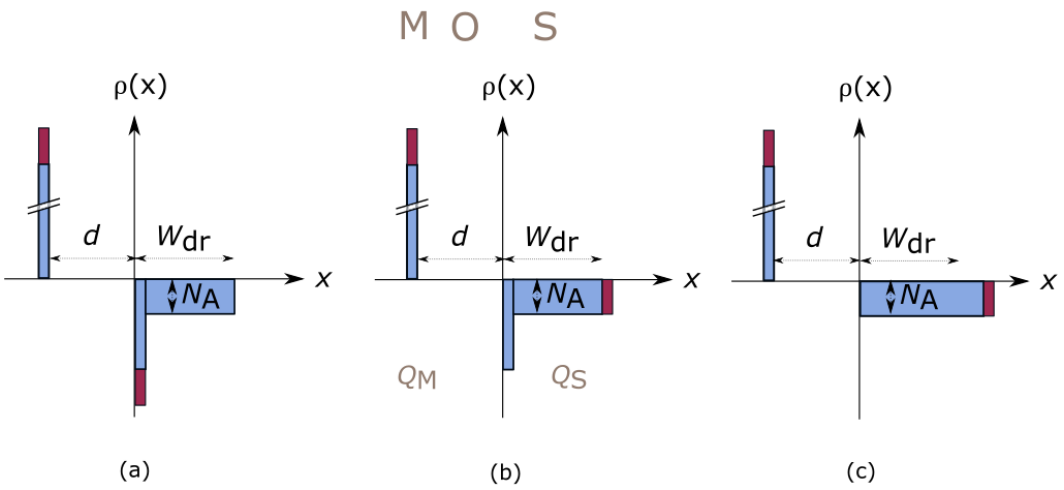


Figure 3.4.6: In the case of strong inversion, the capacitance is strongly frequency dependent. The red area symbolizes the incremental displacement charge for (a) low frequency. (b) high frequency and (c) fast sweep rate and high frequency.

3.4.3 Traps in MOS Capacitors

Since the energy states of traps and oxide charges in the semiconductor-insulator-interface may lie within the band gap of SiC, they can have an impact on the ideal MOS characteristic.

When applying a voltage the Fermi-level is moved which leads to a change in the occupation of the interface traps. This causes the CV-curves to stretch out towards more positive voltages in case of acceptor like traps. Due to the charges trapped at the interface states more voltage is needed in order to reach the same surface potential. This situation is shown in Figure 3.4.7. Hence, it is possible to measure the impact of trap levels on the capacitance and thereby deduce the number of trap states and their energy levels. The different measurement techniques to do so are discussed in the following sections.

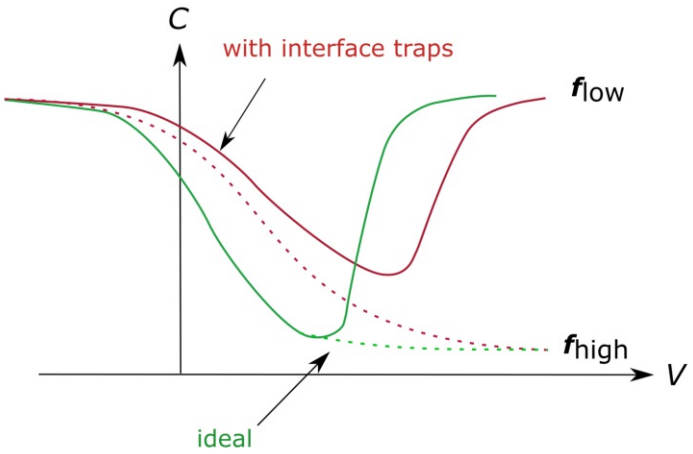


Figure 3.4.7: The ideal CV-curves are depicted in green for low and high frequencies, whereas the CV-curves of a MOS capacitance with trap states are represented by the red lines, as well for low and high frequencies.

4 Cryogenic Measurement Methods

The following measurement techniques are performed at a wide temperature range, starting from cryogenic temperatures up to room temperature.
In order to highlight the differences between the well established methods (DLTS and Drain Current - Deep Level Transient Spectroscopy (ID-DLTS)) and admittance spectroscopy each method is explained in detail and comparisons will be drawn.

4.1 DLTS - Deep Level Transient Spectroscopy

Deep Level Transient Spectroscopy (DLTS) is a powerful measurement technique to characterize trap states in the band gap of semiconductors. It was first introduced by Lang [29] to evaluate the trap state concentration, their binding energy and their trapping rate. Since then many variations of DLTS have evolved. The basic concept of a DLTS measurement as well as the Drain Current - Deep Level Transient Spectroscopy (ID-DLTS) measurement will be explained in the following sections.

4.1.1 DLTS - Capacitance Measurement

When talking about DLTS one usually refers to the capacitance transient measurement, not to confuse with ID-DLTS, which is discussed in the following section. For the purpose of this thesis, the MOSFET is considered a capacitor, as explained above. Since the width of the depletion region W_{dr} depends on the applied voltage V_{ext} (Equation 4.1.1.1) also the capacitance C changes accordingly with an external bias V_{ext} (Equation 4.1.1.2).

$$W_{\mathrm{dr}} = \sqrt{\frac{2\epsilon\epsilon_0}{qN_{\mathrm{A}}}(V_{\mathrm{D}} - V_{\mathrm{ext}})} \tag{4.1.1.1}$$

$$C = \frac{\epsilon\epsilon_0 A}{W_{\mathrm{dr}}} = A^2\sqrt{\frac{\epsilon\epsilon_0 q N_{\mathrm{A}}}{2(V_{\mathrm{D}} - V_{\mathrm{ext}})}} \tag{4.1.1.2}$$

The boundaries of the depletion region are basically extended with increasing external voltage V_{ext}. Hence, when measuring the capacitance C versus the external voltage

V_{ext} one obtains information about the trap state concentration in the area where the depletion region extends and carriers are trapped. An external voltage pulse can fill traps with charges. The relation between the capacitance transient $C(t)$ and the equilibrium capacitance $C_{equil.}$ is proportional to the number of traps N_T.

4.1.2 Recombination via Deep Traps

Deep traps that are measured during a DLTS measurement assist carrier transitions between conduction band E_C and valence band E_V. The Shockley-Read-Hall Model (Figure 4.1.1) describes the generation and recombination processes involved in these transitions [30], see Figure 4.1.1.

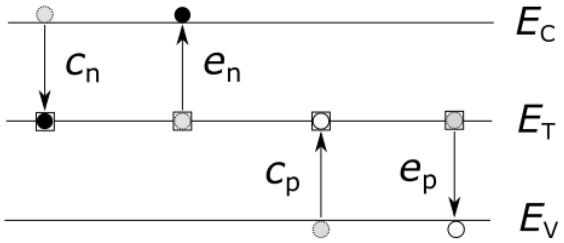


Figure 4.1.1: Shockley Read Hall Modell: Capture c and emission e of electrons n and holes p. Transitions between valence band E_V and conduction band E_C via trap states E_T. Black circles symbolize electrons, white ones stand for holes. The gray shaded circles show the previous state of the electron / hole.

The thermal emission (e) and capture (c) of electrons (n) and holes (p) can be calculated in case the thermal velocity of the carriers ($< v_{th\ n} >$ and $< v_{th\ p} >$), the capture cross sections (σ_n and σ_p) and the effective density of states in the conduction and valence band (N_C and N_V) are known.

Emission:

$$e_n = \sigma_n < v_{th\ n} > N_C \exp((E_T - E_C)/kT) \tag{4.1.2.1}$$

$$e_p = \sigma_p < v_{th\ p} > N_V \exp((E_V - E_T)/kT) \tag{4.1.2.2}$$

Capture:

$$c_n = \sigma_n < v_{th\ n} > N_C \exp((E_F - E_C)/kT) \tag{4.1.2.3}$$

$$c_{\mathrm{p}} = \sigma_{\mathrm{p}} < v_{\mathrm{th\ p}} > N_{\mathrm{V}} \exp((E_{\mathrm{V}} - E_{\mathrm{F}})/kT) \tag{4.1.2.4}$$

Since each trap level has characteristic capture and emission rates for holes and electrons, it is possible to distinguish different defect states. This concept is used not only for the here described DLTS measurement, but also for ID-DLTS and admittance spectroscopy.The probability for a trap to be filled can be described by the Fermi-Dirac-Statistic (Equation 4.1.2.5). Further it is possible to describe the electron occupancy n_{T} of a defect state N_{T} over time t after the fill pulse ended (Equation 4.1.2.6).

$$P = \frac{1}{1 + \exp(\frac{E_{\mathrm{C}} - E_{\mathrm{F}}}{kT})} \tag{4.1.2.5}$$

$$n_{\mathrm{T}}(t) = N_{\mathrm{T}} \exp(-e_{\mathrm{n}} t) \tag{4.1.2.6}$$

4.1.3 Capacitance Transients

Since free carriers are trapped during the forward pulse and are therefore missing in the areas next to the depletion region, the width of the depletion region increases temporarily. Hence, as shown in Equation 4.1.1.1 the capacitance decreases at that time. After the external voltage pulse is over the trapped carriers can escape from the traps via thermal emission and move back to their equilibrium position outside the depletion region. When this process is finished, the depletion region reaches its initial width again. Therefore, DLTS can detect capture and emission processes of charges. The capacitance over time $C(t)$ can be written as

$$C(t) = C_{\mathrm{equil.}} - \Delta C \exp(\frac{t}{\tau}) \tag{4.1.3.1}$$

where $C_{\mathrm{equil.}}$ represents the equilibrium capacitance, which means, the capacitance of the capacitor before the external pulse and after the pulse when all trapped carriers are emitted again. τ stands for the emission time given by $\tau = \frac{1}{e_{\mathrm{n}}}$, e_{n} being the emission rate of electrons. During the emission process the capacitance is measured and one obtains a capacitance transient.

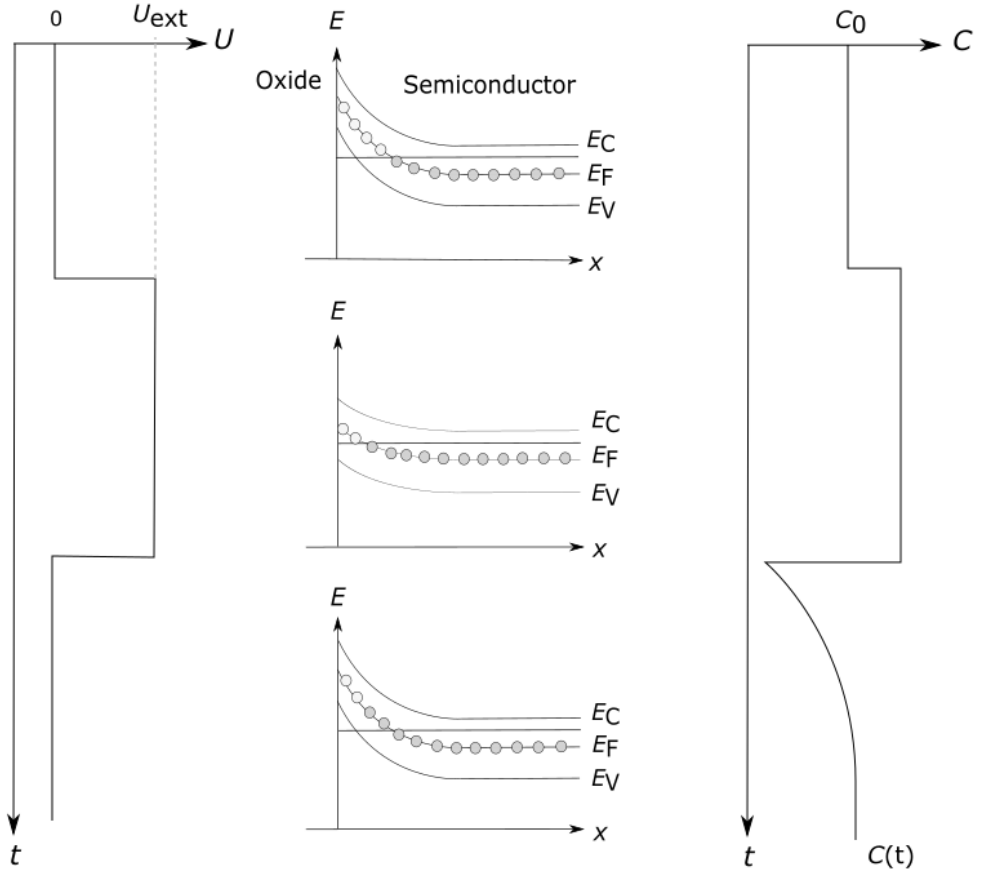


Figure 4.1.2: External voltage pulse V_{ext}, band model and capacitance $C(t)$ during DLTS measurement

Figure 4.1.2 illustrates the DLTS measurement process. On the left hand side the applied voltage pulse V_{ext} over time during a DLTS measurement is shown. In the middle the corresponding band models are depicted, where the charging of traps is visualized. On the right hand side one can see the capacitance over time during the measurement process.

The emission rate e_{n} of the trapped carriers is temperature dependent, since the captured electrons are thermally excited into the conduction band E_{C} and can move outside the depletion region again. For this reason a DLTS measurement is always performed in a wide temperature range. Furthermore, it is possible to determine the mean apparent activation energy $E_{\text{t}} = E_{\text{C}} - E_{\text{T}}$ of the emission process for a specific trap level at the mean energy E_{T}.

4.1.4 Boxcar - Method

The simplest method to extract the activation energy of the trapped carrier process is the so called *Boxcar-Method* first introduced by Lang in 1974 [31]. One evaluates the capacitance at two different times t_1, t_2 in the measurement phase for different temperatures T (Figure 4.1.3):

$$D = C(t_2) - C(t_1) \tag{4.1.4.1}$$

The time interval $[t_1, t_2]$ (also called the rate window) is used to calculate the DLTS peak. Figure 4.1.3 visualizes the determination of a DLTS peak. At low temperatures the capture and emission processes are slow, leaving the capacitance C in the rate window almost unchanged. At higher temperatures capture and emission times decrease and the difference in capacitance between t_1 and t_2 increases. At a certain temperature ($T_{\max}$) the difference $C(t_2) - C(t_1)$ reaches a maximum. As temperature increases further, time constants become very small, which results in a fast capture and emission processes. The capacitance change in the rate window decreases again.

By varying the rate window the temperature $T_{\max}$ is changing as well. Since every trap state has its characteristic capture and emission rate for carriers, different peaks in the DLTS spectrum will occur. Consequently individual trap levels can be detected by analyzing the position and the height of the peak. It is important to note that if the number of traps N_{T} is too high, the capacitance transients cannot be described by an exponential functions anymore and this DLTS method must not be used then.

4.2 Admittance Spectroscopy

The admittance spectroscopy is an electrical measurement technique used to explore traps and dopants in the space charge region of a device. It resembles DLTS concerning the arising effects during measurement. The prominent difference between those two methods is the cause for traps to change occupancy. During a DLTS measurement, a voltage pulse disturbs the equilibrium position, whereas in an admittance spectroscopy an applied AC signal periodically changes the trap occupancies in the space charge region.

This measurement technique is based on a capacitance C and a conductance G recording at different temperatures while frequency sweeps of an applied signal are performed. Since the capacitance C and the conductance G are influenced by defect states N_{T}, it is

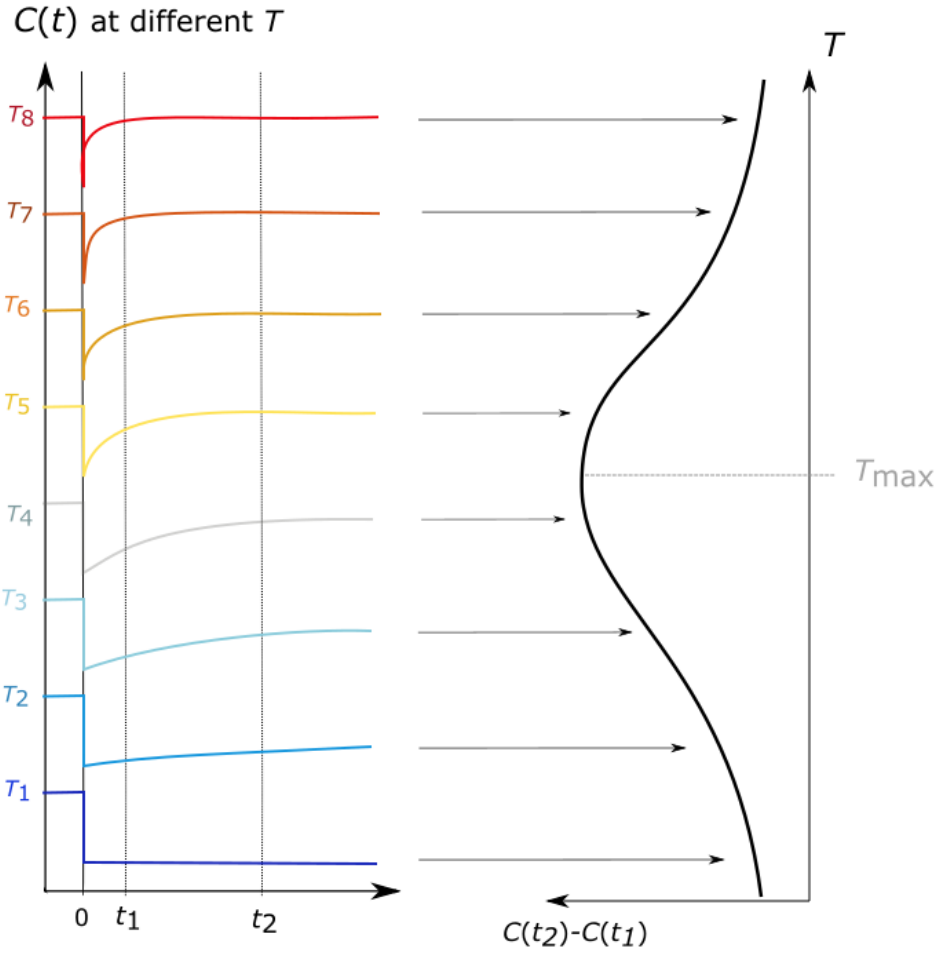


Figure 4.1.3: Capacitance transients for different $C(t)$ and increasing temperatures $T_1 < T_2 < T_3 < ... < T_8$ and the resulting DLTS-Peak.

possible to determine certain trap parameters, such as activation energy or capture cross section.

4.2.1 Definition of Admittance

The admittance $\underline{Y}$ is defined as the reciprocal of the impedance $\underline{Z} = \frac{dV}{dI} + jX$:

$$\underline{Y} = \frac{\mathrm{d}I}{\mathrm{d}V} + jB \tag{4.2.1.1}$$

The conductance is defined as the real part of the admittance $\underline{Y}$:

$$G = \mathfrak{Re}(\underline{Y}) = \frac{\mathrm{d}I}{\mathrm{d}V} \tag{4.2.1.2}$$

It is possible to determine $\underline{Y}$ by adding a signal to the applied gate voltage.

$$V_{\mathrm{Gate}}(t) = V_{\mathrm{ext}} + V_{\mathrm{AC}} \exp(j\omega t) \tag{4.2.1.3}$$

An applied gate voltage leads to the charging of defect states near the interface following the Fermi statistics. If a signal with period τ and small amplitude is added, the occupancy probability changes periodically in the area around the Fermi energy. In case capture and emission constants are in the same range as the period of the signal, charging and discharging of defect states is measurable. The resulting current, which has a phase shift of ϕ compared to the AC signal, is measured.

$$I(t) = I_0 + I_{\mathrm{AC}} \exp(j(\phi + \omega t)) \tag{4.2.1.4}$$

4.2.2 Change in Signal due to Interface Traps

As Nicollian describes [28], at almost all frequencies an energy loss is caused by capture and emission of carriers. The exceptions are the very lowest frequency where all traps immediately respond to the signal and the very highest frequency where no interface trap response is found. The reason for an energy loss at all other frequencies is that on both halves of the AC cycle electrons can be captured by interface traps and emitted again. These processes need energy that is taken from the signal source and can be measured as a parallel conductance. Furthermore, interface traps can store charge for a certain time and hence, lead to a change in capacitance that correlates with the interface trap level density.

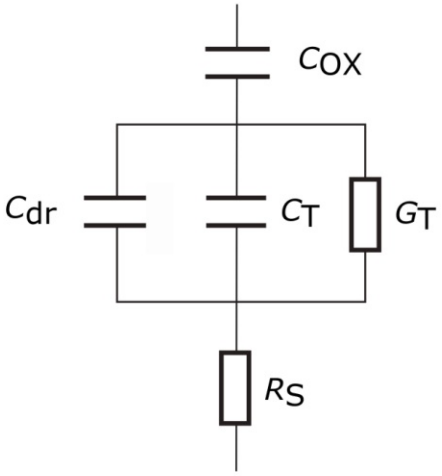


Figure 4.2.1: The equivalent circuit for the Metal Oxide Semiconductor (MOS) response to the signal consists of the oxide capacitance C_{ox}, the capacitance of the depletion region C_{dr}, the trap capacitance C_{T}, the trap conductance G_{T} and a series resistance R_{S}.

The equivalent circuit that describes the MOS response to the signal is depicted in Figure 4.2.1. The capacitance of the depletion region C_{dr}, the trap capacitance C_{T} and the trap conductance G_{T} are in parallel [28]. According to Nicollian [28] the parallel capacitance C_{P} can be described as:

$$C_{\mathrm{P}} = C_{\mathrm{T}}(1 + (\omega\tau)^2)^{-1} + C_{\mathrm{dr}} \tag{4.2.2.1}$$

The parallel conductance (G_{T}=G_{P}) behavior changes in dependence on $\omega\tau$:

$$G_{\mathrm{P}}/\omega = C_{\mathrm{T}}\omega\tau(1 + (\omega\tau)^2)^{-1} \tag{4.2.2.2}$$

With the parallel admittance $Y_{\mathrm{P}} = G_{\mathrm{P}} + j\omega C_{\mathrm{P}}$ the total impedance Z can be written as:

$$Z = \frac{G_{\mathrm{P}}}{|Y_{\mathrm{P}}|^2} - j\omega\frac{C_{\mathrm{P}}}{|Y_{\mathrm{P}}|^2} - \frac{j\omega}{C_{\mathrm{ox}}} + R_{\mathrm{S}} \tag{4.2.2.3}$$

As the measured capacitance and conductance one gets:

$$C_{\mathrm{m}} = \frac{\mathfrak{Re}(Z)}{|Z|^2} \tag{4.2.2.4}$$

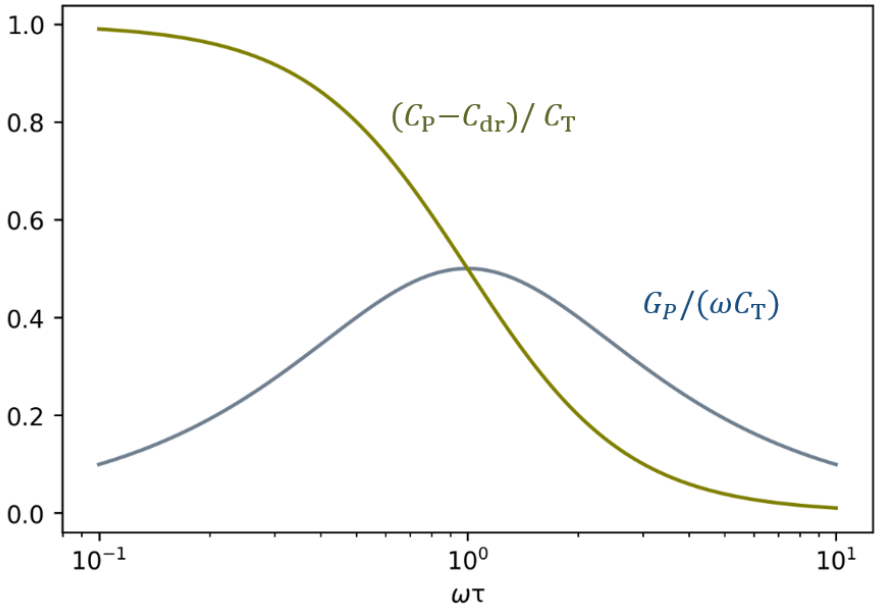


Figure 4.2.2: $(C_\mathrm{p} - C_\mathrm{dr})/C_\mathrm{T}$ and $G_\mathrm{p}/(\omega C_\mathrm{T})$ as a function of $\omega\tau$ for a single level interface trap in depletion [28].

$$G_\mathrm{m} = \frac{\mathfrak{Im}(Z)}{|Z|^2} \tag{4.2.2.5}$$

Figure 4.2.2 shows the capacitance and conductance curve for a single level interface trap. Nicollian [28] states that in case of $\omega\tau \to 0$ there is an immediate change in interface trap occupancy that follows the gate voltage. With increasing $\omega\tau$ interface traps lag behind, since they no longer respond immediately to the gate voltage. As $\omega\tau \to \infty$, the gate voltage causes very little change in the interface trap occupancy. A peak in conductance occurs when $\omega\tau = 1$, since the frequency of the ac signal corresponds to the mean capture time of the traps.

4.2.3 Temperature Dependence of the Capacitance and Conductance

In order to predict the capacitance and conductance over temperature, Vincent [32] considers a diode with traps in the depletion region. His calculations are based on the change in the width of the depletion region due to an additional external signal.
The following approach is similar, but the diode is replaced by a MOSFET and doping atoms are treated as traps.

We consider the depletion region of a MOSFET with a build in potential V_{bi} to which an external bias V_{ext} is applied. The total voltage results in: $V = V_{\mathrm{bi}} + V_{\mathrm{ext}}$. With an additional small voltage change by an AC signal δV_{AC} the depletion region extends by δW_{AC} and the total voltage makes: $V = V_{\mathrm{bi}} + V_{\mathrm{ext}} + \delta V_{\mathrm{AC}}$. The depletion region width W_{dr} can be written as

$$W_{\mathrm{dr}} = \sqrt{\frac{2\epsilon V}{qN_{\mathrm{A}}}} \tag{4.2.3.1}$$

q representing the elementary charge. The band diagrams for the two cases (V=V_{bi}+V_{ext} and V=V_{bi}+V_{ext}+δV_{AC}) are depicted in Figure 4.2.3. One can see the change in the depletion region width δW_{AC}. For dopant activation energies near the valence band one can assume that the change in W_0 equals the change in W_{dr}.

The thereby emitted charge δQ can be calculated as:

$$\delta Q = qN_{\mathrm{A}}^{-} A \delta W_{\mathrm{AC}} \tag{4.2.3.2}$$

with δW_{AC} as the change of the depletion region width caused by δV_{AC} and A the area of the MOSFET. N_{A}^{-} describes the number of ionized acceptors, which contribute to the charge emission.

$$N_{\mathrm{A}}^{-} = \frac{N_{\mathrm{A}}}{1 + g_{\mathrm{A}} \exp\left(E_{\mathrm{A}} - E_{\mathrm{F}}\right)/kT} \tag{4.2.3.3}$$

It is desired to know the change in the depletion region δW_{AC} caused by the additional voltage δV_{AC}:

$$\frac{\delta W_{\mathrm{AC}}}{\delta V_{\mathrm{AC}}} \tag{4.2.3.4}$$

A simple approach is to assume:

$$\frac{\delta W_{\mathrm{AC}}}{W_{\mathrm{dr}}} = \frac{\delta V_{\mathrm{AC}}}{V} \tag{4.2.3.5}$$

From Equation 4.2.3.1 one can deduce:

$$V = \frac{{W_{\mathrm{dr}}}^2 q N_{\mathrm{A}}}{2\epsilon} \tag{4.2.3.6}$$

This can be used in Equation 4.2.3.5, which leads to:

$$\frac{\delta W_{\mathrm{AC}}}{W_{\mathrm{dr}}} = \frac{\delta V_{\mathrm{AC}}}{{W_{\mathrm{dr}}}^2 q N_{\mathrm{A}}/(2\epsilon)} \tag{4.2.3.7}$$

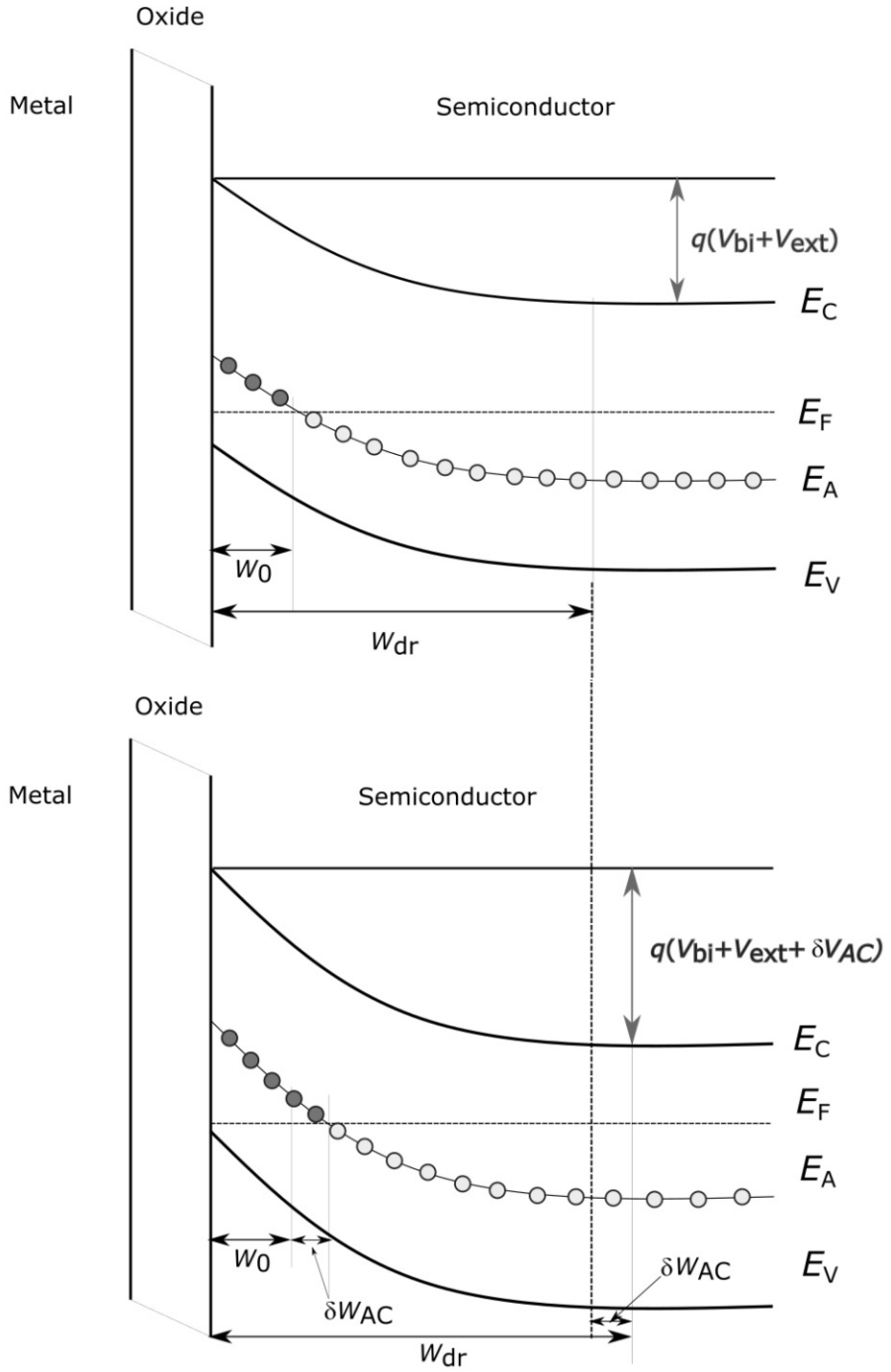


Figure 4.2.3: Band diagram for a MOSFET on top with applied voltage $V{=}V_{\mathrm{bi}}{+}V_{\mathrm{ext}}$ and on bottom with an additional bias $V{=}V_{\mathrm{bi}}{+}V_{\mathrm{ext}}{+}\delta V_{\mathrm{AC}}$. The resulting change in the depletion region width is depicted.

Since $\rho(W_{\mathrm{dr}}) = qN_{\mathrm{A}}$ describes the local density of charge one gets:

$$\delta W_{\mathrm{AC}} = \frac{2\epsilon}{W_{\mathrm{dr}}\rho(W_{\mathrm{dr}})}\delta V_{\mathrm{AC}} \tag{4.2.3.8}$$

Now we assume $\rho(W_{\mathrm{dr}}) = qn$, n being the number of free carriers in the bulk. Using this and Equation 4.2.3.1 and the assumption that $\delta W_{\mathrm{AC}} = \delta W_{\mathrm{dr}}$ one gets

$$\begin{aligned}\delta W_{\mathrm{dr}} =& \frac{1}{\sqrt{\frac{2\epsilon V}{qN_{\mathrm{A}}}}}\frac{2\epsilon}{qn}\delta V_{\mathrm{AC}} \\ =& \frac{1}{n}\sqrt{\frac{2\epsilon N_{\mathrm{A}}}{Vq}}\delta V_{\mathrm{AC}}\end{aligned} \tag{4.2.3.9}$$

The total charge emitted due to the applied voltage δV_{AC} can be described as

$$\begin{aligned}\delta Q &= qN_{\mathrm{A}}^{-}A\delta W_{\mathrm{dr}} \\ &= \frac{qN_{\mathrm{A}}^{-}A}{n}\sqrt{\frac{2\epsilon N_{\mathrm{A}}}{Vq}}\delta V_{\mathrm{AC}} \\ &= \frac{N_{\mathrm{A}}^{-}A}{n}\sqrt{\frac{2\epsilon qN_{\mathrm{A}}}{V}}\delta V_{\mathrm{AC}}\end{aligned} \tag{4.2.3.10}$$

Now it is possible to replace the AC signal δV_{AC} by the actual formula:

$$\delta V_{\mathrm{AC}} = \delta V_0 \exp(j\omega t) \tag{4.2.3.11}$$

The resulting diode current is written as:

$$I(t) = -\frac{\mathrm{d}Q(t)}{\mathrm{d}t} = e_{\mathrm{n}}Q(t) \tag{4.2.3.12}$$

e_{n} stands for the electron emission rate and the charge $Q(t)$ consists of two parts: the charge change caused by the δV_{AC} and the integral of the resulting current.

$$Q(t) = \delta Q(t) - \int_0^t I dt \tag{4.2.3.13}$$

To simplify the following formulas we define

$$\chi = \frac{N_{\mathrm{A}}^{-}A}{n}\sqrt{\frac{2\epsilon qN_{\mathrm{A}}}{V}} \tag{4.2.3.14}$$

In that case $I(t)$ can be expressed as:

$$\begin{aligned} I(t) &= e_{\mathrm{n}}(\delta Q(t) - \int_0^t I\mathrm{d}t) \\ &= e_{\mathrm{n}}(\chi \delta V_{\mathrm{AC}} - \int_0^t I\mathrm{d}t) \\ &= e_{\mathrm{n}}(\chi \delta V_0 \exp(j\omega t) - \int_0^t I\mathrm{d}t) \\ &= e_{\mathrm{n}} \chi \cos(\psi) \delta V_0 \exp(j(\omega t + \psi)) \end{aligned} \tag{4.2.3.15}$$

With the relation

$$\tan(\psi) = \frac{e_{\mathrm{n}}}{\omega} \tag{4.2.3.16}$$

one can determine the two components of the current $I(t)$, one in phase and one in quadrature with δV_{AC}.

$$I_{\mathrm{phase}} = \frac{{e_{\mathrm{n}}}^2 \omega}{{e_{\mathrm{n}}}^2 + \omega^2} \frac{\omega}{e_{\mathrm{n}}} \chi \delta V_0 \exp(j\omega t) \tag{4.2.3.17}$$

$$I_{\mathrm{quad}} = \frac{{e_{\mathrm{n}}}^2 \omega}{{e_{\mathrm{n}}}^2 + \omega^2} \chi \delta V_0 \exp(j(\omega t + \frac{\pi}{2})) \tag{4.2.3.18}$$

For further calculations the electron emission rate e_{n} needs to be known. For acceptor levels close to the valence band it can be determined by

$$e_{\mathrm{n}} = \sigma \langle v_{\mathrm{th}} \rangle N_{\mathrm{V}} \exp(E_{\mathrm{A}}/kT) \tag{4.2.3.19}$$

where σ refers to the capture cross section, $\langle v_{\mathrm{th}} \rangle$ stands for the thermal velocity and N_{V} represents the effective desity of states in the valence band. The activation energy E_{A} needs to be chosen according to the doping atom as shown in Table I.

Table I: Activation energy for different dopants on hexagonal and cubic lattice sites in meV [6]

	Nitrogen	**Almuminum**	**Boron**
hexagonal	61	198	280
cubic	126	201	

$$
\begin{aligned}
C_{\mathrm{T}} &= \frac{1}{\omega}\frac{I_{\mathrm{quad}}}{\delta V_{\mathrm{AC}}} \\
&= \frac{1}{\omega}\frac{{e_{\mathrm{n}}}^2\omega}{{e_{\mathrm{n}}}^2+\omega^2}\chi\delta V_0\exp(j(\omega t+\frac{\pi}{2}))\frac{1}{\delta V_0\exp(j\omega t)} \\
&= \frac{{e_{\mathrm{n}}}^2}{{e_{\mathrm{n}}}^2+\omega^2}\frac{N_{\mathrm{A}}^-}{n}A\sqrt{\frac{2\epsilon q N_{\mathrm{A}}}{V}}
\end{aligned}
\tag{4.2.3.20}
$$

Also the conductance G_{T} of a diode with doping can be calculated with:

$$
\begin{aligned}
G_{\mathrm{T}} &= \frac{I_{\mathrm{phase}}}{\delta V_{\mathrm{AC}}} \\
&= \frac{{e_{\mathrm{n}}}^2\omega}{{e_{\mathrm{n}}}^2+\omega^2}\frac{\omega}{e_{\mathrm{n}}}\chi\delta V_0\exp(j\omega t)\frac{1}{\delta V_0\exp(j\omega t)} \\
&= \frac{e_{\mathrm{n}}\omega^2}{{e_{\mathrm{n}}}^2+\omega^2}\frac{N_{\mathrm{A}}^-}{n}A\sqrt{\frac{2\epsilon q N_{\mathrm{A}}}{V}}
\end{aligned}
\tag{4.2.3.21}
$$

Figure 4.2.4 and Figure 4.2.5 show the calculated curves for C_{T} and G_{T} versus temperature T for different frequencies ω according to Equation 4.2.3.20 and Equation 4.2.3.21. The capture cross section was assumed to be $\sigma = 2.5 \times 10^{-13}\,\mathrm{cm}^2$. A change in the value of the capture cross section σ shifts the spectrum along the temperature axis. The shape of the spectrum does not significantly change with σ.

The appearing peaks are determined by trapping effects of donor/acceptor levels close to the conduction/valence band, according to [32] and [33]. It is possible to detect a trap state when the frequency of the measurement signal resonates with the time constant of the defect state. The additional conductance G_{T} raises with higher frequencies ω. As different trap levels have different thermal and electrical behavior, their activity depends on the temperature as well as.

Since the emission rate e_{n} increases with temperature T, the peaks in G_{T} shift towards higher temperatures as frequencies increase. This allows the determination of ionization energies and emission/capture rates of these levels.

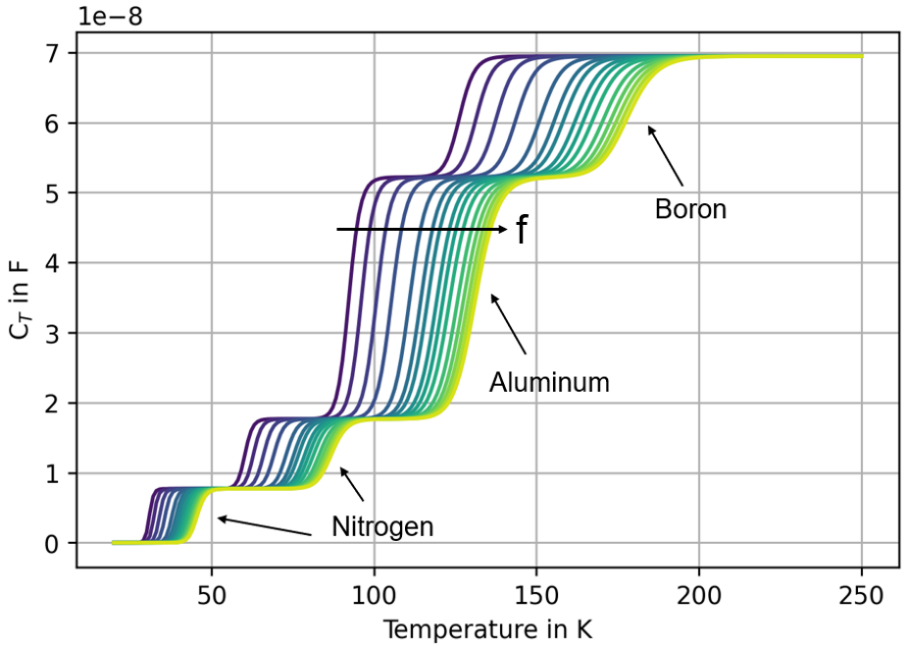


Figure 4.2.4: Theoretical values for capacitance C depending on temperature T and frequency f (dark violet: low frequency, yellow: high frequency). The steps caused by doping atoms are indicated.

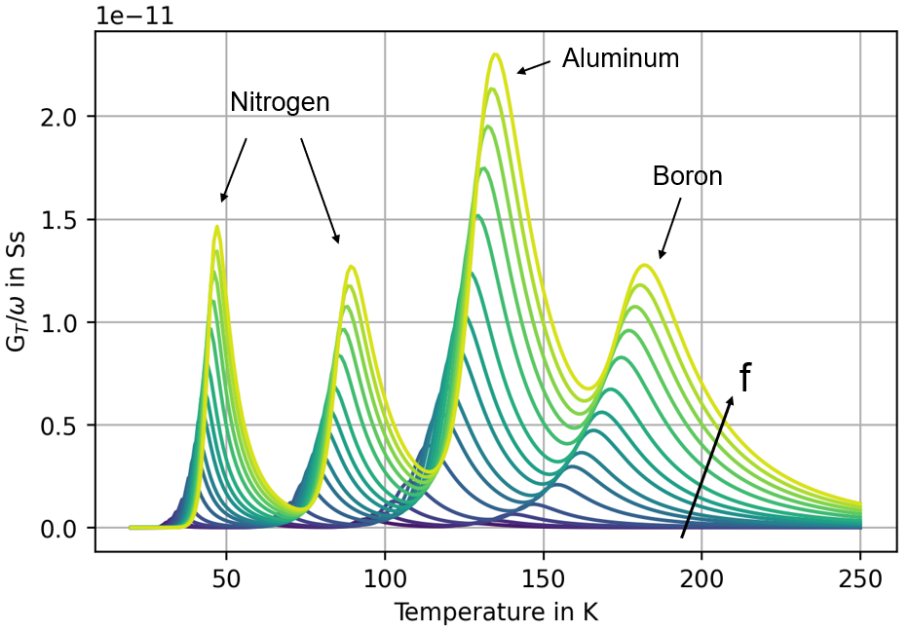


Figure 4.2.5: Theoretical values for conductance G/ω depending on temperature T and frequency f (dark violet: low frequency, yellow: high frequency). The peaks caused by doping atoms are indicated.

5 Experimental Setup - Probe Stations

There are three different probe stations that can be used to measure and characterize the devices. Two of them provide a temperature range of −60 °C-200 °C, whereas the cryogenic probe station allows measure from 6.5 K up to 675 K. Each of them has certain advantages over the others, which made all of the above mentioned measurement methods feasible.

5.1 Süss MicroTec Probe Station

The *Süss MicroTec Probe Station* (SÜSS MicroTec SE, Garching, Germany) allows to do basic electric characterizations on wafer level as well as on device level. The sample is placed on the chuck, held there by vacuum and contacted via tungsten needles, as shown in Figure 5.1.1.

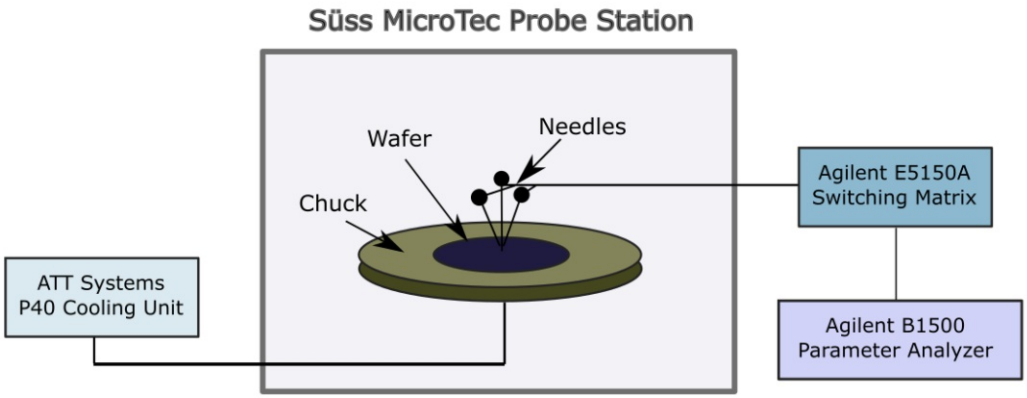


Figure 5.1.1: Measurement setup with the *Süss MicroTec Probe Station*. Inside the wafer is placed on the chuck and contacted via the needles.

The *Agilent E5150A* is a switching matrix, that connects multiple needles to one current or voltage source, the *Agilent B1500 Parameter Analyzer*. Via the *ATT Systems*

P40 Cooling Unit the chuck can either be heated or cooled. The temperature range that is accessible with this probe station reaches from −60 °C to 200 °C. For CV-measurements also an *Agilent 4294A* precision impedance analyzer can be connected to the probe station. With this probe station automatized stepping over the wafer is not possible. Only one device can be contacted at a time and stepping from one to the next device needs to be done manually.

5.2 MPI-AST - TS3000HP Semiautomatic Probe Stations

Compared to the *Süss MicroTec Probe Station* the *MPI-AST - TS3000HP Semiautomatic Probe Station* (MPI CORPORATION, Taipeh, Taiwan) allows stepping over the wafer and measuring all desired devices automatically. According to the manufacturer, *ShielDEnvironment*, this probe station is especially designed for ultra-low noise, extremely accurate and highly reliable DC/CV, $1/f$, RTS and RF measurements, addressing primarily the needs of the device characterization, wafer level reliability and RF and mmW applications. The temperature range of the *MPI-AST - TS3000HP Semiautomatic Probe Station* reaches from −60 °C up to 300 °C. The measurement setup of the *MPI-AST - TS3000HP Semiautomatic Probe Station* is similar to the one of the *Süss MicroTec Probe Station* (see Figure 5.2.1).

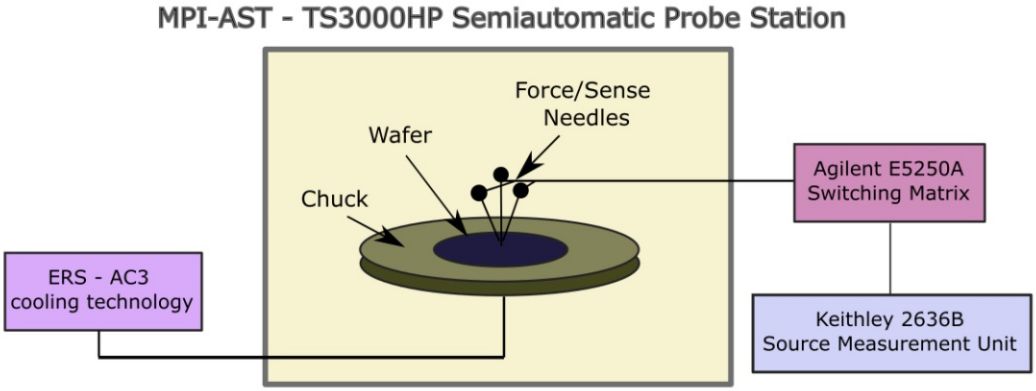


Figure 5.2.1: Measurement setup at the *MPI-AST - TS3000HP Semiautomatic Probe Station*. The wafer is placed on the chuck inside the probe station and contacted via the force/sense needles. Additional appliances are connected to perform measurements.

The wafer or device is placed on the chuck, which can be heated or cooled, and is held in place by vacuum. One device can be contacted at a time, but the stepping from one

device to the next can be automated, which allows electric characterization of the entire wafer with low effort. The used switching matrix is an *Agilent E5250A* connected to a *Keithley 2636B*, which is a source measurement unit. Since force/sense needles are used, two of each appliances are needed. This allows easy four point measurements. For the temperature variation an *ERS* patented *AC3 cooling technology* is used as a thermal control system.

5.3 Cryogenic Probe Station

With a cryogenic probe station it is possible to perform measurements at a wide temperature range from ideally 6.5 K up to 675 K.
Since defects become much more prominent at cryogenic temperatures, it is easier to measure them. Furthermore, the thermionic emission reduces with decreasing temperatures and one gets a reduced on-off-ratio due to lower leakage. While at higher temperatures the carrier transport is dominated by lattice scattering, at low temperatures impurities play an import role and can therefore be measured.
Another advantage of a cryogenic probe station is the possibility to control device environment conditions such as atmosphere, temperature, field and light. This allows very precise and reproducible measurements at cryogenic temperatures.

5.3.1 Setup of a Lake Shore CRX-6.5K Probe Station

The *Lake Shore CRX-6.5K probe station* (Lake Shore Cryotronics, Inc., Westerville, USA) allows measurements from 6.5 K up to 650 K, which is essential for DLTS and admittance spectroscopy. The general measurement setup is depicted in Figure 5.3.1.

Inside the cryogenic probe station there is a sample stage, where the device is placed, as shown in Figure 5.3.2. To reduce the radiative heat load on the device a two-stage cooling assembly is build in (radiation shield and second shield). This setup is inside a vacuum chamber to evacuate the probing environment and maintain the desired temperature. From outside a probe arm reaches into the vacuum area. It has a micro manipulated stage with probe cabling to contact the device. To further reduce the conductive heat load on the device it is thermally anchored. At the end of the probe arm, inside the vacuum chamber, there is a DC/RF probe to electrically contact the sample. The probes are flexible with springs that allow measurements at different temperatures without the needle sliding of the probe due to thermal expansion. The needle itself has a tip radius

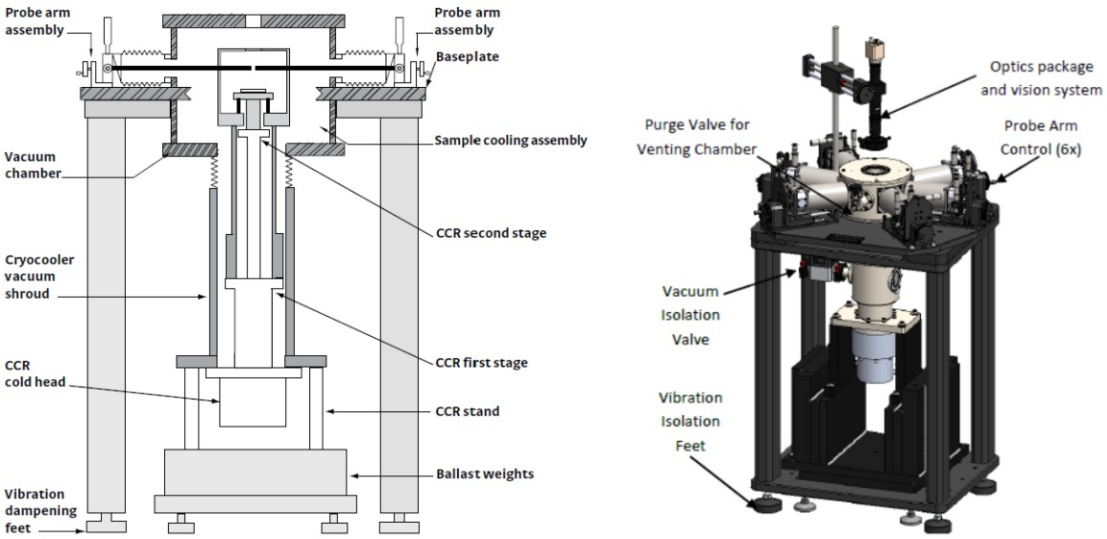


Figure 5.3.1: *CRX-6.5K cryogenic probe station*
Left: the schematic setup of a cryogenic probe station with all essential parts. Right: entire probe station used for the measurements.
Source: Manual of the *CRX-6.5K cryogenic probe station*

of 25 µm and is made of tungsten.

Figure 5.3.2 only shows one probe, but in order to electrically characterize the device more probes are needed and the chuck also has to be electrically contactable. With a temperature controller, that is connected to temperature sensors incorporated in the chuck, different heating and cooling ramps can be performed. In order to reach cryogenic temperautres a vacuum pump, a cold head and a heliumcompressor are used. For certain measurements an *Agilent 4294A* precision impedance analyzer can be connected to the cryogenic probe station.

The basic electric characterizations such as the recording of a transfer curves, mobility and hysteresis determination as well as the capacitance-voltage-dependencies are performed with the *Süss MicroTec Probe Station* and the *MPI-AST - TS3000HP Semiautomatic Probe Station*. These measurements are mainly conducted at ambient temperatures. However, when measuring DLTS, ID-DLTS and admittance spectroscopy, a temperature sweep from cryogenic up to room temperatures is essential and hence, the cryogenic probe station is used.

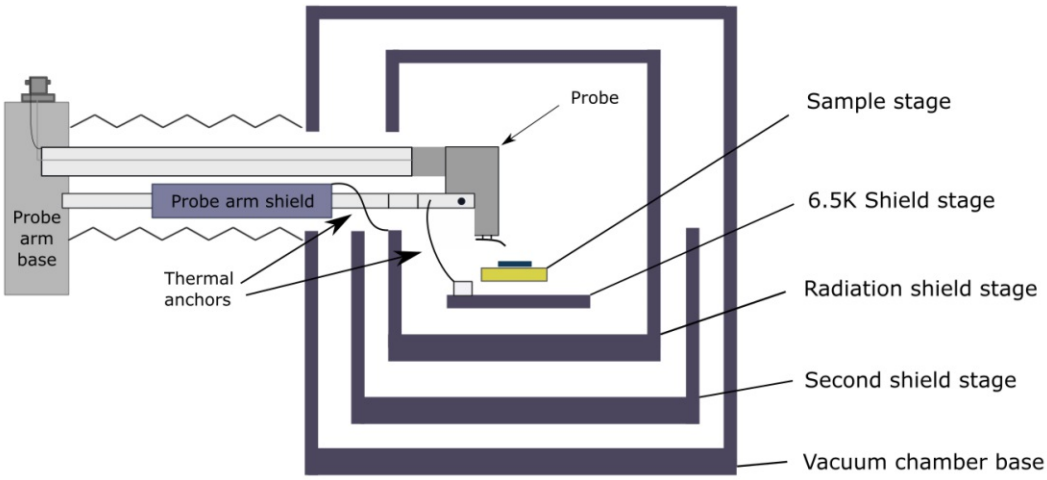


Figure 5.3.2: The schematic setup inside the cryogenic probe station with the probe arm base and the probe arm shield. Inside the vacuum chamber base there are the sample stage, the 6.5 K shield stage, the radiation shield stage and the second shield stage.

6 Investigated Samples and Performed Measurements

In order to establish a good overview over the boron (B) implantation caused effects and the resulting device performance, various measurements on differently processed samples are conducted.

6.1 Tested Devices

The tested samples are SiC-trench-MOSFETs implanted with boron (B) produced by *Infineon Technologies Austria AG*. Since it is the aim to investigate the impact of B on the device characteristics, different doping dosages are tried out. Furthermore, there is always a reference sample within each split, that is manufactured with state of the art standard process using aluminum p-body implant.
In the p-implanted channel region, different doping atoms were tried out. The reference sample was doped with 100%Al, whereas the three B implanted devices have either 10%B, 30%B or 100%B. In case for the 10%B and 30%B devices the other doping atoms are Al, in order to reach the same p-doping concentration as in the reference sample. Due to an unknown degree of diffusion of B in SiC during the post implantation high temperature anneal, the actual remaining B content in the devices is unknown. Each of the samples (reference, 10% B, 30% B and 100% B) is characterized with the above mentioned measurement techniques. The measurement outcomes are discussed in the following section.

7 Results

In the following sections the results of the basic device characterization (such as I_D/V_G measurements, threshold voltage and mobility determination) as well as the outcomes from DLTS and admittance spectroscopy are displayed. Comparisons between the reference (Al) and the B implanted sample are drawn.

7.1 Transfer Characteristic

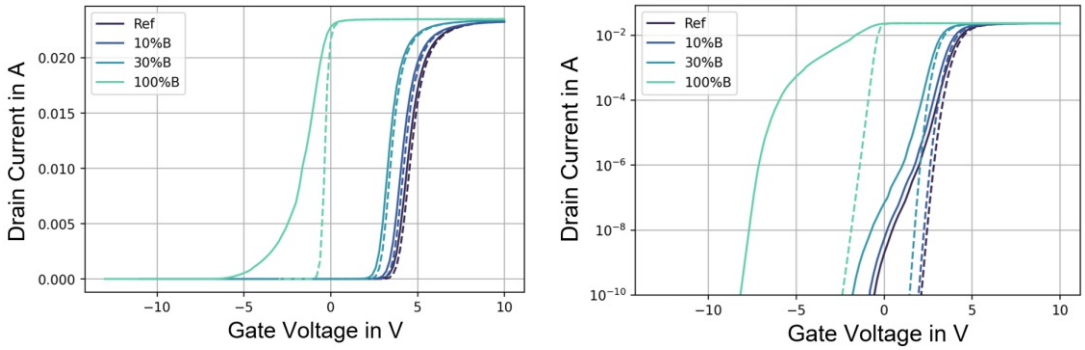
The basic measurement is the analysis of the I_D/V_G curves and the determination of the threshold voltage V_{th}. With these characterizations a primary picture of the device behavior can be drawn.

7.1.1 Current Voltage Characteristics

The current voltage characteristic was recorded for the reference device as well as for the ones implanted with Boron. An up-sweep from $-15\,V$ to $10\,V$ (solid lines) and a down-sweep from $10\,V$ to $-15\,V$ (dashed lines) were performed at a drain voltage V_D=0.1 V. The sweep rate during this measurement was 0.1 V/s.
The reference sample has the highest threshold voltage, closely followed by the 10% B and 30% B samples. The device implanted with 100% B has a negative threshold voltage of about $-5\,V$, which makes it a normally-on device. That is caused by the p-body implantation, which is below the background n-implantation in epitaxially grown SiC layer. In case of a successful B implantation in the channel area, one would expect a threshold voltage close to the one of the reference device. Consequently, the device does not act as a normal MOSFET, but rather behaves like a parasitic JFET.

7.1.2 Test Structures Analysis

Special test structures with certain geometric variations are fabricated along side the original MOSFET. They are electrically characterized to gain more information about the B implanted device behavior. Figure 7.1.2 shows the result of an I_D/V_G measurement



(a) $I_D(V_G)$ - linear

(b) $I_D(V_G)$ - logarithmic

Figure 7.1.1: Transfer characteristics $I_D(V_G)$ for Al-implanted reference sample and B implanted devices at a drain voltage of V_D=0.1 V. Straight line: up sweep (−15 V to 10 V), dashed line: down sweep (10 V to −15 V)

of such a test structure, where the distance between the two p-body and the p-emitter area is varied. Since the threshold voltage decreases with increasing distance between the p-areas (in 0.2 µm steps), a normal channel behavior can be ruled out. In the case of a fully working device the threshold voltage should remain the same for all devices. Since the transfer characteristics change with distances to the p-area, one can assume to have a parasitic JFET, that creates a normally-on device, where the current flow is pinched off when the gate voltage becomes high enough. Consequently, the p-doping of the channel area with B is unsatisfying.

7.1.3 Temperature Dependence of Threshold Voltage

Experimental results from a $V_{th}(T)$ measurement on the reference and 100% B samples confirm the theoretical calculations in subsection 3.1.2, which predict a decrease in threshold voltage over temperature. The recorded data is plotted in Figure 7.1.3. Due to the hysteresis effect the threshold voltage is negative for the up sweep of the 100% Al sample, while the down sweep shows positive threshold voltage values over temperature. The behavior seems to be similar for the reference and the 100% B device. Only, the decrease of V_{th} over T is higher for the B implanted device, due to a higher activation energy of B compared to Al.

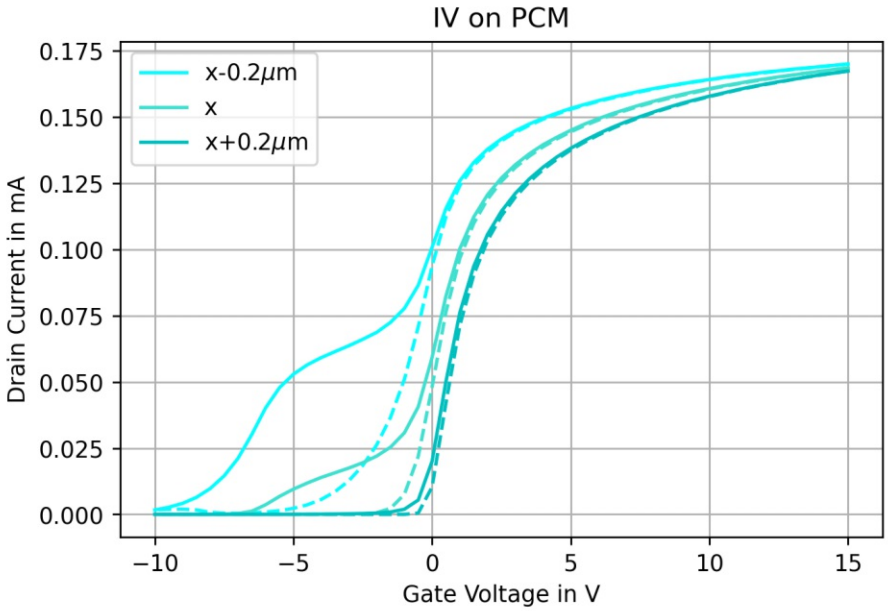


Figure 7.1.2: I_D/V_G measurement of a **100% B** test structure MOSFET. The distance to the p-area is varied between $x - 0.2\mu m$ and $x + 0.2\mu m$. Straight line: up sweep (−10 V to 15 V), dashed line: down sweep (15 V to −10 V)

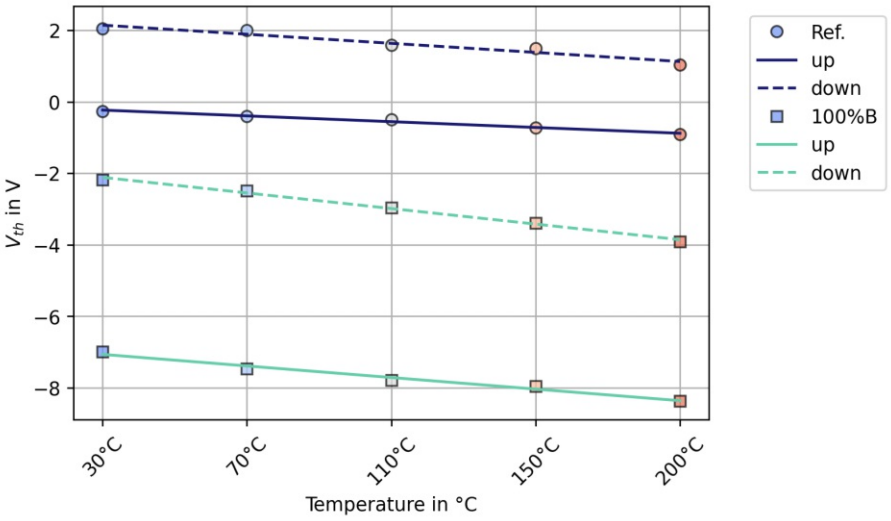
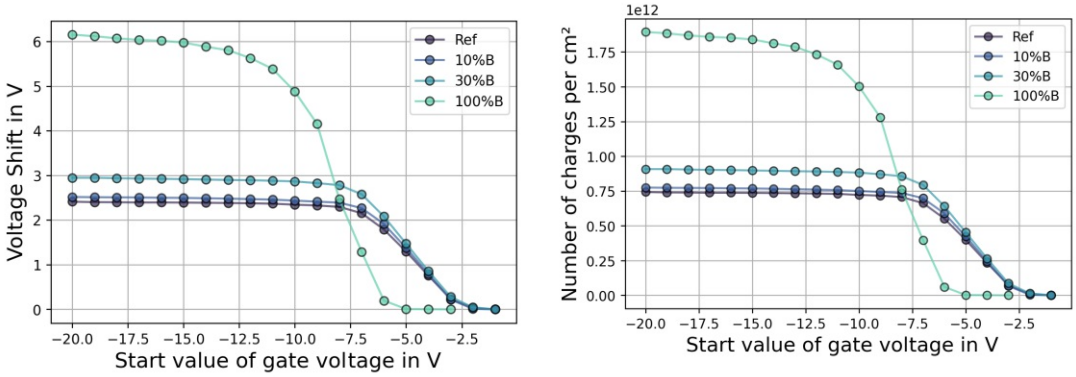


Figure 7.1.3: The threshold voltage V_{th} over temperature T for a 100% Al implanted reference sample and a 100% B implanted device is shown. Solid lines stand for the up-sweep whereas dashed lines represent the down-sweep.



(a) Subthreshold voltage shift

(b) Number of charges per area stored at the interface

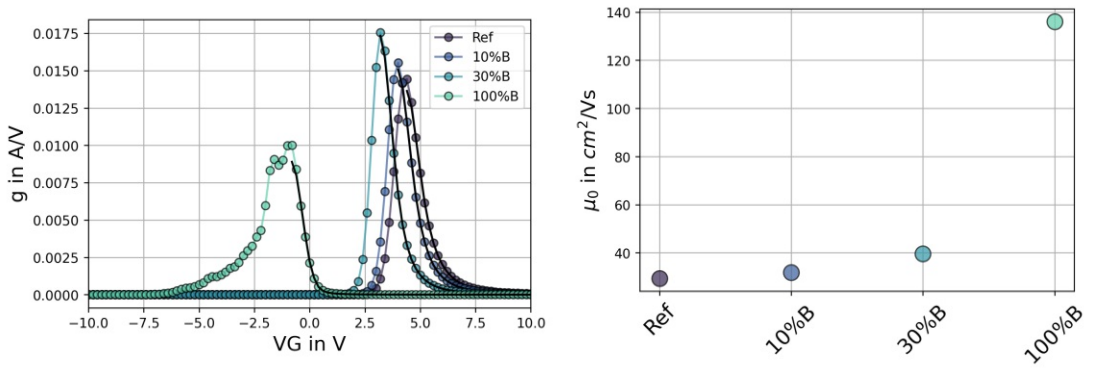
Figure 7.2.1: The subthreshold sweep hysteresis is depicted for the reference device and the B implanted devices. (a) Threshold voltage shift in dependence on the start value of the gate voltage. (b) Calculated number of charges per cm^2.

7.2 Subthreshold Sweep Hysteresis

The experimental results from the subthreshold sweep hysteresis measurement allow to determine the difference between up- and down-sweep for the same gate voltage in the subthreshold regime. Furthermore, it is possible to quantify the number of charges stored at the interface between up- and down-sweep, which quantifies the number ot traps at the interface. Figure 7.2.1 shows the measured subthreshold sweep hysteresis for the reference device as well as for device with B as channel implant for different sweep starting voltages. The measurement was performed at room temperature and with a drain bias of V_D=0.1 V. As one can see, the devices, in which the Al dopant was substituted by only 10% B or 30% B, show similar subthreshold voltage shifts as the reference device. Also the number of charges stored at the interface is almost equal for reference, 10% B and 30% B. The device implanted with 100% B, however, seems to have a very high subthreshold sweep hysteresis and consequently a high number of charges stored at the interface.

7.3 Mobility - Ghibaudo Method

The mobility of a device can be extracted from the I_D/V_G characteristic with the method of Ghibaudo [27], as shown in section 3.3. In this procedure the transconductance g is calculated to determine the low field carrier mobility μ_0. The results from the measurements are shown in Figure 7.3.1. As already expected from slope of the I_D/V_G



(a) Transconductance g for all four measured devices

(b) Calculated mobility by the method of Ghibaudo

Figure 7.3.1: The I_D/V_G relation is used to calculate the transconductance g, from which the low field carrier mobility μ_0 is extracted.

curves (Figure 7.1.1) the 100% B device has the highest mobility, far above the one of the 30% B, 10% B and the reference sample. This might be explained by the fact, that the 100% B device is not a regular MOSFET but a parasitic JFET.
The difference in mobility between the reference sample and the 10% B or 30% B can be deduced from less lattice damage introduced by Al implantation. Since B atoms damage the lattice less compared to Al during the implantation process, the electric behavior of the channel is less impacted [11].

7.4 Capacitance Voltage Characteristics

The capacitance of a MOSFET strongly depends on the applied gate voltage, since the depletion region width, that impacts the capacitance, varies with the gate bias, as explained in section 3.4. The $C(V)$ measurement was performed at room temperature for the Al implanted reference sample and the three B implanted devices, as shown in Figure 7.4.1. The 10% B and 30% B samples show similar $C(V)$ curves as the reference with a minimal shift to lower voltages. The $C(V)$ characteristic of the 100% B device is clearly shifted to lower voltages. This is considered in the admittance spectroscopy, where DC voltages are applied so that the capacitance reaches a certain value. The $C(V)$ curve of the 100% B sample in depletion exhibits a bulge and shows a steeper increase compared to the other samples. This plot is normalized to the capacitance value at 15 V in order to make the four curves comparable regarding their behavior in depletion and inversion.

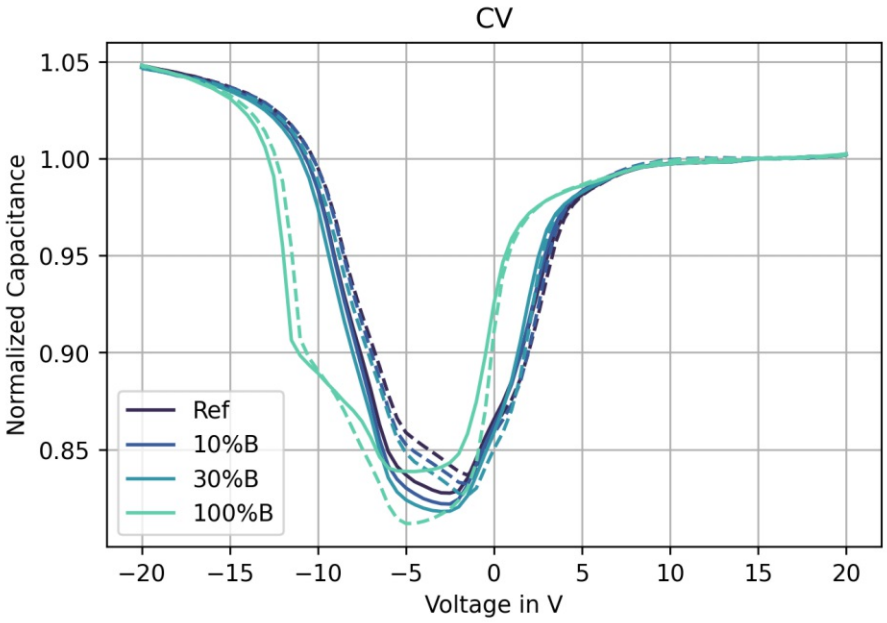


Figure 7.4.1: Capacitance-Voltage measurement for the reference device and for the B sample normalized to the capacitance value at 15 V. Straight lines: up sweep from −20 V to 20 V, dashed lines: down sweep 20 V to −20 V.

7.5 DLTS Measurement Outcome

Since the 100% B sample is a normally on device due to insufficient p-body implantation, the DLTS measurements are only performed on the 30% B and on the reference sample. Each device is tested via the body diode in blocking direction. The source terminal is biased with 0 V during the stress for 100 ms and with 2 V during recovery also for 100 ms, while the gate is floating. The temperature is increased with a rate of 1 K/min. Figure 7.5.1 shows the results from these measurements. The first peak around 40 K can be attributed to the N in the device. According to Berens [34] the peak around 70 K might be an Al-related defect. However, it is important to note, that Berens *et al.* [4] performed the measurement under slightly different conditions. The measured devices in their work are not exactly the same as shown here and the applied voltage pulse might vary as well. This can lead to a discrepancy in the DLTS peaks. Another B caused peak cannot be found in the spectrum of the 30% B. There is no significant difference in the DLTS spectra of the reference and the 30% B sample, which is in accordance with previous measurements, where the results from 30% B and reference are very similar.

Hence, also the DLTS body diode measurement does not indicate any difference in the device caused by B.

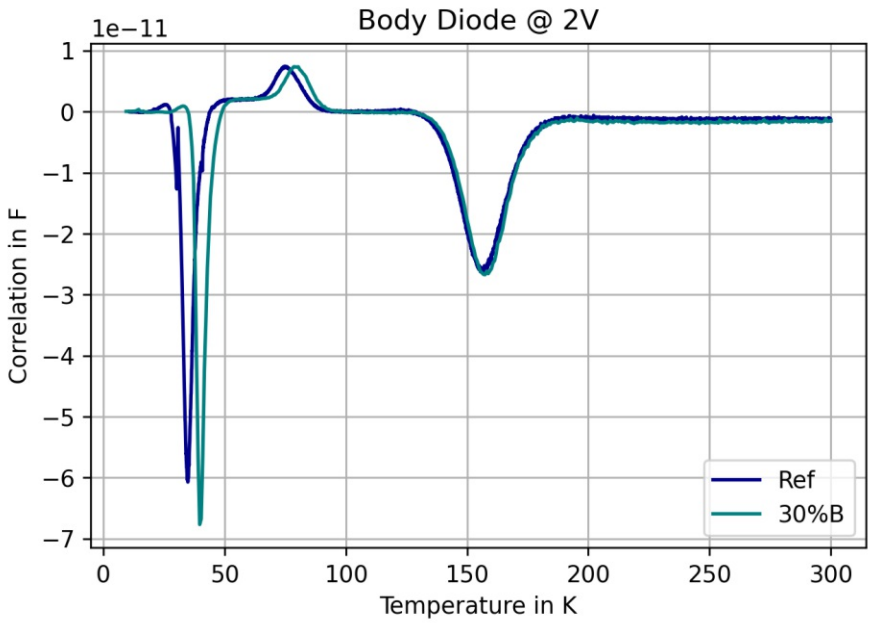


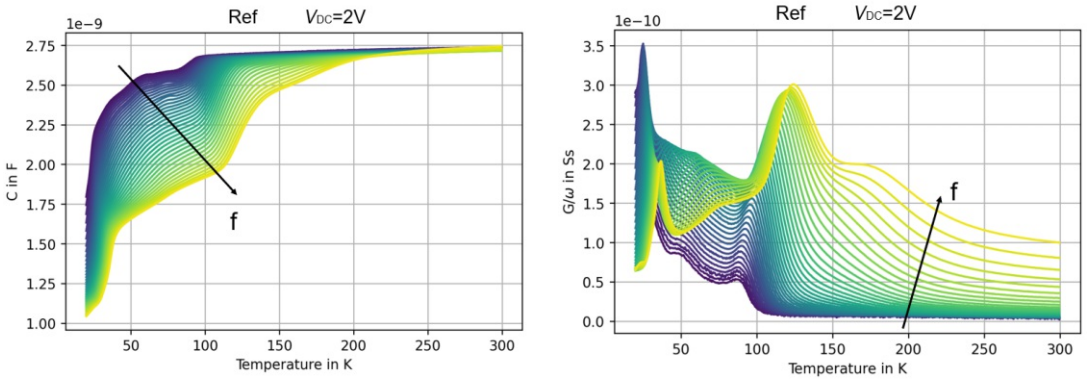
Figure 7.5.1: DLTS measurement for the reference and the 30% B sample via the body diode with a bias of 2 V.

7.6 Admittance Spectroscopy Results

The admittance spectroscopy is always performed at a certain DC voltage, that determines the width of the depletion region. On top of that there is a small AC signal with an amplitude of 0.1 V. The small change in the depletion region width due to that additional signal is tested during the admittance spectroscopy measurement. The temperature is increased with a rate of 1 K/min. One entire frequency sweep from 40 Hz to 1 MHz takes exactly 1 min.

7.6.1 Characteristic Results from an Admittance Spectroscopy

For the case of a reference sample at a DC bias of 2 V the resulting change in capacitance and conductance over temperature is depicted in Figure 7.6.1. As one can see in Figure 7.6.1a the capacitance C rises between 30 K and 40 K, when the implanted N is activated. Another increase in capacitance can be found around 100 K and 120 K as



(a) Capacitance over temperature for the reference sample at 2 V

(b) Conductance over temperature for the reference sample at 2 V

Figure 7.6.1: A representative admittance spectroscopy with $C(T)$ and $G/\omega(T)$. Violet lines represent very low frequencies around 100 Hz while yellow lines stand for almost 1 MHz. The frequency increases logarithmically.

the Al atoms start to contribute to the capacitance. At the same temperatures peaks in the conductance G/ω can be found, as the doping atoms cause losses at a certain temperature and frequency. The small peak around 70 K can also be attributed to N, but to those N atoms sitting on cubic lattice sites, whereas the peak around 35 K is caused by N atoms in hexagonal lattice sites [35]. Since Al atoms on hexagonl and cubic lattice sites have almost the same activation energy there is only one peak in the conductance, which is the one around 120 K.

As mentioned above this measurement was conducted at a reference sample with only N and Al implantation. Considering the theoretical calculations in Figure 4.2.4 and Figure 4.2.5 another third large peak caused by B atoms at temperatures around 230 K is expected for B implanted devices. Admittance spectroscopy measurements on the 100% B device are shown in subsection 7.6.2, where the third large peak in conductance caused by B appears.

7.6.2 Reference Sample compared to 100% B Sample

In the following measurements only the reference (100% Al) and 100% B implanted devices are analyzed and compared to each other. The measurement results from the 10% B and 30% B samples are displayed in the appendix (chapter 10). For the sake of simplicity only five frequencies are depicted in each plot. The DC voltage is varied in

order to test different regions in the channel area.

As shown in section 7.4 the CV-curves of the reference sample and the 100% B sample differ. In order to make the admittance spectroscopy measurements of these two devices comparable, a DC voltage is chosen so that both samples have the same capacitance values. Figure 7.6.2 shows the CV-curves of the reference and 100% B sample and indicates at which DC voltages admittance spectroscopy was measured (depletion, depletion to inversion and inversion).

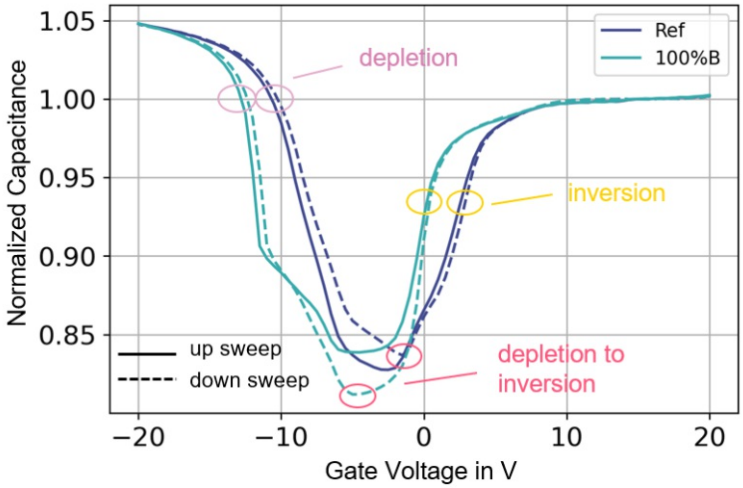


Figure 7.6.2: CV-curves for the reference and for 100% B. The DC voltage values where admittance spectroscopy is measured are marked with circles. The tests are performed in depletion (Ref: −10 V and 100% B: −13 V), between depletion and weak inversion (Ref: −2 V and 100% B: −5 V) and weak inversion (Ref: 2 V and 100% B: 0 V).

Depletion: The admittance spectroscopy results for a device in depletion are displayed in Figure 7.6.3. $C(T)$ and $G/\omega(T)$ from the reference sample are compared to the 100% B sample. The $C(T)$ curve of the 100% B sample (top right) has another increase in capacitance from 2.75 nF to 3 nF compared to the reference sample (top left), which can be attributed to the B in the device. The assumption that there is B in the device is supported by the peak around 150 K to 200 K in the $G/\omega(T)$ curve from the 100% B sample (bottom right). As one can see this peak does not occur in the reference sample (bottom left), where only the N peak (around 50 K) and the Al peak (around 110 K) appear. Hence, there is B in the channel area, but the concentration might be too low, to create a p-implanted area.

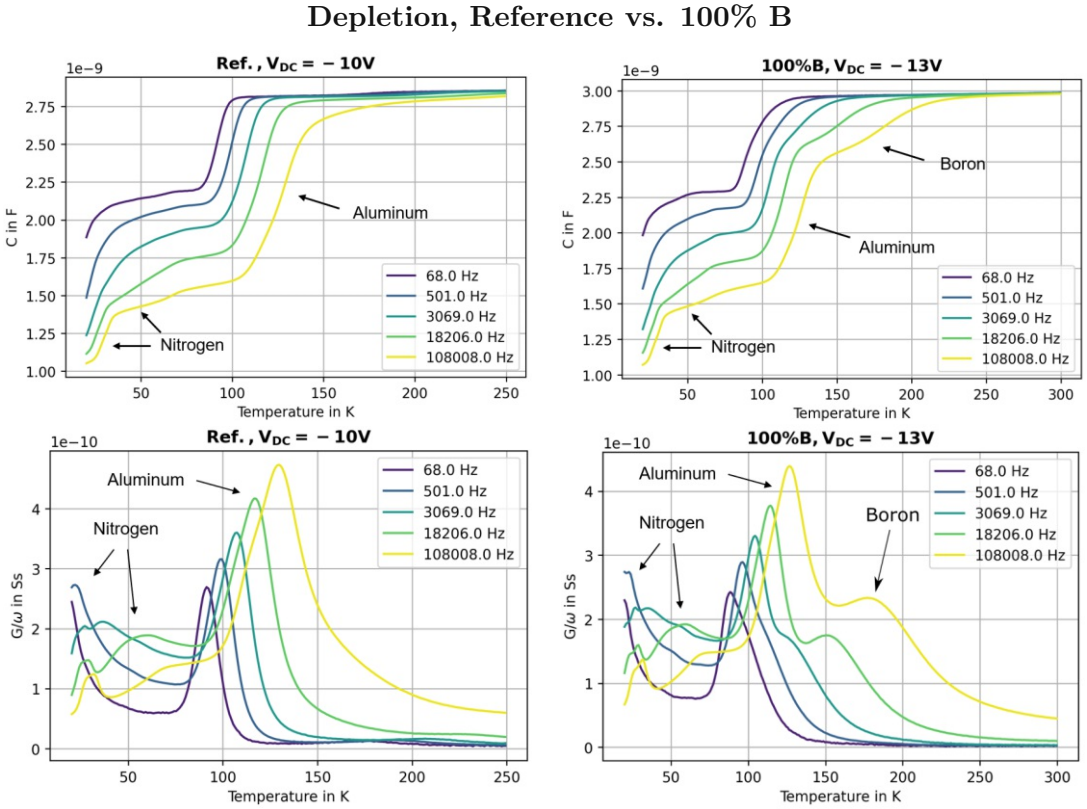


Figure 7.6.3: Admittance spectroscopy in depletion for the reference and the 100% B sample.

Depletion to Inversion: When the admittance spectroscopy is performed with a DC bias that brings the device to a state between depletion and inversion, one gets the results shown in Figure 7.6.4. The additional increase in capacitance of the 100% B sample (top right) disappears just like the peak in the conductance around 150 K to 200 K (bottom right). This might suggest that the area of the depletion region created by the DC voltage does not extend to the region where B was implanted.

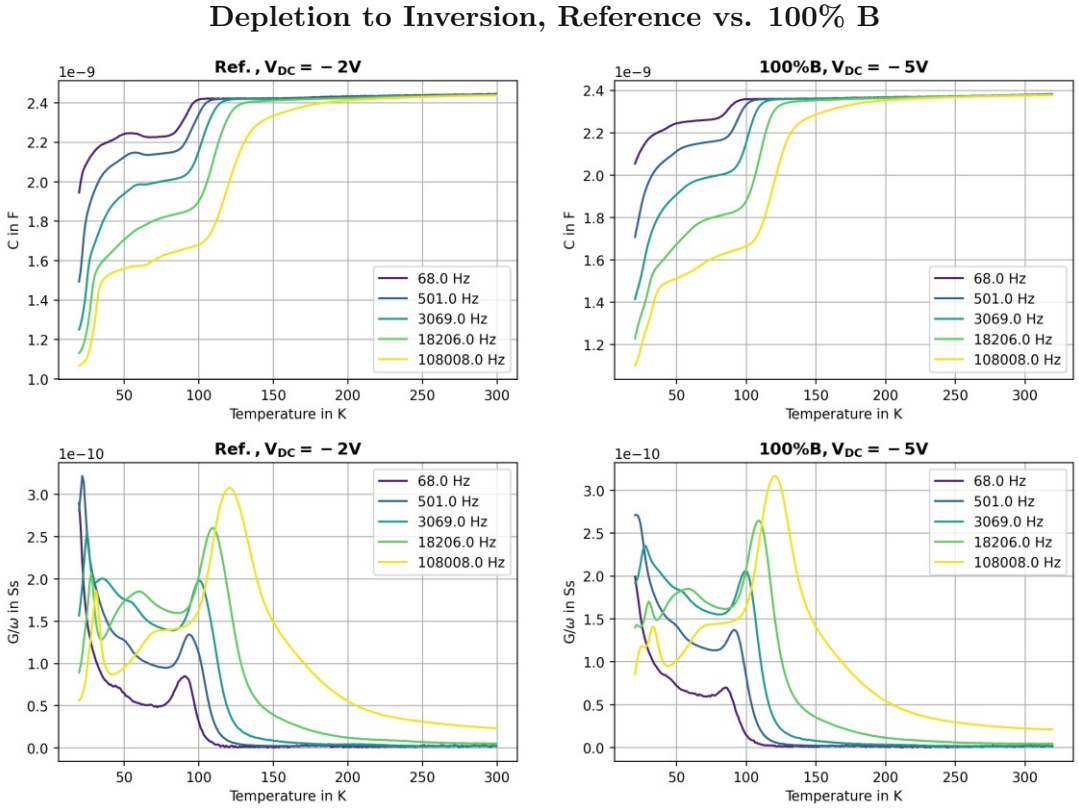


Figure 7.6.4: Admittance spectroscopy at depletion to inversion for the reference and the 100%B sample.

Inversion: Considering Figure 7.6.5 one can see that the $C(T)$ and $G/\omega(T)$ curves between the reference and the 100% B sample differ. As these results show, there might be a different dosage of N and Al in the two devices, which can be explained by the fact that different doping atoms were used for the two samples. However, an increase or a peak caused by B cannot be found.

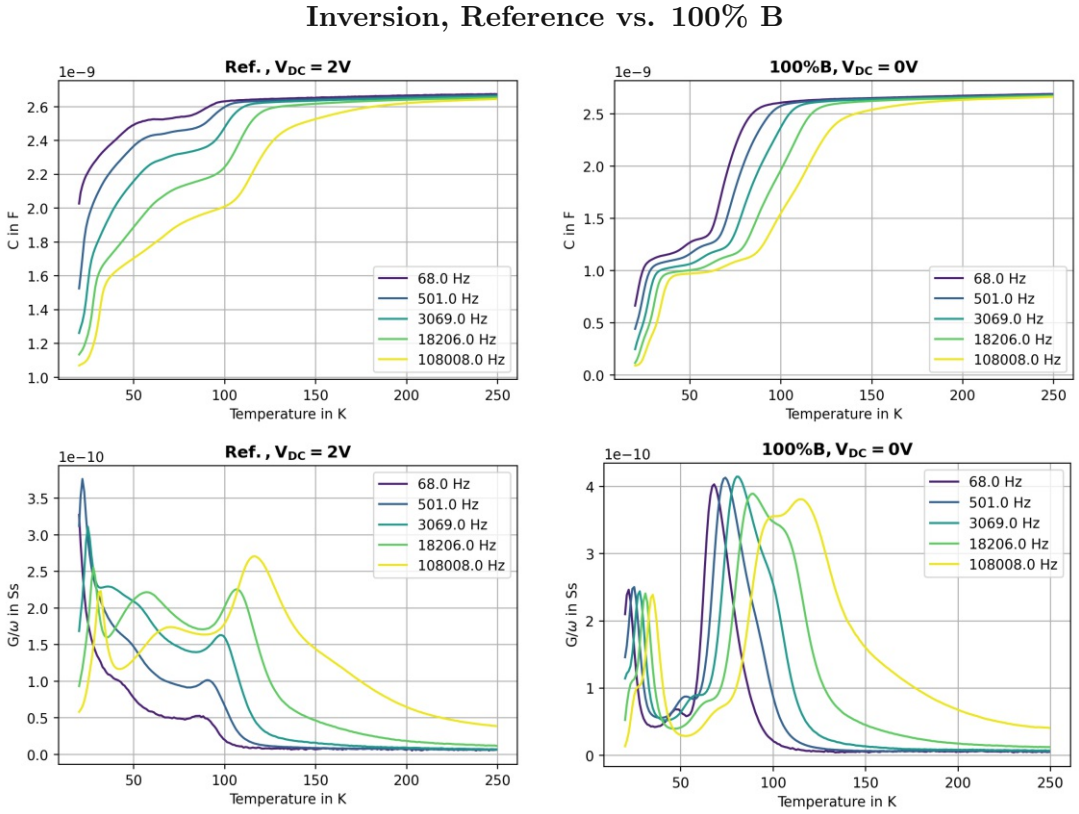


Figure 7.6.5: Admittance spectroscopy in inversion for the reference and the 100%B sample.

In the following plots (Figure 7.6.6, Figure 7.6.7 and Figure 7.6.8) only single frequencies of 108 008 Hz, 3069 Hz and 68 Hz of the admittance measurement are displayed. The reference sample is directly compared to the 100% B sample for depletion, depletion to inversion and inversion.

The comparison at 108 008 Hz in depletion (Figure 7.6.6) shows the most prominent difference between the reference and the 100% B sample, which is the peak at 180 K of the 100% B sample (top right). At a lower frequency of 3069 Hz (Figure 7.6.7, top right) the peak diminishes until it is no longer visible at 68 Hz (Figure 7.6.8, top right). Considering depletion to inversion the two samples show similar outcomes for all frequencies. The results recorded in inversion show differences between the reference and the 100% B sample over the entire frequency range, but none of them is relevant for the detection of B.

108008 Hz, Reference vs. 100% B

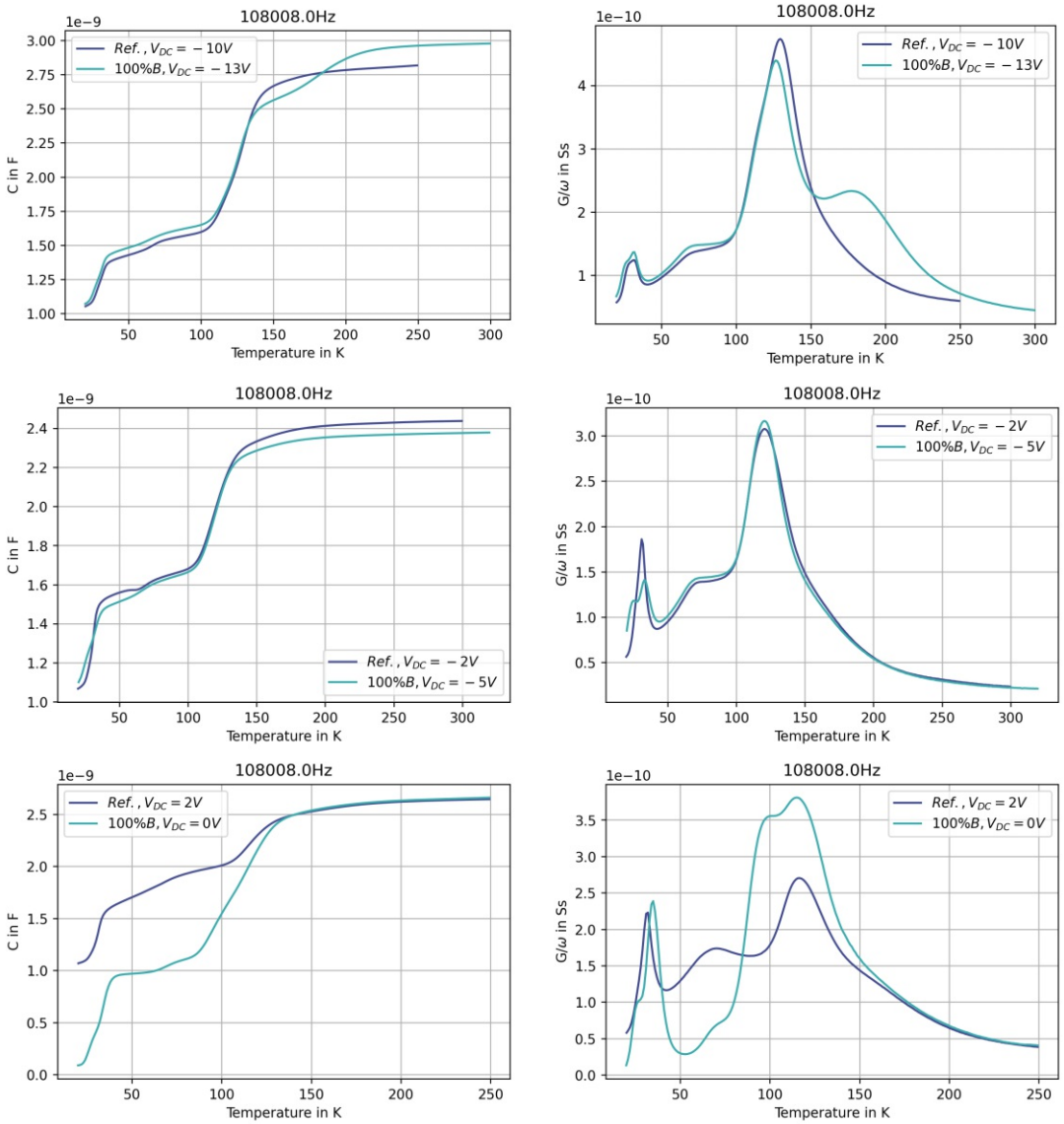


Figure 7.6.6: Admittance spectroscopy for the reference and the 100%B sample at 108 kHz. Depletion, depletion to inversion and inversion.

3069 Hz, Reference vs. 100% B

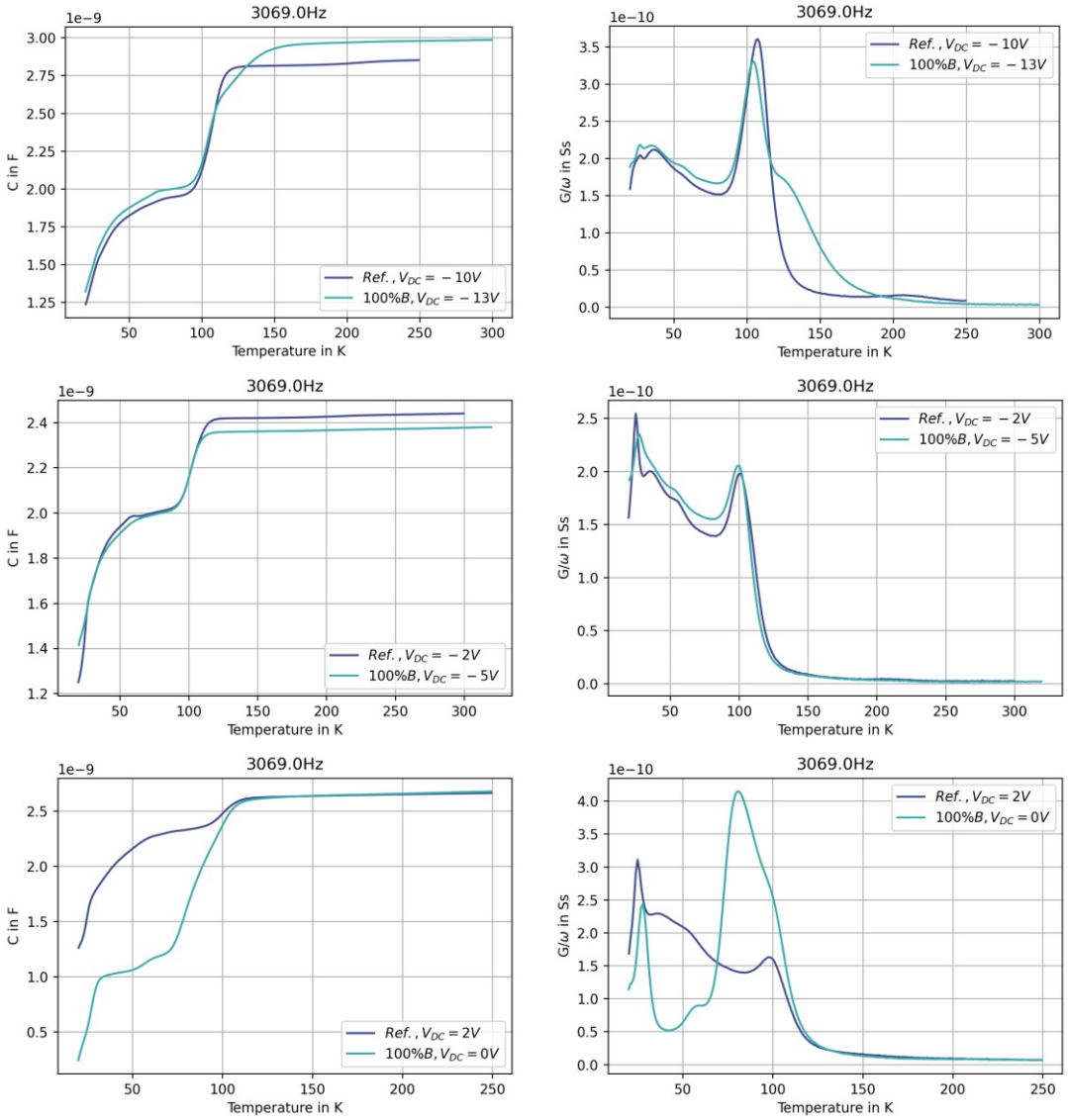


Figure 7.6.7: Admittance spectroscopy for the reference and the 100%B sample at 3069 Hz. Depletion, depletion to inversion and inversion.

68 Hz, Reference vs. 100% B

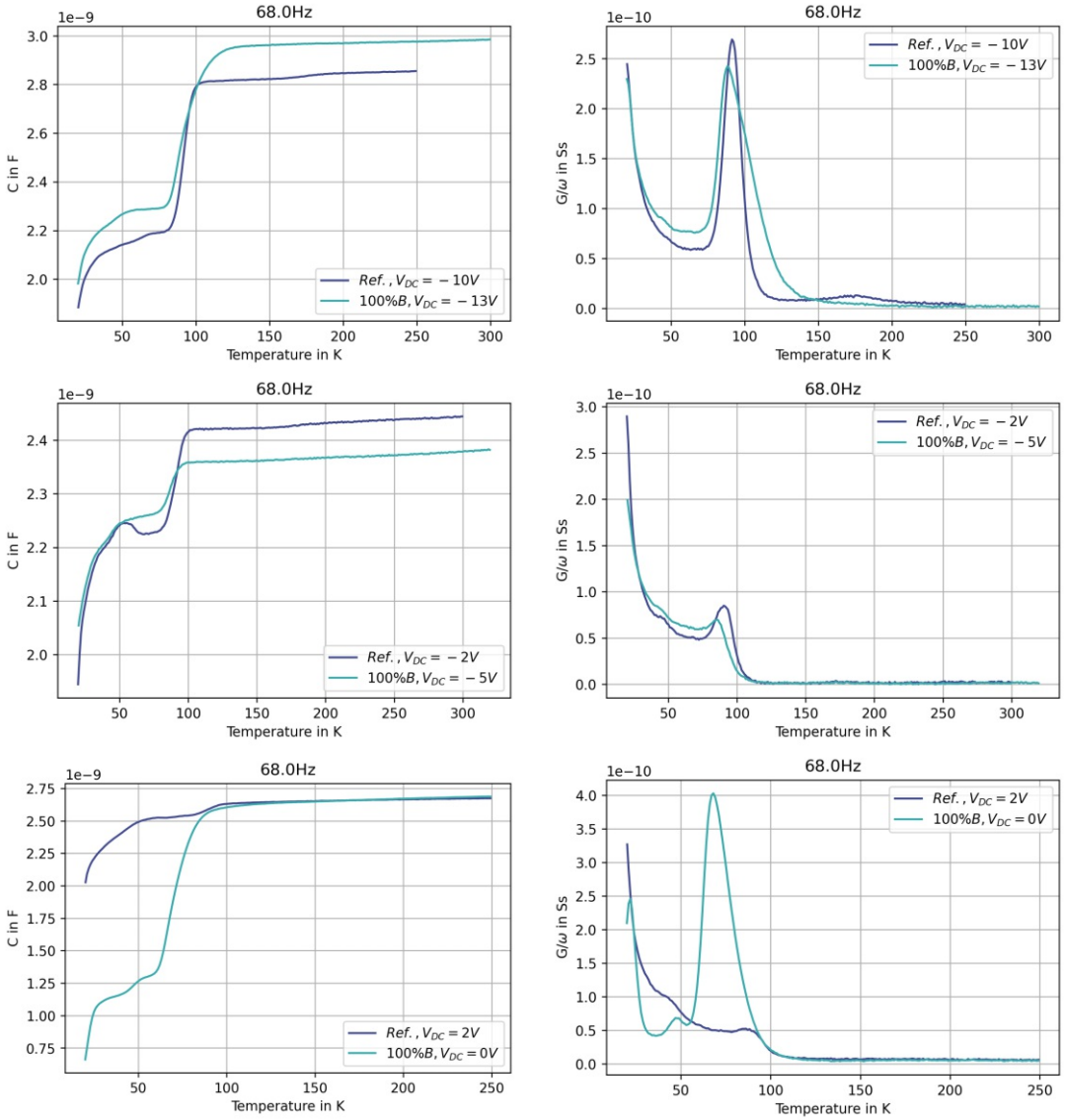


Figure 7.6.8: Admittance spectroscopy for the reference and the 100%B sample at 68 Hz. Depletion, depletion to inversion and inversion.

7.6.3 Results for the 10% B and 30% B Samples

The corresponding admittance measurement results for the 10% B and 30% B samples are displayed in the appendix (chapter 10). It seems that the B concentration in these two samples is too low to detect the B in the device with admittance spectroscopy. Their

electrical behavior is very similar to the reference sample, as also seen in the basic electric measurements.

7.6.4 Derivative of Capacitance over Temperature

The derivative of the capacitance over temperature can visualize the difference in capacitance between the reference sample and the 100% B sample, that is cause by the implanted B. Figure 7.6.9 shows the four samples in depletion. The 100% B sample exhibits a small peak around 150 K, that shifts to higher temperature as the frequency increases. This peak can be attributed to the B inside the 100% B sample, since it does not occur in any of the other three samples, with either no B or very little B. It is a small change in capacitance, but when plotted as the derivative one can identify B related changes in the device.

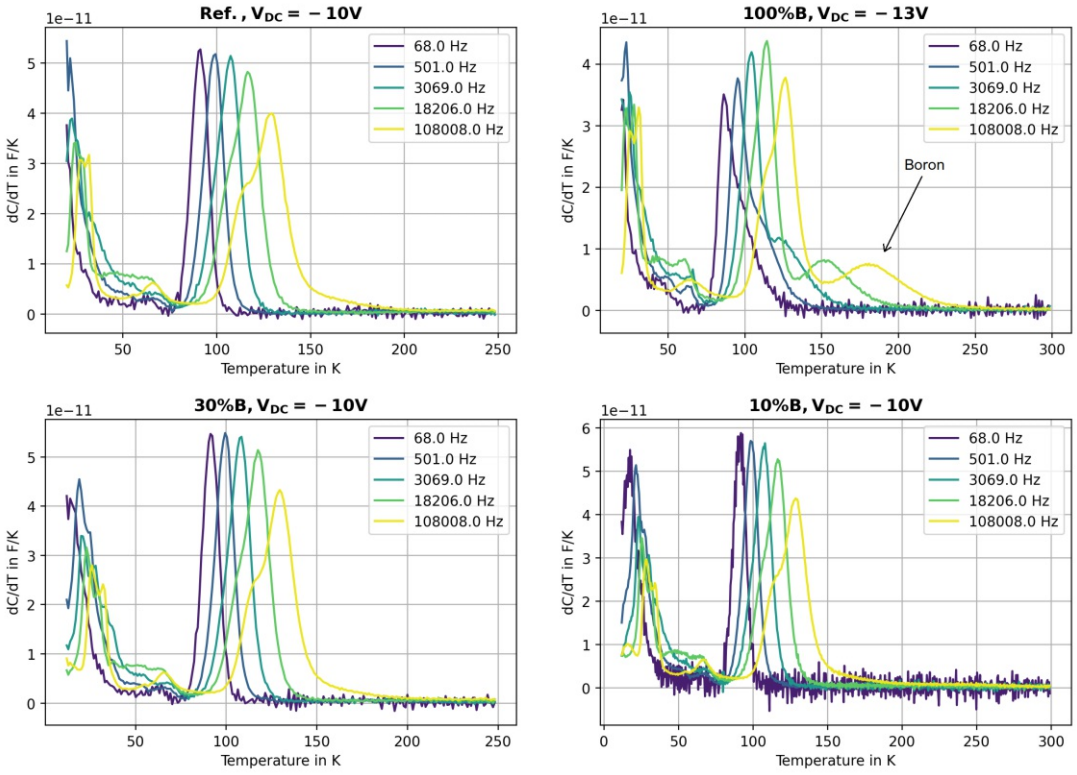


Figure 7.6.9: Derivative of capacitance over temperature for reference, 100% B, 30% and 10% B in depletion.

7.6.5 Influence of Temperature-Ramp-Rate on the measurement outcome

In order to prove that the temperature ramp does not effect the admittance spectroscopy results, one measurement with 0.5 K/min and one with 2 K/min are shown in Figure 7.6.10. Those two measurements almost look alike although the temperature ramp between the two measurements is increased by a factor four. This leads to the assumption that the temperature-ramp-rate does not impact the measurement results, as long as the rate is not too high (e.g. 10 K/min), since capture and emission processes of carriers could not happen under almost equilibrium conditions.

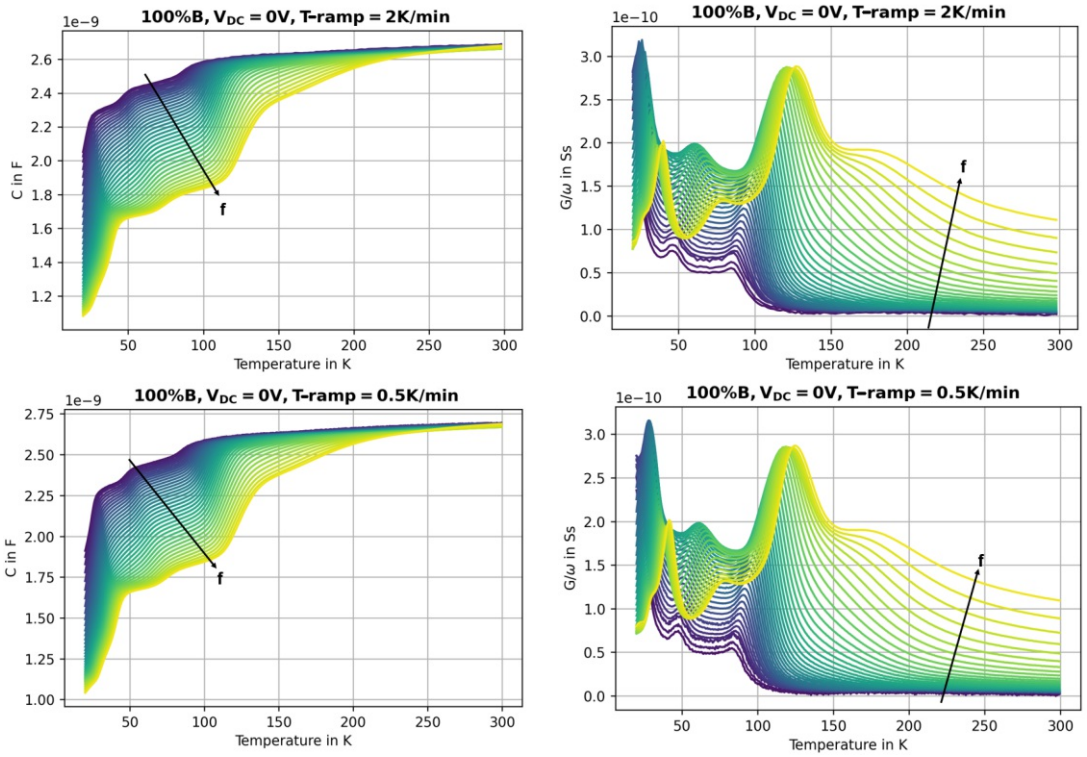


Figure 7.6.10: Admittance spectroscopy performed with different temperature ramps of 0.5 K/min and 2 K/min.

8 Measurement versus Simulation

The measurement results from the 100% B sample in depletion are taken and compared to the calculated $C(T)$ and $G/\omega(T)$ curves from Equation 4.2.3.20 and Equation 4.2.3.21. Since the B related peak is most prominent at the highest frequency (108 008 Hz), the results are compared at that frequency, as depicted in Figure 8.0.1.

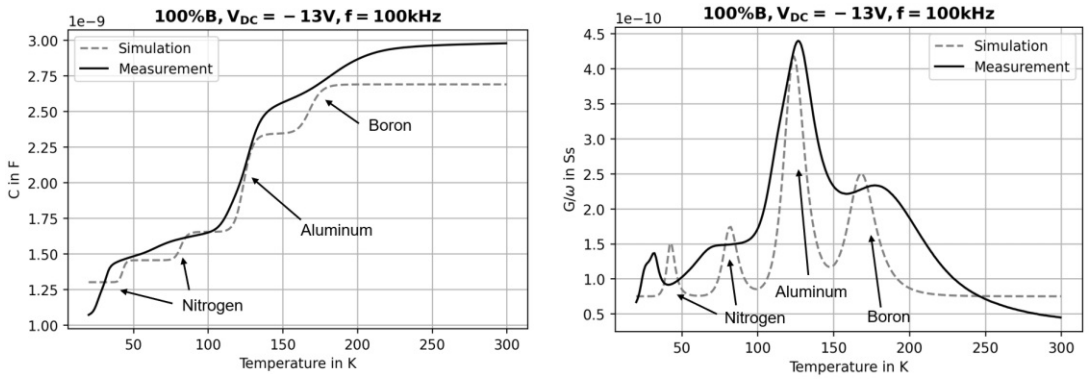


Figure 8.0.1: Measured and calculated $C(T)$ and $G/\omega(T)$ at a frequency of 108 008 Hz and a DC bias of −13 V (depletion).

The rises in capacitance look alike for the measurement and the simulation. The first two capacitance increases can be attributed to N on hexagonal and cubic lattice sites, the third increase around 120 K is caused by Al on cubic and hexagonal lattice sites. The last increase is due to the B in the device.
The N, Al and B related peaks in the conductance appear at similar positions for the measurement and the simulation. A significant difference show the areas between the peaks, where the simulated conductance decreases, while the measured conductance remains at a certain value. This might be explained by additional effects in the measured device that cannot be simulated with an idealized formula like Equation 4.2.3.21. Furthermore, the capture cross section σ used in the simulation can only be assumed to be $\sigma = 2.5 \times 10^{-13}\,\mathrm{cm}^2$ and shifts the spectrum along the temperature axis. However, the accordance between measurement and simulation to some extend suggests that the measurement outcome can be understood in theory and, hence, interpreted correctly.

9 SIMS Measurements

In order to gain deeper understanding about the location of the B in the device, Secondary Ion Mass Spectroscopy (SIMS) was used as an additional measurement technique. SIMS is a powerful measurement technique to quantify atoms in a lattice and to determine their distance to the crystal surface. In order to estimate the B concentration in the measured devices, a test wafer was implanted with a 500% higher B concentration compared to the electrically tested devices, followed by a High Temperature Anneal (HTA) and was characterized with SIMS afterwards. The exact results of the SIMS measurement must not be shown in this thesis, however, a schematic picture of the measurement outcome is depicted in Figure 9.0.1. During the HTA part of the implanted B dosage seems to have diffused out of the lattice. This supports the assumption, that the B concentration in the device is lower than the implanted dosage, since a major part of the B atoms diffuse out of the SiC lattice. However, there is still a significant concentration of B left in the device.

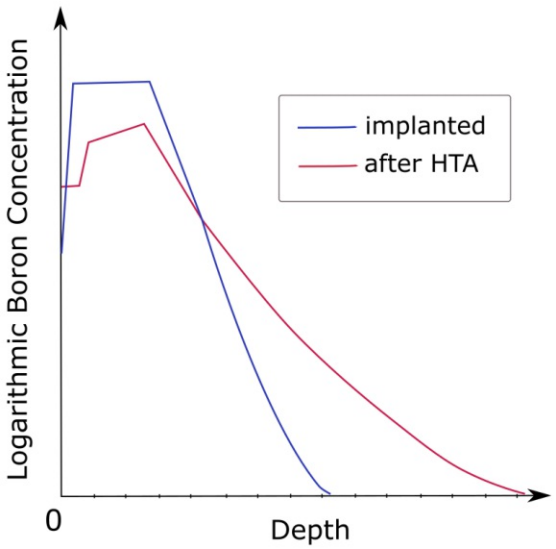


Figure 9.0.1: schematic SIMS measurement outcome of a test wafer that was implanted with 500% more B than the electrically measured devices.

10 Conclusion and Outlook

The aim of this thesis was to investigate B implanted trench MOSFETs with basic and advanced measurement techniques. The transfer characteristic of the 100% B device shows no MOSFET behavior but the behavior of a parasitic JFET. The other two devices (10% B and 30% B) have a similar behavior like the reference device concerning the I_D/V_G curves. As the 100% B device has only B as channel implant, whereas other regions are partially or entirely doped with Al, the device behavior fully depends on the concentration of activated B in the p-body area. A conductance peak in the admittance spectroscopy of the 100% B device in depletion can be attributed to B. Hence, there is B in the channel area, however, in these devices the concentration of electrically active B in the p-body area is too low, but not negligibly small. No working p-body area leads to a continuous n-drift zone from drain to source, which results in a normally on parasitic JFET instead of MOSFET. SIMS measurements, which indicate the B concentration to be in the same range as the n-dopant concentration in the n-drift zone, give reason to believe, that with a higher initial B doping concentration in the channel area, a working MOSFET can be built. Hence, in theory, it is possible to replace Al entirely with B but two major correlating challenges must be overcome: First, the B concentration must not be too low to produce a desired p-body area and, second, the implanted B has to be sufficiently electrically activated.

As a conclusion, the concentration of activated B in channel area of the measured devices is too low, but as SIMS measurements show, the outdiffusion of implanted B is still manageable. In order to compensate the loss due to outdiffusion, a higher initial B concentration could be implanted. Further, it is important to find the optimal annealing temperature to minimize outdiffusion and to reach a high enough electrical activation of B.

APPENDIX

10.1 Additional Results from the Admittance Spectroscopy

10.1.1 Samples with Al and B doping combined

The following figures show results form 30% B and 10% B devices each compared to the reference sample. Also these were measured in depletion, depletion to inversion and inversion.

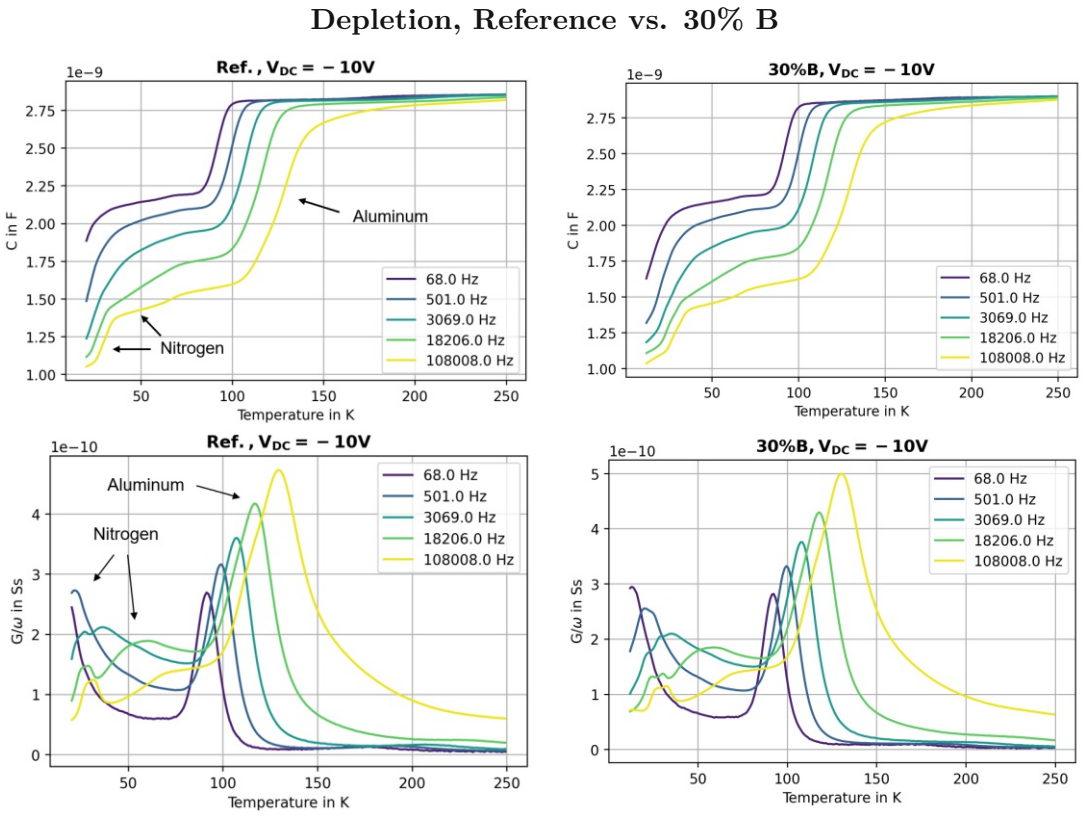


Figure 10.1.1: Admittance spectroscopy in depletion for the reference and the 30% B sample.

The B peak in conductance in depletion, that appeared in the 100% B device, cannot be found in the 30% B nor in the 10% B sample. This might be due to the lower B concentration in these two samples, compared to the 100% B one.

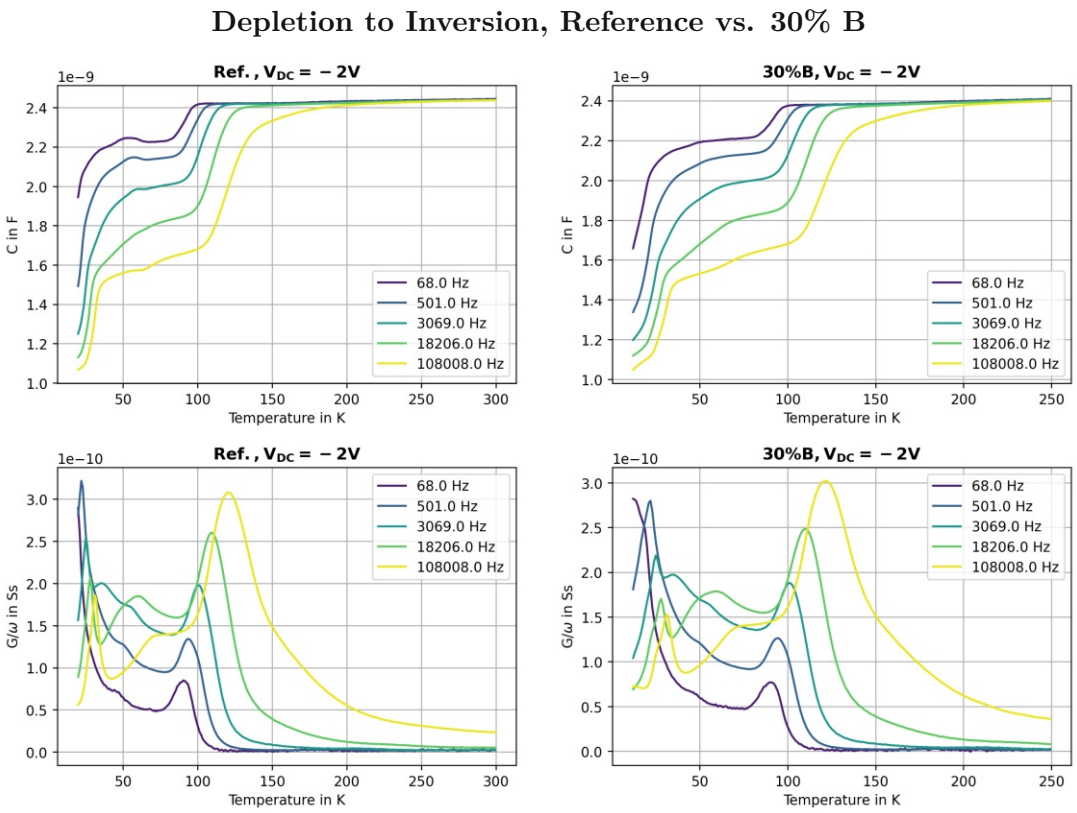


Figure 10.1.2: Admittance spectroscopy at depletion to inversion for the reference and the 30% B sample.

There seems to be no significant difference when comparing the 30% B and 10% B sample with the reference in depletion and depletion to inversion. Only when looking at the devices in inversion the $C(T)$ and $G/\omega(T)$ curves of the reference and B implanted devices differ. That can be explained by the different doping processes between the reference sample and the B implanted samples. The decrease in capacitance around 60 K can be caused by geometric effects in the device.

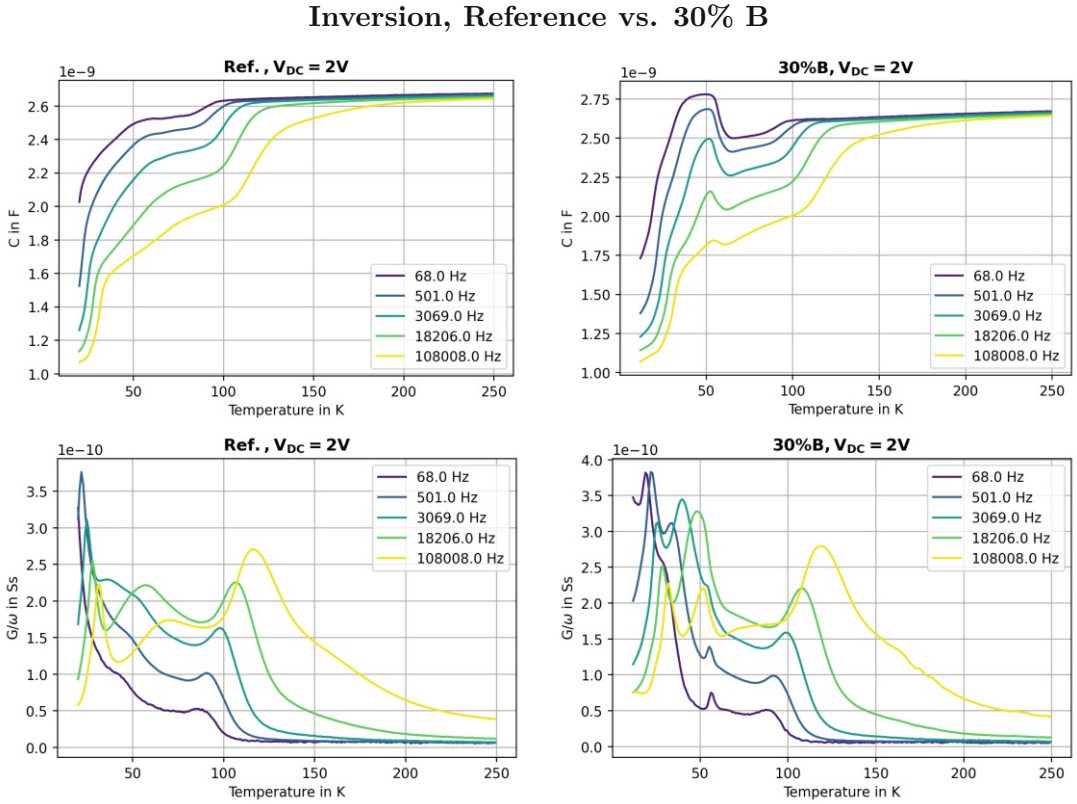


Figure 10.1.3: Admittance spectroscopy in inversion for the reference and the 30% B sample.

For the 30% B and 10% B samples only the highest frequency of 108 008 Hz is shown, when comparing them directly to the reference. The B related peak in the conductance should be most prominent at that frequency.

There are almost no differences in $C(T)$ and $G/\omega(T)$ between the reference and the B implanted devices, especially not in the depletion, where a B related peak is most likely to appear. This supports the hypothesis that there is not enough B left to detect it with admittance spectroscopy.

108008 Hz, Reference vs. 30% B

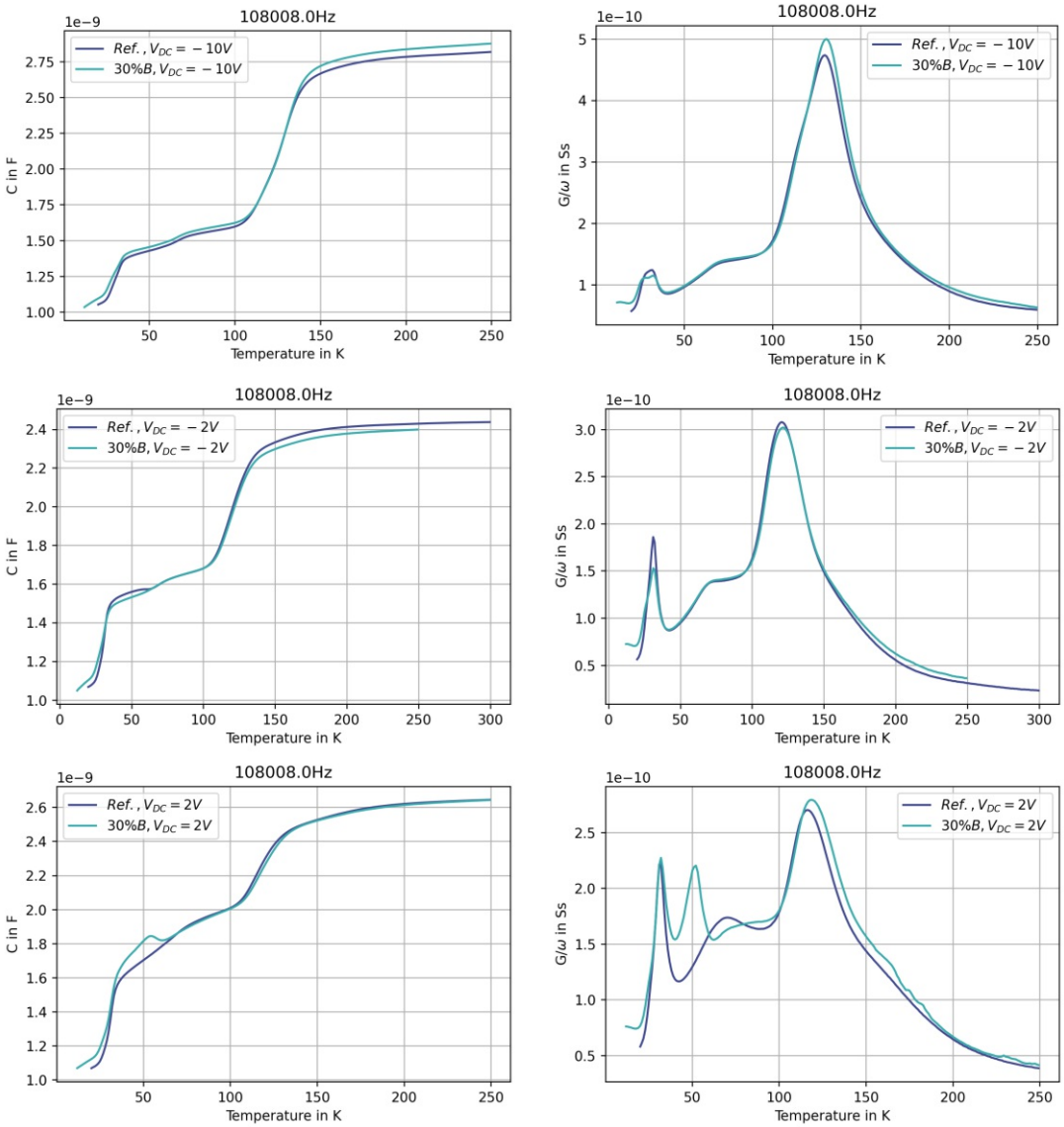


Figure 10.1.4: Admittance spectroscopy for the reference and the 30% B sample at 108 kHz.

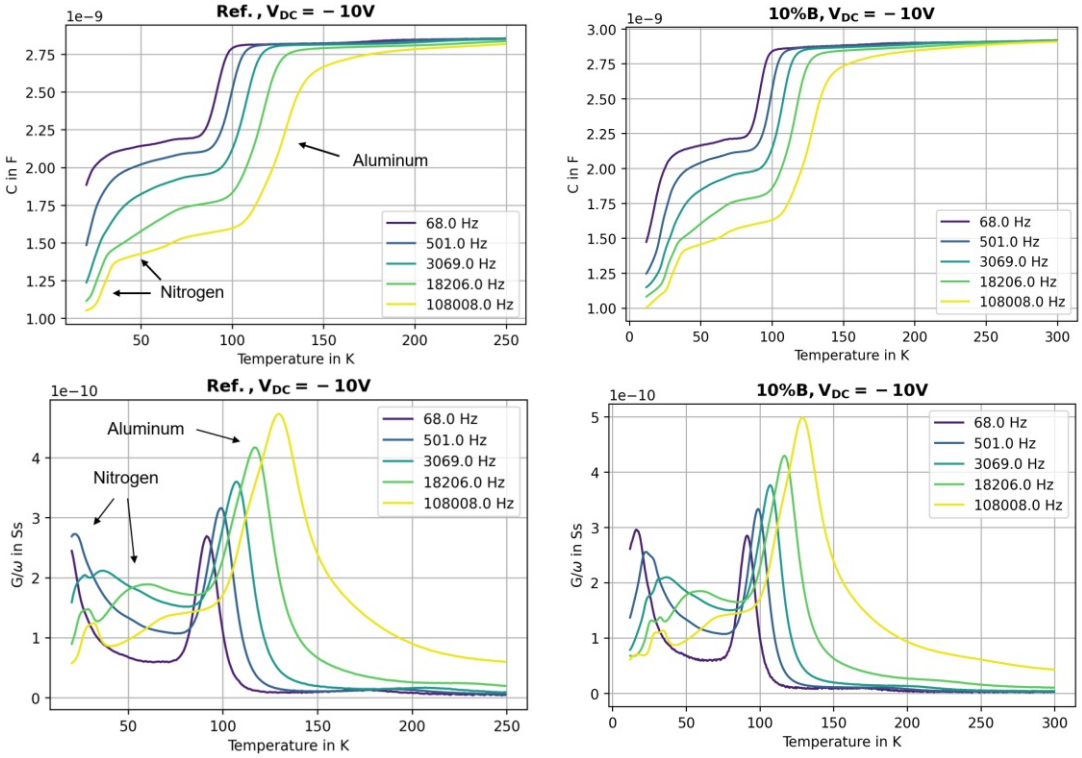


Figure 10.1.5: Admittance spectroscopy in depletion for the reference and the 10% B sample.

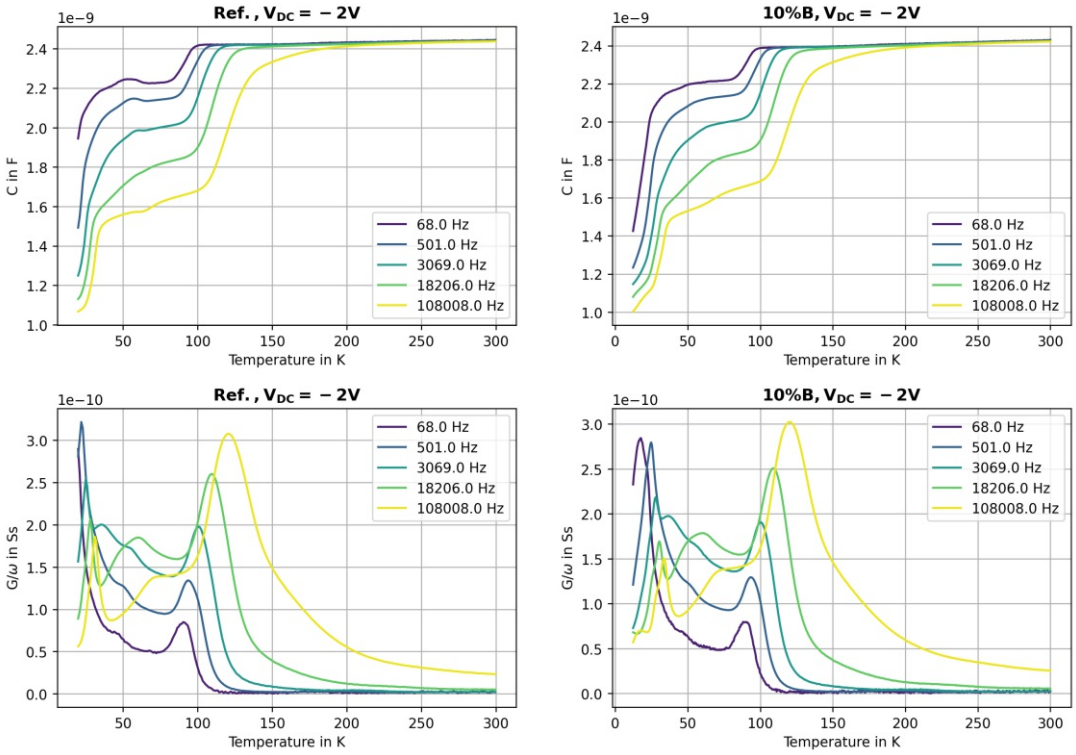


Figure 10.1.6: Admittance spectroscopy at depletion to inversion for the reference and the 10% B sample.

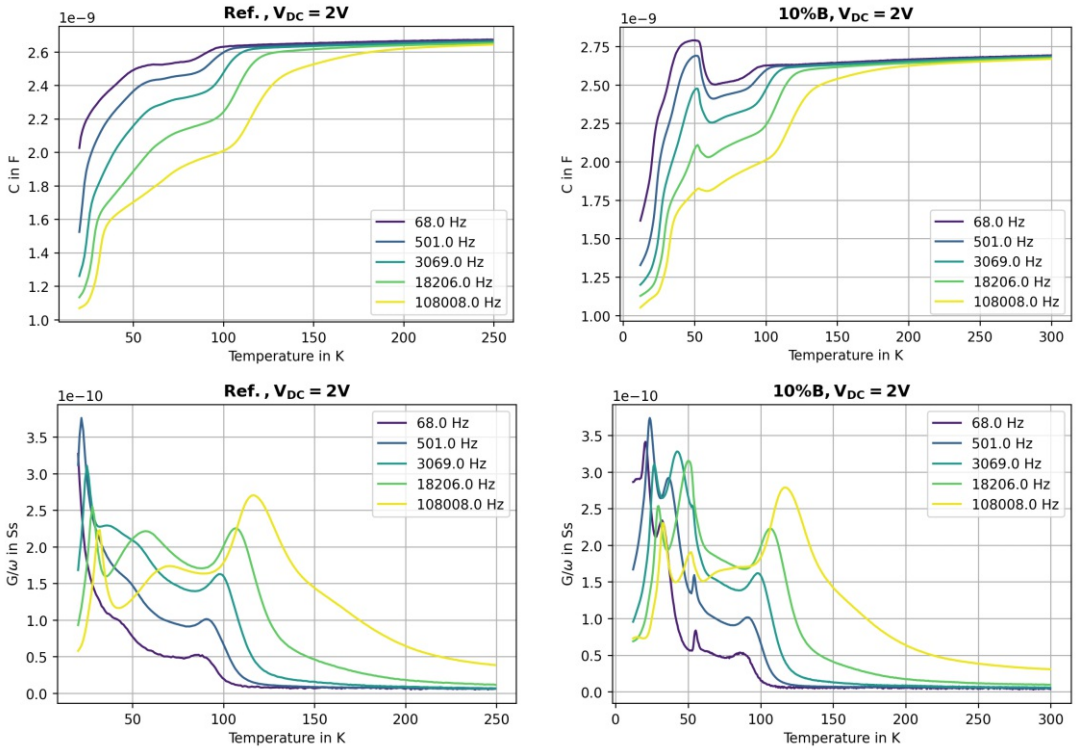


Figure 10.1.7: Admittance spectroscopy in inversion for the reference and the 10% B sample.

108008 Hz, Reference vs. 10% B

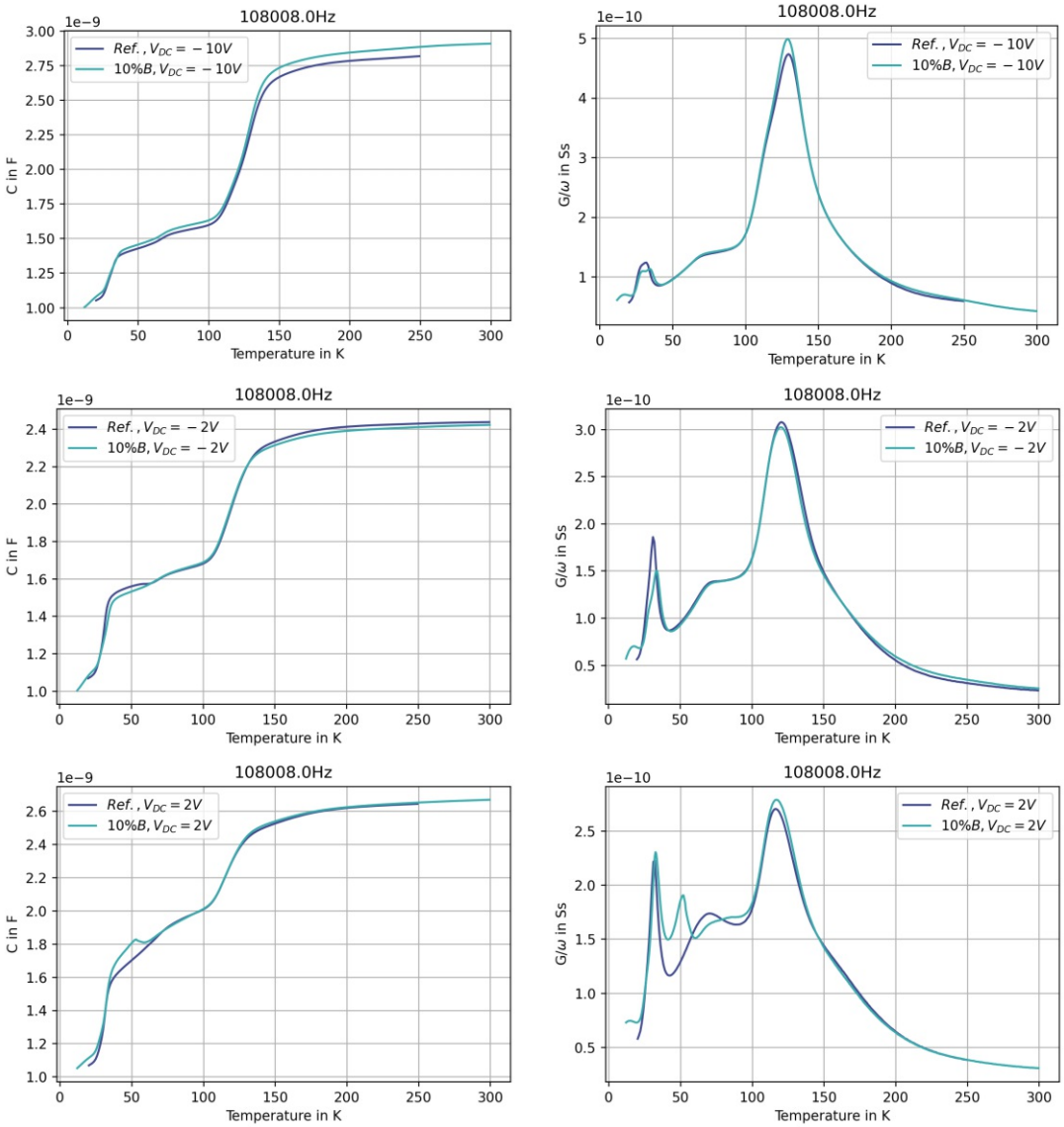


Figure 10.1.8: Admittance spectroscopy for the reference and the 10% B sample at 108 kHz.

List of Figures

Bibliography

[1] G. Chung, C. Tin, J. Williams, K. McDonald, R. Chanana, R. A. Weller, S. Pantelides, L. C. Feldman, O. Holland, M. Das *et al.*, "Improved inversion channel mobility for 4h-sic mosfets following high temperature anneals in nitric oxide," *IEEE Electron Device Letters*, vol. 22, no. 4, pp. 176–178, 2001.

[2] J. Rozen, A. C. Ahyi, X. Zhu, J. R. Williams, and L. C. Feldman, "Scaling between channel mobility and interface state density in sic mosfets," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 3808–3811, 2011.

[3] K. Chain, J.-h. Huang, J. Duster, P. K. Ko, and C. Hu, "A mosfet electron mobility model of wide temperature range (77-400 k) for ic simulation," *Semiconductor science and technology*, vol. 12, no. 4, p. 355, 1997.

[4] J. Berens, F. Rasinger, T. Aichinger, M. Heuken, M. Krieger, and G. Pobegen, "Detection and cryogenic characterization of defects at the sio 2/4h-sic interface in trench mosfet," *IEEE Transactions on Electron Devices*, vol. 66, no. 3, pp. 1213–1217, 2019.

[5] L. Balogh, "Design and application guide for high speed mosfet gate drive circuits," in *Power Supply Design Seminar SEM-1400, Topic*, vol. 2, 2001.

[6] T. Kimoto and J. A. Cooper, *Fundamentals of silicon carbide technology: growth, characterization, devices and applications*. John Wiley & Sons, 2014.

[7] J. Rozen, "Electronic properties and reliability of the sio2/sic interface," Ph.D. dissertation, Vanderbilt University, 2008.

[8] J. Casady and R. W. Johnson, "Status of silicon carbide (sic) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics*, vol. 39, no. 10, pp. 1409–1422, 1996.

[9] N. Son, W. Chen, O. Kordina, A. Konstantinov, B. Monemar, E. Janzen, D. Hofman, D. Volm, M. Drechsler, and B. Meyer, "Electron effective masses in 4h sic," *Applied physics letters*, vol. 66, no. 9, pp. 1074–1076, 1995.

[10] A. Evwaraye, S. Smith, and W. Mitchel, "Shallow and deep levels in n-type 4h-sic," *Journal of applied physics*, vol. 79, no. 10, pp. 7726–7730, 1996.

[11] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, J. Heindl, H. Strunk, and M. Maier, "Doping of sic by implantation of boron and aluminum," *physica status solidi (a)*, vol. 162, no. 1, pp. 277–298, 1997.

[12] R. Nipoti, H. M. Ayedh, and B. G. Svensson, "Defects related to electrical doping of 4h-sic by ion implantation," *Materials Science in Semiconductor Processing*, vol. 78, pp. 13–21, 2018.

[13] S. Sasaki, J. Suda, and T. Kimoto, "Lattice mismatch and crystallographic tilt induced by high-dose ion-implantation into 4h-sic," *Journal of Applied Physics*, vol. 111, no. 10, p. 103715, 2012.

[14] R. Nipoti, A. Parisini, G. Sozzi, M. Puzzanghera, A. Parisini, and A. Carnera, "Structural and functional characterizations of al+ implanted 4h-sic layers and al+ implanted 4h-sic pn junctions after 1950° c post implantation annealing," *ECS Journal of Solid State Science and Technology*, vol. 5, no. 10, p. P621, 2016.

[15] K. Danno, D. Nakamura, and T. Kimoto, "Investigation of carrier lifetime in 4 h-si c epilayers and lifetime control by electron irradiation," *Applied physics letters*, vol. 90, no. 20, p. 202109, 2007.

[16] P. B. Klein, "Identification and carrier dynamics of the dominant lifetime limiting defect in n–4h-sic epitaxial layers," *physica status solidi (a)*, vol. 206, no. 10, pp. 2257–2272, 2009.

[17] Y. A. Vodakov, "Diffusion of boron and aluminium in n-sic," *Sov. Phys. Solid State*, vol. 8, p. 1040, 1966.

[18] J. Ryu, H. Kim, R. Davis, T. Sedgwick, T. E. Seidel, and B. Tsaur, "Rapid thermal processing," vol. 52, p. 165, 1986.

[19] S. Ahmed, C. Barbero, and T. Sigmon, "Activation of ion implanted dopants in α-sic," *Applied physics letters*, vol. 66, no. 6, pp. 712–714, 1995.

[20] M. W. C. M. Bohn, HG, "Recrystallization of ionimplanted &sic," *J. Mater. Sci*, vol. 2, p. 107, 1987.

[21] S. Y. Chou, Y. Chang, K. Weiner, T. Sigmon, and J. Parsons, "Annealing of implantation damage and redistribution of impurities in sic using a pulsed excimer laser," *Applied physics letters*, vol. 56, no. 6, pp. 530–532, 1990.

[22] D. Peters, R. Siemieniec, T. Aichinger, T. Basler, R. Esteve, W. Bergner, and D. Kueck, "Performance and ruggedness of 1200v sic—trench—mosfet," pp. 239–242, 2017.

[23] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2006.

[24] G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser, "On the subthreshold drain current sweep hysteresis of 4h-sic nmosfets," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016, pp. 10–8.

[25] J. Cottom, G. Gruber, G. Pobegen, T. Aichinger, and A. Shluger, "Recombination defects at the 4h-sic/sio2 interface investigated with electrically detected magnetic resonance and ab initio calculations," *Journal of Applied Physics*, vol. 124, no. 4, p. 045302, 2018.

[26] G. Gruber, "Performance and reliability limiting point defects in sic power devices," *Technischen Universität Graz*, 2016.

[27] G. Ghibaudo, "New method for the extraction of mosfet parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988.

[28] E. H. Nicollian, J. R. Brews, and E. H. Nicollian, *MOS (metal oxide semiconductor) physics and technology*. Wiley New York, 1982, vol. 1987.

[29] D. Lang, J. Cohen, J. Harbison, M. Chen, and A. Sergent, "Resolution of the a-si: H dlts energy scale controversy," *Journal of Non-Crystalline Solids*, vol. 66, no. 1-2, pp. 217–222, 1984.

[30] W. Shockley and W. Read Jr, "Statistics of the recombinations of holes and electrons," *Physical review*, vol. 87, no. 5, p. 835, 1952.

[31] D. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of applied physics*, vol. 45, no. 7, pp. 3023–3032, 1974.

[32] G. Vincent, D. Bois, and P. Pinard, "Conductance and capacitance studies in gap schottky barriers," *Journal of Applied Physics*, vol. 46, no. 12, pp. 5173–5178, 1975.

[33] S. Smith, A. Evwaraye, and W. Mitchel, "Admittance spectroscopy of 6h, 4h, and 15r silicon carbide," *physica status solidi (a)*, vol. 162, no. 1, pp. 227–238, 1997.

[34] J. V. Berens, "Carrier mobility and reliability of 4h-sic trench mosfets," Ph.D. dissertation, Wien, 2021.

[35] W. Kaindl, M. Lades, N. Kaminski, E. Niemann, and G. Wachutka, "Experimental characterization and numerical simulation of the electrical properties of nitrogen, aluminum, and boron in 4h/6h-sic," *Journal of electronic materials*, vol. 28, no. 3, pp. 154–160, 1999.

Glossary

Al aluminum.

As arsenic.

B boron.

C carbon.

DLTS Deep Level Transient Spectroscopy.

Ga gallium.

ID-DLTS Drain Current - Deep Level Transient Spectroscopy.

JFET junction gate field effect transistor.

MOS Metal Oxide Semiconductor.

MOSFET metal oxide semiconductor field effect transistor.

N nitrogen.

P phosphorous.

Si silicon.

SiC silicon carbide.

SiO_2 silicon dioxide.

Symbols

A area of depletion region.

B susceptance.

$C_{\mathbf{P}}$ parallel capacitance.

$C_{\mathbf{T}}$ capacitance of a trap level.

$C_{\mathbf{dr}}$ depletion layer capacitance.

$C_{\mathbf{equil.}}$ equilibrium capacitance.

$C_{\mathbf{m}}$ measured capacitance.

$C_{\mathbf{ox}}$ oxide capaxitance.

C capacity.

D difference.

$E_{\mathbf{A}}$ activation energy of acceptor.

$E_{\mathbf{B}}$ binding energy.

$E_{\mathbf{C}}$ conduction band.

$E_{\mathbf{F}}$ Fermi level.

$E_{\mathbf{T}}$ Energy of trap lavel.

$E_{\mathbf{V}}$ valence band.

$E_{\mathbf{gap}}$ band gap.

$E_{\mathbf{i}}$ intrinsic Fermi-level.

$E_{\mathbf{t}}$ activation energy of trap level.

$G_{\mathbf{P}}$ parallel conductance.

$G_{\mathbf{T}}$ conductance of a trap level.

$G_{\mathbf{m}}$ measured conductance.

G conductance.

$I_{\mathbf{D}}$ drain current.

I current.

L channel length.

$N_{\mathbf{A}}^{-}$ number of ionized acceptors.

$N_{\mathbf{A}}$ number of acceptors.

$N_{\mathbf{C}}$ effective desity of states in the conduction band.

$N_{\mathbf{T}}$ number of traps.

$N_{\mathbf{V}}$ effective desity of states in the valence band.

P propability for a trap to be filled.

$Q_{\mathbf{S}}$ space-charge density.

Q charge.

$R_{\mathbf{S}}$ series resistance.

$T_{\mathbf{max}}$ termperature where difference in capacity reaches maximum.

T temperature.

$V_{\mathbf{D}}$ diffusion voltage.

$V_{\mathbf{FB}}$ flat band voltage.

$V_{\mathbf{G}}$ gate volatage.

$V_{\mathbf{bi}}$ built in voltage.

$V_{\mathbf{ext}}$ erternal voltage.

$V_{\mathbf{ox}}$ voltage across oxide.

$V_{\mathbf{th}}$ threshold voltage.

V voltage.

$W_{\mathbf{0}}$ initial depletion region width.

$W_{\mathbf{dr}}$ depletion region width.

W channel width.

X reactance.

$Y_{\mathbf{P}}$ parallel admittance.

Y admittance.

Z impedance.

$\Phi_{\mathbf{Bp}}$ potential difference between E_{i} and E_{F}.

$\Phi_{\mathbf{S}}$ surface potential.

$\Phi_{\mathbf{p}}$ potential.

Θ mobility reduction coefficient.

$\delta V_{\mathbf{0}}$ lamplitude of AC signal.

$\delta V_{\mathbf{AC}}$ AC signal.

$\delta W_{\mathbf{AC}}$ change in depletion region width through ac signal.

$\delta W_{\mathbf{dr}}$ change in the depletion region.

$\epsilon_{\mathbf{S}}$ permitivity of the semiconductor.

ϵ permitivity.

$\mu_{\mathbf{0}}$ low field carrier mobility.

μ mobility.

ω omega.

ϕ phase shift.

$\psi_{\mathbf{Bp}}$ energy difference between E_{F} and E_{i}.

ψ phase.

ρ local density of charge.

$\sigma_{\mathbf{n}}$ capture cross section of electrons.

$\sigma_{\mathbf{p}}$ capture cross section of holes.

σ capture cross section.

τ AC signal period.

τ emission time.

$c_{\mathbf{n}}$ capture rate of electrons.

$c_{\mathbf{p}}$ capture rate of holes.

c capture of carriers.

d oxide thicckness.

$e_{\mathbf{n}}$ emission rate of electrons.

$e_{\mathbf{p}}$ emission rate of holes.

e emission of carriers.

f frequency.

$g_{\mathbf{A}}$ degeneracy factor (acceptors).

g transconductance.

k Boltzmann constant.

$n_{\mathbf{T}}$ electron occupancy of a defect state.

$n_{\mathbf{i}}$ intrinsic carrier density of undoped semiconductor.

n negative charged carrier, electron.

p positve charged carrier, holes.

q elementary charge.

t time.

$v_{\mathbf{C}}$ Carbon vacancy.

$v_{\mathbf{th\ n}}$ thermal velocity of electrons.

$v_{\mathbf{th\ p}}$ thermal velocity of holes.

$v_{\mathbf{th}}$ thermal velocity.