DISSERTATION

Degradation of Electrical Parameters of Power Semiconductor Devices – Process Influences and Modeling

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Abstract

Power semiconductor switches are utilized in cars, trains, the power supply system, industrial automation and many other fields. They allow to electrically connect and disconnect loads from sources despite large supply currents. The actual switch is nowadays a metal oxide semiconductor (MOS) field effect transistor (MOSFET). These devices conduct the load current directly at the interface between the oxide and the semiconductor.

Since the application of these devices inherently requires steady functionality, which can naturally only be guaranteed for finite time durations, investigations towards the reliability of such devices is important. Reliability is the probability for the operation of a product without failure for a given time under specified conditions. Semiconductor manufacturers try to increase the probability for the full operation of the product to the highest possible level. However, reliable product operation can only be guaranteed up to the target lifetime of a device which is about ten years in the automotive market.

Limits for the reliability of MOSFETs can result from imperfections of the materials used to manufacture the device as well as from degradation mechanisms which occur during operation. While imperfections or impurities which interfere with the device performance can usually be ruled out at the end of the production process through burn-in tests, degradation mechanisms which eventually occur after years of operation are challenging to characterize and understand. The key to reliable devices is to understand the influences which accelerate the degradation, and to use this knowledge to transfer the degradation behavior from qualifying tests to the whole lifetime period. Such lifetime projections to use conditions can be done by scaling degradation measurement results with temperature, device area, voltage or with percentile of a failure criterion. The only possibility for device manufacturers to advance the reliability of devices is then to adjust particular processing parameters during production. The impact of these adjustments are then identified with qualifying tests which reflect the long-term degradation behavior of the device to the largest possible extent.

A power MOSFET operated within the defined automotive temperature range of $-40\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$, usually experiences only electric fields across the gate oxide which are well below the breakdown field of the gate oxide. Still, these use conditions can already lead to an instability of the threshold voltage of the MOSFET which in turn reduces the drain current and the cutoff frequency. In extreme cases, the threshold voltage might increase such that complete failure occurs. This effect is usually referred to as bias temperature instability (BTI). Compared to other degradation mechanisms which affect MOSFETs, BTI occurs close to the equilibrium condition of the device (room temperature, little bias) whereas other mechanisms as for example time dependent dielectric breakdown (TDDB) or hot carrier degradation (HCD) occur at large gate or drain bias, respectively. As a logical consequence, the BTI which occurs already at weak stress conditions is investigated in detail in this thesis before any other mechanism at harsher conditions can be studied.

One of the main results of the present work is that the occurrence of BTI is hypothesized to be due the electrical activation of initially electrically inactive point defect precursors during stress. The range of the mean activation energies of a part of the available precursors is known to be between 1.5 eV and 2.9 eV. Such rather large activation energies would need hundreds of years of continuous stress at typical BTI conditions of 100 °C to 200 °C until a measurable amount of defect precursors become activated. In this thesis, support is given for the assumption that activation energies for point defect precursors follow a very broad normal distribution, and only the low-energy tail of the distribution is activated during device operation.

Kurzfassung

Halbleiterschalter für Leistungsanwendungen haben eine breite Anwendungpalette in Personenkraftwagen, im Schienenverkehr, im Stromnetz, in der industriellen Automatisierung und in vielen anderen Bereichen. Sie ermöglichen das elektrische Verbinden und Trennen von Strom- und Spannungsquellen von ihrer Last trotz großer Versorgungsströme. Der eigentliche Schalter ist heutzutage ein Metall-Oxid-Halbleiter Feldeffekttransistor (englisch: MOSFET). Diese Strukturen leiten den Strom direkt an der Grenzfläche zwischen dem Oxid und dem Halbleiter.

Da die Anwendung dieser Bauteile von Natur aus eine fortwährenden Funktionalität voraussetzt, die aber klarerweise nur für einen begrenzten Zeitraum sichergestellt werden kann, sind Untersuchungen bezüglich der Zuverlässigkeit solcher Bauteile unerlässlich. Dabei ist Zuverlässigkeit die Wahrscheinlichkeit für den Betrieb eines Produkts ohne Ausfall über einen definierten Zeitraum unter definierten Bedingungen. Halbleiterhersteller versuchen die Wahrscheinlichkeit für das ordnungsgemäße Funktionieren des Produkts auf das größtmögliche Maß zu erhöhen. Tatsächlich kann der zuverlässige Betrieb des Produkts nur für eine begrenzte Ziellebensdauer garantiert werden. In der Automobilindustrie beträgt diese geplante Lebensdauer in etwa zehn Jahre.

Grenzen für die Zuverlässigkeit eines MOSFET können aus Defektstellen der Materialien die für den Aufbau des Bauteils verwendet werden resultieren, aber auch erst durch Degradationmechanismen während des Betriebs entstehen. Während Fehlstellen oder Unreinheiten, die mit dem Verhalten des Bauteils wechselwirken, noch am Ende der Prozessierung durch Frühfehlerüberprüfungen erkannt werden können, sind Degradationsmechanismen, welche erst nach Jahren der Verwendung des Bauteils auftreten können, sehr schwierig zu charakterisieren und zu untersuchen. Der Schlüssel zu zuverlässigen Bauteilen liegt nun darin, jene Einflüsse genauer zu verstehen, welche die Degradation beschleunigen und dieses Wissen zu nutzen um das Verhalten in Qualifikationstest auf die Lebensdauer des Bauteils zu übertragen. Für MOSFETs kann der Transfer der Ergebnisse einer Degradationsmessung zu Einsatzbedingungen entweder über die Temperatur, die Bauteilgröße, die Spannung oder aber auch über die statistische Häufigkeit erfolgen. Die einzige Möglichkeit für Halbleiterhersteller die Zuverlässigkeit der Bauteile weiter zu verbessern ist es, spezielle Prozesseinstellungen der Produktion zu verändern. Die Einflüsse dieser Adjustierungen werden dann mit Qualifikationstests bewertet, welche das Langzeitdegradationsverhalten des Bauteils bestmöglich abbilden.

Ein Leistungs-MOSFET betrieben im festgesetzten Temperaturbereich der Automobilindustrie zwischen $-40\,^{\circ}\mathrm{C}$ und $150\,^{\circ}\mathrm{C}$ wird normalerweise nur mit Oxidfelder viel kleiner als die Durchbruchspannung des Oxids belastet. Trotzdem können diese Betriebsbedingungen bereits eine Instabilität der Einsatzspannung des MOSFET verursachen, die den maximalen Senkenstrom und die Grenzfrequenz des Transistors reduziert. Im Extremfall kann die Einsatzspannung auch soweit vergrößert werden, dass der Transistor überhaupt nicht mehr einschaltet. Man nennt diesen Effekt

überlicherweise Spannungs-Temperatur Instabilität (englisch: bias temperature instability, BTI). Verglichen zu anderen Degradationsmechanismen welche MOSFETs beeinflussen, tritt BTI nahe am Gleichgewichtszustand des Bauteils auf (Raumtemperatur, kleine Spannung), während andere Mechanismen wie zum Beispiel der Oxiddurchbruch bei hohen Steuerelektrodenspannungen beziehungsweise Degradation durch hochenergetische Ladungsträger bei hohen Quellenspannungen auftreten. Als logische Konsequenz wird in dieser Arbeit BTI untersucht, da man zuerst jenen Mechanismus verstanden haben muss der bei Betriebsbedingungen auftritt, bevor man die Degradation unter raueren Bedingungen untersucht.

Eines der Hauptresultate der vorliegenden Arbeit ist die Untermauerung der Hypothese, dass BTI die elektrische Aktivierung von zuerst elektrisch inaktiven Präkursor-Defekten während der Belastung ist. Der Bereich der mittleren Aktivierungsenergien dieser Präkursor ist bekannt und wird mit 1.5 eV bis 2.9 eV angegeben. Mit diesen eher großen Aktivierungsenergien würde es hunderte Jahre dauern bis die Präkursor unter typischen BTI Bedingungen aktiviert werden. Die vorliegende Arbeit unterstützt die Annahme, dass die Aktivierungsenergien für die Präkursor-Defekte einer sehr breiten Normalverteilung gehorchen und dass nur der niedrigenergetische Ausläufer der Verteilung während der Betriebsdauer des Bauteils aktiviert wird.

Contents

Disclaimer

A few of the central findings of this thesis base on material which has been partly published during the work on the thesis in different forms of media like journal publications, conference proceedings and contributions to a book. See own publications list at the end of the thesis. According to the consensus of several guidelines of Austrian funding agencies and Austrian Universities regarding proper scientific work [Gam09], the ideas of these publications are re-used with explicit citation at several positions in this thesis. The thesis puts the individual topics of the publications together with unreported topics into a larger context.

Ich erkläre hiermit an Eides statt, dass ich die vorliegende Arbeit selbständig sowie ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel angefertigt habe. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet.

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1

Introduction

The present thesis is based on the excellent work of many researchers who dealt with the reliability of metal oxide semiconductor (MOS) devices during the last five decades. In the following a rough and short overview of the literature which was of particular interest for the results of the thesis are summarized. The following compilation is not complete and only introduces a few of the concepts used in this thesis.

1.1 Degradation mechanisms and their characteristics

Based on previous work on possibly lifetime limiting effects in MOS field effect transistors (MOSFETs) [Sch06], a separation of degradation mechanisms into a few mechanisms can be performed. Only two of them, which are of particular importance in this thesis, are presented here.

1.1.1 Bias temperature instability

The positive or negative bias temperature instability (BTI) has become the most prominent degradation mechanism during the last couple of years, limiting the reliability of state-of-the-art MOSFETs in the whole application range from deca-nanometer sized devices for fast switching of low currents [TL+11b; Fra+12; Lee+13] to millimeter sized power devices which are capable of switching several Amperes [Are+08]. BTI occurs through the application of positive or negative voltage at the gate with respect to all other terminals of the device at elevated temperatures as 50 °C to 200 °C. The mechanism is temperature activated, meaning that higher temperatures increase the magnitude of the degradation [GN66; MM66]. The measurable result of bias temperature stress (BTS) is a reduction of the drain current due to a shift of the threshold voltage V_{TH} and a reduction of the channel mobility μ_{FET} [GN66; MM66; JS77; Kac+08]. Negative BTI (NBTI) is more severe in p-channel MOSFETs (pMOSFETs) where it shifts the V_{TH} towards larger negative values, indicating the creation of positive charges close to the semiconductor-insulator interface [AM05; HDP06; Sch07]. Consistently, the application of positive bias at the gate causes an accumulation of electrons at the semiconductor-insulator interface which typically results in a V_{TH} shift towards more positive values, indicating the creation of negative charges.

BTS may occur due to biasing of the device close to or above the maximum operation voltage range, during operation of the device at elevated temperatures or because of combinations of both. The magnitude of the degradation measured by the shift of the threshold voltage ΔV_{TH} varies approximately as a power of the stress duration t_{str} [JS77].

1.1.2 Hot carrier degradation

When a MOSFET is operated with a voltage across source and drain, the carriers in the channel of the device are accelerated by the lateral electric field. For increasing source drain bias, the kinetic energy of the carriers eventually becomes sufficiently large to overcome a potential barrier for the activation of point defects close to the semiconductor-insulator interface [Sch06]. These point defects act as charges at the interface and interfere with the performance of the device. The term *hot* thereby indicates the large kinetic energy of the carriers. Similarly to BTI, hot carrier degradation (HCD) is observable as a decrease of the drain current due to a shift of the threshold voltage V_{TH} and a decrease of the mobility μ_{FET} [Sch06; RR10; BH10; TG12].

The degradation is usually most efficient at positions along the channel where the carriers have the largest kinetic energy. This causes a strong localization of the created damage near the drain side of the MOSFET [TG12]. The high energetic carriers may also cause impact ionization close to the drain of the MOSFET [Sch06; TG12]. If the creation of an electron-hole pair through impact ionization occurs within the volume of the space charge region of the drain-body diode of the MOSFET, the electric field of the space charge region separates the pair. This leads to an impact ionization induced current between the body and the drain of the MOSFET [BH10]. For a fixed drain bias, the body current increases with increasing gate voltage up to a maximum point, where the mechanism is most efficient, before it decreases as the transistor enters its linear region [Sch06]. This peak in the body current occurs for silicon (Si) devices with a channel length in the micrometer range at a gate voltage of $V_{\mathrm{G}} = 1/\alpha \times V_{\mathrm{D}}$ with $\alpha = 2\text{–}3$ [BH10]. The biasing for the maximum of the body current is also considered to be efficient for HCD [TG12].

1.2 Methods

The electrically observable result of a degradation mechanism like BTI is a change of the parameters of the transistor. Thereby, the threshold voltage V_{TH} and mobility of the MOSFET μ_{FET} decrease. Usually, only the change of the threshold voltage is investigated since it is directly proportional to the number of charges created at the interface or within the oxide. If the charges are situated at the exact interface between the oxide and the semiconductor their number is straightforwardly calculated as

$$N = -\frac{C_{\mathrm{ox}} \Delta V_{\mathrm{TH}}}{q}, \tag{1.1}$$

where C_{ox} is the oxide capacitance per square centimeter and q the elementary charge. A distribution of charges $\rho(x)$ along the depth within the oxide x, where x is zero at the gate-oxide interface

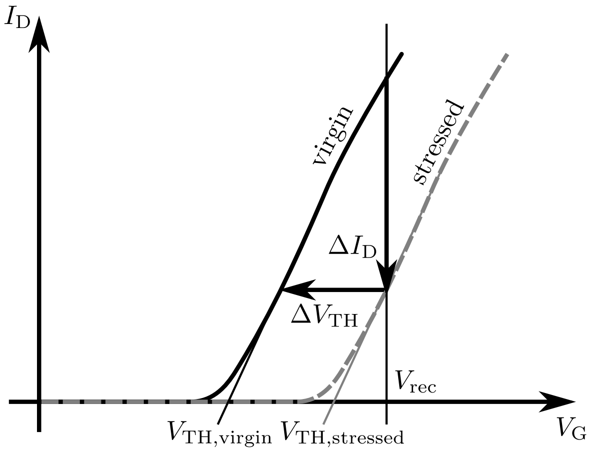

Fig. 1.1: Schematics of the effective change of the drain current of a pMOSFET transistor with a shift of V_{TH}. Neglecting transconductance changes a decrease of the drain current ΔI_D at constant gate bias V_G can be mapped to a threshold voltage shift ΔV_{TH}.

and d_{ox} at the oxide-semiconductor interface, gives rise to a threshold voltage drift according to the Gauss law as [See; Sch06]

$$\Delta V_{TH} = -\frac{1}{C_{ox}}\frac{1}{d_{ox}}\int_0^{d_{ox}} x\rho(x)\mathrm{d}x. \tag{1.2}$$

Due to the partial recovery of the charges created during BTS [Sch07], it is important to measure ΔV_{TH} in a time-resolved manner after termination of stress.

1.2.1 Time-resolved ΔV_{TH} measurements

Fig. 1.1 shows the concept of how the change of the threshold voltage is calculated from a change in the drain current [Kac+08]. This approach has several advantages:

- The measurement is a simple time-resolved current measurement for constant biases and can be performed usually on standard equipment with low experimental effort.
- Stress-induced degradation recovers quickly after a switch from stress to recovery bias. This raises the need to measure the drain current with a minimum delay after the gate voltage switch. With modern parameter analyzer equipment 100 µs to 10 ms delay times are possible. To further reduce the time to the first data point special setups using fast operational amplifiers are used [Rei+06]. The delay time of these setups is limited by the inverse of the maximum transfer frequency of the operational amplifier, which is approximately 1 µs. For even faster measurements the impedance of the gate of the transistor needs to be matched with the output impedance of the source measurement unit (SMU).
- Depending on the biasing of the MOSFET, the drain current is usually in the µA to mA range. Such currents can be measured with good accuracy. This leads to a very low noise level in the ΔV_{TH} transients typically below 1 mV.

However, there are also several disadvantages connected with this method:

- The drain current depends on the mobility and on the threshold voltage of the device. Since BTI changes both parameters, the ΔV_{TH} value calculated from ΔI_D is polluted with mobility changes. However, usually it is assumed that close to the threshold voltage of the device the impact of mobility changes is very small and can thus be neglected.

- The change in the drain current depends, to a small extend, on the supplied drain voltage. While it is important to keep the drain bias low during recovery to ensure symmetrical recovery conditions along the channel, a larger drain bias reduces the influence of mobility changes on the extracted ΔV_{TH} value [Aic10].

- The recovery voltage after BTS must be in a range where the drain current is large enough to be measured. So in a simplified view, for an n-channel MOSFET (nMOSFET) only positive recovery voltages and for a pMOSFET only negative recovery voltages are possible, respectively. In particular, it is not possible to measure the recovery after BTS at the flat-band voltage, which would be very beneficial to determine the number of oxide charges created during stress. However, through a combination of measurements on nMOSFETs and pMOSFETs it is possible to acquire recovery data at arbitrary recovery voltages [ANG09b]. Also, the response at the threshold voltage following bias phases at arbitrary voltages can be studied [Gra+13a].

Despite these disadvantages, the measurement of the ΔV_{TH} by recording the ΔI_{D} will be predominantly used throughout this thesis.

1.2.2 Charge pumping

Charge pumping (CP) is a measurement method where the gate voltage is periodically switched such that the MOSFET is brought from inversion to accumulation and vice versa. At every transition from the inversion to the accumulation phase a fraction of all charges remain in traps close to the interface due to finite trap emission time constants. In the subsequent accumulation phase these carriers are emitted and recombine with oppositely charged carriers of the body. This results in a current between the source-drain junctions and the bulk or body junction. This current is proportional to the density of traps with time constants smaller than about half of the inverse of the frequency [BJ69].

The commonly acknowledged model for CP is based on the Shockley–Read–Hall (SRH) theory [SR52; Hal52] for recombinations in semiconductors, which was extended for fast responding interface traps at the semiconductor-insulator interface [Gro+84]. The central result of the CP model is the equation

$$I_{\mathrm{CP}} = q D_{\mathrm{IT}} f A \Delta E_{\mathrm{CP}}, \tag{1.3}$$

where D_{IT} is the density of interface traps averaged across ΔE_{CP}, f the frequency of the trapezoidal gate voltage signal, A the area of the gate of the MOSFET and ΔE_{CP} the energy range symmetrically around the middle of the band gap of the semiconductor. This energy is given by

$$\Delta E_{\mathrm{CP}} = 2 k_{\mathrm{B}} T \ln\left(v_{\mathrm{th}} n_{\mathrm{i}} \sqrt{\sigma_{\mathrm{n}} \sigma_{\mathrm{p}}} \frac{|V_{\mathrm{FB}} - V_{\mathrm{TH}}|}{\Delta V_{\mathrm{G}}} \sqrt{t_{\mathrm{f}} t_{\mathrm{r}}} \right), \tag{1.4}$$

where v_{th} is the thermal drift velocity, n_{i} the intrinsic carrier density, σ_{n} and σ_{p} are the capture cross sections of an interface trap for electrons and holes, respectively, V_{FB} and V_{TH} are the flat-band and the threshold voltage of the device, respectively, ΔV_{G} is the voltage swing of the gate voltage signal and t_{f} and t_{r} are the falling and the rising times of the gate voltage signal, respectively.

The method is very precise, average interface trap densities down to about $10^9\,\mathrm{cm}^{-1}\,\mathrm{eV}^{-2}$ or even individual charges [SGD96] can be resolved.

1.3 Semiconductor-insulator interface point defects

Electron spin resonance (ESR), which is also frequently referred as electron paramagnetic resonance (EPR), allows investigating the composition of point defects in semiconductors and insulators by analysis of the interaction of microwave absorption or carrier generation/recombination processes under the influence of a magnetic field [Lep72; WB06; LSS11]. In detail, the interaction occurs with unpaired electrons of unsaturated atomic bonds. For a semiconductor-insulator system these paramagnetic point defects may act as trapped charges which change the device parameters. Consequently, ESR investigations are very valuable for device degradation research.

In the following the most important results of ESR studies of the interface between silicon (Si) and silicon dioxide (SiO_2) are reviewed. Subsequently, the manifold reactions of hydrogen with point defects near the Si-SiO_2 interface are discussed to provide a basis for the discussions in the subsequent Chapters. To divide between the possible reactions, the two most prominent point defects, the dangling bond on a Si atom at the Si-SiO_2 interface (P_b center) and the dangling bond on a Si atom bonded to three oxygen (O) atoms within the SiO_2 (E' center), are handled individually, while other reactions are only briefly summarized. A few of the conclusions of this review Section are also documented in [PAN p].

1.3.1 P_b center

The natural lattice mismatch between silicon (Si) and the amorphous layer of thermally grown silicon dioxide (SiO_2) causes the existence of unsaturated bonds at the interface of these two materials [HP94]. These dangling bonds are visible in ESR and identified as a dangling bond on a Si atom at the Si-SiO_2 interface (P_b center) because of their anisotropy and their Landé g-factor [Cap+79]. These point defects were then connected to the electrically measurable interface traps [LD82]. The orientation of the surface of Si has an impact on the type and properties of the P_b center. On (111)Si-SiO_2 surfaces only one type of the P_b center exists. However, for (100)Si a first P_b center variant at the (100)Si-SiO_2 interface (P_{b0} center) and a second P_b center variant at the (100)Si-SiO_2 interface (P_{b1} center) exist. See Fig. 1.2 for a sketch of the structure of the two P_b center variants.

To obtain an upper limit for the number of interfacial dangling bonds the atomic density of Si atoms at the Si surface can be calculated from the lattice constant of Si of 0.5431 nm [Lig61]. For the technologically relevant (100) and (111) surfaces of Si this equates to a density of $6.78 \times 10^{14}\,\mathrm{cm}^{-2}$ and $11.76 \times 10^{14}\,\mathrm{cm}^{-2}$ [Lig61; KA+02], respectively. Using ESR it was found that the interface to SiO_2 exhibits a two decades smaller number of $10^{13}\,\mathrm{cm}^{-2}$ dangling bonds at the interface for both (111) and (100)Si [Ste93; SNA98].

Hydrogen interaction

Annealing in a neutral hydrogen atom (H) containing atmosphere at temperatures of 400 °C to 600 °C is widely used to reduce the number of interface traps or P_b centers [Kar+00]. Optimization of the annealing process in forming gas (mixture of nitrogen and hydrogen gas) can bring the

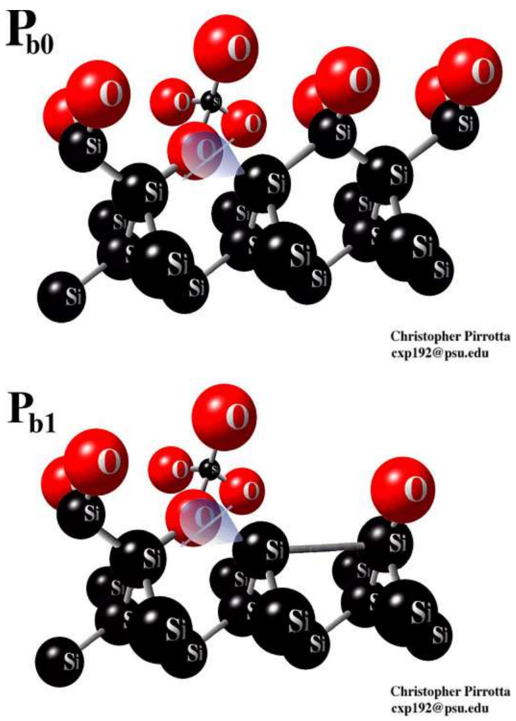

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Fig. 1.2: Schematic drawing of a P_{b0} center and P_{b1} center at the (100)Si-SiO_2 interface from [Cam+07].

remaining electrically active dangling bond density down to $10^9\,\mathrm{cm}^{-2}$. This results in an interface where approximately every hundredth atom at the Si side of the interface is passivated by an H atom and about every millionth of these could not find an H atom for passivation or the nearest neighbor of the SiO_2 and are left unsaturated and thus electrically active. The mean distance between two hydrogen passivated Si dangling bonds is thereby in the nanometer range and two unsaturated bonds are separated by a few hundred nanometers, respectively. This points out that even devices with just a few tens of nanometer width and length will have a few interface traps [PAN p].

First investigations towards the understanding of the BTI of Si based MOSFETs [JS77] suspected the dissociation of hydrogen from H passivated interface traps as the root cause of the instability. However, later performed studies revealed that the values for the dissociation of a H passivated P_b center (P_bH complex) are greater than 2.83 eV. In detail, the passivation and dissociation energy values are normally distributed due to the amorphous nature of the oxide [Ste96b; Ste96a; Ste00; Sta95a; Sta95b] (and not single-valued [BM90; Bro88; Bro90]). See Table 1.1 for a summary. Also theoretical calculations for H passivated silicon dangling bonds (Si–Hs) in bulk

Table 1.1: Dissociation and passivation energy values for the P_b center family of defects at the Si–SiO_2 interface [Sta95a; Sta95b; Ste96b; Ste96a; Ste00]. All values are given in electron-volt.

		$P_b^{(111)}$	$P_{b0}^{(100)}$	$P_{b1}^{(100)}$
Passivation	mean	1.51	1.51	1.57
	variance	0.06	0.14	0.15
Dissociation	mean	2.83	2.86	2.91
	variance	0.08	0.07	0.07

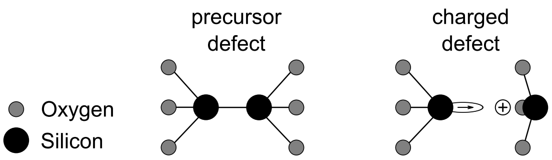

Fig. 1.3: Schematic drawing of an E′ center in SiO_2 (right) and its precursor state, an oxygen vacancy.

silicon revealed rather large activation energies for H depassivation [TW99; PAN p]. Such rather large dissociation energies cannot normally be reached during operation of a device.

Consequently, in the context of negative BTS (NBTS) in Si based devices, the challenging question arises how the rather strong Si–H bond can be broken at typical BTS temperatures of 100 °C to 150 °C. Various possible explanations will be discussed in Section 3.1.

1.3.2 E′ center

Electrical measurements and ESR studies on the Si-SiO_2 system revealed also several types of defects which are situated in the bulk of the oxide [Dea+67; Bun+00]. Among them, the dangling bond on a Si atom bonded to three O atoms within the SiO_2 (E′ center), as sketched in Fig. 1.3, and its variants are most important [Wee56; Sil61; FFY74]. Also for this family of defects possible interactions with hydrogen have been reported.

Hydrogen interaction

Transitions involving H and E′ centers have been studied widely by ESR measurements. It was shown that the interaction of the E′ center with hydrogen may either lead to paramagnetic variants of the E′ center [Vit78; Tak+87; TTS87; TG87; CL92; LJFC98] or to passivation of the dangling bond [AS97; BS99]. Only the former is important for argumentations conducted later in this thesis.

The E′ center may turn to a particular paramagnetic variant, the 74 G doublet, when one of the three oxygen atoms bonded to the silicon atom is exchanged with a hydrogen atom. The 10.4 G doublet is formed when one of the three oxygen atoms bonds to a hydrogen atom. These two variants were shown to form even at room temperature when the sample is exposed to molecular hydrogen gas [CL92]. Therefore these defect types could also be existent in the devices used in this thesis.

1.3.3 Proton

Even though not measurable with ESR, the positively charged hydrogen ion (H^+) in SiO_2 deserves a brief mention because it could be involved in defect creation during NBTS. Experimental studies [AS98; AS99; AS01; AAS01] and theoretical calculations [BS99; Bun+00; Pan+00] indicate that a proton may reside within the SiO_2 and may give rise to a positive fixed charge. Especially, calculations suggest that H^+ is the only stable state of H at the Si-SiO_2 interface [Ras+01]. Experimental work using ESR provided evidence that the proton bonds to an intact Si–O–Si complex through rearrangement of the surrounding amorphous SiO_2 lattice [AS98]. Theoretical calculations using density functional theory and supercells suspect the proton to bond to the oxygen vacancy [Pan+00] instead of an intact Si–O–Si complex. Thus, the H atom could become trapped in the close vicinity of the P_b center after P_bH complex dissociation. This idea has already been formulated in context of NBTI [Soo+03].

2

Impact of the gate bias polarity on BTI

The application of positive or negative BTS to a p- or n-channel MOSFET degrades the transistor to a certain amount. The most pronounced instability, however, occurs in pMOSFETs subjected to negative BTS [Sch07; HDP06; MKA04; Pob+11a]. Because of this, the negative BTI has been studied extensively in the literature and numerous physical degradation models have been proposed. However, for a few applications, especially for an nMOSFET as a power switch, only positive but no negative BTS is possible during device operation. Due to the effect of the bias polarity on the type of majority carriers at the interface – during NBTS holes and during positive BTS (PBTS) electrons, respectively – one would expect different microscopic processes to occur which cannot be covered by the models for NBTI alone. Consequently, it is important to understand the exact differences in the degradation behavior for n- and pMOSFETs following N- and PBTS [Pob+11a].

2.1 Impact of the gate poly doping type

For investigations of the impact of the bias polarity on BTI it is important to consider also the doping type of the polycrystalline silicon (poly) gate. The doping type changes the flat band voltage of the device and therefore impacts the oxide field value for a given stress gate voltage. It is further speculated to have an impact on the inherent degradation mechanism [Aba+93]. Additionally, the gate poly doping type can act as a source of charge carriers, namely electrons and holes, which can participate in the microscopic degradation mechanism.

In Fig. 2.1 the band structures of pMOSFETs during BTS with either n^{++} or p^{++} gate poly doping are sketched. Additionally, equations derived from various approximations for the field across the oxide and the semiconductor for the stress bias are given in Fig. 2.1. In particular it is assumed that the oxide and the interface are charge-free, the gate poly is not depleted, the quantum confinement of the carriers of the channel can be neglected, and that the semiconductor

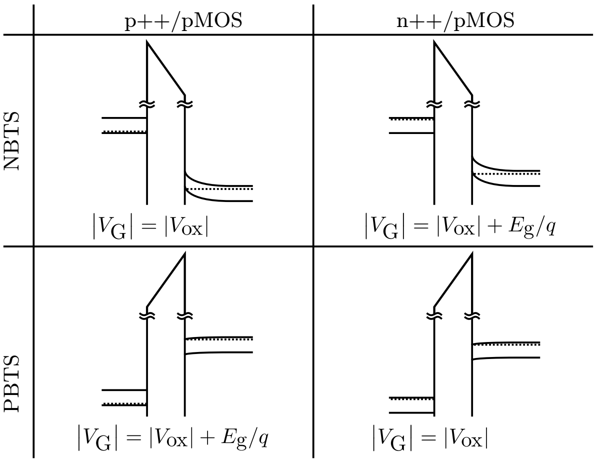

Fig. 2.1: Band diagram for the four possible combinations of n^{++} and p^{++} doped poly gate pMOSFETs and negative/positive BTS [Pob+11a]. Approximations for the splitting of the gate bias V_G between the oxide and the semiconductor are given, where E_g is the band gap energy of Si.

bands are bended exactly to intersect with the valence and conduction band edges (Fermi level pinning). With the equations of Fig. 2.1 the appropriate gate voltages for a target oxide field can be estimated with sufficient accuracy for the present purpose. The gate voltage for n^{++} poly gated nMOSFETs are calculated in analogy. A possible voltage across the gate poly [SKH93] is not considered due to the high doping of the gate of about $10^{19}\,\mathrm{cm}^{-3}$.

The devices used in this work are fabricated using complementary MOS (CMOS) technology (n^{++} gated nMOSFETs and p^{++} gated pMOSFETs) and an n^{++} poly gated technology (both n- and pMOSFETs). The last combination, an nMOSFET with a p^{++} poly gate, is missing. However, this does not affect the main conclusions since the available combinations are sufficient to reconstruct the presumable result of the missing device.

To fully understand the impact of the gate poly doping type in detail, devices with different oxide thicknesses were used for the investigation of the impact of the distance between the gate poly and the active device interface.

2.2 Oxide thickness dependence

First, the dependence of NBTI and positive BTI (PBTI) of pMOSFETs on the gate oxide thickness is investigated. The threshold voltage drifts can be directly compared considering the thickness dependence of the drift magnitude. The shift of the threshold voltage ΔV_TH depends inversely on the gate oxide capacitance. Furthermore, because of $C_\mathrm{ox} = \varepsilon_{\mathrm{SiO}_2}/d_\mathrm{ox}$, ΔV_TH scales linearly with the oxide thickness. With consideration of (1.1) the normalized threshold voltage shift [Rei+08; Pob+10; Pob+11a],

$$\Delta V_\mathrm{TH}^\mathrm{norm} = \frac{\Delta V_\mathrm{TH}}{d_\mathrm{ox}}, \tag{2.1}$$

accounts properly for the oxide thickness, assuming [Rei+08; Pob+10] that all charges created through BTS reside close to the active device Si-SiO$_2$ interface. The recovery voltage is the threshold voltage of the particular device. This ensures an equivalent hole density at the interface and thus equivalent recovery conditions for all investigated oxide thicknesses.

For a comparison of CP measurements of devices with different oxide thicknesses it is important to ensure that the high and low levels of the gate pulse are sufficiently large such that always the maximum CP current is measured. Constant rising and falling slopes provide an equivalent probed energy interval for all devices [Gro+84; ANG08] as already described in Section 1.2.2.

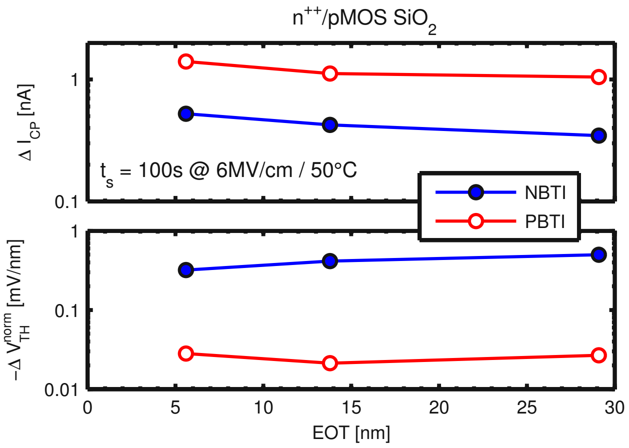

Fig. 2.2: EOT dependence of the degradation following N- (blue closed symbols) or PBTS (red open symbols) for pMOSFETs with an n^{++} doped poly gate [Pob+11a]. Minimum delay charge pumping measurements (upper plot) and threshold voltage shifts (lower plot) measured at the same chuck temperature of 50 °C.

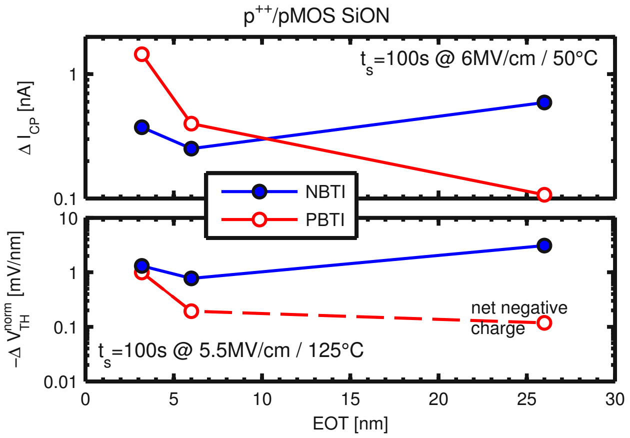

Fig. 2.3: EOT dependence of the degradation following N- or PBTS for pMOSFET with a p^{++} doped poly gate [Pob+11a]. Charge pumping measurements (upper plot) and threshold voltage shifts (lower plot) measured at different chuck temperatures.

Taking these considerations into account, the impact of N- and PBTI on n^{++} and p^{++} poly gate pMOSFETs can be compared as shown in Fig. 2.2 and Fig. 2.3, respectively. Both N- and PBTI are independent of the EOT for the n^{++} poly gated pMOSFETs in Fig. 2.2. This is consistent with earlier work [Pob+10; Rei+08; Pob+11a]. These results indicate that the degradation is not due to impact ionization [DCA93] or anode hole injection [SH94; DiM00; Hua+03], since those mechanisms would strongly depend on the *voltage* across the oxide and not on the electric oxide *field*. Although PBTS causes a large change in the CP current, it results in a vanishingly small V_{TH} shift measured by the change in the drain current.

A similar result is found for the p^{++} poly gate pMOSFETs following NBTS, for which no consistent dependence on the EOT is observed in Fig. 2.3. In contrast, following PBTS, the degradation decreases strongly with increasing EOT. Remarkably, the drift polarity changes its sign between 6 nm and 26 nm. The thick oxide device experiences rather a positive drift after PBTS indicating the creation of negative charges [Pob+11a]. From this observation a different degradation mechanism is suspected to occur for PBTS on p^{++}/pMOSFETs with thin gate oxides.

In order to better understand the different behavior for the PBTI on p^{++}/pMOSFETs the dependence on the stress oxide field is investigated.

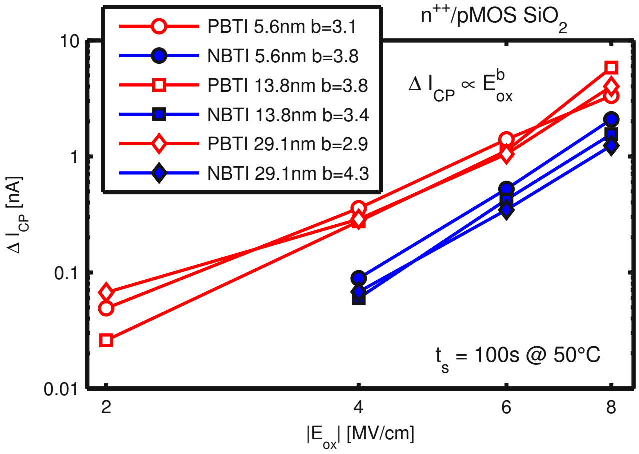

Fig. 2.4: Oxide field dependence of the change of the CP current 41 ms after termination of a 100 s long stress at 50 °C for pMOSFETs with a n^{++} doped poly gate [Pob+11a]. The different symbols correspond to three different devices with three different oxide thicknesses between 5.6 nm and 29 nm.

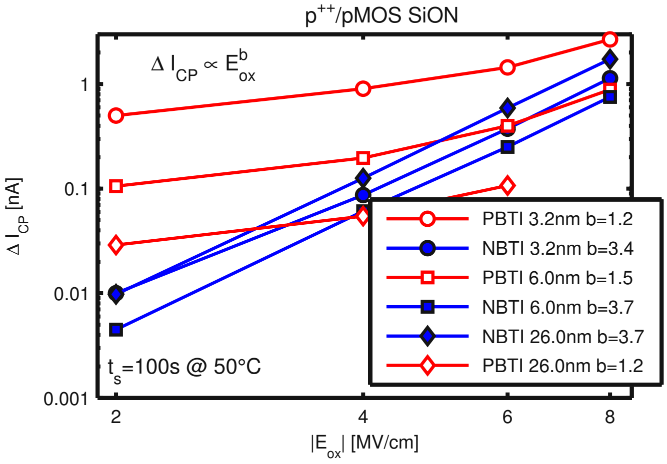

Fig. 2.5: The same as in Fig. 2.4 but for pMOSFETs with a p^{++} doped poly gate. [Pob+11a]

2.3 Oxide field dependence

The oxide field for all devices was estimated by using the formulas presented in Fig. 2.1. The oxide field dependence is illustrated in Fig. 2.4 for the n^{++}/pMOSFETs and in Fig. 2.5 for the p^{++}/pMOSFETs, respectively.

For the n^{++} poly gate devices both N- and PBTI show an equivalent behavior with a power law coefficient of about 4 which is close to the often reported value [Hua10; Gra+11c]. No visible influence of the gate oxide thickness is evident. For a stress and recovery temperature of 50 °C PBTI is more severe than NBTI.

For the p^{++} poly gate pMOSFETs only NBTI has a comparable behavior and exhibits a power law coefficient of about 4. In contrast, the PBTI has a much lower power law coefficient of about 1.3. The different power law coefficient for PBTI suggests that it is not only the common N- or PBTI degradation mechanism which accounts for the degradation, but another mechanism might be involved. This becomes clearer in an investigation of the recovery behavior after stress.

In Fig. 2.6 the recovery of the CP current and the ΔV_{TH} following PBTS is shown for thick oxide devices. As mentioned previously, PBTS causes a negative or a vanishingly small charge build-up close to the interface [Pob+11a]. Despite this, all devices experience about the same change in the CP current, but only the nMOSFETs, which is unfortunately only available with n^{++} poly gate, experiences a drift in the threshold voltage. This shows that PBTS creates acceptor-like defects

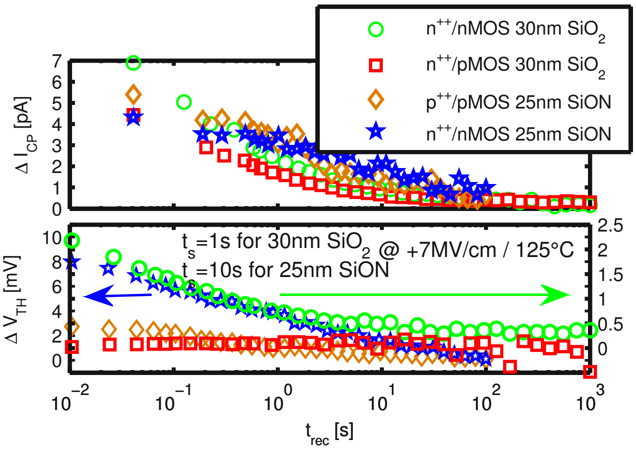

Fig. 2.6: Recovery after PBTS for thick oxide n- and pMOSFETs with either an n^{++} doped poly gate or with n^{++} or p^{++} doped poly gate for either nMOSFETs or pMOSFETs, respectively [Pob+11a]. pMOSFETs do not show any drift in the ΔV_{TH} regardless of the gate poly doping type.

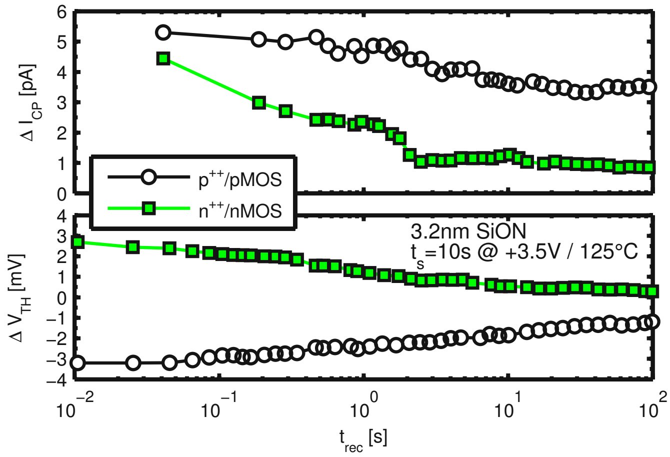

Fig. 2.7: Recovery of the CP current and the threshold voltage shift in a thin oxide n^{++}/nMOSFET and a thin oxide p^{++}/pMOSFET after PBTS [Pob+11a]. The pMOSFET shows an NBTI-like recovery behavior after PBTS.

close to the interface which are either negatively charged or neutral depending on their charge state. Since the defects are all visible in the CP current but only for the nMOSFETs visible in the ΔV_{TH} the energy level for the charge state transition must lie within the Si band gap, probably close to the intrinsic energy level E_{i}. Thus for thick oxide devices PBTS can create acceptor-like charges which affect the drain current only if the Fermi level is close to the conduction band edge, as it is the case for an nMOSFET during operation.

For devices with a thin oxide a build-up of positive charges after PBTS was observed. This is remarkable because the positive bias at the gate accumulates electrons at the interface and positive charge is in principle absent. The only region that contains a sufficient amount of holes is the p^{++} doped poly gate at the other side of the oxide. This is because the high doping level of the gate poly of around $10^{19}\,\mathrm{cm}^{-3}$ inhibits its depletion. If the holes for the positive charge build-up during PBTS are indeed supplied by the poly gate, a positive charge build-up is supposed to be absent if the gate is replaced by n^{++} doped poly. Unfortunately, no n^{++}/pMOSFET with the thinnest 3.2 nm gate oxide is available. However, as mentioned previously, n- and pMOSFETs experience the same degradation except for a different Fermi level position during readout. Consequently, also a comparison with an n^{++}/nMOSFET instead of a pMOSFET is possible. In Fig. 2.7 a comparison of the recovery behavior of those two devices after PBTS is shown. The p^{++}/pMOSFET shows an NBTI-like recovery behavior meaning that positive charges are created during stress which recover subsequently after termination of stress. As suspected before, the n^{++} gated nMOSFET shows

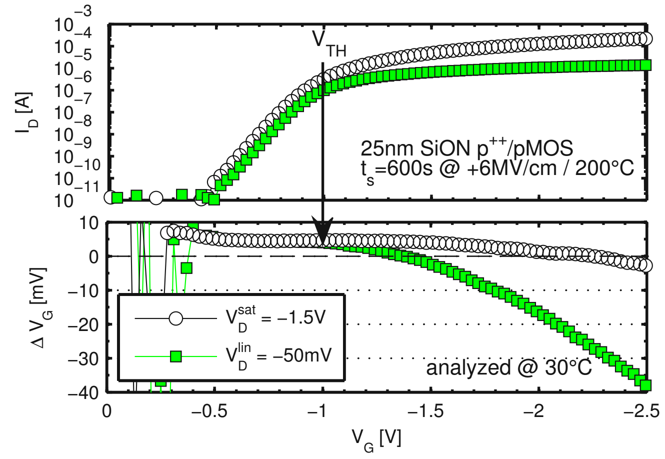

Fig. 2.8: Virgin transfer characteristics (upper plot) and drift versus gate voltage dependence after PBTS (lower plot) for two different drain voltages V_D in the linear and in the saturation regime of the pMOSFET [Pob+11a].

indeed the creation and recovery of negatively charged defects. Thus a positive charge build-up after PBTS is only possible if the device has a p^{++} doped poly gate and a sufficiently thin oxide such that the holes can tunnel from the gate towards the device into the defect [Pob+11a; Rot+12; TL+11a].

It is remarked that the finding that acceptor-like defects are created through PBTS is in contradiction to literature [Kat01; Den+04b; Gra+07]. A plausible cause for this contradiction is that these studies were performed on devices of CMOS technology. Other work on pMOSFETs with thick gate oxides [ZE98] still reported donor-like charges after PBTS. The results in [ZE98] are based on drain current–gate voltage ($I_\mathrm{D}V_\mathrm{G}$) sweeps in the linear regime of the transistor before and after stress. However, in a repetition of the experiment a strong dependence of the ΔV_G on the voltage applied to the drain V_D, as illustrated in Fig. 2.8, was found [Pob+11a]. In the linear regime of the transistor where $V_\mathrm{D} < {V_\mathrm{D}}^\mathrm{sat}$, ΔV_G is largely negative above the threshold voltage of the device. It is remarked that the ΔV_G is measured with $V_\mathrm{G} > V_\mathrm{TH}$ in [ZE98]. This negative shift nearly vanishes provided the characteristic is measured in saturation, even though the V_D should not affect the ΔV_G at all.

The strong difference in ΔV_G with different V_D occurs because changes in the effective channel mobility μ_FET have a different impact on the measured drain current from which the ΔV_TH is calculated [Aic10]. A possible explanation is that the pinch-off effect in saturation reduces the channel length and thus decreases the impact of the channel mobility on the change of the drain current. This may be deduced from first order models for the drain current in the linear (lin) and saturation (sat) regime of a transistor [SN06]

$$I_\mathrm{D}^\mathrm{lin} = -\frac{W}{L}\mu C_\mathrm{ox}\left(V_\mathrm{G} - V_\mathrm{TH} - \frac{V_\mathrm{D}}{2}\right)V_\mathrm{D}, \tag{2.2}$$

$$I_\mathrm{D}^\mathrm{sat} = -\frac{1}{2}\frac{W}{L}\mu C_\mathrm{ox}\left(V_\mathrm{G} - V_\mathrm{TH}\right)^2, \tag{2.3}$$

where W is the channel width, L the channel length and C_{ox} the oxide capacitance. From these equations it follows that changes in the drain current may be due to mobility changes or shifts of the V_{TH} as [Aic10]

$$\frac{\Delta I_{\mathrm{D}}^{\mathrm{lin}}}{I_{\mathrm{D}}^{\mathrm{lin}}} = \frac{\Delta\mu}{\mu} - \frac{\Delta V_{\mathrm{TH}}}{V_{\mathrm{G}} - V_{\mathrm{TH}} - V_{\mathrm{D}}/2} \tag{2.4}$$

$$\frac{\Delta I_{\mathrm{D}}^{\mathrm{sat}}}{I_{\mathrm{D}}^{\mathrm{sat}}} = \frac{\Delta\mu}{\mu} - \frac{2\Delta V_{\mathrm{TH}}}{V_{\mathrm{G}} - V_{\mathrm{TH}}}. \tag{2.5}$$

For a large overdrive, $V_{\mathrm{G}} - V_{\mathrm{TH}} \gg \Delta V_{\mathrm{TH}}$, the change in effective channel mobility μ_{FET} dominates the change of I_{D}. Operation of the transistor in the saturation regime increases the impact of the V_{TH} shift on the change of the drain current. In saturation the drift is roughly two times larger compared to the linear regime [Pob+11a].

3

Process influences on BTI

Having established the qualitative difference of the degradation following negative or positive BTS, the focus is shifted towards the influences of individual processing steps of manufacturing on the quantitative degradation behavior. Considering the majority of microscopic models for BTI, the electrical activation of defect precursors is suspected as the root cause of the instability [JS77; Sch07; HDP06; Gra+11b]. Several types of these defect precursors are, as described in Section 1.3, partly composed of hydrogen. This suggests the involvement of H in the microscopic BTI degradation mechanism. A second argument for the participation of H is that several of the later listed BTI relevant process steps cause the incorporation of H in a device. The oxidation of the gate oxide is thereby not of importance, since the temperatures during oxidation of Si to form the Si-SiO_2 interface are usually too high for hydrogen to stay in the gate oxide stack [DG65; Ste00; Pet05]. Instead, the hydrogen is introduced later, after formation of the Si-SiO_2 interface, through different process steps during device manufacturing. The most important process step among them is most probably the annealing of the device in forming gas (mixture of nitrogen and hydrogen gas) after gate oxide formation. This process step has become a standard for the production of MOSFETs because it considerably decreases the number of electrically active interface traps [Kar+00]. But also during the deposition of dielectric layers of silicon nitride (SiN) a large amount of H is available for precursor defect creation. That is to say, every conventionally manufactured MOSFETs should have a considerable amount of H incorporated within the gate dielectric or at the active device interface and therefore H related precursor defects will be available in the majority of the devices.

Considering BTI, the most important hydrogen-related precursor defect is the H passivated P_b center, also because it was shown that BTS causes the creation of interface traps [JS77]. Consequently, the following chapter reviews models for the dissociation of the P_bH complex and other reactions involving hydrogen-related defect precursors. In an attempt to verify these models, the degradation following BTS is investigated for devices with a varying amount of H within the gate dielectric. Additionally, the impact of a particular process close to the end of the production cycle of a device, namely the power metallization, is investigated in more detail, since earlier results [Aic10] suggested an impact on BTI.

3.1 Hydrogen

The impact of hydrogen on BTI is studied in greater detail because interface traps are created during NBTS [JS77] and numerous Si–H precursors are existent at the Si-SiO$_2$ interface [HKM70; BH71]. The main findings of this Section are also documented in [PNG12; PAN p; PNG13].

3.1.1 $\mathrm{P_b}$H complex dissociation

Since the electrical activation of interface traps includes the dissociation of Si–H, this subsection discusses the possible microscopic transitions which have been proposed to occur during NBTS and result in electrically active interface traps.

Experimental evidence for the occurrence of the dissociation

Two main arguments propose the dissociation of Si–H to occur during NBTS. The first is direct experimental evidence from ESR measurements of three independent groups [Len+90; Fuj+03; Cam+06; Rya+10; YA11; Aic+12; Yon13] who report an increase of the signal density of defects from the $\mathrm{P_b}$ center family following NBTS. The second are purely electrical measurements which showed an increase in interface trap density [JS77; BNP91; Hua+03; SB03; AM05; Mah+06; ANG09b; Aic+10b; Ho+12] following NBTS. Both together give strong support that interface traps are indeed created through NBTS.

It is unlikely that the stress causes a dissociation of intact Si–O bonds at the exact interface between Si and SiO$_2$. This is because thermochemical measurements for bond dissociation energies suggest that the bond strength of Si–O in bulk SiO$_2$ is with 8.3 eV [Ben65] much larger than the dissociation energy for Si–H in bulk Si with 3.3 eV [Dou57]. It is therefore evident that the $\mathrm{P_b}$H complex precursor at the Si-SiO$_2$ interface will be broken during NBTS rather than an intact Si–O bond. Consequently, the involvement of hydrogen in the creation of interface traps during NBTS appears as a requirement.

As already stated in Section 1.3.1, the dissociation energy of the $\mathrm{P_b}$H complex was experimentally [Sta95a; Sta95b; Ste96b; Ste96a; Ste00; BM90; Bro88; Bro90] and theoretically [Edw91; TW99; KYK03; GHB09] determined to be around 2.5 eV to 2.9 eV. The time dynamics for thermal dissociation of a $\mathrm{P_b}$H complex follows [Bro90]

$$\frac{[P_b]}{N_0} = 1 - \exp\left(-k_{\mathrm{d}0} t e^{-\frac{E_{\mathrm{d}}}{k_{\mathrm{B}} T}}\right), \tag{3.1}$$

assuming a single-valued dissociation energy for the $\mathrm{P_b}$H complex. One can estimate the time durations for purely thermal dissociation using the following values: maximum number of passivated $\mathrm{P_b}$H complexes $N_0 = 10^{13}\,\mathrm{cm}^{-2}$ [Ste93; SNA98], single-valued dissociation energy $E_{\mathrm{d}} = 2.56\,\mathrm{eV}$ and forward rate constant $k_{\mathrm{d}0} = 1.2 \times 10^{12}\,\mathrm{s}^{-1}$ [Bro90]. For a rather small increase in the interface trap density of only $10^9\,\mathrm{cm}^{-2}$ at a typical NBTS temperature of 125 °C already around 10^{16} s (3×10^8 years) are obtained by solving

$$t = \frac{\log\left(1 - \frac{[P_b]}{N_0}\right)}{-k_{\mathrm{d}0}\mathrm{e}^{-\frac{E_\mathrm{d}}{k_\mathrm{B}T}}}. \tag{3.2}$$

As a result, the dissociation of a $\mathrm{P_bH}$ complex as a purely thermal process under typical NBTS conditions is very improbable and other mechanisms must be involved in the transition. In the following several approaches which attempt to resolve this issue are summarized.

Hole capture

The most prominent argument for a decrease of the dissociation energy of the Si–H bond is the capture of a hole prior to bond dissociation

$$\text{Si–H} + h^+ \longrightarrow \text{Si}\cdot + \text{H}^+. \tag{3.3}$$

This argument is often used in a rather vague form [BNP91; OS95; AM05] as if it would not need any detailed clarification. In fact, a consistent and detailed explanation of how and why a captured hole reduces the bond-dissociation energy of Si–H is unclear. Questionable support for the idea stems mostly from density functional theory calculations for different defect types. The amount of dissociation energy reduction is thereby unclear and varies largely. The largest reduction is suggested for the Si–O bond in the context of time dependent dielectric breakdown (TDDB), where it is stated that a capture of a hole reduces the bond-dissociation energy by 2 eV [MKS00]. In the context of NBTI, the calculated decrease of the dissociation energy of Si–H is only 0.3 eV [Pan+07]. Accordingly, the applied electric stress field might only reduce the dissociation energy by another 0.1 eV, a reduction which is still far too small to make the dissociation likely under NBTS conditions.

Despite the too large dissociation energy it was suggested that the diffusion of the released hydrogen species determines the dynamics of NBTI instead of the reaction. The reaction-diffusion theory [JS77; BNP91; OS95; AM05; MKA04; Mah+11], which evolved from this idea, could, in spite of several attempts [Aic+10b; Gra+11c; SG11; SG12], not be used to consistently explain all features of experimental data. Hence, the focus in this Section lies in the reaction process of hydrogen dissociation which must precede any discussion on diffusion [Ree89].

Atomic hydrogen

An energetically more favorable reaction than the direct dissociation of Si–H with the capture of a hole is the dissociation with the help of a hydrogen atom

$$\text{Si–H} + \text{H} \longrightarrow \text{Si} + \text{H}_2 \tag{3.4}$$

which forms molecular hydrogen. This transition has a calculated barrier energy in the range of 0.95 eV [Tse+05]. This means that the existence of atomic hydrogen or a proton (also positively charged variants of reaction (3.4) are possible [Ras+01]) in the vicinity of a hydrogen passivated interface trap may lead to bond dissociation. A possible source for the atomic hydrogen might be the metal layers above the device [Hou+07], H passivated dopants within Si [Fuk+05; Tse+05] or hydrogen from molecular hydrogen (H_2) cracked at E' centers [Cam+06; Li+90; CL93; Edw95] or at trapped holes [Zha+00; Sta+93].

The occurrence of transition (3.4) during NBTS is supported by nuclear reaction analysis. This method detects gamma rays emitted by a nuclear reaction from a sample [Wil+02]. One of these nuclear reactions is

$$^{1}\mathrm{H} + {}^{15}\mathrm{N} \longrightarrow {}^{12}\mathrm{C} + {}^{4}\mathrm{He} + \gamma, \tag{3.5}$$

which occurs with high probability under bombardment with $^{15}\mathrm{N}^{2+}$ nitrogen (N) ions of a material containing hydrogen. This technique has revealed that NBTS causes an accumulation of hydrogen atoms near the Si-SiO_2 interface [Liu+02]. The hydrogen atoms concentration thereby peaks at a position roughly 4 nm away from the interface with a spread of about 8 nm [Wil+02]. This peak already exists before stress but increases through NBTS [Liu+02]. Since the overall number of $^{15}N^{2+}$ ions has to be kept low to avoid a measurement induced redistribution of hydrogen atoms, the work of Liu et al. [Liu+02] documented NBTS induced changes in the number of hydrogen atoms per square centimeter only for the estimated position of the interface. They could still show that the increase of hydrogen atoms at the interface with NBTS is larger than the increase of interface traps, which means that hydrogen is transported from other places within the semiconductor towards the interface. This indicates that additional H is available at the interface which can cause the creation of new interface traps via reaction (3.4).

Reference [Aic+12] gives another indication that atomic hydrogen could be involved in the microscopic NBTI degradation mechanism. It was found that a positive bias phase at room temperature after NBTS can lead to an increase in interfacial recombination centers even though the gate bias is too low to trigger PBTI. According to their explanation, atomic hydrogen, previously released through NBTS, returns to the interface because it is repelled from the positively charged gate and creates additional interface traps through transition (3.4). Additionally, the gated diode leakage current measured by the direct current–current voltage (DCIV) technique [Sah62; Neu+95; Cam+05] showed two distinct peaks where only one of them increased through the positive bias treatment. This coincided with ESR measurements which showed that the P_{b0} center variant of the P_b center family on (100)Si-SiO_2 reacts more readily with hydrogen than the other P_{b1} center variant. This leads to the conclusion that atomic hydrogen is released from the P_bH complexes and may return to the interface and interact with the P_{b0} center through a small positive bias at the gate. Furthermore, the ESR data of reference [Aic+12] indicated hyperfine peaks symmetrically around the P_{b0} center, rather than around the E' center. Symmetrical hyperfine peaks around the E' center would have indicated the 10.4 G or 74 G variants of the E' center described in Section 1.3.2. The symmetry around the P_{b0} center signal indicates rather that the P_{b0} center itself has a hyperfine interaction due to a hydrogen atom in the close vicinity, as e.g. in an anti-bonding configuration [TW99; AP07] or in a neighboring Si–Si bond [Ste00].

Trapped hole in vicinity

Another explanation for the creation of interface traps during NBTS stems from thermodynamical considerations [Len03]. Previous work showed that numerous E' centers are created in the SiO_2 layer during NBTS through hole trapping [Cam+06; Gra+09; Rya+10] and that E' centers may become passivated with hydrogen [Li+90; CL93; LTM08]. The electrical activation of E' centers during NBTS creates now a completely different environment for the hydrogen atoms bonded to Si atoms at the interface. The hydrogen atoms suddenly have an increasing number of possible states where they could reside. Now, from a thermodynamic perspective, the hydrogen atoms need to occupy the newly created free sites to minimize the Gibbs free energy of the whole system [Len03]. Many of the hydrogen atoms of the passivated P_bH complexes will transfer to the E' centers in the SiO_2, leaving interface traps behind. That is, the creation of P_b centers may occur having E' centers situated close to the interface.

Studies which tried to identify such a transition use ESR measurements which need to be conducted after the devices have been stressed. But after stress, most of the E' centers either neutralize through emitting their positive charge, which can be understood as the commonly observed recovery, or become passivated by a hydrogen atom. Consistently, researchers observed either no E' center signal [Fuj+03; Hou+07] or just a very small one close to the sensitivity limit of the equipment [Cam+06; Cam+05]. Only later studies [Rya+10] in a on the fly manner *during* NBTS showed that the E' center signal can be large but vanishes quickly after termination of the stress.

The idea of the transition of H from a P_b center to an E' center was combined with the Harry–Diamond–Laboratories (HDL) model for switching oxide traps [Lel+88; Lel+89; LO94] for the recoverable component to form the two-stage model for NBTI [Gra+09]. Two stages were needed because to independent components, one independent of the recovery bias having relatively long time constants and one susceptible to gate bias changes having relatively short time constants, were identified. This model states that the transition of hydrogen from a P_bH complex to an E' centers in SiO_2 [CL92; CL93] leads to a lock-in of the E' center [Len03; Len07] and is summarized in Fig. 3.1. The result of this transition is an equal amount of positive oxide charges and interface traps for the quasi-permanent component permanent component (P) of NBTI.

Variance in dissociation energy

ESR studies [Ste93; Ste02; Ste96b; Ste96a] revealed that the oxidation process of the SiO_2 layer and there in particular the oxidation temperature can impact the variance of the distribution of the Si–H bond-dissociation energy. The reason for the variance is thereby the configurational distribution in the vicinity of the P_b center on an atomistic scale. The variance decreases with higher oxidation temperature because the temperature induced relaxation decreases the spread in configurational compositions for the P_b center defects [Ste02]. The largest reported variance for a P_bH complex association is 0.11 eV for (111)Si-SiO_2 [Ste02] and 0.15 eV for (100)Si-SiO_2 [Ste96b; Ste96a]. With this variance only a negligible part of the distribution around the mean dissociation energy of 2.83 eV could be dissociated at typical temperature ranges of NBTS.

However, there are at least two possible explanations how the dissociation energy, including the inherent spread, is further reduced. The first idea stems from studies concerning TDDB [MRM97], where it is proposed that the dissociation energy is reduced through a polarization effect. This means that the electric field pulls the negative and positive charge centroids, and therefore the molecule itself, apart. This results in a distortion of the atomic bond which reduces its dissociation energy. The dissociation energy reduces linearly by about 0.6 eV for a large NBTI oxide field of $10\,\mathrm{MV\,cm^{-1}}$ [Hua+07]. Another probable explanation is that for NBTI only one of the two vibrational modes of the Si–H bond may be crucial [Hua+07; GHB09]. This is because the bending mode is supposed to have a smaller dissociation energy of about 1.5 eV than the stretching mode [KYK03; TW99; GHB09] of the Si–H bond of about 2.5 eV. Both concepts together predict

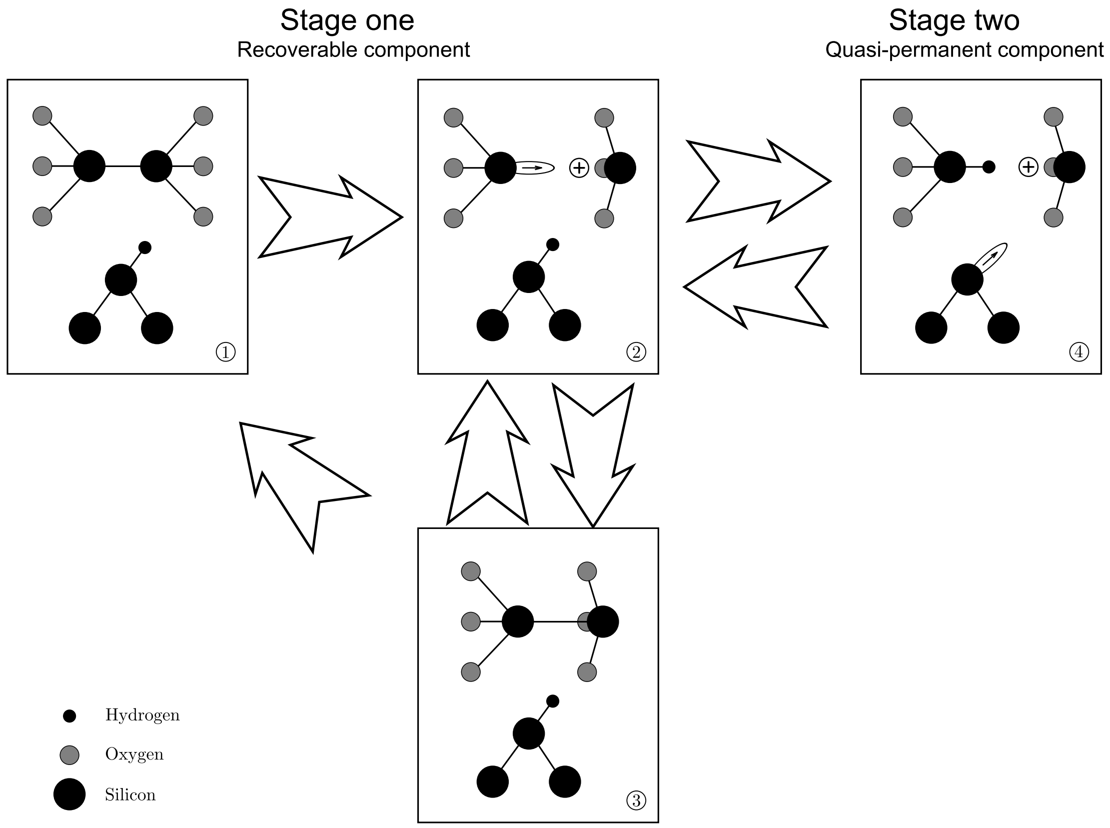

Fig. 3.1: The two stage model for NBTI [Gra+09, Fig. 9a]. The recoverable component (stage one) is a switching oxide trap. A transition of H from a neighboring P_bH complex effectively locks this cycle (stage two).

that there exists a distribution of activation energies a spread of up to 0.15 eV around the mean value of about 0.9 eV at 10 MV cm^{-1}. As a result, at least a low-energy fraction of the available Si–H bonds could be broken during NBTS [HDP06; Hua+07; GHB09].

Provided these assumptions are correct, the normal distribution of activation energies should be visible in NBTI stress and recovery data. Indeed, the normal distribution can be directly measured [HDP06], also through acceleration of the NBTS with high stress temperatures using the poly-heater [Pob+11b], see Section 5.3 for details. Furthermore, a model for NBTI, which was tested for large ranges of temperature, bias and time on several technologies, is based on the assumption of normally distributed activation energies [Gra+11a].

3.1.2 Process steps relevant for the H passivation degree

The ideas described above for P_bH complex dissociation give an idea for the possible microscopic transitions for the charge build-up during NBTS, but hardly provide any quantitative information concerning the impact of hydrogen. Furthermore, the results are mostly obtained on millimeter sized MOS capacitors (MOSCAPs) and not on micrometer sized MOSFETs, where a different situation may be observed.

In order to investigate the impact of hydrogen on BTI a variation of the hydrogen concentration near the Si-SiO_2 interface through adapted processing is needed. A standard approach to passivate

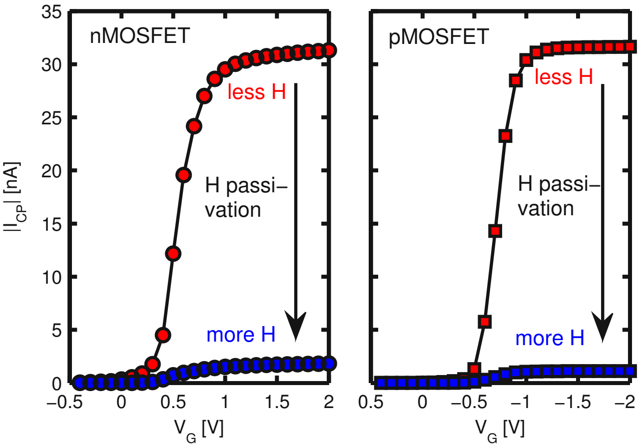

Fig. 3.2: Constant base level CP measurements for devices with more or less H at the interface through variation of the Ti layer thickness in the BEOL stack. The base level is ±1 V for the p- and nMOSFETs, respectively. Rising/falling slopes are $40\,\mathrm{ns\,V^{-1}}$ at 1 MHz frequency.

dangling bonds at the interface by hydrogen is to anneal the device in forming gas. However, the encapsulation layers of a fully processed device impede any further passivation making an experimental study on completely processed devices impossible. Consequently, the hydrogen passivation degree must be changed by specific process steps and adjustments during manufacturing.

Titanium layer thickness

The hydrogen passivation degree is impacted largely by the thickness of the titanium (Ti) layer between the metal and the dielectric layers, i.e. by the amount of Ti within the back end of line (BEOL) stack [Pom+05; Aic+10b; Aic10; Aic+10a; CK11; PNG12; PNG13]. Ti was shown to gather H efficiently [MLR91; WME92; Pom+05]. Therefore, the Ti suppresses the diffusion of hydrogen from H-rich layers located in a higher level of the stack towards the Si-SiO_2 interface. Time of flight secondary ion mass spectroscopy measurements [Aic+10b; Puc11] showed that a thinner Ti barrier leads to an increased accumulation of hydrogen near the Si-SiO_2 interface. Also, electrical measurements using CP [Aic+10b; PNG12; PNG13] illustrated in Fig. 3.2 show that the amount of electrically detectable defects increases with decreasing thickness of the Ti layer.

Silicon nitride deposition

SiN is frequently used as an encapsulation layer in semiconductor processing due to its good insulating (resistance and electric breakdown field) and elastic properties. Commonly, SiN is deposited in a low-pressure chemical vapor deposition (LPCVD) process from silane (SiH_4) mixed with molecular N (N_2) or ammonia (NH_3) [SCN80]. As a byproduct of the reaction, a lot of H is released which either stays in the SiN layer or diffuses towards the interface [SCN80; Nel+05]. In essence, the deposition of SiN can have a large impact on the device reliability, despite this process step being carried out after the device is already completed. It is speculated here that the SiN deposition is the most important process step for the passivation of interface traps with hydrogen for production quality devices. The impact of SiN deposition may only be reduced by diffusion hindering layers from materials such as Ti.

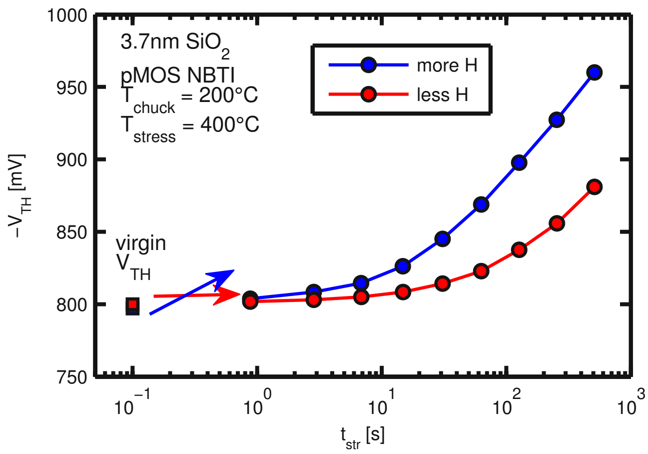

Fig. 3.3: Change of the threshold voltage with intensive 400 °C stress for two devices with more or less H near the interface [PNG12]. At 100 ms the value of the virgin threshold voltage determined by the linear extrapolation method [Sch06] is marked.

Metal layers

The type of metal used for wiring may also have an impact on the reliability of the devices on the wafer. This is because some metals are believed to have the ability to split H_2 into two reactive H which may cause additional damage at the Si-SiO_2 interface. See Section 3.2 for details.

3.1.3 Quantitative impact on the quasi-permanent NBTI

A previously investigated [Aic+10b; Aic10] wafer split with differently thick Ti layers within the BEOL stack was available in the thesis. The main result of [Aic+10b; Aic10] is the two-stage model described in Section 3.1.1 and in this respect especially the finding that the degree of hydrogen passivation impacts only the quasi-permanent component of NBTI and leaves the quickly recovering component mostly unaffected. Please refer to references [Aic+10b; Aic10] for details on this topic.

Maximum drift

In [Aic+10b] the impact of hydrogen passivation on the maximum drift potential of a device, that is the sum of precursors and defects, was not investigated. In reference [Aic+10b] it was speculated, but not shown, that the maximum drift of a device increases with hydrogen passivation. One might expect that the device with more H near the interface will drift more since it has a larger number of passivated defects which make up the difference to the device with less H near the interface. If hydrogen only transforms existing defects at the interface to precursors, one single maximum degradation level $\Delta V_{\mathrm{TH}}^{\mathrm{max}}$ for both devices is expected. The measurement of $\Delta V_{\mathrm{TH}}^{\mathrm{max}}$ remains unachievable because a complete saturation of NBTI degradation has not been reported yet [HDP06; Pob+11b]. However, an estimate of $\Delta V_{\mathrm{TH}}^{\mathrm{max}}$ can be given through acceleration of the stress with very high stress temperatures, which was shown to considerably reduce the time constants of all defects constituting NBTI [Pob+11b]. In Fig. 3.3 the result of an NBTI test at 400 °C stress temperature is shown. The high stress temperature is achieved using the poly-heater, an on-chip heating structure, as described in more detail in Chapter 4. The V_{TH} of the device with more H near the interface exceeds the value of the device with less H already after less than a second of stress at 400 °C. At lower temperatures this happens after considerable longer times of about 100 ks [Aic+10b]. Even though a complete saturation of the degradation is not observed also at this high stress temperature, it is shown that the maximum drift potential of

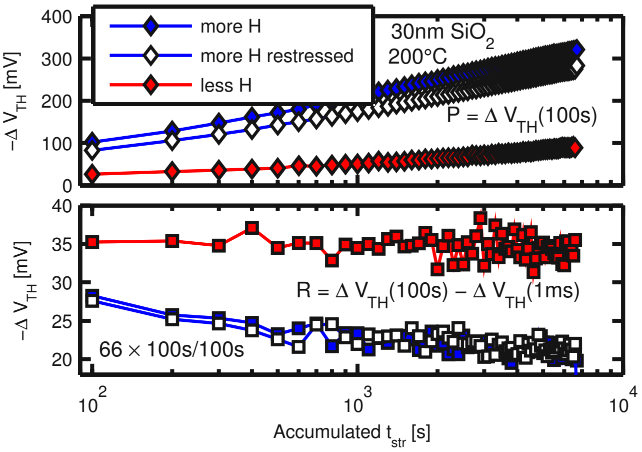

Fig. 3.4: Stress time dependence of R and P (see definition in the figure or subsequent paragraph for details) of two devices with a different hydrogen passivation level and a 30 nm thick gate oxide. The more H device was baked with the poly-heater at 400 °C for 60 s and re-stressed which lead to an equivalent result.

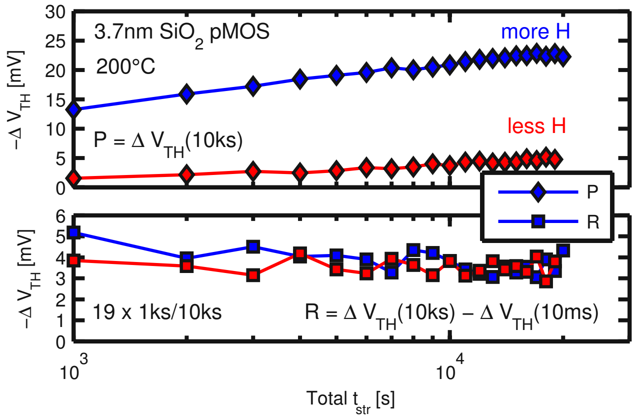

Fig. 3.5: Stress time dependence of R and P for two devices with more or less H near the interface and a rather thin 3.7 nm gate oxide [PNG12].

the device with more H near the interface is much larger compared to the device with less H. To conclude, hydrogen passivation increases the precursor density for NBTI [Zha+00; Pom+05; Nel+05; Aic+10b; PNG12].

H dependence of the decrease of the recoverable component

The two stage model for NBTI as described in Section 3.1.1 suggests that a hydrogen atom is detached from a P_bH complex at the interface and transfers into an E' center to lock the switching oxide trap. Therefore, not only an increase of the permanent damage but also a decrease in the number of recoverable charges with increasing stress should be observed. If the lock-in mechanism is efficient, a large decrease of the cyclic charge in a measurement–stress–measurement (MSM) experiment should be observed. In contrast, the experimental data shown in Fig. 3.4 and Fig. 3.5 indicates an existence of this mechanism which is rather close to the detection limit. The main difference between the experiments in Fig. 3.4 and Fig. 3.5 is the thickness of the SiO_2. While Fig. 3.4 displays data measured on a device with a 30 nm thick gate oxide, Fig. 3.5 shows data of a device with a 3.7 nm thick gate oxide. The 3.7 nm device shows a smaller decrease in R because of the smaller impact of a single charge on the ΔV_{TH} as described in Section 1.2 and equation (1.1). An unambiguous identification of the decrease of R with increasing P would resolve the large debate whether [Gra+09; Aic+10b] or not [Ho+12; Hua10] R and P are connected on a microscopic scale.

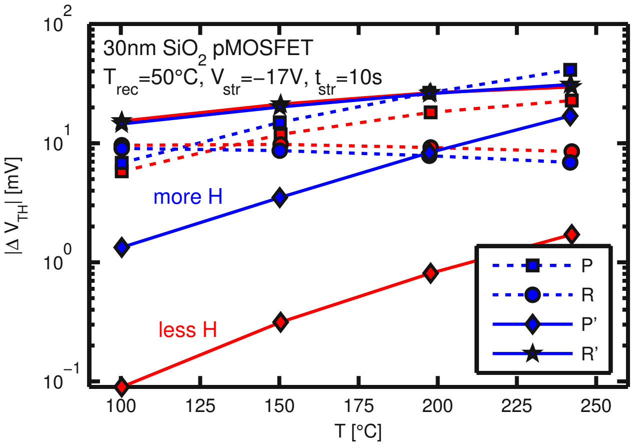

Fig. 3.6: Dependence of NBTI degradation on the stress temperature with the unique feature of a constant recovery temperature [PNG13]. The definitions of R, R', P and P' are described in more detail in the text.

Stress temperature dependence

To investigate the temperature dependence of BTI it is important to vary the stress temperature independently of the recovery temperature. This can be performed with the poly-heater, which will be explained in more detail in Chapter 4. The possibility of rapid temperature switches while keeping the bias applied to the gate is a unique possibility which provides more accurate degradation data. Especially compared to conventionally measured data where equal stress and recovery temperature accelerates not only the stress phase but also the recovery phase. A common approach is thereby to model the recovery behavior at different temperatures and subtract the recovery temperature influence from the stress data [Pob+11b]. This approach, however, introduces errors which alter the conclusions deduced from such measurements.

In the particular example shown in Fig. 3.6 the stress temperature is varied between 100 °C and 250 °C, while the recovery or measurement temperature is always at 50 °C. In Fig. 3.6 two possible definitions of the recoverable R and permanent component P are compared.

- The unprimed R and P values are defined by the recovery time constants (and not the bias dependence) of the previously charged defects similar as in Fig. 3.5 and 3.4. That is, R is the amount of ΔV_{TH} which recovers between the first and the last measurement point (10 ms and 10 s after the termination of stress, respectively). P is defined as the remaining ΔV_{TH} at the end of the 10 s recovery period.
- In contrast, the primed R' and P' values reflect the susceptibility of the defects to a short phase of zero or positive bias at the gate. In particular, R' is the difference between the ΔV_{TH} 10 ms after stress and the ΔV_{TH} after the accumulation period, while P' is the ΔV_{TH} value after the accumulation period.

One observes that, independent of the particular definition, mostly the permanent part of the NBTI degradation is impacted by the hydrogen content near the interface. Especially the primed drift P', i.e. the charge which is activated through NBTS and cannot be annihilated by a short phase with zero or positive bias at the gate, is largely affected by the hydrogen passivation. Also the unprimed permanent drift P is affected by the hydrogen passivation. It is remarked that the visible impact on P only appears small but is in fact rather large. The short recovery phase of only 10 s annihilates only a fraction of the recoverable charges. Consequently, the unprimed permanent component P includes also a large fraction of recoverable charges which shift the characteristic

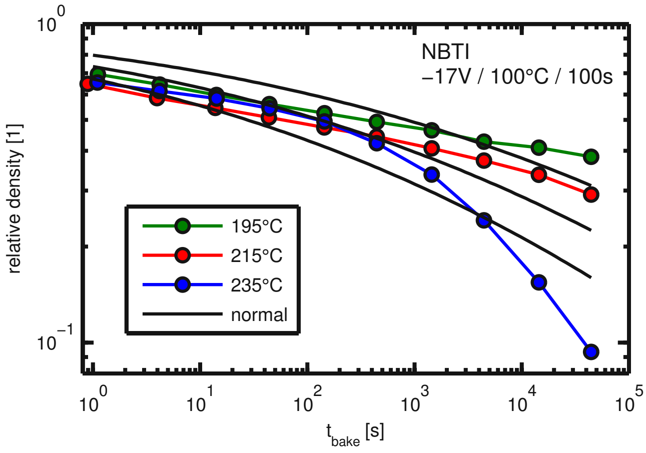

Fig. 3.7: Relative decrease of the density of interface traps measured with CP over constant temperature baking time at zero gate and drain bias. The data is compared to the assumption of normally distributed activation energies for defect discharging, see Section 5.3 for details [Ste96a].

upwards in the semi-logarithmic plot, making the difference to appear vanishingly small. The largest impact of the hydrogen passivation is evident for P'. The different H passivation causes a parallel vertical shift between the two characteristics. The vertical shift in the logarithmic plot corresponds to a multiplicative factor of 10. This means that there exist about 10 times less defect precursors for P' if there is less H near the interface. Furthermore, a vertical shift also indicates that the capture parameters of these defect precursors are not changed with hydrogen passivation, only the number of precursor defects changes.

3.1.4 Recovery of the quasi-permanent component

The remaining ΔV_{TH} after a gate bias switch to accumulation is called quasi-permanent because it usually cannot be further reduced [ANG09a; Aic+10b; Gra+11c]. Through a CP measurement after NBTS, the device is frequently accumulated and P' is usually obtained already after only a few pulses [Aic+10b]. Consequently, CP after NBTS allows to conveniently analyze the quasi-permanent component P' of NBTI. Since the degradation is temperature activated, it is likely that increased temperatures may also allow to remove P'. Indeed, the degradation can be nullified by heating the device to high temperatures with the poly-heater (see Chapter 4 for details to the poly-heater), as shown in Fig. 3.7 [Kat08; BOG08; Pob+ pa].

If the quasi-permanent component consists of interface traps the recovery must behave similarly as $\mathrm{P_b}$ center passivation in an $\mathrm{H_2}$ containing atmosphere [Ste96a]. For this case, it was reported that the recovery follows the model

$$\frac{[P_b]}{N_0} = \frac{1}{\sqrt{2\pi}\sigma_{E_f}} \int_{E_f-3\sigma_{E_f}}^{E_f+3\sigma_{E_f}} \exp\left(-\frac{(E-E_f)^2}{2\sigma_{E_f}^2} - k_{f,0}[H_2]t_{\mathrm{bake}}\exp\left(-\frac{E}{k_{\mathrm{B}}T}\right)\right)\mathrm{d}E. \qquad (3.6)$$

which supposes the $\mathrm{P_b}$ center passivation to be a reaction limited process with normally distributed barrier energies. Here, $[H_2]$ is the volume concentration of molecular hydrogen in amorphous $\mathrm{SiO_2}$ after [She77] and $k_{f,0}$ is the forward rate constant. E_f are the normally distributed forward passivation energies and σ_{E_f} is the corresponding variance. The response to an annealing experiment is therefore given by the integration over all possible passivation energies. For numerical reasons integration limits $\pm 3\sigma_{E_f}$ around E_f are sufficient. The values for defects of the $\mathrm{P_b}$ center family at the (100)Si–$\mathrm{SiO_2}$ interface are for $\mathrm{P_{b0}}$ centers: $E_f \approx 1.51\,\mathrm{eV}$,

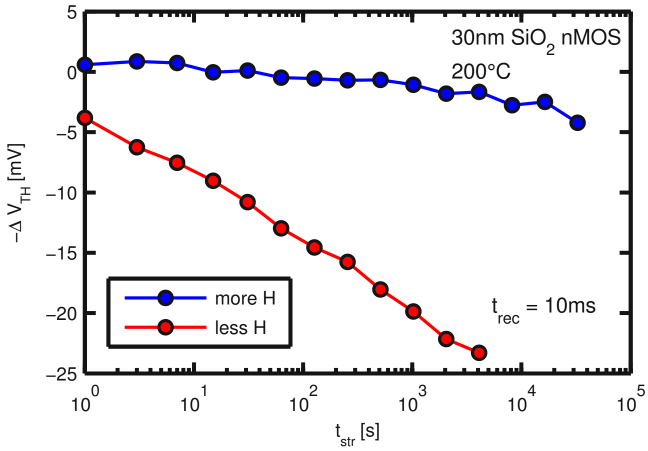

Fig. 3.8: PBTI drift as a function of stress duration in an MSM experiment [PNG12]. H passivation reduces the susceptibility for PBTI.

$\sigma_{E_f} \approx 0.14\,\mathrm{eV}$ and $k_{f,0} \approx 1.43 \times 10^{-6}\,\mathrm{cm^3/s}$ and for $\mathrm{P_{b1}}$ centers: $E_f \approx 1.57\,\mathrm{eV}$, $\sigma_{E_f} \approx 0.15\,\mathrm{eV}$ and $k_{f,0} \approx 1.43 \times 10^{-6}\,\mathrm{cm^3/s}$ [Ste96a].

In order to prove whether interface trap recovery follows this model also in the particular MOSFET devices under study, a test device was subjected to hot carrier stress (HCS). This degradation mechanism is understood to create interface traps close to drain side of the transistor [BH10; RR10; TG12]. That is to say, interface traps are created by purpose to the test the recovery dynamics with high temperatures in the particular device [HOF93]. An analysis of the recovery from this damage using zero bias bake steps lead to the values $E_f = (1.6 \pm 0.1)\,\mathrm{eV}$, $\sigma_{E_f} \approx (0.20 \pm 0.02)\,\mathrm{eV}$ and $k_{f,0} = 7 \times 10^{-4}(6 \times 10^{-5}/9 \times 10^{-3})\,\mathrm{cm^3/s}$, which are very close to the previously reported values [Pob+13]. So temperature assisted interface trap recovery follows the assumption of normally distributed barrier energies for $\mathrm{P_b}$ center passivation.

In contrast (see Fig. 3.7), the removal following NBTS occurs rather slowly, incompatible with the assumption of normally distributed activation energies. This indicates that the quasi-permanent component of NBTI is not due to interface traps alone, but another type of charge with presumably different barrier energy for passivation is involved [ANG13]. It is therefore challenging to answer how exactly the quasi-permanent component is annihilated with baking. However, the temperature activated recovery allows extending the lifetime of a device through irregular baking steps. This idea has already been suggested to extend the lifetime of flash memory cells [Lue+12].

3.1.5 Impact of H passivation on PBTI

In order to study the impact of hydrogen on positive BTI only, preventing any unintentional NBTI, the experiments have been performed on nMOSFETs with n^{++} doped poly-gates. As already described in Chapter 2, PBTI in n^{++} gated devices creates acceptor-like traps in both n- and pMOSFETs, but only in nMOSFETs these charges are visible in ΔV_{TH} [Pob+11a].

In Fig. 3.8 the impact of the hydrogen passivation on the PBTI of an nMOSFET is depicted. The hydrogen passivation has the opposite impact on PBTI compared to NBTI: less degradation after PBTS for devices with more H near the interface is observed. Through analysis of MOSCAP capacitance voltage (CV) measurements before and after PBTS for more and less H it is found that PBTS shifts the flat-band voltage V_{FB} to more positive values, see Fig. 3.9. This indicates either the creation of negative charges or the neutralization of positive charges, respectively.

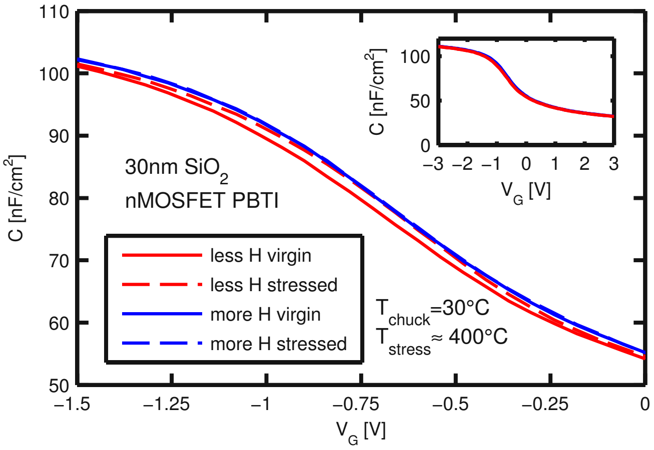

Fig. 3.9: MOSCAP CV characteristics of two devices with more or less H near the interface before/after PBTS [PNG12].

Determination of the charge polarity

Unfortunately, the theoretical charge-free V_{FB} values of the devices under test are not exactly known because of insufficient knowledge of the doping levels of the substrate and the poly gate. The following discussion will give some insight on how to determine the charge sign of the stress induced oxide charges.

- Interstitially incorporated hydrogen: Ab initio calculations [Ras+01] suggest that H^+ is the only stable state of H at the Si-SiO$_2$ interface. So if interstitial H accounts for the difference in the CV characteristics of Fig. 3.9, the more H CV characteristic would need to be shifted toward negative infinity, which is the opposite of our experimental result. From this can also be concluded that all H is bound to other atoms of the solid.

- Hydrogen bonded to boron (B) dopants: H can in principle form a bond with B dopants in the bulk of the Si [Fuk+05]. This passivates the B acceptor which leads to a decreased doping concentration [Fuk+05]. A decrease of the doping level decreases the value of the minimal capacitance in a CV measurement. However, no significant decrease of the minimal capacitance of the nMOSFET CV curve in Fig. 3.9 was observed. Furthermore, NBTI experiments on devices with and without a surface B implantation of about $10^{11}\,\mathrm{cm}^{-2}$ (not shown) did not exhibit any differences regarding BTI behavior.

- Passivation of interface and oxide traps: It is known that hydrogen passivates silicon dangling bonds at the Si-SiO$_2$ interface, namely the P$_\mathrm{b}$ centers, as described in Section 3.1. These traps are amphoteric, meaning that they are charged positively when the Fermi level is close to the silicon valence band edge and charged negatively when the Fermi level is close to the conduction band edge [LD82]. If hydrogen would passivate only amphoteric P$_\mathrm{b}$ centers one would expect positive charge passivation at negative gate voltages and negative charge passivation at positive gate voltages assuming that the gate voltage where the Fermi level is close to the intrinsic energy level is approximately at 0 V. This does not correspond to what is observed in both n- and pMOSFET devices in the CV characteristic as shown in Fig. 3.10. There, H reduces positive charge by about $10^{10}\,\mathrm{cm}^{-2}$, both at the V_{TH} and at the V_{FB} for the pMOSFET as well as at the V_{FB} of the nMOSFET. The reduction is smaller at V_{FB} of the pMOSFET because of the passivation of the P$_\mathrm{b}$ center and for the nMOSFET at the V_{TH} the number of interface traps exceeds the number of positive charges which results in net negative

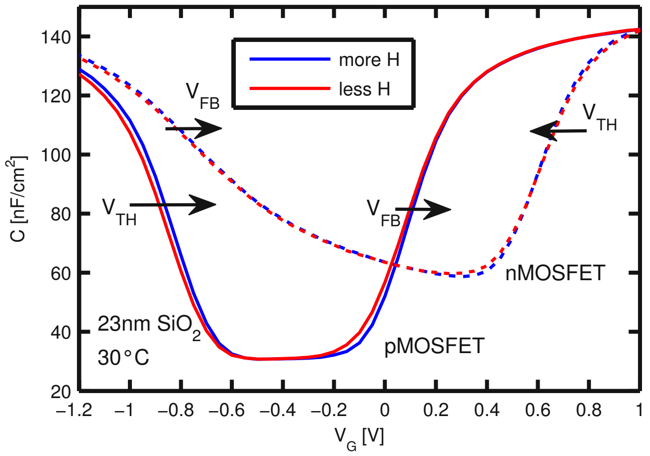

Fig. 3.10: CV characteristics of n- and pMOSFETs with more or less H near the interface [PNG12]. The CV measurements have been performed at an oscillation level of 100 mV and a frequency of 510 kHz.

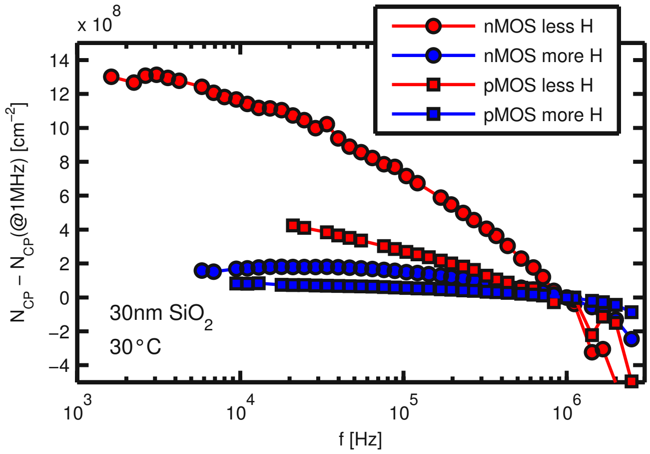

Fig. 3.11: Frequency dependent charge-pumping experiment [PNG12]. Pulse rising and falling slopes are 100 ns V^{-1}. The number of charges pumped per cycle N_{CP} is calculated as $N_{\mathrm{CP}} = I_{\mathrm{CP}}/(qfA)$.

charge. Nevertheless, also for the nMOSFET positive charges are passivated with hydrogen. That is to say, all device types (MOSCAP or MOSFET) and substrate doping types show the passivation of interface traps and positive oxide charges with hydrogen. Consequently, since positive charge passivation for a large voltage range is observed, it has to be concluded that not only amphoteric traps, but also positive charges are passivated through hydrogen. Such an effect has already been reported in literature [CL93; Nel+05].

In order to analyze the electrical properties of the passivated defects, CP measurements with varying frequency f were performed on the two differently passivated devices, see Fig. 3.11. In a frequency dependent CP measurement the number of charges pumped per cycle N_{CP} stays constant over f if only interface traps are considered [Gro+84]. Usually, an increase of N_{CP} with decreasing frequency is observed due to border traps with larger time constants [Fle92]. The characteristics in Fig. 3.11 are normalized at 1 MHz to account for the large difference in virgin interface trap density of the devices (less H: $D_{\mathrm{IT}} \approx 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, more H: $D_{\mathrm{IT}} \approx 10^{9}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$) [Aic+10b]. Numerous border traps on the devices with less H near the interface are observed. This indicates that hydrogen passivates border traps and interface states, the former being positively charged.

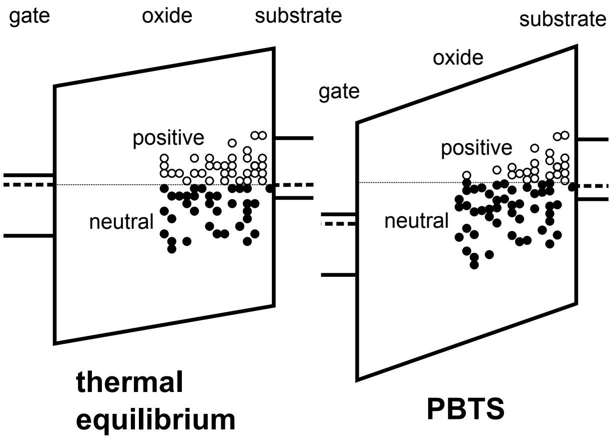

Fig. 3.12: Simplified band diagram of an nMOSFET with an n^{++} doped poly gate in thermal equilibrium and during PBTS [PNG12]. Charge exchange with the gate and band bending are neglected. Empty circles above the Fermi level represent positively charged and filled circles below the Fermi level neutral traps, respectively.

Model for the apparent negative charge build up during PBTS

The larger drift in Fig. 3.8 of the device with less H near the interface means that the PBTS neutralizes previously existing positive charges within the gate oxide or at the Si-SiO_2 interface. That is to say, hydrogen reduces the number of precursors for PBTI, as in stark contrast to NBTI where the precursor density is increased. The neutralization of positive charges appears as a negative charge increase because of the missing reference point which would be the charge-free V_{FB} value. In Fig. 3.12 the band diagram of an nMOSFET device during PBTS and recovery is shown. It is believed [Pob+11b] that the hydrogen passivation decreases the density of positive charges within the SiO_2 which can be activated in a PBTI experiment.

Additionally, Fig. 3.9 reveals that the hydrogen passivation has a similar neutralization effect as PBTS. That is, both shift the CV characteristic towards positive infinity by neutralizing positive charges. In conclusion, the positive charges present after manufacturing of the device may either be neutralized by hydrogen passivation or by PBTS, the latter leading only to a temporary neutralization [PNG12; PNG13].

3.2 Power metal type

In principle, proper encapsulation of a device should impede any influence of BEOL process steps on the NBTS reliability. However, rare observations indicate indeed that particular BEOL process steps may have an impact on NBTI [Nel+05; Ho+06; Aic10]. Also an influence of the type of power metallization, be it aluminium (Al) (usually standard) or copper (Cu) (introduced only recently for power devices [Nel+11]), on the instability was reported [Aic10].

In order to further study this effect a dedicated wafer split with equivalent devices, differing only in the power metallization, has been fabricated and analyzed. The results of this Section are also summarized in [SPN12] and were obtained by the Master Student Roberta Stradiotto [Str13] in cooperation with the author.

3.2.1 Process differences

Considerable differences between the process steps for deposition of aluminium (Al) and copper (Cu) as metal layers to connect power semiconductor devices exist. Al is usually sputtered uni-

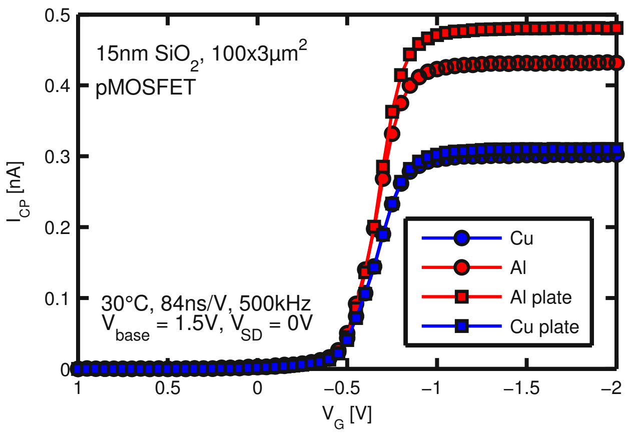

Fig. 3.13: Constant base level CP measurement of four virgin devices which have undergone Al or Cu processing, with or without a power metal plate on top [SPN12].

formly over the whole wafer area. A photoresist mask is then used to expose only certain areas of the wafer to an Al etching agent. In contrast, processing Cu, usually only a thin seed layer is sputtered over the whole wafer area. The photoresist mask is then used to impede the electrochemical deposition of Cu where the material is not needed. After removal of the photoresist mask the thin seed layer of Cu is etched away.

Both variants of power metallization share the initial sputtering step over the whole wafer. So independently of whether there is metal above the device or not, it had been covered by the metal during processing. Consequently, devices with or without a power metal plate on top should perform and degrade equivalently. It will be shown in the next Subsection that this is indeed the case.

3.2.2 Electrical characterization

Remarkably, in a comparison of the transfer characteristics of the virgin devices with Al or Cu metallization the device-to-device variability within one metal type is larger than the impact of the power metallization process (not shown). Only with a CP measurement, which is very sensitive to differences in the virgin interface trap density, a small difference as illustrated in Fig. 3.13 is detected. Thereby, the device with Al power metallization has a larger CP current than the Cu power metallization device, indicating a larger virgin interface trap density [SPN12]. Furthermore, it is irrelevant for the virgin performance of the device whether the metal is kept at the top of the device (traces labeled ‘plate’ in Fig. 3.13) or removed.

Fig. 3.14 shows the result of NBTS for devices with different power metallization. It is observed that the devices with Al power metallization drift more than the devices with Cu power metallization. By using a repetitive MSM experiment it is shown in Fig. 3.14 that the difference is due to the permanent component P while the recoverable component R is equivalent for both types of power metallization. It is remarked that this measurement gives only an estimate of P and R. P is calculated from the remaining shift after a 1 ks long recovery phase around the V_{TH}. R is estimated from the recovery between the first and last measurement point, 10 ms and 1 ks after termination of the stress after a recovery phase at 200 °C.

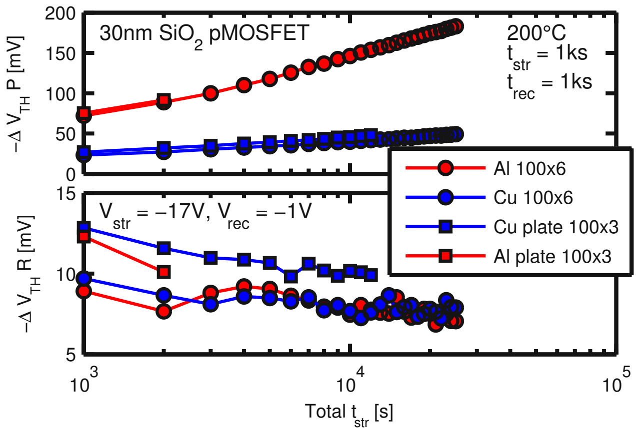

Fig. 3.14: Impact of the power metallization process on the permanent and recoverable component defined by time constants of NBTI in an MSM experiment [SPN12].

3.2.3 Discussion

The larger drift of the devices with Al power metallization despite the very similar virgin characteristics is challenging to understand. One possible reason could be in principle plasma induced damage. This effect is the charging and associated degradation due to accumulation of ions during plasma processing [Eri+12]. If this is the reason for the different drift behavior, also small differences in the performance of the virgin device should be visible. Furthermore, difficult to understand is the aspect that the virgin interface trap density of the Al device is larger than that of Cu processed devices. If the hydrogen passivation degree, as described in Section 3.1, would be responsible for the different behavior, the result should be the opposite, meaning Al should drift less compared to Cu. However, it is still likely that the behavior is connected to hydrogen because only the quasi-permanent component P is affected by the type of the power metallization. This shows similarities to the devices with different hydrogen passivation described in Section 3.1.3, where also only the quasi-permanent component is affected. This indicates that both topics have most probably a common microscopic origin, the interaction of defects near the interface with hydrogen.

A possible explanation for this discrepancy can be found in [DMC69; Dun89], where it is described that Al acts as a catalyst to split molecular H_2 or water (H_2O) into more reactive atomic hydrogen. It is speculated that the high temperature steps during Al deposition cause atomic as well as molecular hydrogen to diffuse towards the Si-SiO_2 interface. There, the two species may either create additional interface traps via the reaction (3.4) which would lead to a larger interface trap density measurable in CP, or may passivate existing interface traps with the inverse reaction. For either power metal type, one of the two mechanisms may have a larger impact than the other.

4

Accurate high temperature measurements

The degradation mechanisms in MOSFETs listed in Section 1.1 usually have a strong temperature activation. This means that these mechanisms become more pronounced when the MOSFET is operated or stressed at temperatures above room temperature. For a detailed characterization of the device it is thus important to be able to conveniently change the temperature of the device in a fast and reliable manner.

There are two main approaches for controlling the temperature of a device during an experiment. For measurements directly on the wafer the device temperature is usually set using a thermal chuck. For packaged devices a temperature-regulated furnace is used. Both approaches suffer from the drawback that reliable changes of the temperature usually require minutes to hours. Particularly in conventional systems the metal shielding is thermally coupled to the chuck and thus follows all temperature switches. As the metal shielding also carries the needle holding manipulators the thermal expansion following a temperature switch causes the needles to move slightly with respect to the pads of the device which may result in contact loss. For a reliable temperature switch it is mandatory to wait until the expansion of the shielding is completed before a long-lasting measurement can be started. This time period can last several hours which renders measurements at different temperatures a cumbersome task.

A second major drawback of thermal chuck systems and dedicated furnaces is that the highest achievable temperature is usually limited to about 200 °C to 300 °C. It is possible to build a system which can endure temperatures up to 700 °C [BW08], but only by using expensive materials which can sustain these high temperatures within the furnace for mounting and connecting the device.

The above mentioned drawbacks can be overcome with justifiable effort using a poly-heater, an in-situ heating structure surrounding the device under test directly on the wafer [MT92; Mut+03; MW04; Wan+06; KWS07; Sch+07; Aic+10c; Pob+ pa]. The following Sections introduce the

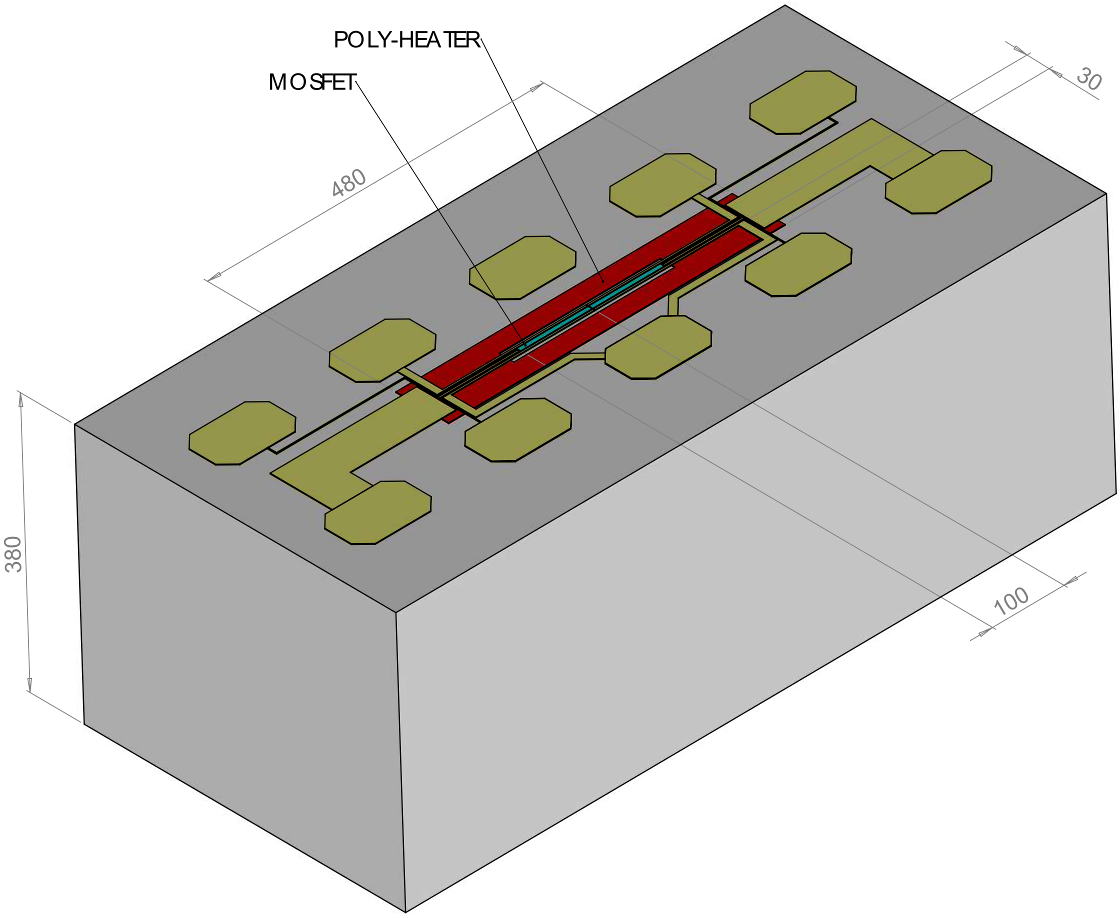

Fig. 4.1: Schematic drawing of the poly-heater (red) with contact pads (yellow) on a part of an Si or SiC wafer (gray). Two devices (blue) are centered in the middle of the heater. Oxide layers between the poly and the metal are omitted for illustration purposes. All dimensions are in micrometer.

use of the poly-heater for measurements featuring fast and reliable temperature changes beyond temperatures provided by conventional chucks or furnaces [Pob+ pa].

4.1 The poly-heater

The poly-heater is a simple arrangement of two polycrystalline silicon (poly) lines around a device as sketched in Fig. 4.1. An electric current fed to the two contacts of the poly-heater causes Joule heating in the heater which also increases the temperature of the adjacent regions, i.e. especially the device under test (DUT). Because the chuck acts as a heat sink, the heat flows mainly towards the bottom. This introduces a temperature gradient within the whole material stack. Of course, the heater and the device need to be electrically isolated from each other to be able to independently bias the heater and the device to perform arbitrary electrical experiments. This electrical isolation introduces also a thermal isolation, as also visible in Fig. 4.2. Consequently, the device temperature will generally differ from the temperature of the heater itself and must be determined individually.

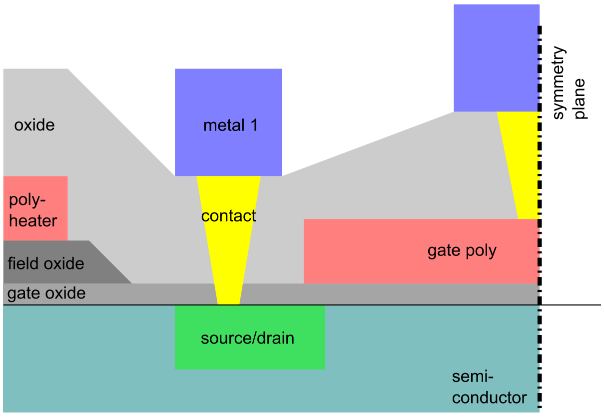

Fig. 4.2: Schematic cross section of the poly-heater and the device highlighting the structure between the device and the heater. The poly-heater is only partially shown and extends further to the left.

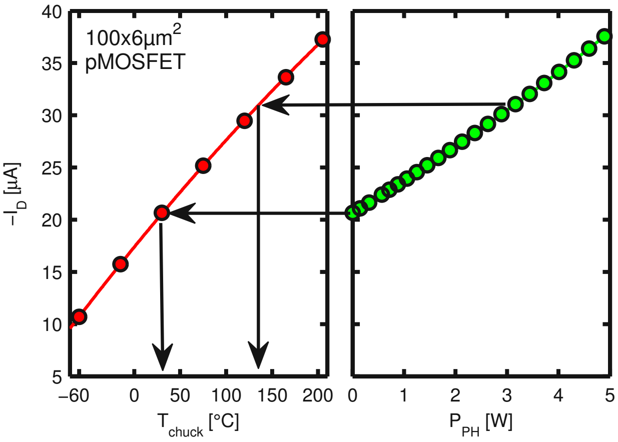

Fig. 4.3: Concept for the determination of the device temperature [Aic+10c; Pob+ pa]. The change of the drain current I_D with the power supplied to the poly-heater P_PH can be mapped to the device temperature T_dev using a previously recorded dependence of I_D on the chuck temperature T_chuck.

4.2 In-situ temperature measurement

4.2.1 Drain current

In order to determine the temperature of the device during poly-heater use, the dependence of the drain current on the chuck temperature $I_\mathrm{D}(T)$ is needed. With this an increase of the drain current due to power dissipation in the poly-heater can be calculated to an according temperature increase. See the left hand side of Fig. 4.3 for a sample dependence of I_D on the chuck temperature. For this an operating point must be chosen which should be different from the temperature compensation point of the MOSFET [Spi+02]. From the full transfer characteristic of the device at every chuck temperature an operating point can be chosen where $I_\mathrm{D}(T)$ can be approximated by a low order polynomial to ease the I_D to T conversion. This dependence can later be used to map every increase of the drain current with poly-heater power supply to an increase of the device temperature [Aic+10c; Pob+ pa] as shown at the right hand side of Fig. 4.3.

4.2.2 Body diode current

The same concept for device temperature determination for the drain current can also be used to determine the body temperature with the current through the body diode, which is the current from source and drain to the bulk. In Fig. 4.4 the temperature measurements with either the drain or the body diode current are compared to each other. The graph shows that the different currents

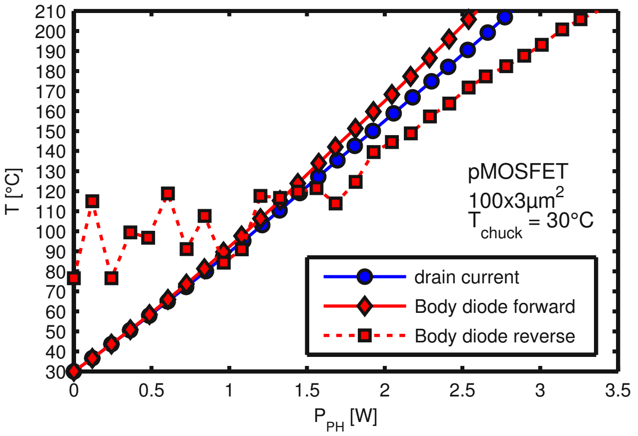

Fig. 4.4: Comparison between T_{dev} measured by using I_{D} or the body diode current in forward or reverse direction. For the particular dimensions of the body diode of the DUT, the reverse body diode current is only resolvable ($I > 10\,\mathrm{pA}$) above approximately 125 °C.

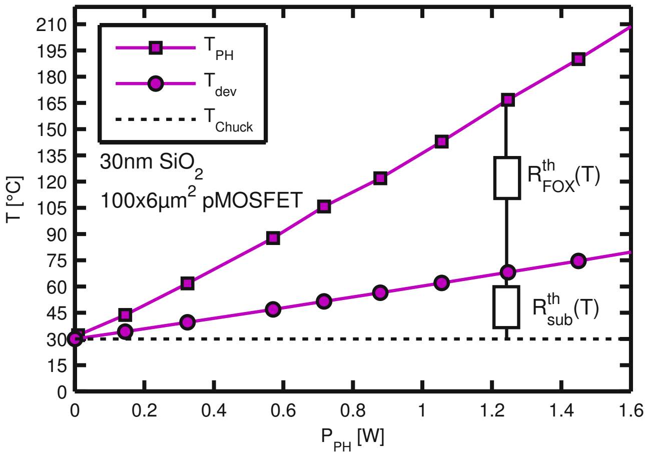

Fig. 4.5: Increase of the device T_{dev} and poly-heater temperature T_{PH} with increasing electrical heater power [Pob+ pa]. The reason for the temperature difference between the poly-heater and the device can be lumped together into a thermal resistance of the field oxide $R^{\mathrm{th}}_{\mathrm{FOX}}$ and a $R^{\mathrm{th}}_{\mathrm{sub}}$ for the substrate.

give vastly different temperature values at the same poly-heater power values. The temperature obtained from the body diode does not reflect the temperature of the interface because of the temperature gradient within the device stack [Aic+10c], cf. also the finite element method (FEM) simulations subjacent depicted in Fig. 4.14. Furthermore, there is a difference in the temperature obtained by biasing the body diode in forward direction compared to the reverse direction. This difference most probably results from the fact that different areas within the semiconductor or pn-junction are responsible for either current. The reverse current exhibits a lower temperature as it averages over the large space charge region which extends into colder parts of the semiconductor. Generally speaking, even though the body diode current is predominately used to determine the device temperature [Mut+03; MW04; Sch+07; Boi+12], the use of the drain current is more appropriate for most studies because it directly reflects the temperature of the active device region [Wan+06; KWS07; Aic+10c; Pob+ pa].

4.2.3 Poly-heater

The change of the resistance of the poly-heater can be used to obtain the temperature of the poly wires. This temperature is always much larger than the device temperature, see Fig. 4.5. The reason why the temperature of the poly wires is always much higher than the device lies in the finite thermal resistances between the heater and the device. As will be described later, the correct understanding of the characteristics of these thermal resistances is important for an accurate determination and extrapolation of the device temperature.

4.3 Reliable device temperature extrapolation

One of the main benefits of the poly-heater is that very high temperatures can be achieved by supplying large electric power to the heater. However, the methods to determine the device temperature presented in the preceding Section can only be used up to the highest temperature of an external heating system like the thermal chuck or a dedicated furnace. For higher temperatures an extrapolation scheme is needed. One could, in principle, extrapolate the $I_\mathrm{D}(T)$ relationship to higher values with the help of a technology computer aided design (TCAD) simulation. However, for this approach calibrated material parameters for the device are needed. Those parameters need to be measured on a test system which can handle such high temperatures. Additionally, at these high temperatures already the biasing for the T dependent drain current measurement can lead to degradation of the device. To overcome these limitations an extrapolation scheme was developed which has the potential to work up to arbitrary temperatures. Only the breakdown field of the field oxide and electromigration in the poly wires should create a limit before the materials which build up the device may melt [Pob+ pa]. This extrapolation method uses the change of the thermal resistance of the substrate to calculate the device temperature directly from the power dissipated in the heater.

4.3.1 Thermal resistance measurement

At the heart of the extrapolation method lies the idea that the change of the thermal resistances between the device and the heat sink with temperature needs to be taken into account. The thermal resistance R^th is defined as

$$R^\mathrm{th} = \frac{d\Delta T}{d\dot{Q}}. \tag{4.1}$$

For Joule heating, the heat flow $\dot{Q}$ equals the dissipated electric power P_PH and leads to a temperature rise ΔT. Consequently, an apparent thermal resistance can be calculated from the rise of the temperature with P_PH. As a particular example, in Fig. 4.5 the device temperature rises by about 30 °C with 1 W of power supplied to the poly-heater. This means that the apparent thermal resistance of the substrate below the device $R^\mathrm{th}_\mathrm{sub}$, which includes the three-dimensional (3D) heat spread in a phenomenological fashion, is about $30\,^\circ\mathrm{C\,W^{-1}}$ at 30 °C chuck temperature. If this measurement is now repeated at several chuck temperatures the experimental temperature dependence of the substrate thermal resistance is obtained. In Fig. 4.6 the $R^\mathrm{th}_\mathrm{sub}(T_\mathrm{chuck})$ values for several technologies are drawn. As can be seen, for the value of $R^\mathrm{th}_\mathrm{sub}$ the type of transistor (n- or pMOSFET), its area and the type and thickness of the gate oxide are irrelevant. Also device-to-device variations are very small. The only important parameters are the type and thickness of the substrate material [Pob+ pa]. For all investigated technologies the dependence of the thermal resistance on the temperature can be approximated by a linear function in the investigated temperature range, as can be seen from the dashed lines in Fig. 4.6.

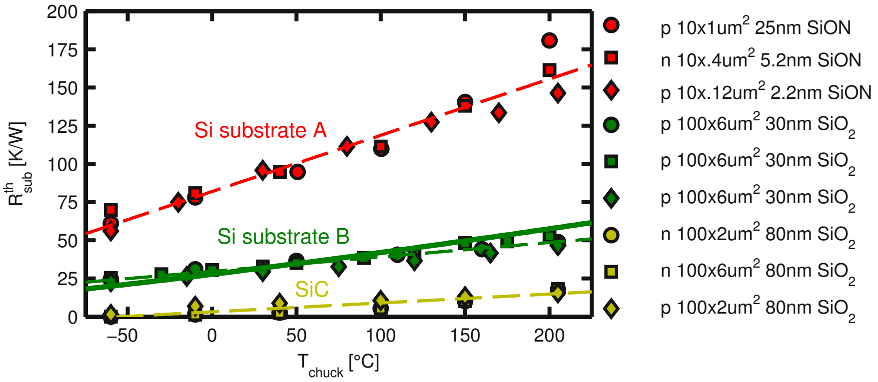

Fig. 4.6: Measured apparent thermal resistances of the substrate for n- and pMOSFET devices with different area and oxide technology [Pob+ pa]. The $R^{\mathrm{th}}_{\mathrm{sub}}$ depends mostly on the type and thickness of the substrate. The thick solid line is the theoretical solution for the actual size of the poly-heater after [Let+87].

4.3.2 Analytical extrapolation method

Using the definition of the thermal resistance

$$R^{\mathrm{th}} = \frac{\mathrm{d}\,T}{\mathrm{d}\,\dot{Q}} \equiv \frac{\mathrm{d}\,T}{\mathrm{d}\,P} = T'(P), \tag{4.2}$$

and an approximately linear dependence of $R^{\mathrm{th}}_{\mathrm{sub}}$ on the temperature

$$R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{dev}}) = aT_{\mathrm{dev}} + b, \tag{4.3}$$

one obtains the differential equation

$$T'_{\mathrm{dev}}(P_{\mathrm{PH}}) = aT_{\mathrm{dev}} + b. \tag{4.4}$$

With the requirement that the device temperature equals the chuck temperature when there is no power supplied to the heater ($T_{\mathrm{dev}}(P_{\mathrm{PH}} = 0) = T_{\mathrm{chuck}}$), the equation has the solution

$$T_{\mathrm{dev}}(P_{\mathrm{PH}}) = T_{\mathrm{chuck}} \exp\left(aP_{\mathrm{PH}}\right) + \frac{b}{a}\left(\exp\left(aP_{\mathrm{PH}}\right) - 1\right). \tag{4.5}$$

This means that the rise of the device temperature is an exponential function of the heater power [Dar+12; Pob+ pa]. For the standard formulation of the thermal resistance with the three constants $R^{\mathrm{th}}_{\mathrm{sub},0}$, α and T_0

$$R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{dev}}) = R^{\mathrm{th}}_{\mathrm{sub},0}\left(1 + \alpha(T_{\mathrm{dev}} - T_0)\right), \tag{4.6}$$

where α is the temperature dependence of $R^{\mathrm{th}}_{\mathrm{sub}}$ and $R^{\mathrm{th}}_{\mathrm{sub},0}$ is the reference thermal resistance at temperature T_0, the solution is

$$T_{\mathrm{dev}}(P) = T_0 - \frac{1}{\alpha} + \left(\frac{1}{\alpha} + T_{\mathrm{chuck}} - T_0\right) \exp\left(\alpha R^{\mathrm{th}}_{\mathrm{sub},0} P_{\mathrm{PH}}\right) \tag{4.7}$$

or, if $\alpha = 0$

$$T_{\mathrm{dev}}(P) = T_{\mathrm{chuck}} + R^{\mathrm{th}}_{\mathrm{sub},0} \times P_{\mathrm{PH}}. \tag{4.8}$$

With this equation it is possible to calculate the temperature of the DUT directly from the power dissipated in the poly-heater. This method has several advantages:

- The extrapolation depends on a linear fit of $R_{\text{sub}}^{\text{th}}(T_{\text{chuck}})$ which is a steady state measurement and can be performed with great accuracy.
- The approach is independent of device-to-device variations because the drain current is only needed once to determine $R_{\text{sub}}^{\text{th}}(T_{\text{chuck}})$. Repeated use of the same parameters on different devices are independent of the characteristics of the actual device. Only the structure and dimensions of the poly-heater must be the same.
- The electrical resistance of the poly-heater can vary within a wafer or a technology because of process variations for the poly deposition. The proposed method is independent of such heater-to-heater variations since the biasing of the poly-heater is adjusted to ensure a constant power dissipation which means a constant heat generation.
- The measurement of $R_{\text{sub}}^{\text{th}}(T_{\text{chuck}})$ needs to be done only once per technology and not once per DUT as for the conventional method described in Section 4.2.1.
- The method is very accurate and precise in the temperature range where it can be compared to measurement data, i.e. in the range of the thermal chuck, cf. Fig. 4.10.
- The extrapolation depends only on the assumption that the temperature dependence of the thermal resistance will not change its *behavior* in the extrapolated region. This is a fairly save assumption considering that the temperature dependence between 0 K and the melting point of Si is well captured by $R^{\text{th}} \propto T^{1.324}$ [Let+87]. Using exactly this dependence, however, leads to a solution of the differential equation (4.4) as

  $$-\frac{32.4088 \times T_{\text{chuck}}^{243/250}}{\left(3.08642/T_{\text{chuck}}^{81/250} - P\right)^{7/81}\left(-3.08642 + P \times T_{\text{chuck}}^{81/250}\right)^{3}}, \tag{4.9}$$

  which is rather annoying to handle. But the temperature dependence of $R_{\text{sub}}^{\text{th}}$ can be approximated reasonably well by a linear function in the range of the poly-heater use which gives also very accurate results and highlights the essential aspect that the device temperature follows roughly an exponential function on the power supply.
- The approach is independent of the actual material between the device and the heat sink. It can be in principle also be used for other technologies like silicon-on-insulator, SiC based MOSFETs or gallium nitride (GaN) based transistors.

In other words, the expression (4.7) approximates the complex thermal problem of the device and the poly-heater by a simple one-dimensional (1D) thermal model as sketched in Fig. 4.7. The main assumption of this model is that the heat is mainly flowing from the poly-heater to the backside of the wafer, which neglects heat transport through the top surface. This is justifiable since heat may leave the top surface only through radiation or convection. Radiation may be estimated by the Stefan–Boltzmann law to be negligibly small ($\dot{Q} < 1\,\text{mW}$ if $T < 500\,^{\circ}\text{C}$). Convection can be estimated from Newton's law of cooling with a heat transfer coefficient of air at atmospheric pressure of about $20\,\text{Wm}^{-2}\text{K}^{-1}$ to $30\,\text{Wm}^{-2}\text{K}^{-1}$ to be on the order of $10\,\text{mW}$ for the small area of a semiconductor test structure [Pob+ pa].

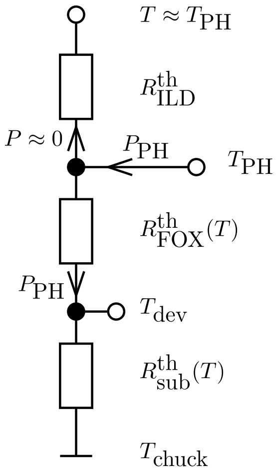

Fig. 4.7: Steady state 1D thermal model of the poly-heater. The materials and the heat spreading are reduced in a phenomenological fashion to the effective thermal resistances of the field oxide $R^{\mathrm{th}}_{\mathrm{FOX}}$ and the effective thermal resistance of the substrate $R^{\mathrm{th}}_{\mathrm{sub}}$. The heat flow towards the top surface can be neglected which makes the thermal resistance of the inter level dielectric (ILD) irrelevant.

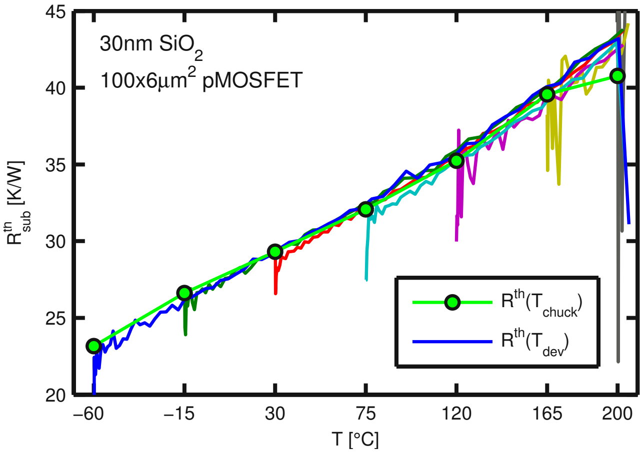

Fig. 4.8: Comparison of the differential thermal resistances $R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{chuck}})$ measured with small poly-heater sweeps at different chuck temperatures and $R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{dev}})$, the derivative of the increase of T_{dev} with P_{PH} during poly-heater use.

The method uses the parameters of $R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{chuck}})$, which represent the effective thermal resistance of the substrate at the chuck temperature. However, during poly-heater use the substrate experiences a rather large temperature gradient since the top of the substrate is at the device temperature and the bottom at the chuck temperature. The increase of the device temperature with heater power during poly-heater use can be expressed by $R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{dev}})$. So this value should be in principle different from the aforementioned value $R^{\mathrm{th}}_{\mathrm{sub}}(T_{\mathrm{chuck}})$ because of the temperature gradient. Still, as shown in Fig. 4.8, the two values coincide. In the following Section it will be shown, utilizing a 3D electro-thermal simulation, that the most probable reason for this is the occurrence of a bottleneck effect.

4.4 Assessment of the extrapolation model

The model for the increase of the device temperature with power supplied to the heater proposed above must be validated. Within the range of the temperature of the thermal chuck the approach can be tested experimentally. Outside this range the extrapolation can be compared to thermal FEM simulations which are capable of handling non-linear thermal resistances. Such simulations give an approximate temperature distribution by transferring the partial differential heat equation to linear equations and solving them numerically.

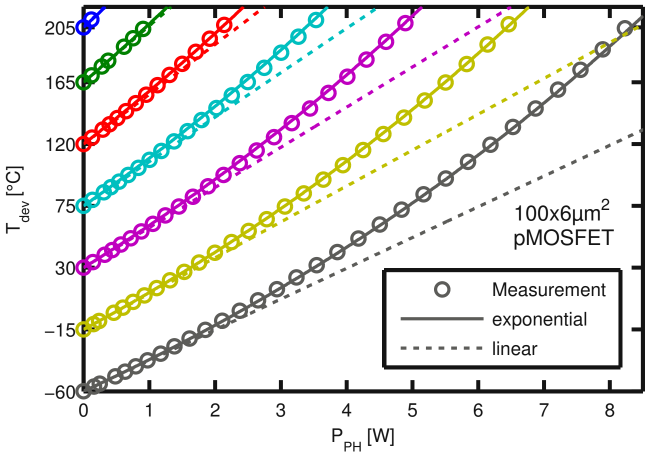

Fig. 4.9: Measured rise of the device temperature with poly-heater power supply in the temperature range of the thermal chuck (symbols) for several T_{chuck} [Pob+ pa]. The lines are the estimations of T_{dev} for linear (4.8) and exponential (4.7) extrapolation.

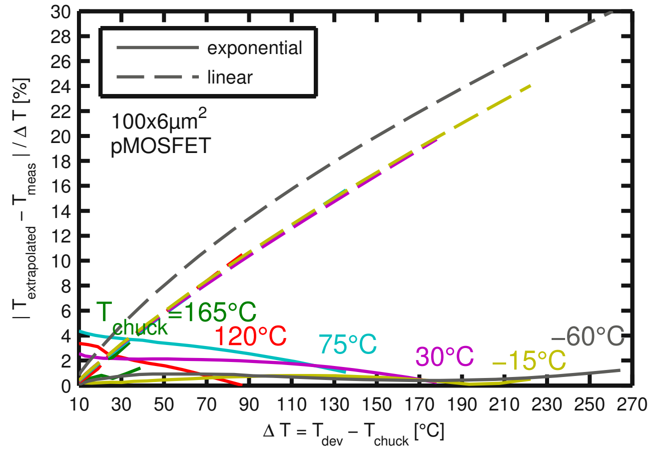

Fig. 4.10: Relative error of the linear (4.8) and exponential (4.7) extrapolation method within the chuck temperature range [Pob+ pa].

4.4.1 Experimental

Within the chuck temperature range the extrapolation methods (4.7) and (4.8) can be compared with experimental data as shown in Fig. 4.9. The exponential extrapolation method can correctly capture the increase of the device temperature with heater power. In order to resolve the correctness of the approach better, Fig. 4.10 shows the relative error of the two methods over the switched temperature range. The error of the linear method rises with temperature difference while the error of the exponential method stays below a few percent.

The exponential extrapolation method includes the thermal resistance between the wafer and the chuck or between the die and the package. Consequently, the method can also be used to estimate the temperature of a device which is thermally decoupled from a heat sink. This allows reaching even higher temperatures in the device because only the inefficient mechanisms radiation and convection cause a reduction of the device temperature. For wafer tests thermal decoupling can be achieved by placing the wafer on a plastic layer or by inserting small area spacers between the wafer and the chuck. This approach considerably increases the accessible temperature range, as shown in Fig. 4.11. Consequently, also semiconductor materials which have a low thermal resistivity, as e.g. four layer hexagonal SiC (4H-SiC), which has about 40 % of the thermal resistivity of Si, can be operated at high temperatures with the poly-heater.

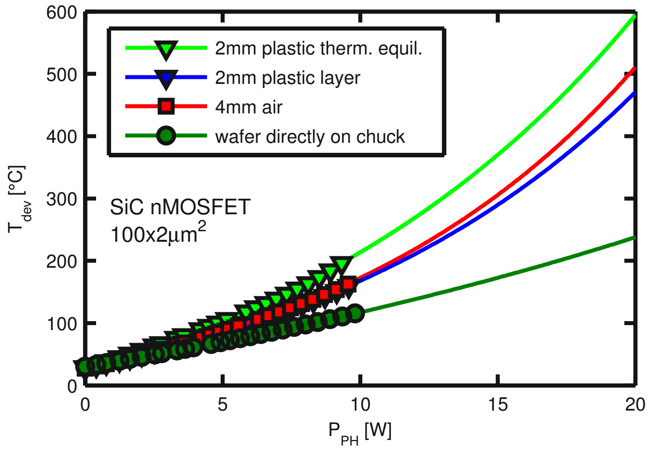

Fig. 4.11: Device temperature increase with heater power for a device on a wafer separated from the chuck by a 2 mm thick plastic board or 4 mm of air. The time until thermal equilibrium is reached is considerably longer than in the presence of a heat sink. For the uppermost line a wait time of 60 s per step is needed. Symbols are measurement data and the lines are the model.

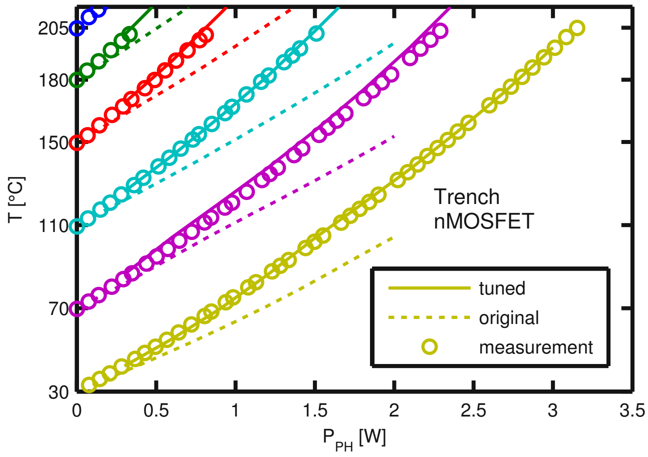

Fig. 4.12: Comparison of a 2D thermal simulation with Ansys with the rise of T_{dev} with heater power. The original temperature dependent thermal conductivity values of the materials of the model cannot capture the dependence. Only by changing the material parameters arbitrarily a good match can be obtained.

4.4.2 Thermal simulations

In a first attempt to model the increase of the device temperature with the power supplied to the poly-heater a two-dimensional (2D) thermal model was created using the commercially available analysis system (Ansys) FEM software by Ansys Incorporated. With this model an overall match with experimental data as shown in Fig. 4.12 could only be obtained by arbitrarily changing the thermal conductivity of the Si substrate and its temperature dependence. The extrapolation of such a simulation to high temperatures is not of particular interest because it is mostly determined by the effective thermal conductivity at high temperatures. That is to say, the simulation depends on the same assumptions as the exponential extrapolation method which should be tested. In order to exempt the simulation from the same assumptions a 3D model was implemented where both the current through the heater and the heat spread was calculated [Pob+ pa]. For this model the structure as sketched in Fig. 4.1 was simplified by omitting the metal wires. Consequently, the model consists basically of two bricks of poly surrounded by SiO_2, and situated on a large block of Si.

To correctly capture the poly-heater behavior, the poly lines were simulated electrically and thermally. For the other materials of the model it was sufficient to perform only a thermal simulation, i.e. no electrical device simulation was conducted. The temperature dependent electrical resistivity of the poly was obtained on a dedicated test structure on the same wafer. The temperature dependent thermal resistivity of the Si substrate was measured externally on an unprocessed

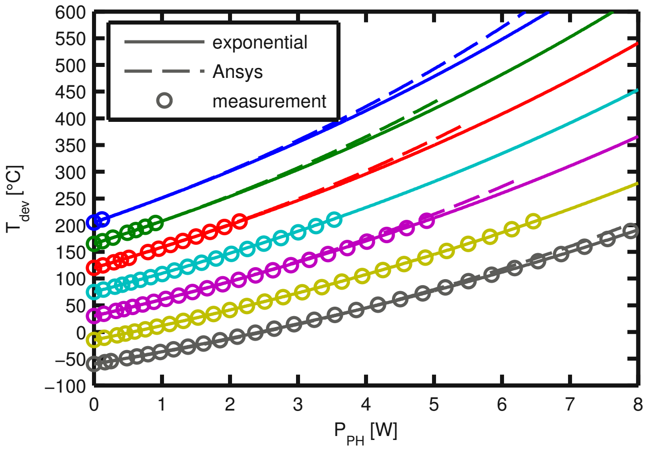

Fig. 4.13: Extrapolation of the device temperature for large heater power and high chuck temperatures [Pob+ pa]. Both the 3D electrothermal Ansys simulation and the exponential extrapolation method (4.7) give equivalent results in the temperature range above the highest chuck temperature of 200 °C.

raw wafer with a calibrated differential scanning calorimetry equipment. The value of the thermal resistivity is rather large compared to standard Si [Let+87; GS64] because of the high doping level of the substrate [Sla64; LA05], needed to reduce the on-resistance of vertical power devices residing on the same wafer. The temperature dependence of the thermal resistivity could be modeled better with a power law coefficient of 1, instead of the suggested coefficient of 1.324 [Let+87]. Also, a cross check of the change of the simulation result with a modification of the power law coefficient between 0.6 and 1.2 showed vanishing influence. That is to say, in a small range the particular choice of the power law coefficient is rather irrelevant and $R^{\text{th}} \propto T$ eases the calculations considerably.

The model has Neumann boundary conditions at all borders except at the bottom surface. Those boundaries act as adiabatic boundaries meaning that heat flow through the boundary is prohibited. At the bottom a phenomenological layer was introduced which accounts for the thermal behavior of the interface between the wafer and the chuck [CS01; IR05; Pob+ pa]. This layer is 20 µm thick and has a thermal conductivity of $0.5\,\text{W}\,\text{m}^{-1}\,\text{K}^{-1}$. The bottom surface of this interface layer was set to Dirichlet boundary conditions with the temperature of the chuck. A 4 mm × 4 mm large Si block was needed to account for the large lateral heat spread visible in an increase of the surface temperature at the outer boundaries. The device temperature was determined by averaging the temperature of the Si substrate near the interface to the SiO_2 at the exact position of the device.

In Fig. 4.13 a comparison between the simulation result and the exponential extrapolation method is shown. The 3D FEM simulation tends to overestimate the device temperature slightly. This might be due to the fact that, even though the exact dimensions of the heater structure and accurate material parameters were simulated, possible cooling parts were neglected. These are especially the power metal pads for device contact and the reduction of the actual wafer diameter from 200 mm to a 4 mm × 4 mm block.

The equivalent behavior of the extrapolation using (4.7) and the 3D simulation shows that the reduction to a 1D problem is a valid approach for the poly-heater structure [Pob+ pa].

Furthermore, the simulation allows investigating the reason for the equivalence of $R^{\text{th}}_{\text{sub}}(T_{\text{dev}})$ and $R^{\text{th}}_{\text{sub}}(T_{\text{chuck}})$. As shown in Fig. 4.14, during poly-heater use (high heater supply power) as well as during calibration (low heater power) approximately the same relative temperature distributions occur. The region of the highest temperature is always very close to the device. Since the R^{th} of

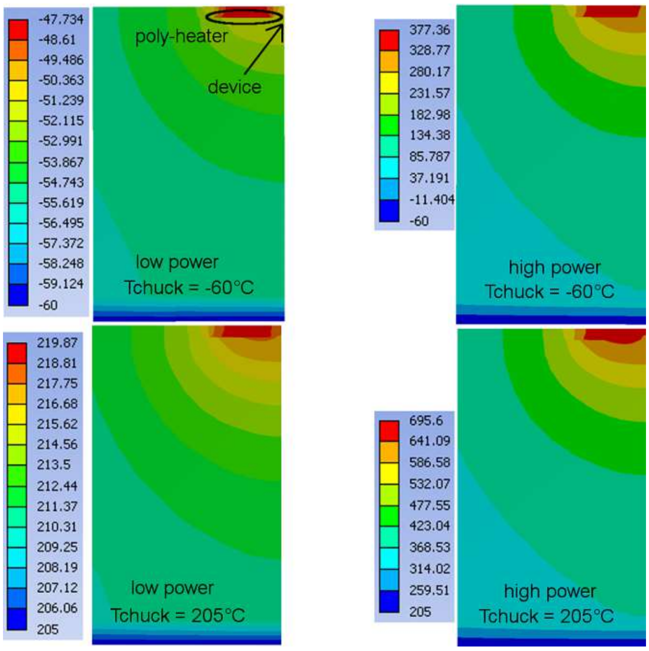

Fig. 4.14: Cross sections of the temperature distributions in the center of a poly-heater device [Pob+ pa]. Illustrated are two different chuck temperatures and two different power supply values. Only the central region of the device/poly-heater structure is shown.

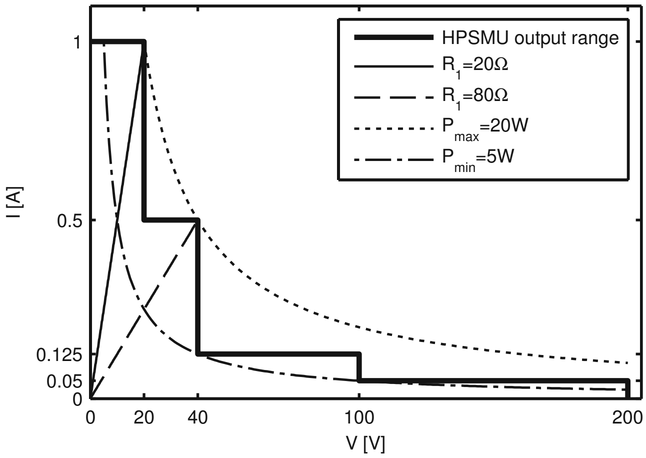

Fig. 4.15: Output range of the HPSMU used in this thesis. Only for load resistances of 20 Ω or 80 Ω the maximum power of 20 W can be reached. A minimum of 5 W can be supplied for most load resistances.

the substrate increases with temperature the same region is responsible for the thermal resistance. Consequently, the thermal resistance of the substrate is determined by the bottleneck region with the highest temperature close to the device and both approaches to measure the thermal resistance give equivalent results.

4.5 Experimental pitfalls

To reliably use the poly-heater a number of experimental issues have to be considered. A few of those are addressed in the following.

In order to reach high device temperatures the overall resistance of the poly-heater must be matched to the output characteristic of the SMU for maximum power transfer. For the particular high power SMU (HPSMU) of the Agilent Technologies B1500A parameter analyzer used in the present thesis, the resistance of the poly-heater needed to be designed to be around 20 Ω or 80 Ω in order to transfer the maximum power of 20 W as illustrated in Fig. 4.15.

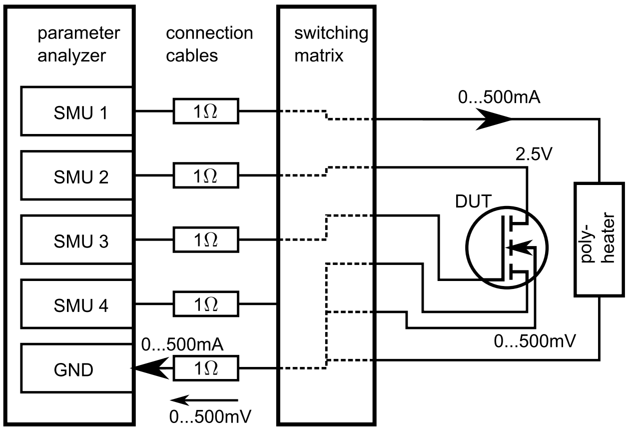

Fig. 4.16: If both the poly-heater and the source and bulk connection of the DUT are connected via a switching matrix to a ground potential a ground shift can occur. In this particular example, the drain-source voltage of the transistor varies between 2.5 V and 2 V depending on the current flowing through the heater.

Another problem can occur if a switching matrix is used to connect the DUT and the poly-heater to the parameter analyzer. As shown in Fig. 4.16, an incorrect connection can cause a ground shift for the potential of the DUT which leads to changes of the device behavior which are not due to temperature. Such a connection mistake can be exposed by inversion of the supply polarity of the poly-heater. If this changes the device characteristics a ground shift problem is a likely cause. It is therefore most convenient to use a secondary SMU as a separate virtual ground potential for the device.

Another possible issue regarding the use of the poly-heater is the occurrence of thermally induced strain. However, there are three major arguments that thermally induced strain does not impact the result of the measurements for poly-heater use.

- In reference [Lea+12], influences of mechanically stress on transistor performance are discussed. The work mentions stress values of up to $\sigma = 500\,\mathrm{MPa}$. By using Young's modulus of Si of about $k = 150\,\mathrm{GPa}$ [BL97; HNK10], the strain in the devices of reference [Lea+12] can be estimated as

  $$\varepsilon = \frac{1}{k}\sigma = \frac{1}{1.5\times10^{11}\,\mathrm{Pa}} 5\times10^{8}\,\mathrm{Pa} \approx 3\times10^{-3}. \tag{4.10}$$

  For comparison, the temperature induced strain in our devices for a deliberately overestimated temperature gradient along the device interface of 10 °C can be estimated from the thermal expansion coefficient of Si $\alpha = 3\times10^{-6}\,{}^{\circ}\mathrm{C}^{-1}$ [OT84] to be about

  $$\varepsilon = \alpha\times\Delta T = 3\times10^{-6}\,{}^{\circ}\mathrm{C}^{-1}\times10\,{}^{\circ}\mathrm{C} = 3\times10^{-5}. \tag{4.11}$$

  From this follows that the strain investigated in reference [Lea+12] is about two decades larger than what can be expected for our test device. Still, the changes in the saturation drain current in reference [Lea+12] are around 15 % for 500 MPa, i.e. for typical poly-heater devices the drain current may change less than 0.3 %, which is too small for any significant impact.

- In order to check for a potential influence of thermally induced strain on the transistor parameters, test structures with or without a several micrometer thick metal plate on top of the device and heater were constructed. As part of the structure, the metal stack is efficiently

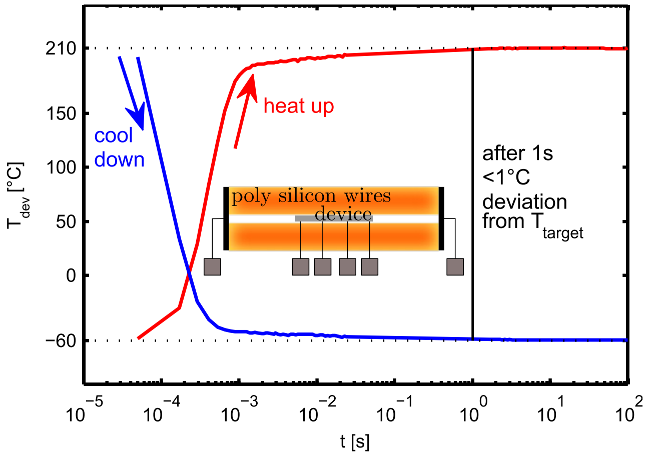

Fig. 4.17: Heating dynamics of the poly-heater [Pob+11b]. The device follows a switch of the power supply to the poly-heater with a small delay because of the finite thermal capacitances of the materials which surround the device and the heater.

heated with the poly-heater because the poly resides between the device and the metal. Metals have usually a much larger thermal expansion coefficient than Si or SiO_2. A device with a metal plate on top should experience different virgin characteristics or degradation behavior with or without a metal plate on top if thermally induced strain is occurring. However, up to now no impact of the metal plate on the device virgin characteristics or degradation behavior [SPN12] has been observed, even with the use of the poly-heater.

- To further check for a possible occurrence of parasitic effects of the poly-heater, NBTI experiments were performed where the stress temperature was either provided by using the poly-heater or by using the thermal chuck, see Chapter 5 for details. Both approaches give identical results of the transistor characteristics and their degradation behavior [PG13b]. This strongly indicates that the poly-heater only impacts the device temperature.

For the use of the poly-heater for time critical experiments care has to be taken that the thermal capacitances of the materials surrounding the heater prevent instantaneous temperature switches. However, for the poly-heater devices used in this thesis, a switch of the temperature from e.g. −60 °C to 210 °C occurs in less than 1 s, as shown in Fig. 4.17. Typically, the temperature switch is mostly completed after about 1 ms and the difference to the target temperature becomes unresolvable after a maximum of 10 s [Aic+10c; Pob+11b]. For NBTI experiments the poly-heater is usually used to provide a high stress temperature while recovery is measured at a much lower temperature to prevent undesirable recovery. There, it is especially important to terminate the stress by first switching off the poly-heater and, subsequently, reducing the gate bias. This approach is called degradation quenching [ANG08; Aic10].

5

Impact of temperature on BTI

The poly-heater described in Chapter 4 allows a thorough investigation of the influence of temperature on the BTI degradation and recovery mechanisms. The two main benefits of the poly-heater, which are unique in the context of BTI research, are temperature switches during the application of bias and the extension of the accessible temperature range. These features give for example the possibility to study the impact of the stress temperature independently of the recovery temperature. This provides extensive insight into the BTI degradation mechanism.

5.1 Measurement results overview

BTI is a temperature activated degradation mechanism, meaning the effect becomes more severe with increasing temperatures. Typically, temperatures at which BTI occurs are around 100 °C to 200 °C [AM05; HDP06; Sch07]. In a conventional BTI experiment the temperature is set by a thermo chuck or a dedicated furnace. There, it is usually not possible to maintain a bias applied to the device while performing a temperature switch. Furthermore, reliable temperature switches require minutes to hours. As a consequence, most T dependent BTI data is measured at the same stress and recovery temperature. This limitation may introduce errors such as inaccurate ΔV_{TH} values because the recovery temperature impacts the ΔV_{TH} value [ZCG07]. Furthermore, higher temperatures accelerate recovery from previously created damage [Kat08; ANG08; Ben+09]. The increased recovery with increasing temperature balances the increasing degradation, resulting in an apparently weak temperature dependence of BTI, which is inconsistent with the rather large activation energies of the defect precursors in the Si-SiO$_2$ system [Gra+11b]. In the following Subsections the impact of temperature is strictly separated in an influence on the stress phase and an influence on the recovery phase. This is achieved by a sophisticated use of the poly-heater.

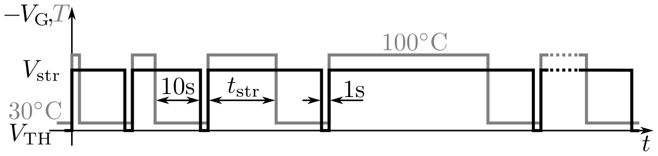

Fig. 5.1: Evolution of V_G and the device temperature in an isothermal MSM experiment.

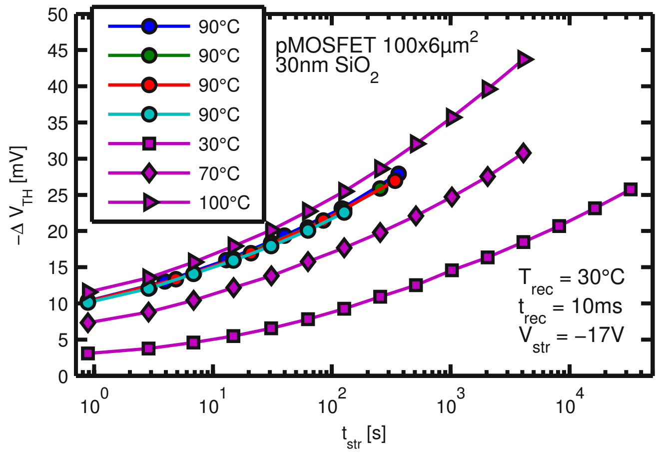

Fig. 5.2: Stress temperature dependence of NBTI in an MSM experiment. A bake phase at ≈ 400 °C for 10 s removes all created damage between each measurement. t_{str} is the cumulative sum of the stress duration. The 90 °C curves prove the reproducibility of the measurement.

5.1.1 Stress temperature dependence of BTI

The poly-heater can be used to vary only the stress temperature in an MSM experiment while maintaining the recovery temperature always at the same level. That is to say, a temperature and gate bias sequence as illustrated in Fig. 5.1 becomes possible. As a particular example, the device temperature is switched between 30 °C for the recovery and 100 °C during the stress. The temperature switch to 30 °C is always performed 10 s before the termination of the stress bias. This assures that the recovery remains unaffected by the choice of the particular stress temperature. The delay between the temperature switch and the bias switch causes a period with stress bias at 30 °C. Due to the temperature activation of the degradation the impact of the stress at 30 °C can be neglected in comparison to the stress at 100 °C. This approach is referred to as *degradation quenching* [ANG08; Aic10].

The results of such isothermal (constant stress temperature) MSM experiments are shown in Fig. 5.2. The recovery phase is an interruption of the stress bias of about 1 s at 30 °C. Within this period, the drain current measurement is performed 10 ms after the gate bias switch from stress to readout level (t_{rec}). The removal of the stress at a low temperature keeps the impact of the recovery small. The data in Fig. 5.2 marked with circles is measured at the same stress temperature but different stress times between each measurement point. The good overlap of all those traces indicates that the influence of the length of an individual stress phase is insignificant considering the sum of the stress time. Furthermore, The characteristics are recorded subsequently on the same device with intermediate bake steps. These bake steps for 10 s at 400 °C assure complete recovery from the NBTS and restore the virgin state of the device [Kat08; BOG08]. The overlap of the characteristics marked with circles therefore also proves that the measurement is reproducible.

The unique feature of the experiment shown in Fig. 5.2 compared to other, similar plots is that the recovery level is always the same, 10 ms at 30 °C, independent of the stress temperature. This gives quite different results compared to the standard approach where the stress temperature equals the recovery temperature as shown in Fig. 5.3. For a measurement with $T_{str} = T_{rec}$ the degradation level is much lower than with $T_{rec} < T_{str}$. This is because in the recovery trace 10 ms

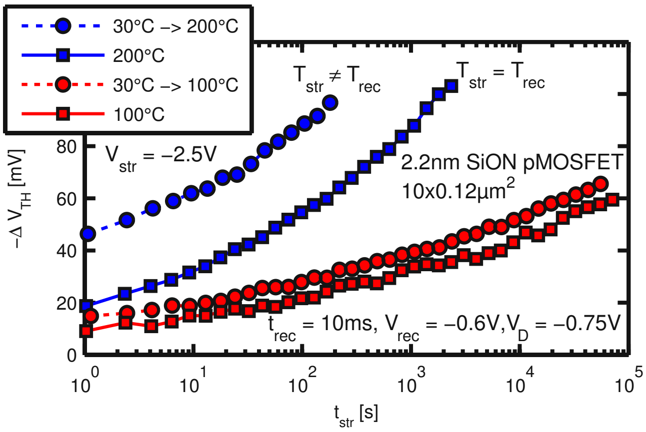

Fig. 5.3: Comparison of MSM experiments where $T_{\mathrm{str}} = T_{\mathrm{rec}}$ and where $T_{\mathrm{str}} \neq T_{\mathrm{rec}}$. The recovery temperature for the $T_{\mathrm{str}} \neq T_{\mathrm{rec}}$ characteristics is 30 °C.

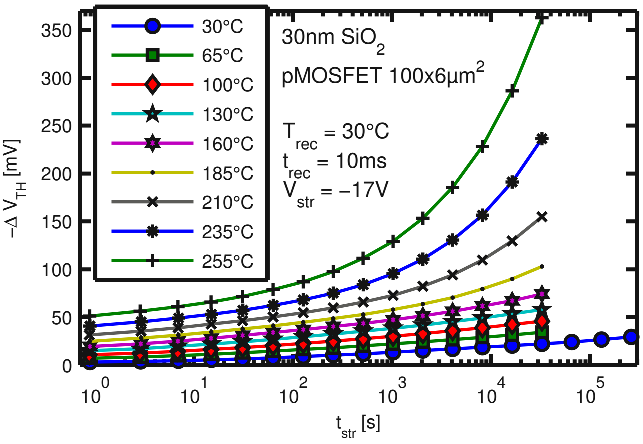

Fig. 5.4: Stress temperature dependence of NBTI in an MSM experiment. Only the stress temperature is varied while the recovery is always reduced to 10 ms at 30 °C.

after termination of the stress a larger part of the degradation has already recovered at higher T_{rec}. Furthermore, the interruption of the stress for about 1 s at 200 °C causes a larger recovery. As a result, this measurement shows that the impact of the stress temperature is larger than what would be expected from measurements where $T_{\mathrm{str}} = T_{\mathrm{rec}}$ and conventional MSM experiments at different temperatures should not be compared with each other.

In Fig. 5.4 the impact of the stress temperature on NBTI is depicted. Particularly evident is the larger increase of the ΔV_{TH} at stress temperatures > 200 °C. Possible reasons for the temperature activation of the degradation will be given in Sections 5.2 to 5.5.

5.1.2 Recovery temperature dependence of BTI

Similarly to the stress temperature, also the dependence of BTI on the recovery temperature can be measured using the poly-heater. However, the sequence of temperature and bias switches is more complex and is sketched in Fig. 5.5. As for the measurement of the stress temperature dependence, a degradation quenching phase is needed to avoid acceleration of the recovery due to unintentionally high recovery temperatures. The lowest temperature of this experiment was chosen to be −60 °C which is the lowest achievable temperature of the thermo chuck used in the thesis.

Simultaneously with the termination of the stress bias the power supply of the poly-heater is switched to a value corresponding to the desired recovery temperature. The thermal capacitances of the materials surrounding the heater and the device will cause the device temperature to follow

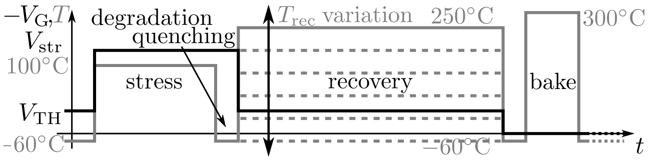

Fig. 5.5: Sequence of voltage and temperature changes for the experiment of Fig. 5.6.

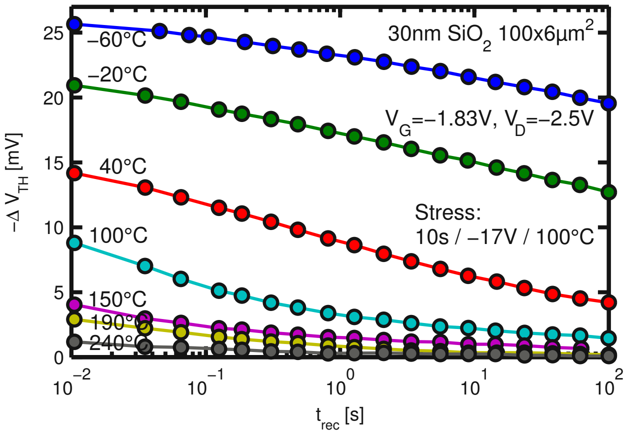

Fig. 5.6: Impact of the recovery temperature on NBTI [PG13b]. The stress phase is always at the same temperature, has the same duration and the same electric oxide field. Higher recovery temperatures decrease the observed ΔV_{TH} values.

the supply switch within a few seconds delay. See Section 4.5 for details on the restrictions of the poly-heater. The recovery in the first seconds after termination of stress will therefore not occur at exactly the desired T_{rec}. However, since the temperature is switched starting from −60 °C, and most of the temperature switch occurs already in the first millisecond (see Fig. 4.17) the recovery is not accelerated. Also, the temporary temperature deviation impacts mostly the dependence of the drain current on the temperature. The small temperature difference to the target T_{rec} causes a change in the drain current which results in a spurious ΔV_{TH} shift [ANG09a].

There are two ways to account for this effect and to obtain $\Delta V_{TH}(t_{rec})$ data which is unaffected by the unstable temperature phase. The first is to record the spurious $\Delta V_{TH}(t)$ characteristic following a temperature switch on the unstressed device prior to stress and to subtract this characteristic from the resulting $\Delta V_{TH}(t_{rec})$ characteristic of the stressed device [ANG09a; Aic10]. This is a very convenient approach and sufficient for most experiments. A second, more precise way is to record virgin $I_D V_G$ characteristics for every recovery temperature prior to stress. This is of course only possible by measuring $I_D V_G$s at a few distinct temperatures in the region of e.g. −60 °C to 250 °C, modeling the change of the transfer characteristics, and interpolating the temperature dependence of the parameters of the $I_D V_G$ model. The latter method is more elaborate but also more accurate because it also accounts for a possible dependence of the ΔV_{TH} value on the particular readout temperature [ZCG07].

The result of a measurement using this correction is shown in Fig. 5.6. In order to avoid inaccuracies related to device-to-device variability, the measurements were performed consecutively on a single device with intermediate bake steps of 10 s duration at 300 °C at zero gate bias to recover from all previous damage of the device [Kat08; BOG08; Pob+11b]. It is clearly evident that lower recovery temperatures cause a larger measurable degradation level [ANG08; Pob+11b; PG13b]. Particularly important is that the recovery occurs at the target recovery temperature already before the first measurement point 10 ms after termination of the stress. This means at higher T_{rec} most of the degradation has recovered before the first drain current measurement 10 ms after stress. Conversely, at −60 °C, most charges do not recover and a large ΔV_{TH} value is measured. Further discussions on the reason for the larger degradation level will be given in the following Sections.

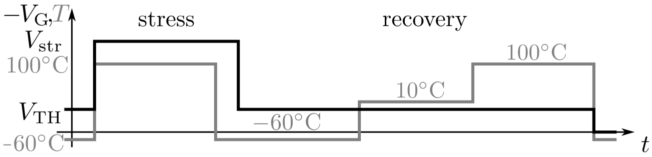

Fig. 5.7: Temperature and V_G sequence for an experiment where T_{rec} is switched during the recovery phase.

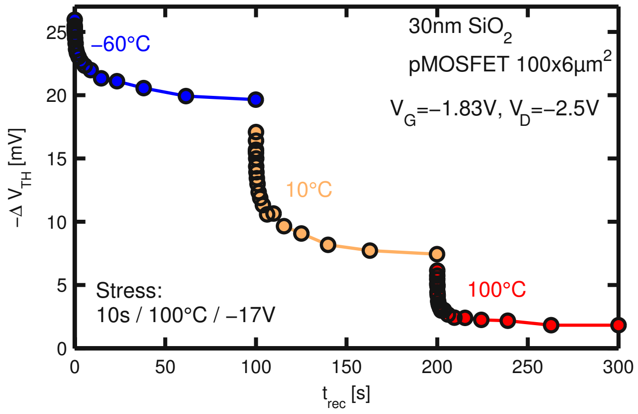

Fig. 5.8: Change of the threshold voltage drift over recovery time with intermediate T_{rec} switches. The recovery temperature is switched to higher values during the application of a constant recovery gate bias V_G. The temperature and gate voltage sequence is sketched in Fig. 5.7.

By using the poly-heater it is also possible to switch the temperature *during* the recovery while keeping the bias applied to the gate. The temperature and gate bias sequence for such an experiment is sketched in Fig. 5.7. The result of an example experiment is shown in Fig. 5.8. The switch to higher temperatures leads to an abrupt decrease of the remaining ΔV_{TH} [ANG08; Aic10]. Inversely, a switch to lower temperatures during recovery leads to a freeze of the degradation at the corresponding ΔV_{TH} value [ANG08; Aic10].

5.2 Interpretation using the temperature-time approach

In the following the results of the preceding Section concerning the temperature dependence of stress and recovery data of BTI are interpreted. The first approach presented in this Section is motivated by recent results on the BTI response of individual defects [Gra+10b]. This work showed that the temperature dependence of the capture and emission time constants of a single defect follow an Arrhenius equation [Gra+10a, Fig. 6&8]. Based on these findings it is possible to calculate how temperature changes accelerate or decelerate BTI stress and recovery. To facilitate presentation, an abstract temperature-time ϑ is introduced and applied to stress and recovery data.

5.2.1 Temperature dependence of single defects time constants

On MOSFETs with channel length and width in the sub-micrometer range the charge state of a single defect near the interface can have a measurable impact on the ΔV_{TH}. This is because following the definition of the capacitance $CA = Q/V$ the impact of a single charge q on the ΔV_{TH} is given by

$$\Delta V_{TH} = \frac{q}{C_{ox} A}. \tag{5.1}$$

If the area of the MOSFET A is reduced, the impact of a single charge on ΔV_{TH} increases. For an SiO$_2$ thickness of 2.2 nm the area of the MOSFET needs to be smaller than about 100 nm × 100 nm to observe a ΔV_{TH} induced by a single defect at the Si-SiO$_2$ interface larger than 1 mV, which is around the precision of a conventional ΔV_{TH} measurements [KU89; Rei+10].

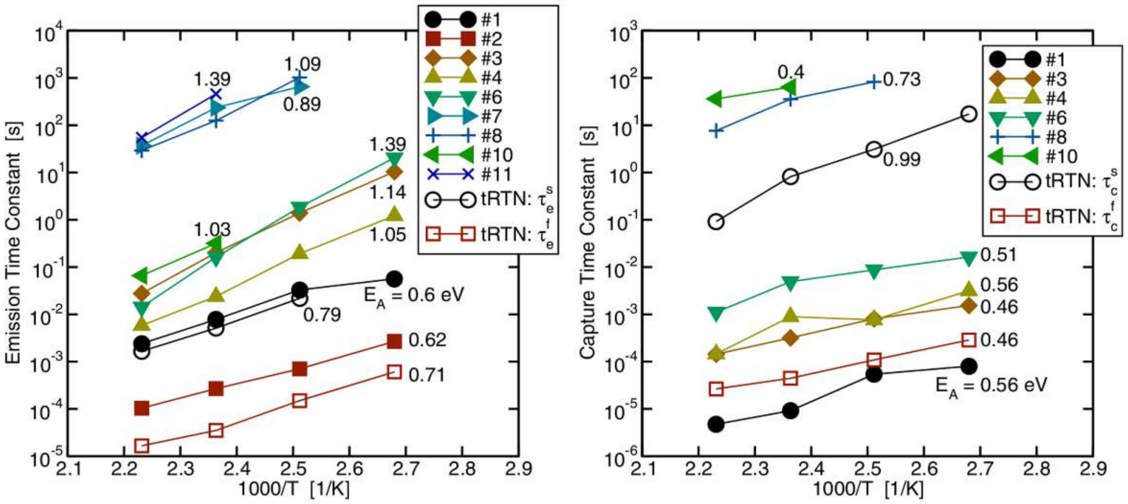

Fig. 5.9: Single defect emission (left) and capture (right) time constant temperature dependence from [Gra+10a, Fig. 8]. The defects are labeled arbitrarily. The almost linear relationship of $\log \tau$ over $1/T$ suggests an Arrhenius-like temperature activation as (5.3). The corresponding activation energy is written next to the particular characteristic.

The discharge of a single defect is visible as discrete steps in the $\Delta V_{\mathrm{TH}}(t_{\mathrm{rec}})$ trace [Rei+10; TL+11c]. The height of this step depends on the position of the defect with respect to the dopants in the channel. The dopants determine regions inside the channel where the drain current flows [Bin+12]. A single defect which is situated at a position where the majority of the drain current flows impacts the drain current more than a defect which is far away from this high current density regions. Consequently, the step height in the recovery trace is a fingerprint of an individual defect. With this it becomes possible to investigate the charge emission of a single defect despite of other emission events of neighboring defects within the same device [Gra+10a]. The analysis of such an experiment is referred to as time dependent defect spectroscopy (TDDS) [Gra+10a].

Thorough analysis of recurring emission events of single defects after stress have revealed that the emission time t_{e} at fixed recovery bias and temperature follows an exponential distribution as

$$p\left(t_{\mathrm{e}}\right) = \frac{t_{\mathrm{e}}}{\tau_{\mathrm{e}}} \exp\left(-\frac{t_{\mathrm{e}}}{\tau_{\mathrm{e}}}\right) \tag{5.2}$$

with a mean emission time constant τ_{e} (also named characteristic emission time) [Gra+10a; TL+11c]. By varying the temperature in those experiments it was found that the emission time constant changes with temperature following an Arrhenius equation [TL+11b; TL+11d; TL+11c; Rei+10; Gra+10a]

$$\tau = \tau_0 \exp\left(\frac{E_{\mathrm{A}}}{k_{\mathrm{B}} T}\right). \tag{5.3}$$

An equivalent argumentation applies for the capture time constants τ_{c} of BTI defects. In Fig. 5.9 the temperature dependence of the emission and capture time constants of a few selected defects in a single device are depicted. The capture and emission time constants of all defects are well represented by an Arrhenius equation (5.3). This temperature activation indicates that the microscopic charge exchange is not an elastic tunneling process [Gra12]. It is rather consistent with a nonradiative multiphonon theory [HR50; Vui+89]. However, the activation energy values appear

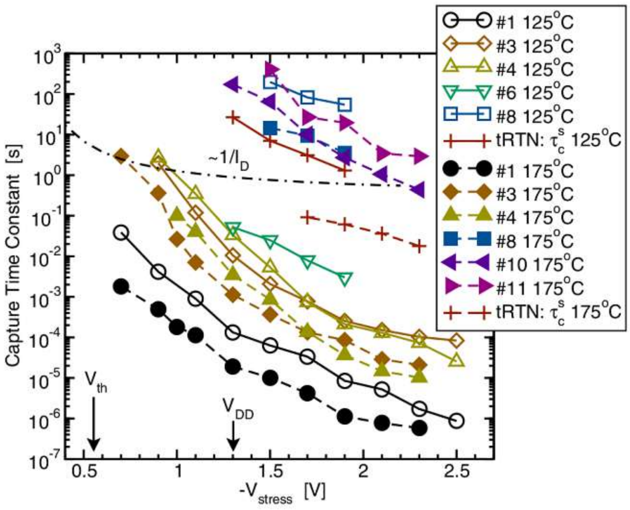

Fig. 5.10: Single defect capture time constant dependence on the stress bias from [Gra+10a, Fig. 6]. The capture time constants of all defects decrease with increasing stress bias or temperature. A model for this decrease based on SRH theory fails to reproduce the data.

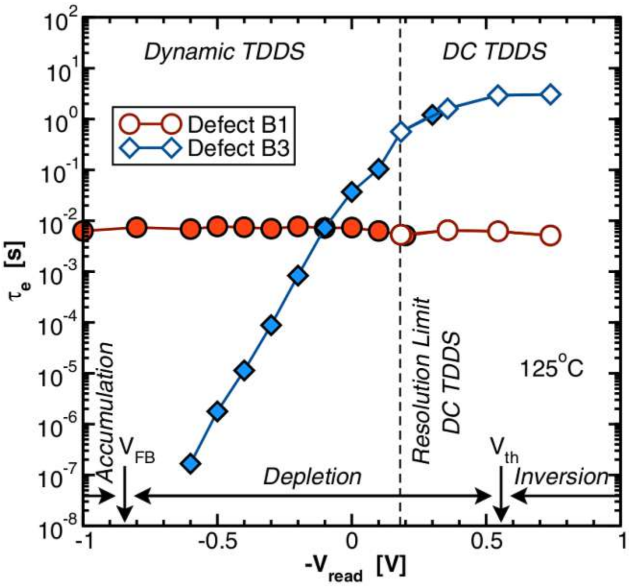

Fig. 5.11: Dependence of the emission time constants of two selected defects on the recovery or readout bias from [Gra+13a, Fig. 9]. The extension of the graph towards the depletion region was achieved using a dynamic TDDS approach [Gra+13a].

to be widely distributed in a range of 0.6 eV to 1.39 eV for the emission and 0.4 eV to 0.99 eV for the capture events, respectively. This suggests that the thousands of defects in a micrometer sized device follow an arbitrary distribution of activation energies. This idea will be treated in detail in Section 5.3.

For the sake of completeness, Fig. 5.10 shows the dependence of the capture time constants of individual defects on the stress bias. A decrease of the capture time constants with increasing stress bias is observed, which does not follow a simple model derived from SRH [SR52; Hal52; Pot+07] theory [Gra+10a]. The emission time constants decrease with decreasing bias as shown in Fig. 5.11, even though there exist also defects whose emission time constants do not change with bias at all [Gra+13a].

To conclude, TDDS studies on individual defects have univocally shown that the mean capture or emission time constants of the defects constituting BTI follow an Arrhenius equation. Using this Arrhenius equation the construction of an abstract temperature-time is possible which accounts for arbitrary distributions of time constants.

5.2.2 Derivation of the temperature-time

To derive a transformation of the time constants of the defects activated during NBTS it is understood that the activation energy E_A does not change from one temperature T_1 to any other temperature T_2. It is remarked that this is only valid if entropy changes are neglected. By rearranging (5.3) for E_A one obtains

$$E_\mathrm{A} = k_\mathrm{B} T \ln\left(\frac{\tau}{\tau_0}\right) \tag{5.4}$$

and further from $E_\mathrm{A}(T_1) = E_\mathrm{A}(T_2)$,

$$\begin{aligned} \tau_2 &= \tau_0 \exp\left(\frac{E_\mathrm{A}(T_1)}{k_\mathrm{B} T_2}\right) \\ &= \tau_0 \exp\left(\frac{k_\mathrm{B} T_1 \ln\left(\tau_1/\tau_0\right)}{k_\mathrm{B} T_2}\right) \\ &= \tau_0 \left(\frac{\tau_1}{\tau_0}\right)^{T_1/T_2} . \end{aligned} \tag{5.5}$$

With this the change of the defect time constant τ_1 at temperature T_1 to another time constant τ_2 at a temperature T_2 can be calculated, provided τ_0 is known. To handle arbitrary time constant distributions of many defects the temperature-time ϑ can be defined as [Pob+11b]

$$\vartheta\left(T\right) = \tau_0 \left(\frac{t}{\tau_0}\right)^{T_\mathrm{meas}/T} , \tag{5.6}$$

which transforms BTI stress or recovery data measured at the temperature T_meas to any other reference temperature T. Providing the physical correctness of our assumption, this approach makes it possible to transform data from a fixed experimental window of about 10^{-6} s to 10^{6} s to an extended time frame. For example, measuring at colder temperatures than the reference temperature rescales the time axis toward smaller values. This allows decelerating fast transitions to measure them with reasonable measurement intervals on conventional equipment. On the other hand, if $T_\mathrm{meas} > T$, defects with time constants much larger than the experimental window may be analyzed in a short-time experiment [Pob+11b; PG13b].

All considerations that follow are based on the assumption that NBTI is the response of numerous defects which behave approximately as a first order process with the time constants given by (5.3). The applicability of this assumption has been demonstrated previously [HDP06; Hua10; Gra+11a; Pob+11b]. It is remarked that the assumption that (5.3) is valid does not imply an assumption on the microscopic nature of the defects constituting NBTI [PG13b].

It is further remarked that the presented approach allows for very precise determination of the lifetime of devices by accelerating the degradation with temperature. This is far more precise and accurate than the conventional stress voltage scaling approach [Pob+11b].

5.2.3 Application to recovery temperature dependence

The temperature-time approach is applied to the NBTI recovery data measured at different temperatures as shown in Fig. 5.12. In order to obtain this plot an average minimal emission time constant τ_0 for 0 eV activation energy is required to be determined by minimizing the vertical

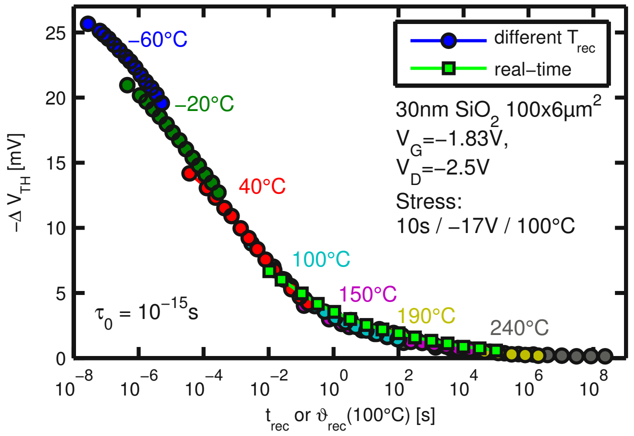

Fig. 5.12: NBTI recovery data from Fig. 5.6 at different T_rec interpreted with the temperature time and compared to a real-time measurement [PG13b]. The voltage and temperature sequence for the experiment is sketched in Fig. 5.5.

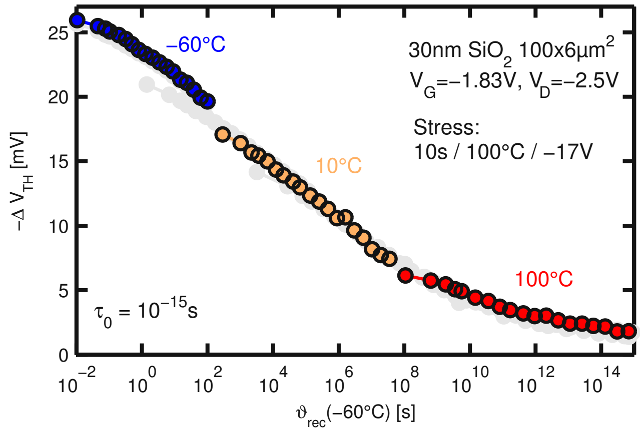

Fig. 5.13: Recovery data of Fig. 5.8 with T switches during recovery interpreted with the temperature-time (5.6) [PG13b]. Refer to Fig. 5.7 for the time and voltage chronological sequence. Data from Fig. 5.12 as gray background.

difference in the overlapping data. The τ_0 value obtained in this way is in the range of the inverse phonon frequency and around 10^{13} Hz [TPZ72; Ber+06; Aic10; Gar+12].

By using the temperature-time approach and finding an appropriate value for τ_0 one single universal recovery trace was observed. This recovery trace reproduces a two day long reference measurement at 100 °C chuck temperature, which proves the validity of the concept. It is remarked that the overlapping of the data could be improved by considering two independent distributions with different values for τ_0 as done previously [Gra+11a]. However, considering a single effective distribution with a single τ_0 appears to be sufficiently accurate for the present purposes [PG13b].

This result confirms that the temperature dependence of NBTI recovery can be understood by a simple collection of temperature activated first-order processes: At low temperatures the time constants become larger and thus a smaller number of defects are able to anneal. Consequently the number of remaining charges and thus the measured ΔV_TH is large. With increasing temperature the time constants become shorter and most charges are emitted during the recovery measurement. In the limiting case, when the recovery temperature even exceeds the stress temperature, nearly all the defects which had been created during stress anneal already before the first measurement point after a 10 ms real-time delay, resulting in a very small ΔV_TH [PG13b].

The universal recovery trace may also be obtained in a single measurement through temperature switches during recovery, as shown in Fig. 5.13. The effect of the time transformation (5.6) is to shift

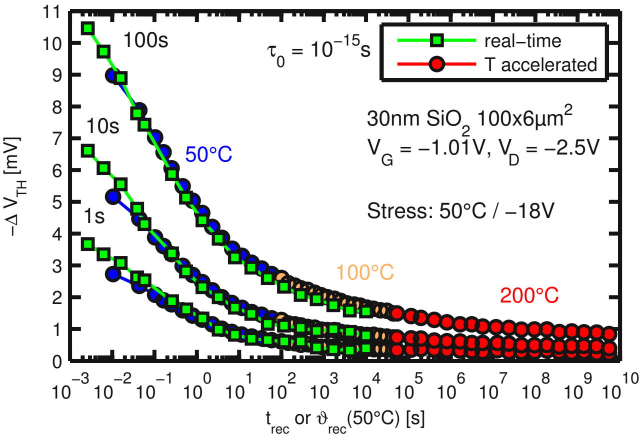

Fig. 5.14: Comparison between temperature accelerated recovery data and real-time data measured at 50 °C chuck temperature [PG13b].

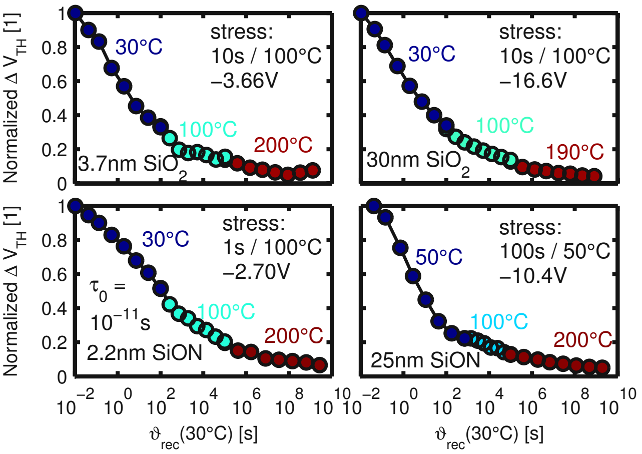

Fig. 5.15: Recovery after NBTS with switches to higher temperature for several technologies [PG13b]. The vertical axis is normalized for better illustration. $\tau_0 = 10^{-11}$ s is suitable for both SiO$_2$ and SiON oxides with different thicknesses.

the experimental data along the time axis to larger values with higher temperatures. This allows extending the recovery transients to otherwise impractically long times, as shown in Fig. 5.14.

It is remarked that further acceleration of the recovery with higher temperatures can lead to degradation even at $V_{\mathrm{G}} = V_{\mathrm{TH}}$, especially in devices with thin gate oxides, which can lead to the appearance of erroneous plateaus in the recovery transient [Gra+11c]. For this reason, recovery acceleration appears mostly beneficial for moderate stress conditions where the stress temperature is considerably lower than the maximum allowed recovery temperature.

An investigation of the quasi-permanent component by temperature acceleration of the recovery following moderate NBTS illustrated in Fig. 5.15 shows that the remaining level of degradation is rather small in devices with SiO$_2$ or silicon oxynitride (SiON) technology. Furthermore, the concept of temperature acceleration for recovery appears to work in a wide variety of technologies with similar values of τ_0. This justifies the use of temperature switches during recovery for the measurement of NBTI recovery data to acquire experimental data sets on long timescales [PG13b].

5.2.4 Application to stress temperature dependence

In Fig. 5.16 the result of the application of the temperature-time on the NBTI data measured at different T_{str} is shown. Provided τ_0 is chosen appropriately, all characteristics align to one single curve. The impact of the particular choice of τ_0 is illustrated in Fig. 5.17. The τ_0 value shifts data measured at a temperature different from the reference temperature horizontally along the ϑ_{str}

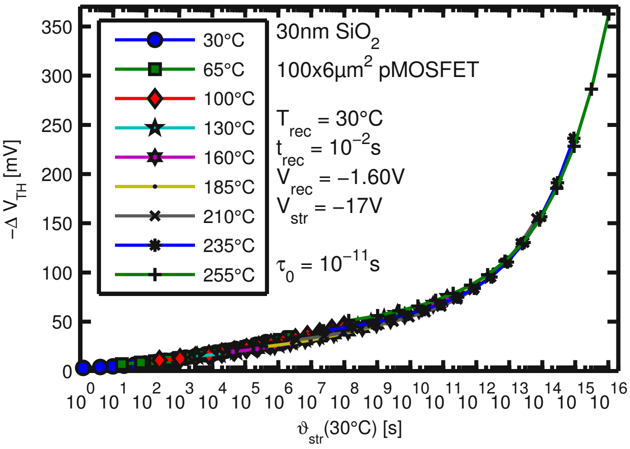

Fig. 5.16: The data of Fig. 5.4 interpreted with the temperature time (5.6). τ_0 was chosen arbitrarily such that the vertical overlap of all traces is minimized.

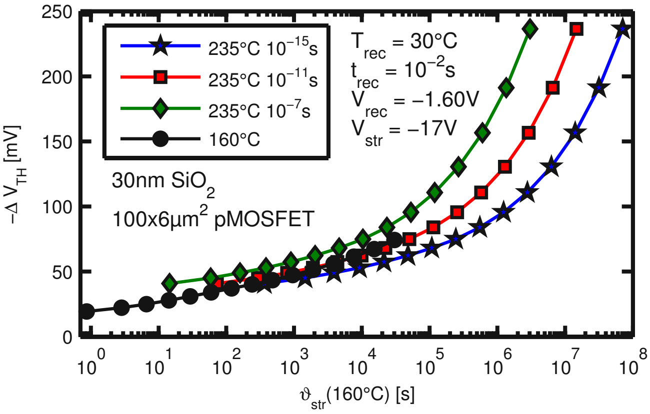

Fig. 5.17: Impact of the particular choice of τ_0 on the horizontal position of a characteristic measured at a T_{str} larger than the reference temperature.

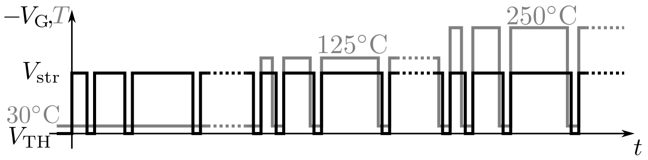

Fig. 5.18: Evolution of the device temperature and gate bias for the experimental data shown in Fig. 5.19.

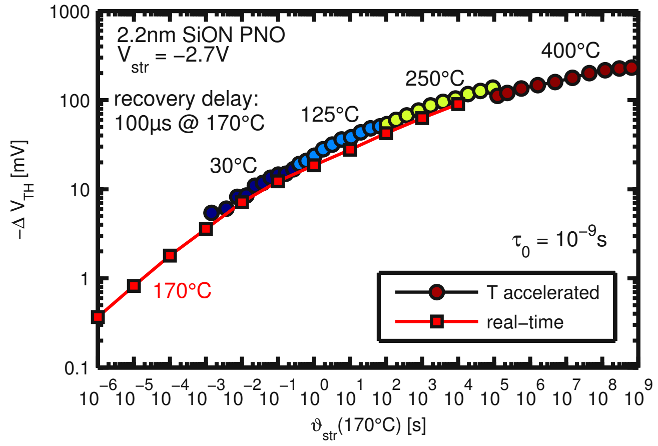

Fig. 5.19: Comparison between a long real-time MSM experiment and a T_{str} accelerated MSM experiment [PG13b]. The different recovery delay times at different T_{rec} are accounted for by using (5.6). Chronological sequence of T and V_{G} can be found in Fig. 5.18.

axis. Provided the assumptions for the derivation of the temperature-time are correct the data measured at 160 °C have to match the data measured at 235 °C after a certain amount of time. In the present thesis the exact value of τ_0 is determined by reducing the mean square of the sum of the vertical difference of two traces in the region of overlap.

The good matching of the data at different T_{str} suggests already that the analysis using (5.6) is a valid approach to interpret the acceleration of BTI stress with temperature. However, the approach opens also a way to acquire large experimental data sets in a minimum amount of measurement time. In order to prove this, a comparison of T accelerated MSM data to real-time data is shown in Fig. 5.19. This comparison requires to use (5.6) also for the recovery phase, in order to properly account for the different recovery delay times at different chuck temperatures. The according time and voltage sequences for the experiment are illustrated in Fig. 5.18. The real-time MSM experiment needs half a week and was performed on a different wafer of the same technology with a different measurement equipment [Gra+11a]. In contrast, the temperature accelerated MSM experiment needed approximately one hour. The real-time MSM experiment measured the degradation with a 100 µs delay, which decreases the ΔV_{TH} value due to recovery. These 100 µs at 170 °C correspond to approximately 20 ms at 30 °C for the temperature accelerated measurement. Exactly this delay time was used for the temperature accelerated measurement.

The T accelerated data is in agreement with the real-time data and exhibits the same gradual change in the power law exponent as the real-time data. The T acceleration appears therefore to be applicable to extend the experimental accessible time range to acquire long-term experimental stress data sets in a short amount of time [PG13b]. It is remarked that the approach works on all investigated technologies.

5.3 Interpretation as distributed activation energies

An alternative interpretation of the temperature dependence of BTI stress and recovery can be given by applying models for chemical reactions involving distributed activation energies. Such reactions occur frequently for natural materials as e.g. fossil fuels, coals or natural gases and are therefore important in the petrochemical industry. These application fields lead to a good theoretical background for such reactions [Pri55; BB87] which is utilized here on BTI data. In fact, considering that the creation of charges close to the Si-SiO_2 interface occurs mostly through the dissociation of atomic bonds [LD84; Fuj+03; Cam+06], a characterization from a chemical point of view seems very appropriate. In the following, the derivation of the equations needed to analyze the BTI data of Section 5.1 in this respect is presented. Naturally, this approach shows similarities to the temperature time approach of the previous section.

5.3.1 Derivation

A general assumption about the kinetics of processes which form a chemical transition is that they obey the differential equation [Pri55]

$$-\frac{\mathrm{d}g}{\mathrm{d}t} = kg^n \tag{5.7}$$

where g is the concentration of the reactant of the kinetic process, k the rate constant and n the order of the reaction. For the time being, it is assumed that the processes which occur during the degradation of MOSFETs follow a first-order model ($n = 1$) [Ste00; Gra+11a; PG13b], keeping in mind that an expansion to higher orders remains possible. Also, if the concentration of reactants g is not directly observable in the experiment, which is true within this thesis, the equations for a derived quantity as e.g. the ΔV_{TH} are equivalent to the equations for g [Pri55].

The rate constant k is considered to follow Arrhenius' equation leading to

$$-\frac{\mathrm{d}g}{\mathrm{d}t} = k_0 g \exp\left(-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right) \tag{5.8}$$

which can be integrated for isothermal experiments to

$$g = g_0 \exp\left(-k_0 t \mathrm{e}^{-\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}}\right). \tag{5.9}$$

g_0 is the value of g at $t = 0\,\mathrm{s}$ and k_0 the rate constant (also named frequency constant) with unit s^{-1}. The measurable quantity is the integral of the first order characteristic isothermal annealing function

$$\Theta_1 = \exp\left(-k_0 t \mathrm{e}^{-E_{\mathrm{A}}/k_{\mathrm{B}}T}\right) \tag{5.10}$$

over all possible energy values

$$G = \int_0^\infty g_0(E_{\mathrm{A}})\Theta_1(E_{\mathrm{A}}, t)\mathrm{d}E_{\mathrm{A}}. \tag{5.11}$$

The heart of this approach is the approximation of the characteristic isothermal annealing function (5.10) by a unit step function at $E_{\mathrm{A},0} = k_{\mathrm{B}}T\ln(k_0 t)$ as shown in Fig. 5.20. The width of the transition in Fig. 5.20 is $4 \times k_{\mathrm{B}}T$ or approximately 150 meV at 147 °C. That is to say, details in the activation energy spectrum smaller than a few $k_{\mathrm{B}}T$ are neglected. This will be verified later by suggesting particular activation energy spectra and comparing them to the results of simulated isothermal annealing data (cf. Fig. 5.21).

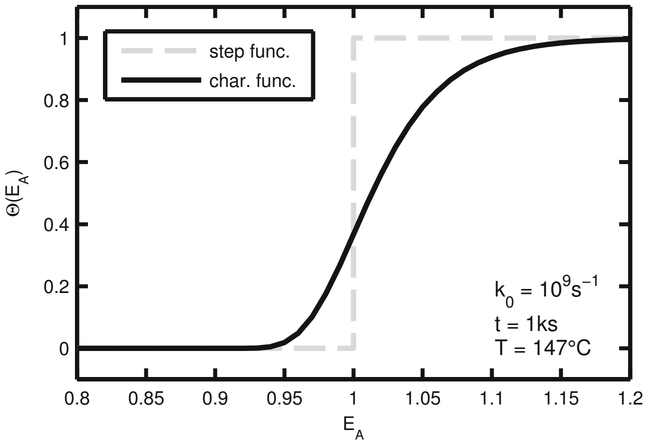

Fig. 5.20: Comparison of the isothermal annealing function (5.10) with a unit step function at the energy $E_{\mathrm{A},0} = k_\mathrm{B}T\ln(k_0 t)$.

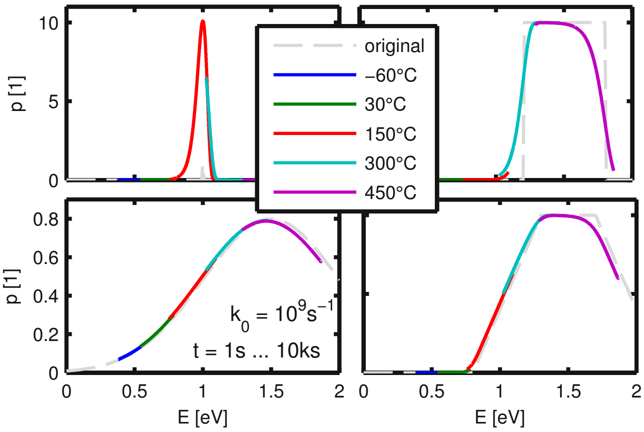

Fig. 5.21: Reproducibility of the approach after [Pri55] for different suggested activation energy distributions (from left to right and top to bottom: single Ea value, box distribution, normal distribution and trapezoidal distribution). The quantity k_0 is chosen arbitrarily.

Replacing the isothermal annealing function with a unit step function allows solving (5.11) conveniently as

$$G \cong \int_{E_{\mathrm{A},0}}^{\infty} g_0(E_\mathrm{A})\mathrm{d}E_\mathrm{A} \tag{5.12}$$

$$\frac{\mathrm{d}G}{\mathrm{d}t} \cong -g_0(E_{\mathrm{A},0})\frac{\mathrm{d}E_{\mathrm{A},0}}{\mathrm{d}t} \tag{5.13}$$

and, since $E_{\mathrm{A},0} = k_\mathrm{B}T\ln(k_0 t)$,

$$g_0\left(k_\mathrm{B}T\ln(k_0 t)\right) \cong -\frac{t}{k_\mathrm{B}T}\frac{\mathrm{d}G}{\mathrm{d}t}. \tag{5.14}$$

To verify this, Fig. 5.21 compares some selected activation energy distributions with the result of isothermal experiments analyzed with the Primak approach [Pri55]. Indeed, the approach does not resolve abrupt changes in the distribution of the activation energies accurately but catches the general aspects of the distributions. The method is only a valid approach to analyze a distribution of activation energies if the distribution is sufficiently broad.

However, a disadvantage of this approach is that the rate constant k_0 is undefined and must be chosen appropriately. The only way to determine k_0 is by comparing isothermal experiments at different temperatures [Pri55]. The traces in the energy spectrum need to overlap for correct rate constant values. This can be used to determine the unknown rate constant from isothermal

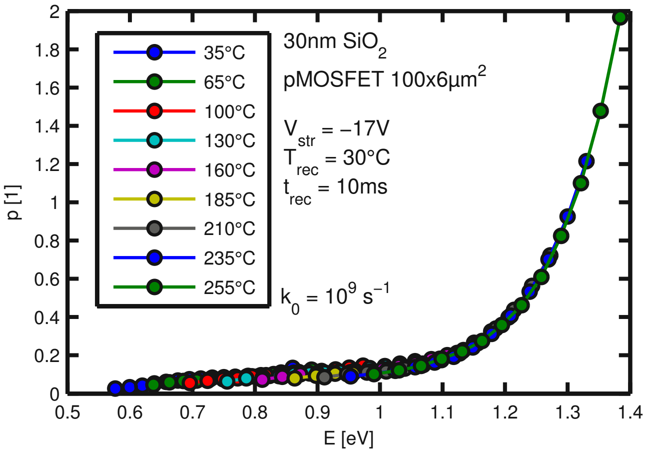

Fig. 5.22: Analysis of the $\Delta V_{\mathrm{TH}}\,(t_{\mathrm{str}})$ data from Fig. 5.4 measured at $T_{\mathrm{str}} \neq T_{\mathrm{rec}}$ with the Primak approach. k_0 is chosen such that the high temperature traces tend to overlap each other.

experiments. Also the opposite is true: if different rate constants for different processes are existent isochronal experiments at different temperatures exhibit different energy distributions. In other words, the effect of the frequency factor is to shift the energy distribution along the activation energy axis in an isothermal experiment [Pri55].

In solid state reactions the frequency factor can be dependent on the temperature as $k_0 \propto T^m$ with $m = -1.5 \ldots 2.5$ [CL08]. This means that in a T range far away from the absolute zero temperature point, k_0 either increases or decreases with temperature according to the power law coefficient. This does not include a distribution of k_0 [BB87] as it is expected for BTI defects from TDDS studies where the individual defects show very different minimum time constants [Gra+10a].

5.3.2 Application to BTI data

The Primak approach is well applicable to NBTI data as shown in Fig. 5.22, when only T_{str} is varied and T_{rec} and t_{rec} are always kept at the same value. The rate constant k_0 is chosen to be $10^9\,\mathrm{s}^{-1}$ such that a good overlap is given in the high energy region of the plot. However, for an improved matching in the low energy region below about 1 eV a lower rate constant of about $10^6\,\mathrm{s}^{-1}$ leads to better results (not shown). This indicates already that, despite the fact that an average value may also capture the behavior approximately, the reactions occurring during NBTS do experience different frequency constants.

Considering only the high energy tail of the activation energy distribution by measuring at the maximum achievable $T_{\mathrm{str}} = 430\,°\mathrm{C}$, while keeping T_{rec} at $30\,°\mathrm{C}$, the maximum of the spectrum can be unambiguously measured. See Fig. 5.23 for the $\Delta V_{\mathrm{TH}}(t_{\mathrm{str}})$ data and Fig. 5.24 for the energy spectrum. The characteristics in Fig. 5.23 and Fig. 5.24 are measured at different readout voltages (-2.0 V and -6.5 V) to account for the large shift of the V_{TH} of up to 4.5 V. This is necessary because at -2.0 V readout bias the shift is as large that the drain current becomes too small to be measurable. Increasing the readout bias to -6.5 V allows measuring also such large drifts and does not considerably change the parameters of the distribution, see the two characteristics at -9 V stress bias. The exact impact of the recovery bias is shown in Fig. 5.25 by comparing a virgin versus a stressed transfer characteristics. The shift is fairly horizontal but includes a decrease of the sub-threshold slope which is usually attributed to an increase of the interface trap density [Sch06; ANG09b]. That is to say, the ΔV_{TH} value might be altered by more or less interface traps but still reflects the relative number of NBTS created charges, as can also be seen in the

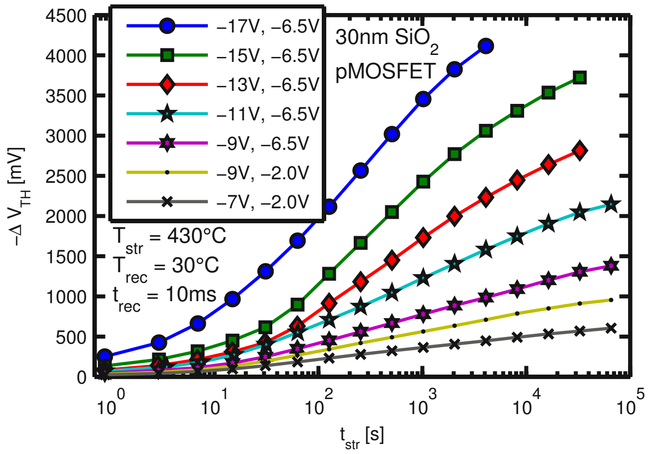

Fig. 5.23: Stress voltage dependence of intensive NBTS. For lower stress voltages (first values in the legend) the readout or recovery bias was reduced (second values in the legend).

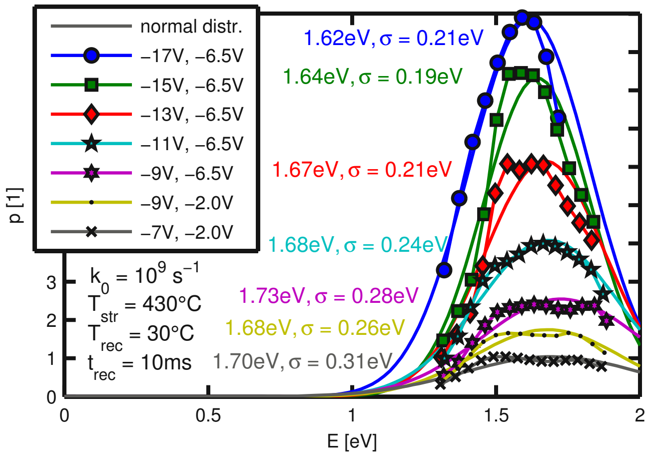

Fig. 5.24: Stress voltage (first values in the legend) dependence of the energy spectrum of 30 nm SiO_2 pMOSFET NBTI analyzed with the Primak approach. For low stress voltages the readout or recovery bias V_{rec} (second values in the legend) was reduced.

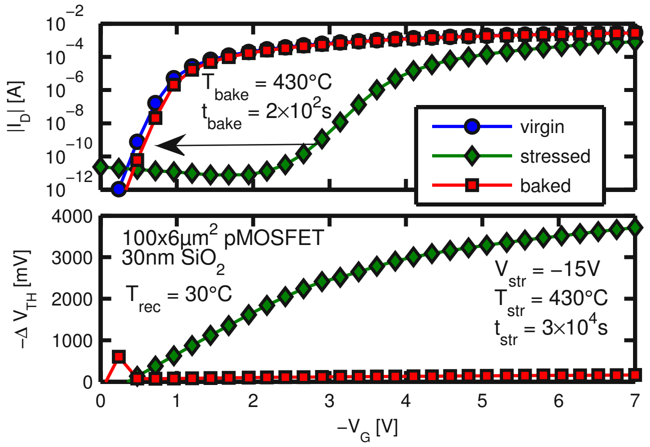

Fig. 5.25: Change of the transfer characteristic with intensive NBTS and a subsequent bake with zero gate and drain bias (upper plot). The lower plot shows the dependence of ΔV_{TH} on the gate bias.

$V_{\mathrm{str}} = -9\,\mathrm{V}$ characteristics with different recovery biases in Fig. 5.23. Also, the $-6.5\,\mathrm{V}$ recovery bias occurs only at the much lower recovery temperature which prevents any further degradation. Furthermore, also the impact of a zero gate and drain bias bake phase on the stressed device is shown in Fig. 5.25. The bake phase allows to return very close to the virgin state of the device [Kat08; BOG08].

The activation energy maximum is visible in the $\Delta V_{\mathrm{TH}}(t_{\mathrm{str}})$ data as a slight saturation. The activation energy spectrum is in principle the derivative of the $\Delta V_{\mathrm{TH}}(t_{\mathrm{str}})$ data. The point of inflection in the $\Delta V_{\mathrm{TH}}(t_{\mathrm{str}})$ plot marks the maximum in the activation energy spectrum. Having a sufficient amount of data points near the maximum it is a rather facile task to fit a distribution of activation energies to the spectrum. The energy spectra resemble normal distributions. This is consistent with results from ESR measurements which propose the dissociation energy of, e.g. Si–H, to be normally distributed due to the amorphous structure of the $\mathrm{SiO_2}$ [Ste00]. The particular values of the mean activation energies could be erroneous since they depend largely on the frequency constant k_0, which in turn can only be approximately evaluated by matching the vertical overlap of the data of the energy spectra plots. The dependence of the parameters on the stress bias is given in Fig. 5.33 in Section 5.5.

A particularity of the presented approach is that it is important to provide BTI data where only the T_{str} temperature is varied and the recovery is kept always at the same level. This is because the product of chemical reactions is usually directly observable during the experiment. This would match most closely to on-the-fly (OTF) measurements for BTI research [Den+04a]. However, OTF measurements are seriously affected by errors due to the change of the mobility [Gra+08]. Furthermore, a transfer characteristic of the virgin device at the stress temperature is needed for the OTF approach. But at temperatures as high as 430 °C the measurement of the transfer characteristic itself degrades the device already considerably. Therefore, it would not be possible to obtain non-erroneous data from OTF experiments at high temperatures and therefore MSM data is favored.

5.4 Other interpretations

In this Section a few other approaches to understand the temperature activation of BTI stress and recovery are given.

5.4.1 Direct interpretation

The common approach is to draw BTI data measured at $T_{\mathrm{rec}} = T_{\mathrm{str}}$ in an Arrhenius plot as ΔV_{TH} over $1/(k_{\mathrm{B}}T)$ and to extract the activation energy by fitting a linear function to the data. This assumes an Arrhenius equation for as

$$-\Delta V_{\mathrm{TH}} = -\Delta V_{\mathrm{TH},0} \exp\left(\frac{E_{\mathrm{A}}}{k_{\mathrm{B}}T}\right), \tag{5.15}$$

which actually predicts a negative activation energy value for increasing degradation with increasing temperature.

Such an interpretation leads to absolute activation energy values in the range of $0.019\,\mathrm{eV}$ to $0.58\,\mathrm{eV}$ [JS77; OS95; MKA04; AWL05]. It is remarked that all these values are obtained through measurements where $T_{\mathrm{str}} = T_{\mathrm{rec}}$, a limitation which has been already shown in the previous Sections

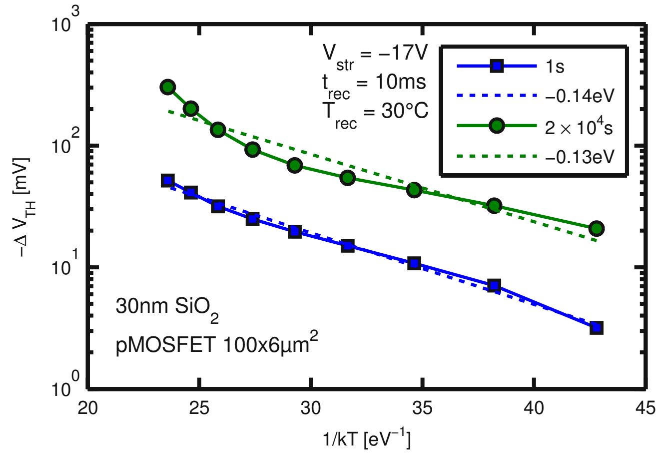

Fig. 5.26: Standard approach for the determination of the activation energy extracted from Fig. 5.4 at stress times 1 s and 2×10^4 s between 35 °C and 255 °C. T_{rec} is constant and only T_{str} is varied.

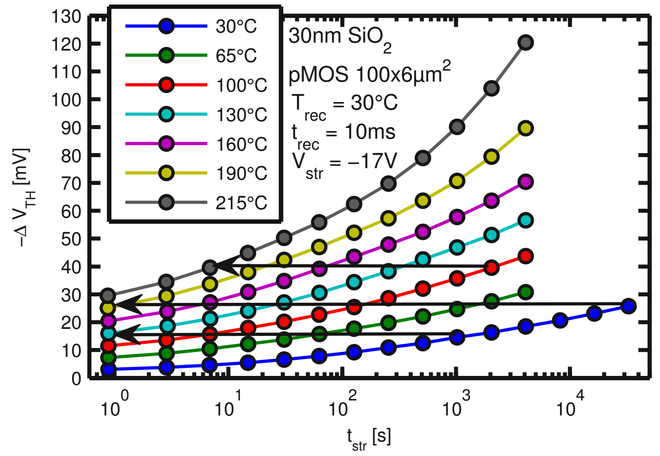

Fig. 5.27: Threshold voltage drift in an MSM experiment with constant T_{rec}. The three arrows show the decrease of the time constants for certain levels of ΔV_{TH}.

to cause questionable results. However, even for analyses of $T_{\mathrm{str}} \neq T_{\mathrm{rec}}$ data as e.g. from Fig. 5.4, E_{A} values within a 0.13 eV and 0.14 eV range are obtained as shown in Fig. 5.26. The in this way extracted activation energies are rather low and thus in stark contrast to chemical activation energies for the dissociation of atomic bonds in the Si-SiO$_2$ system of about 1.5 eV to 2.91 eV [Ste00].

5.4.2 Ensemble of time constants

Motivated by the temperature activation of individual defects as described in Section 5.2.1, the $T_{\mathrm{str}} \neq T_{\mathrm{rec}}$ data could also be interpreted in the following way (cf. also Fig. 5.27): On a micrometer-sized device the individual charging or discharging event of a single defect is not resolvable since the step size is too small and there are simply too many defects to distinguish. Still, a group of defects with short capture time constants will shift the V_{TH}, e.g. up to 16 mV, before a second group of defects with slightly larger capture time constants will shift the V_{TH} another 10 mV to a total drift of 26 mV. When the experiment is repeated at a higher T_{str} the first group of defects will, provided the two groups have a similar activation energy, still be charged before the second group. Also, the ΔV_{TH} of the first group will not change. Consequently, by searching for the occurrence of $\Delta V_{\mathrm{TH}} = 16$ mV in the $\Delta V_{\mathrm{TH}}(t_{\mathrm{str}})$ data at both stress temperatures it is possible to extract the change of the time values of the group of defects with temperature. Fig. 5.28 shows the

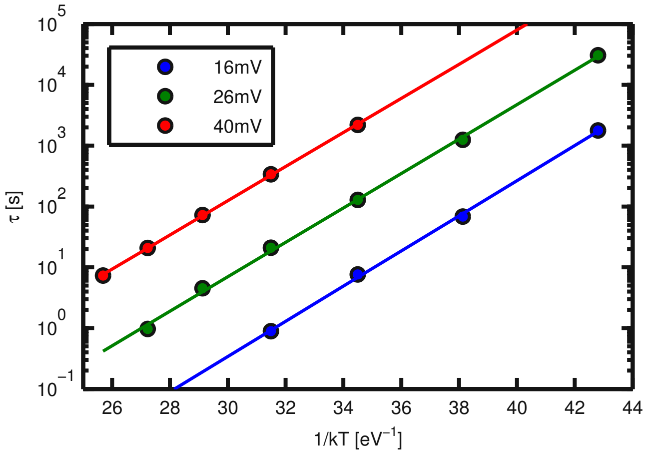

Fig. 5.28: Change of the time constants of Fig. 5.27 for three example values of ΔV_{TH} in an Arrhenius plot. A good correlation to the Arrhenius equation is evident.

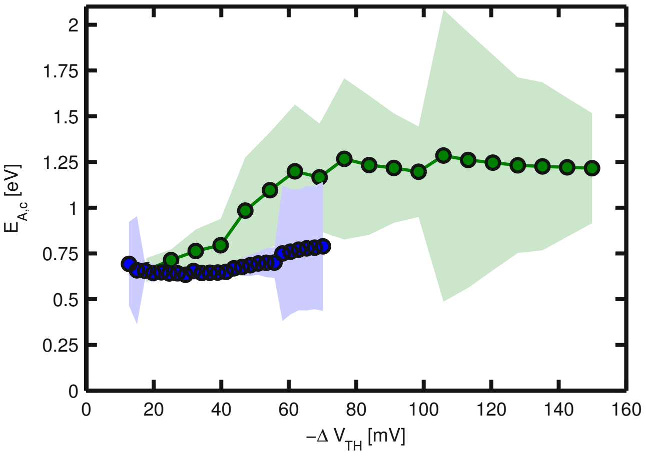

Fig. 5.29: Extracted activation energy E_{A} for numerous different ΔV_{TH} values of the MSM experiments of Fig. 5.27 (blue) and Fig. 5.4 (green). The shaded areas indicate the borders of a 95 % confidence interval of each fit.

dependence of the stress time needed for 16 mV, 26 mV and 40 mV of drift over stress temperature. The decrease of the time constants for the three groups indeed follows an Arrhenius equation as suggested from individual defects experiments.

This idea can now be applied with a finer grid on the ΔV_{TH} axis and the activation energy E_{A} as well as the minimum time constant τ_0 can be extracted for every group. Fig. 5.29 shows the results of such an interpretation for two example experiments for the activation energy E_{A} and Fig. 5.30 for the minimum time constant τ_0, respectively. The E_{A} and the τ_0 values are comparable to the values of individual defects as described in Section 5.2.1: E_{A} from 0.4 eV to 0.99 eV, τ_0 from 10^{-12} s to 10^{-7} s. Considering the less intense experiment (blue characteristic in Fig. 5.29 or 5.30) the E_{A} and τ_0 values are rather well-defined and the error becomes larger only at the border regions of low or high ΔV_{TH} where only a few data points are available. In contrast, for the higher temperature experiment (green characteristic in Fig. 5.29 or 5.30) the confidence interval of the fit is always rather large. This is because in the Arrhenius plot the wide range data shows a certain degree of curvature which can only be approximated by a linear fit. This is another suggestion that the processes occurring during NBTS do not show a single valued activation energy but rather a distribution of activation energies. If several values of E_{A} are evident the in this Subsection presented concept does not apply any more because the occurrence of a group of defects can invisibly exchange with another group, making it impossible to identify an individual group of defects solely by the ΔV_{TH} value.

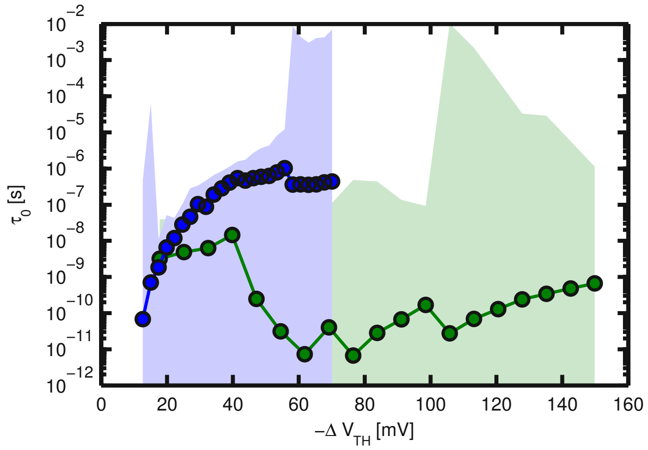

Fig. 5.30: Extracted τ_0 values for a large number of different ΔV_{TH} values from the data of Fig. 5.27 (blue) and Fig. 5.4 (green). The thin lines are the borders of 95 % confidence intervals.

However, the approach shows that approximately the same activation energy and minimal time constant values can be obtained on micrometer sized devices and not only on nanometer sized devices [Gra+10a].

5.5 Comparison of the interpretation methods

The above described interpretation approaches for the temperature activation of NBTI stress and recovery appear to be comparable. Through a more close analysis of the result of the temperature-time approach an important similarity becomes apparent: E.g. the NBTI recovery data in Fig. 5.12 analyzed with the temperature-time of Section 5.2 shows one single recovery trace which seems to follow a cumulative normal distribution function. Indeed, assuming that the emission time constants of the defects activated during NBTS are log-normally distributed, it follows that recovery has to obey [Gra+11a]

$$\Delta V_{\mathrm{TH}}{}^{\mathrm{rec}} = \frac{\Delta V_{\mathrm{TH}}^{\max}}{2} \operatorname{erfc}\left(\frac{k_{\mathrm{B}}T\ln\left(\frac{\vartheta_{\mathrm{rec}}}{\tau_0}\right) - \mu}{\sqrt{2}\sigma}\right), \tag{5.16}$$

where $\Delta V_{\mathrm{TH}}^{\max}$ is the maximum drift after the given stress, μ, σ are the parameters of the normal distribution of the energy barriers and erfc is the complementary error function [PG13b]. In Fig. 5.31 a comparison of this model with the T accelerated recovery data is given. The mean and the variance of the distribution are given in eV. The Arrhenius equation for the time constants (5.3) allows transforming the mean of 0.71 eV at 100 °C with the experimentally determined τ_0 value of 10^{-15} s to a mean emission time constant value of 10^{-5} s. This means a stress with 10 s duration charges defects with a mean emission time constant of 10^{-5} s and most experiments with the first measurement point around 10 ms after termination of stress do not capture the mean but only the long time constant part of the distribution. This is due to the large variance of the emission time constant distribution. The approach assumes that the distribution of the emission time constants is due to a distribution of emission activation energies, an assumption which cannot be unequivocally verified at the time.

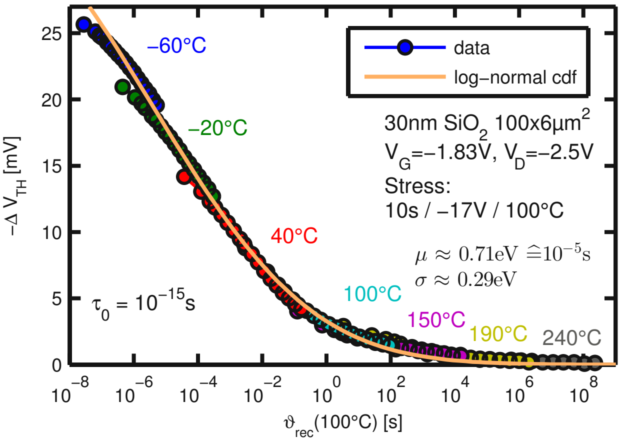

Fig. 5.31: Cumulative normal distribution function (5.16) fitted to the T accelerated NBTI recovery data of Fig. 5.12 [PG13b].

Similarly, also for the stress time dependence of NBTI a cumulative log-normal distribution function as

$$\Delta V_{\mathrm{TH}}{}^{\mathrm{str}} = \frac{\Delta V_{\mathrm{TH}}^{\max}}{2}\,\mathrm{erfc}\left(-\frac{k_{\mathrm{B}}T\ln\left(\frac{\vartheta_{\mathrm{str}}}{\tau_0}\right)-\mu}{\sqrt{2}\sigma}\right), \tag{5.17}$$

where $\Delta V_{\mathrm{TH}}^{\max}$ is the maximum drift capability of the device for a given stress oxide field, is evident. Fig. 5.32 compares a large data set with a wide range of time and temperature values with the prediction of the reaction–diffusion (RD) theory [AM05; Mah+11] and the assumption of log-normally distributed time constants. Fig. 5.32 b) is the semi-logarithmic plot of the degradation versus the stress time. The derivative of this function gives the probability density function of the distribution in Fig. 5.32 a). A good match between the data and the log-normal distribution is evident. Fig. 5.32 c) is the data plotted on log-log scale which shows a power law for short stress times. For larger stress times the data clearly deviates from this power law. A slow but continuous decrease of the power law coefficient is observed as shown in Fig. 5.32 d). It is mandatory for the degradation to saturate from a microscopic perspective, since eventually all possible defect sites have become charged at a certain time. But the details on *how* the degradation saturates is a very interesting observation which has been mentioned only rarely [HDP06; RMY03]. This is primarily due to the logarithmic nature of NBTI degradation and the consequential extreme need of measurement time. Consequently, the approach enables a convenient study of the long-term behavior of BTI. Bear in mind that the Arrhenius temperature activation of the time constants (5.3) together with the experimentally obtained τ_0 value of 10^{-9} s allows transforming the ϑ axis to an activation energy axis as shown in Fig. 5.32 a). Also, a mean capture time constant value of 10^{12} s at 30 °C can be calculated from the mean value of the distribution. This large value indicates that most of the defects of the MOSFET, which can be activated for a given stress gate voltage, have a capture time constant which is much larger than the intended lifetime of the device of ten years or $\approx 3 \times 10^8$ s. Consequently, during the lifetime of the product under use conditions only the tail of the distribution of all defects becomes charged.

To conclude, the temperature-time approach described in Section 5.2 is able to handle arbitrary distributions of time constants. By applying this approach to NBTS data measured at high temperatures and long time ranges it is observed that the emission and capture time constants for NBTI defects are log-normally distributed. A possible reason for the log-normal distribution of the time constants could be a normal distribution of activation energies due to the Arrhenius temper-

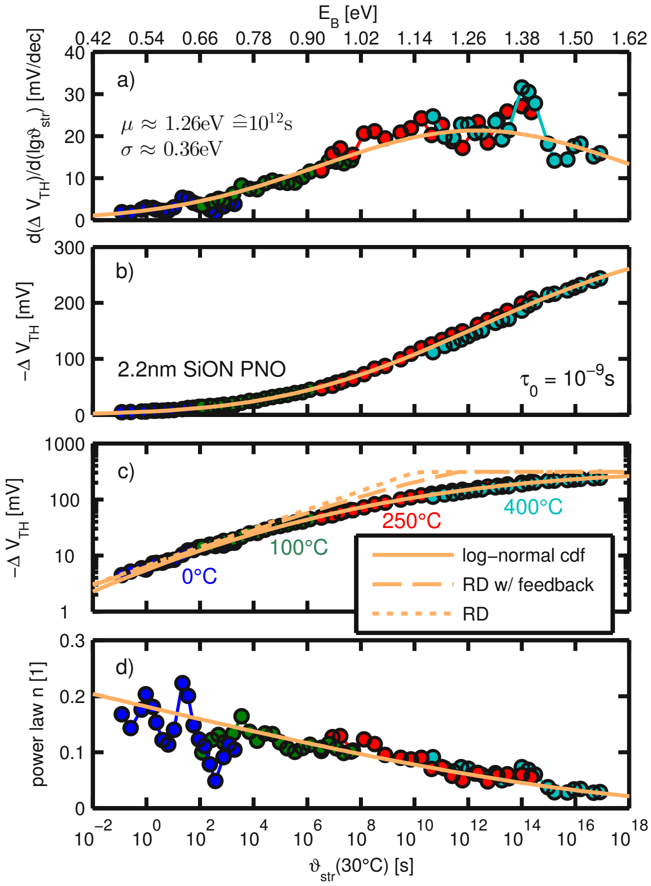

Fig. 5.32: Comparison of T accelerated NBTS data with the assumption of log-normally distributed capture time constants and the RD model [PG13b]. From top to bottom are plotted: *a)* The derivative of $\Delta V_{\mathrm{TH}}(\lg t_{\mathrm{str}})$ giving the probability density function, *b)* the semi-logarithmic $\Delta V_{\mathrm{TH}}(\lg t_{\mathrm{str}})$ showing the cumulative distribution function (5.17), *c)* the log-log diagram common for NBTI research and *d)* its derivative giving the change of the power law coefficient with stress duration.

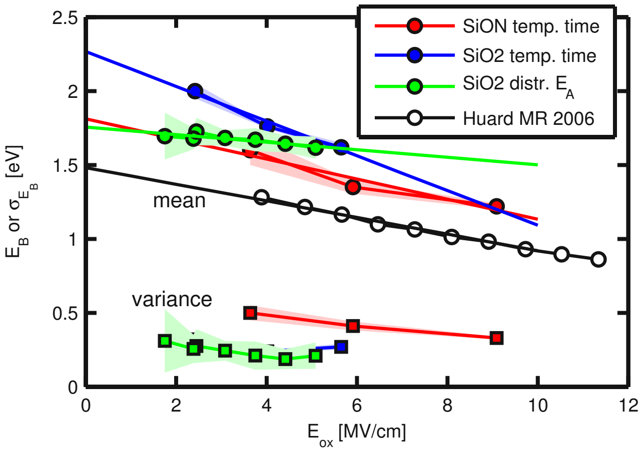

Fig. 5.33: Stress electric oxide field dependence of the activation energy for MOSFETs with 30 nm SiO_2 or 2.2 nm SiON gate dielectrics. The extraction using the temperature time approach is compared with measuring the E_A distribution directly.

ature activation of the defect time constants (5.3). In accordance, the temperature-time approach and the distributed activation energies approach give equivalent results. This is not surprising since both methods rely on the similar, though important, assumption of constant scaling factors for all temperatures; τ_0 for the temperature-time approach and k_0 for the distributed activation energy approach.

Fig. 5.33 shows a comparison of the activation energy values obtained by the temperature-time and the distributed activation energy methods over the stress oxide field. The colored areas around the data points indicate the confidence interval of the fit of the distribution but miss the impact of τ_0 or k_0 on the mean and variance values. All technologies available in this thesis are considered, including Si based MOSFETs with either 30 nm SiO_2 or 2.2 nm SiON gate dielectrics. Also a comparison to previously published data [HDP06] is included. Both methods and all technologies give comparable mean activation energy values. However, there are still differences between the methods. Especially for the SiO_2 data no difference is expected because the measurements are performed on the same technology. Naturally, a better agreement between the two methods can be achieved when the same data sets are used. However, the in Fig. 5.33 observed deviations may arise from the following origins:

- The two MSM experiments were recorded at different chuck temperatures. The distributed E_A measurement was recorded at 30 °C while the temperature time measurement was recorded at 180 °C. Both measurements had the same time delay of 10 ms and are differently affected by recovery. Provided the emission and capture activation energies are correlated [Gra+11a], the particular amount of recovery could affect the extracted mean capture activation energies.

- The two data sets are measured on two different devices, which always includes small device variations, as well as on two slightly differently processed wafers. The impact of processing variants on the mean activation energy could unfortunately not be analyzed in this thesis.

- The temperature-time data lacks the point of inflection in the $\Delta V_{TH}(\lg t_{str})$ plot which indicates the mean of the time constants distribution. Consequently, the mean value of the distribution is not fully fixed and also largely dependent on measurement errors of the last t_{str} values.

- Both methods rely on the experimentally determined constants τ_0 and k_0 which are mean values representing distributed variables. The particular choice of τ_0 or k_0 has a certain impact on the extracted E_A value which could affect the conclusions. However, for the distributed E_A approach different values of k_0 mainly shift the $E_\mathrm{A}(\mathcal{E}_\mathrm{ox})$ dependence upwards or downwards, respectively. Considering Fig. 5.33, this would not allow to fully match the two methods.

Despite the uncertainty regarding the exact activation energy values, the approaches presented in this Section show that NBTI is *not* an intrinsic low energy effect as occasionally stated [MKA04; AM05; AWL05]. On the contrary, NBTS only activates the low energy *fraction* of a wide distribution of activation energies [Tya+09]. The obtained E_A values do not exactly point to dissociation energies of certain defect precursors in the Si-SiO$_2$ system which would identify the defect precursors responsible for NBTI. But the values are all within the expected range of 1.5 eV to 2.8 eV [Bro90; Sta95a; Ste00], which is consistent with other recent results [Yon13].

6

SiC-SiO$_2$ interface characterization

In the following Chapter peculiarities regarding the characterization and degradation of SiC based MOSFETs are discussed. Peculiarities concerning the degradation of SiC-MOSFETs will be treated in Chapter 7. A few of the main differences between SiC and Si based MOSFETs are the occurrence of a virgin threshold voltage instability for SiC based MOSFETs [Gur+08] and the larger virgin trap density of SiC at the interface to the native oxide SiO$_2$ [Afa+97; Cio05]. It is remarked that all subsequently presented measurements were performed on the four layer hexagonal SiC (4H-SiC) polytype.

The later in detail explained virgin threshold voltage shift is shown to be due to oxide traps and modeled using the analytical capture-emission time (CET) map model after [Gra+11a]. The model is shown to accurately predict the instability for a temperature range between room temperature and 200 °C, for positive gate voltages and in a time range from milliseconds to several days. The contents of that Section are also summarized in [PG13a].

The interface trap density of SiC based MOSFETs is determined by transferring the CP technique known from Si to SiC. Contrary to existing work regarding CP on SiC-MOSFETs [KTL96; SM98], it is shown that this characterization method can be used consistently and reliably on SiC, just as known from Si-MOSFETs.

6.1 Virgin threshold voltage instabilities

A simple turn-on of an SiC-MOSFET by simultaneously switching the gate and drain voltages to e.g. 15 V and 0.1 V, respectively, results in a continuous decrease of the drain current of the transistor. After this constant bias measurement an $I_\mathrm{D}V_\mathrm{G}$ characteristic can be recorded which allows transforming the drain current change to a shift of the threshold voltage of the device [Kac+08] as shown in Fig. 6.1. Plotting this data on a logarithmic time axis reveals that the

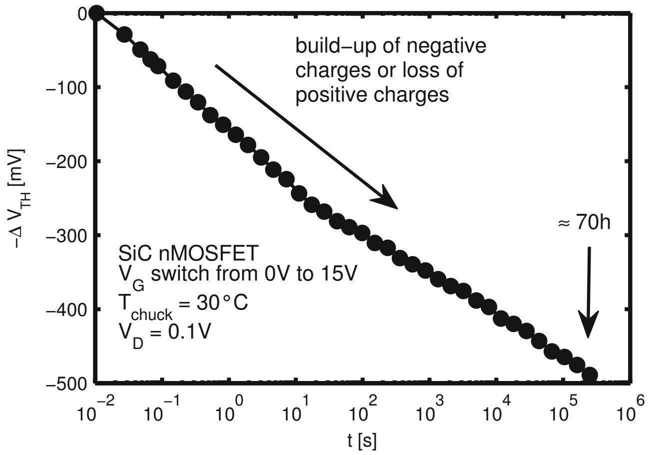

Fig. 6.1: Virgin drain current instability at a fixed operating point $V_G = 15\,\text{V}$, $V_D = 0.1\,\text{V}$ converted in an equivalent ΔV_{TH} using a subsequently recorded $I_D V_G$ [PG13a]. The measurement data is shifted along the y-axis such that the first measurement point is at 0 V.

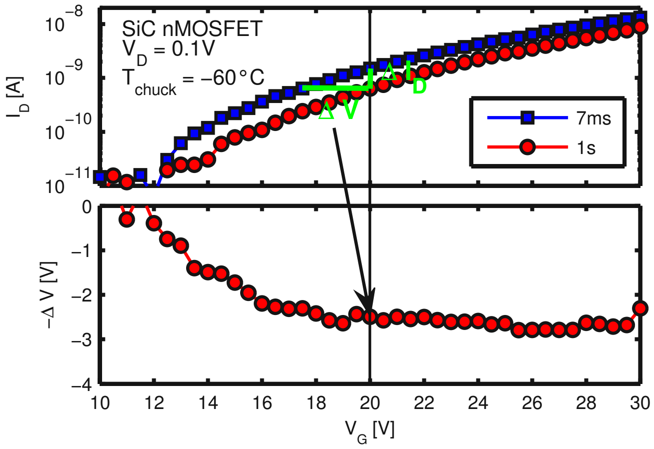

Fig. 6.2: Virgin transfer characteristic of 100 µm × 2 µm large SiC nMOSFET recorded with either 7 ms or 1 s delay between the bias switch and the current measurement (upper plot) and the according horizontal shift (lower plot).

instability of the drain current does not saturate even after three days of constant biasing. The total change of the threshold voltage may be as large as 500 mV, which is small in comparison to the threshold voltage of about 15 V but still significant and undesirable for application purposes. If charging of the SiC-SiO_2 interface or the oxide is the root cause of the instability then the decrease of the drain current can be due to either the creation of negative charges or the loss of positive charges. A reference which allows the identification of the charge polarity cannot be obtained since its measurement already changes the charge state of the MOSFET. Consequently, the first obtained measurement point must be defined as 0 V drift, even though the shape of the charging characteristic suggests that the device drifted already in the 10 ms before the first measurement point.

The instability is also visible in the $I_D V_G$ curve of a virgin device by a comparison of two characteristics with different delays for each measurement point as shown in Fig. 6.2. The characteristic with longer measurement delay is shifted towards positive infinity with respect to the faster characteristic. This shows that already the measurement of a virgin $I_D V_G$ is affected by the measurement timing. That is to say, SiC-MOSFETs do not exhibit a unique virgin transfer characteristic. This makes the characterization of SiC-MOSFETs more challenging.

The instability of the threshold voltage of SiC-MOSFETs is conventionally attributed to trapping of channel electrons (for nMOSFETs) into interface and/or oxide traps [Gur+08]. The effect was previously modeled using standard SRH theory [SR52; Hal52; Pot+07]. Negative charge build-

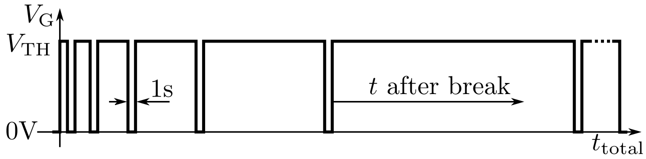

Fig. 6.3: Sequence of V_{G} for the subsequent experiments. The time at the V_{TH} is multiplied by 10 after every break.

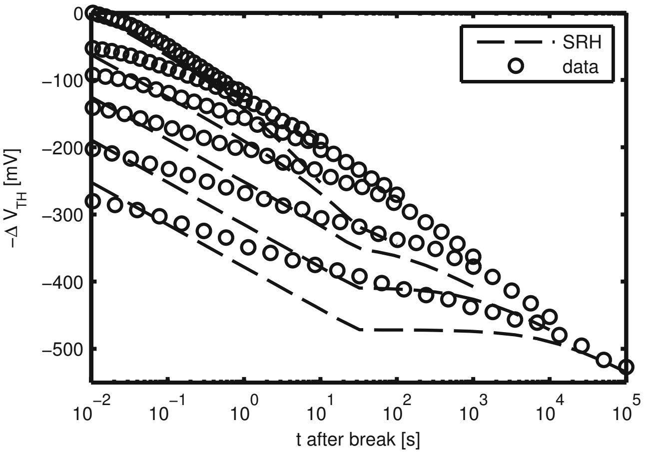

Fig. 6.4: Interrupted charging of an SiC nMOSFET with break time 1 s at room temperature and a comparison to the extended SRH model for oxide traps equation (6.3) and (6.4) [PG13a].

up can only be due to either electron capture or hole emission. Within SRH theory, the former is independent of the position of the Fermi level because the emission time constants are described as

$$\tau_{\mathrm{ep}} \propto \exp\left(\frac{E_{\mathrm{T}} - E_{\mathrm{V}}}{k_{\mathrm{B}}T}\right) \tag{6.1}$$

with E_{T} the trap level energy. That is to say, hole emission is not affected by a gate bias switch. In turn, electron capture time constants are modeled as

$$\tau_{\mathrm{cn}} = \frac{1}{v_{\mathrm{th},n}\sigma_n n_{\mathrm{i}}} \exp\left(\frac{E_{\mathrm{C}} - E_{\mathrm{F}}}{k_{\mathrm{B}}T}\right), \tag{6.2}$$

which means that a bias switch changes the capture times for electrons quasi-instantaneously. However, even if the Fermi level is pinned to the conduction band edge, which results in the smallest τ_{cn} values, one obtains 10^{17} s to 10^{22} s for typical values of $v_{\mathrm{th},n}$, σ_n and n_{i}. See Section 6.2 for a discussion on these material parameters. Accordingly, a distribution of electron capture time constants from 10^{-2} s to 10^{5} s as shown in Fig. 6.1 cannot be explained with standard SRH theory.

Also, an adapted SRH model for oxide charges was tested which accounts for the depth x of the charge within the oxide by an exponential term as [Gra12, eq. (76)]

$$\tau_{\mathrm{c}} = \frac{\mathrm{e}^{x/x_0}}{n v_{\mathrm{th}} \sigma_0} \tag{6.3}$$

for capture events and

$$\tau_{\mathrm{e}} = \frac{\mathrm{e}^{x/x_0}}{N_{\mathrm{C}} v_{\mathrm{th}} \sigma_0} \tag{6.4}$$

for emission events. Fig. 6.4 shows the resulting fit of this model to an interrupted MSM experiment. Consider Fig. 6.3 for the gate voltage sequence. The model fails to explain the behavior of the SiC-nMOSFET because of the strong coupling of the capture and emission time constants resulting from the depth of the charge. Consequently, SRH-like models cannot describe the charg-

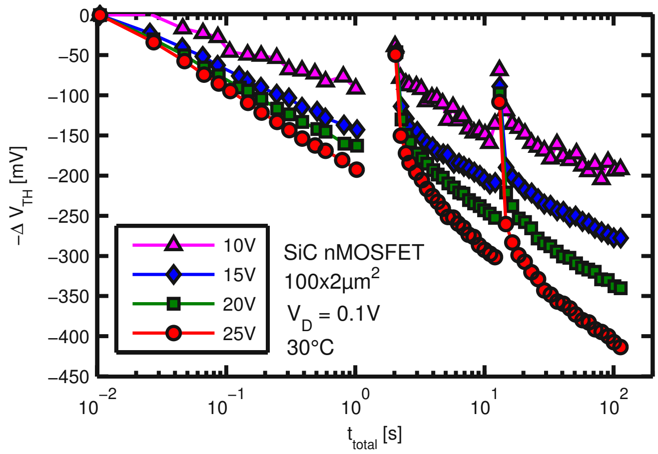

Fig. 6.5: Impact of the gate bias for the charging of a virgin device. The charging was interrupted at 1 s and 10 s after the beginning of the constant bias phase for a duration of 1 s. The $I_D V_G$ is always recorded after the measurement of the drain current instability.

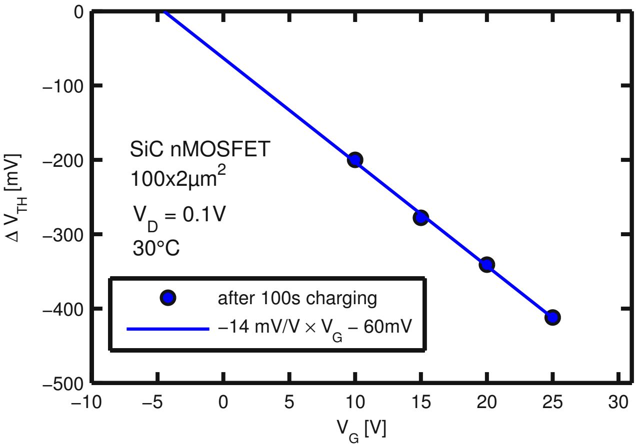

Fig. 6.6: Dependence of the virgin threshold voltage drift on the gate bias. The result of a linear fit is given in the legend.

ing behavior of SiC-MOSFETs. This indicates that it is unlikely that the charges which cause the virgin threshold voltage instability are interface traps. More support for this argument is given subsequently.

6.1.1 Gate voltage influence

Before continuing with the analysis, the impact of the gate bias is analyzed. The choice of a particular gate voltage impacts not only the amount of ΔV_{TH}, as could be speculated from Fig. 6.2, but also the increase of ΔV_{TH} per decade in time as shown in Fig. 6.5. That is to say, the larger V_G the larger the number of charges which can be activated with the constant bias phase. An intermediate bake steps of 10 s duration at approximately 130 °C with the poly-heater could be used to restore the virgin state of the device. Consequently, the experiments were conducted on the same device, even though the use of several virgin devices gives the same result (not shown). An analysis of the dependence of the drift after 100 s of charging in Fig. 6.6 shows a linear relationship between the ΔV_{TH} and V_G. Also, applying a gate voltage sequence as sketched in Fig. 6.7 proves that different gate voltages give access to different defects [Lag+12]. Indeed, as shown in Fig. 6.8, independent energy regions are activated through different gate voltages. See also the sketch of the band diagram for this experiment in Fig. 6.9.

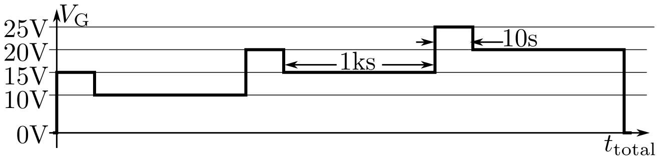

Fig. 6.7: Sequence of the gate voltage for the experiment depicted in Fig. 6.8.

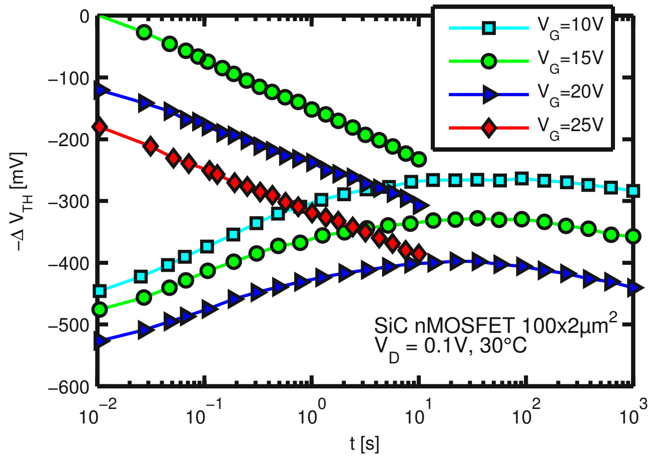

Fig. 6.8: Consecutive interrupted stress with different gate voltages. The sequence of the gate voltage is sketched in Fig. 6.7. All data is shifted on the vertical axis such that the first measurement point is at 0 mV.

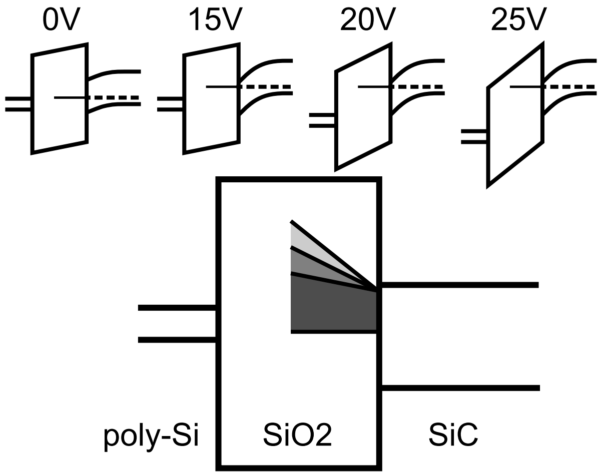

Fig. 6.9: Simple sketch of the band bending in the MOS system (upper plots) and the extension of the Fermi level into the oxide (lower plot) for different gate voltages.

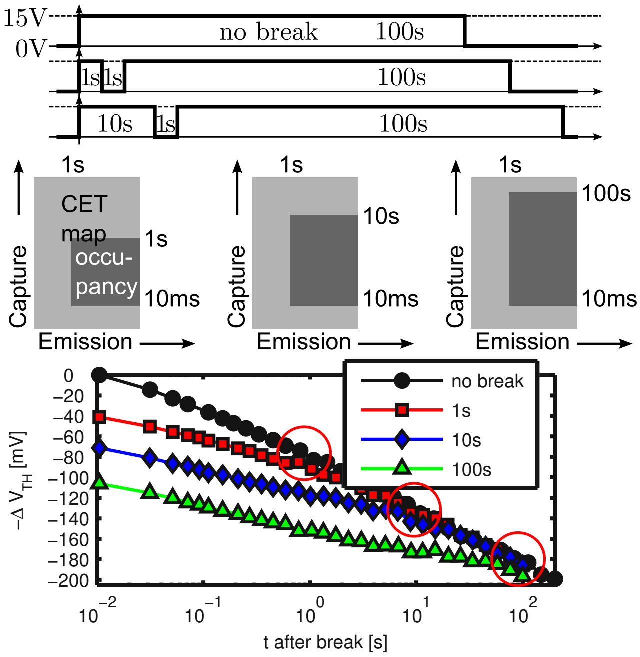

Fig. 6.10: Gate voltage sequence (top plot), CET map occupancies (middle plots) for V_{TH} phases of different length before a break and experimental result (bottom plot) [PG13a]. Longer charging phases before the break cause larger parts of the CET map to be occupied for the second charging phase. The red circles in the bottom plot indicate the theoretical merging points.

To conclude, for a proper description an alternative model not based on SRH-like theories is needed. However, before discussing a possible physical origin of the instability, the problem is analyzed in a systematic way using CET maps [Rei+10; Gra+11a].

6.1.2 The CET map

A capture-emission time (CET) map is a two-dimensional plot of the density of traps versus their corresponding logarithmic capture and emission times [Rei+10]. For example, the CET map of the adapted SRH model is a narrow density parallel to the diagonal $\tau_{\mathrm{c}} = \tau_{\mathrm{e}}$ because of the strong correlation of capture and emission times [Gra12, Fig. 47]. Integration of the CET map gives the number of trapped charges and thus the ΔV_{TH} at arbitrary times. The integration area is defined through the duration of charging/discharging periods due to bias switches at the gate. The simplest case for charging traps in an SiC-MOSFET is to switch the gate bias from 0 V to the V_{TH} of the device as for the experiment shown in Fig. 6.1, which corresponds to a filling of the CET map from bottom to top. This typically results in a semi-logarithmic charging behavior [Oka+08b], which is due to a superposition of numerous individual charging events with a very broad distribution of capture time constants τ_{c} [Rei+10]. The energetic position of the traps responsible for the charging is between $E_{\mathrm{F}}(V_{\mathrm{G}} = 0\mathrm{V})$ and $E_{\mathrm{F}}(V_{\mathrm{G}} = V_{\mathrm{TH}})$. When the constant bias phase is interrupted, several defects emit their charge again, provided the interruption was longer than their emission time constants τ_{e}. This leads to rather complicated charging transients like those shown in Fig. 6.10 and Fig. 6.11. Independently of the exact distribution of τ_{c} and τ_{e}, the transients of Fig. 6.10 and Fig. 6.11 can already be understood in terms of an occupation pattern in the CET map [PG13a].

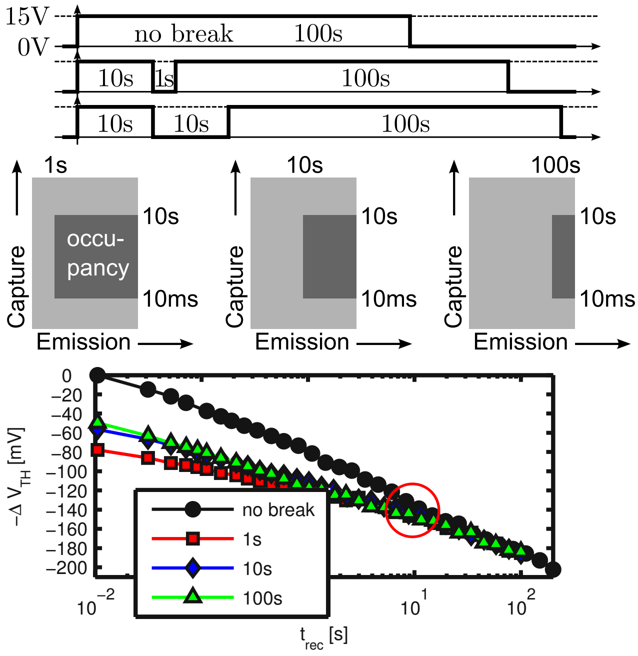

Fig. 6.11: Gate voltage sequence (top plot), CET map occupancies (middle plots) for varying duration breaks and experimental result (bottom plot) [PG13a]. The longer break phases remove a larger part of the previously charged parts of the CET map. All characteristic should theoretically merge at the same point in time with the continuous charging (no break) characteristic.

6.1.3 CET map model

As seen before in Fig. 6.4, the experimental charging characteristic of an SiC-nMOSFET cannot be explained by an SRH-like model where the capture and emission time constants are strongly correlated. Also, the capture time constants are broadly distributed which causes the continuous charging characteristic shown in Fig. 6.1. This broad distribution of time constants makes a direct determination of the parameters of the distribution unfeasible because the tails of the distribution carry a lot of information. Therefore, an analytical ansatz following reference [Gra+11a] is validated against experimental data. The analytical model consists of two bivariate normal distributions of effective activation energies

$$E_{\mathrm{A,c;e}} = k_{\mathrm{B}} T \log\left(\tau_{c;e}/\tau_0\right) \tag{6.5}$$

for capture and emission time constants τ_{e} and τ_{c}, respectively. Here, the scaling factor τ_0 is an individual fitting variable for either bivariate normal distribution. The temperature activation is inherently considered since the distribution of activation energies instead of the time constants is directly fitted. The model has 12 parameters. For either bivariate distribution there are two values for the mean μ_{c} and μ_{e}, two parameters for the variance σ_{c} and σ_{e} (the correlation is restricted and calculated from these two values as $\rho = \sigma_{\mathrm{c}}/(\sqrt{\sigma_{\mathrm{c}}^2 + \sigma_{\mathrm{e}}^2})$), one minimum time constants τ_0 and an amplitude giving the density of charges per eV^2.

In a particular example, it was possible to fit one analytical model of two bivariate normal distributions to SiC-nMOSFET charging data measured at several temperatures between 30 °C and 200 °C. To illustrate this, Fig. 6.12 shows the result of the fit of the activation energy map shown in Fig. 6.13 to an example data set at 150 °C. The fitting result for other temperatures is equivalent. It is emphasized that this model accurately predicts the threshold voltage instability of this particular MOSFET within a few days and allows for accurate extrapolation to much longer times. This is true for temperatures of 30 °C to 200 °C and to gate voltages up to 25 V. That is to say, every charging/discharging pattern which might occur during operation of the device can be

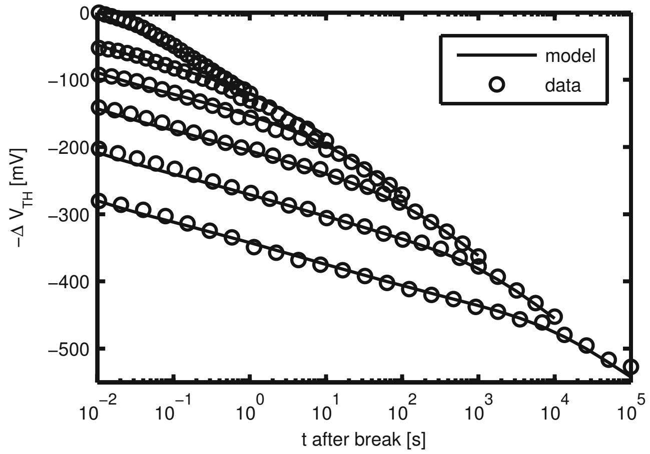

Fig. 6.12: Interrupted charging of an SiC-nMOSFET at 150 °C chuck temperature compared with the fitted analytical model after [Gra+11a] [PG13a].

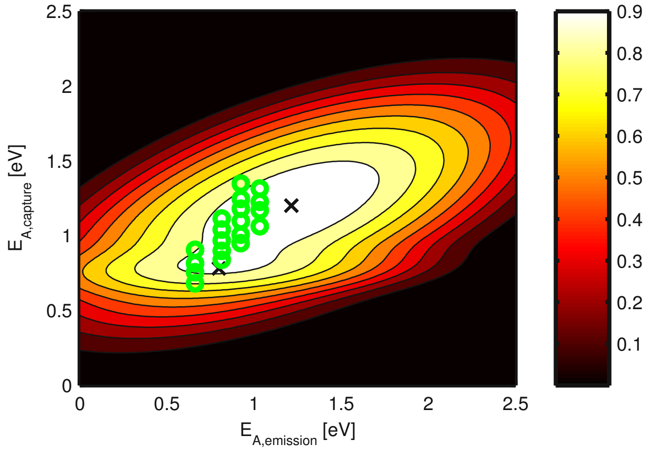

Fig. 6.13: Example activation energy distribution for the interrupted charging shown in Fig. 6.12 [PG13a]. The green circles indicate the position of the experimental data used to fit the map. The color axis is normalized to display all details [Gra+11a].

calculated with this model. This is especially beneficial for circuit designers who need to account for threshold voltage changes of a SiC-MOSFET in the design of the application circuit.

6.2 Charge pumping for SiC-SiO$_2$ interface characterization

The interpretation of Charge pumping (CP) experiments, as described in more detail in the review Section 1.2.2, follows a standard model [Gro+84] which is based on SRH theory [SR52; Hal52] on Si based MOSFETs. In the following, it is shown that this model is also capable to accurately describe CP results on SiC-nMOSFETs.

It is remarked that the following measurement results are displayed in terms of charges pumped per cycle [Gro+84; Aic+10c; Rya+11]

$$N_{\mathrm{CP}} = D_{\mathrm{IT}} \Delta E_{\mathrm{CP}} = \frac{I_{\mathrm{CP}}}{qfA}. \tag{6.6}$$

This has the advantage that the area and frequency dependencies of the CP current are inherently considered to simplify comparisons. Naturally, an analysis of the density of interface traps D_{IT} in $\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ would be even more desirable. However, for a determination of the active CP energy region

$$\Delta E_{\mathrm{CP}} = 2 k_{\mathrm{B}} T \ln\left(v_{\mathrm{th}} n_{\mathrm{i}} \sqrt{\sigma_{\mathrm{n}} \sigma_{\mathrm{p}}} \frac{|V_{\mathrm{FB}} - V_{\mathrm{TH}}|}{\Delta V_{\mathrm{G}}} \sqrt{t_{\mathrm{f}} t_{\mathrm{r}}} \right), \tag{6.7}$$

the material dependent capture cross section σ of SiC-SiO$_2$ interface traps, the thermal drift velocity v_{th} and the intrinsic carrier density of 4H-SiC are needed. Unfortunately, those parameters are only poorly determined for 4H-SiC and are therefore afflicted by large uncertainties. In detail:

- Different studies [Oui+94; Pip+05; Rud+05; Che+08; Roz08] have obtained values for the electron capture cross section σ of interface traps at the 4H-SiC-SiO$_2$ interface in the range from $10^{-21}\,\mathrm{cm}^2$ to $10^{-16}\,\mathrm{cm}^2$. Even values as low as $10^{-5}\,\mathrm{cm}^2$ to $10^{-4}\,\mathrm{cm}^2$ [KTL96] were reported. Another study has suggested that the capture cross section depends on the energetic trap position for six layer hexagonal SiC (6H-SiC)-SiO$_2$ MOS capacitors [Oui+94] and a similar situation is expected for 4H-SiC based MOSFETs.

- The thermal drift velocity v_{th} of the carriers is reported to be around $10^7\,\mathrm{cm\,s^{-1}}$. Simulation results report $1.6 \times 10^7\,\mathrm{cm\,s^{-1}}$ whereas experimental results are $0.8 \times 10^7\,\mathrm{cm\,s^{-1}}$ [Vas+00]. A temperature dependent model is

  $$v_{\mathrm{th}} = v_{\mathrm{th},0} \times \sqrt{T}, \tag{6.8}$$

  with $v_{\mathrm{th},0,n} = 6.74 \times 10^5\,\mathrm{cms^{-1}K^{-1/2}}$ and $v_{\mathrm{th},0,p} = 1.55 \times 10^5\,\mathrm{cms^{-1}K^{-1/2}}$ for electrons and holes, respectively [Cio05].

- The intrinsic carrier density n_{i} is calculated as

  $$n_{\mathrm{i}} = 1.7 \times 10^{16}\,\mathrm{K^{-3/2}cm^{-3}} \times T^{3/2} \exp\left(-\frac{2.08 \times 10^4}{T} \right), \tag{6.9}$$

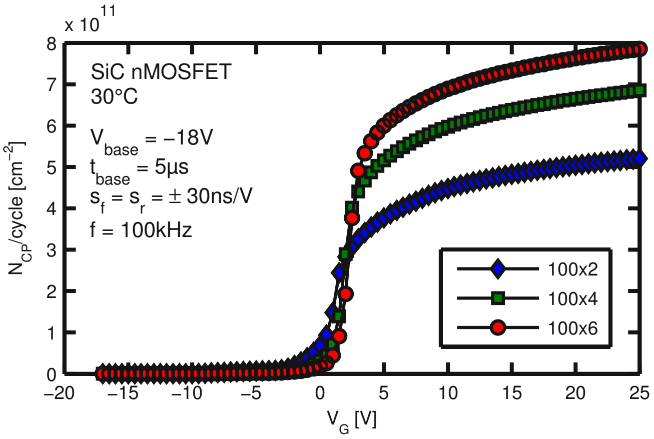

Fig. 6.14: Constant base CP on nMOSFETs with 2 µm to 6 µm channel length. The number of charges pumped per cycle is assigned to the y-axis. The channel is about 0.4 µm smaller than the drawn length, explaining the remaining discrepancy in the maximum CP current at V_G = 25 V.

which is a simplification of the temperature dependence resulting from [Aya04]

$$n_\mathrm{i} = \sqrt{N_\mathrm{C}(T)N_\mathrm{V}(T)}\exp\left(-\frac{E_\mathrm{g}(T)}{2k_\mathrm{B}T}\right). \tag{6.10}$$

This approach gives a carrier density of $n_\mathrm{i} = 4\times10^{-11}\,\mathrm{cm}^{-3}$ at 25 °C. Still, other references [FBS96] report a value of $n_\mathrm{i} = 10^{-8}\,\mathrm{cm}^{-3}$ for room temperature.

The large uncertainty of these material parameters make the calculation of the density of interface traps for SiC-MOSFETs uncertain. However, a possible approach is to calculate the impact of the maximum error on the ΔE_CP [Pob+ pb]. The error in ΔE_CP becomes as small as 0.1 eV by suggesting ranges of possible values as $\sigma = 10^{-18}\,\mathrm{cm}^2 \ldots 10^{-16}\,\mathrm{cm}^2$, $v_\mathrm{th} = 0.75\times10^{7}\,\mathrm{cm\,s}^{-1} \ldots 2\times10^{7}\,\mathrm{cm\,s}^{-1}$, and $n_\mathrm{i} = 0.5\times10^{-8}\,\mathrm{cm}^{-3} \ldots 1\times10^{-8}\,\mathrm{cm}^{-3}$.

Still the number of charges pumped per cycle N_CP is primarily used to separate the influence of the particular choice of material parameters from variations in the number of interface traps.

It is remarked that in SiC MOS structures an inversion of the interface is in principle only possible at very high temperatures above a few hundred degree Celsius or if an external source provides minority carriers. For SiC-nMOSFETs the presence of the n^{++} doped source/drain junctions close to the active device interface allows the inversion of the interface due to the lateral supply of minority carriers. So for MOSFETs all interface traps within the band gap can exchange their charge frequently, also during the CP measurement. In contrast, SiC MOS capacitors posses a region around the mid of the band gap with traps which are charged only once with the first use of the device [FBS96].

6.2.1 Characteristics

To check the behavior of the measured CP current, the impact of the gate area on I_CP is inspected. Fig. 6.14 displays the results of constant base level CP measurements on devices with different gate lengths. The number of charges pumped per cycle is depicted, so the result of Fig. 6.14 is that the CP current *does* scale with the device area.

In Fig. 6.15 a constant base level measurement is compared to a constant peak level CP measurement. The constant base level CP measurement shows the CP threshold voltage, defined at the gate voltage where the maximum increase of the I_CP versus V_G is given [AN08; Aic07]. The equiva-

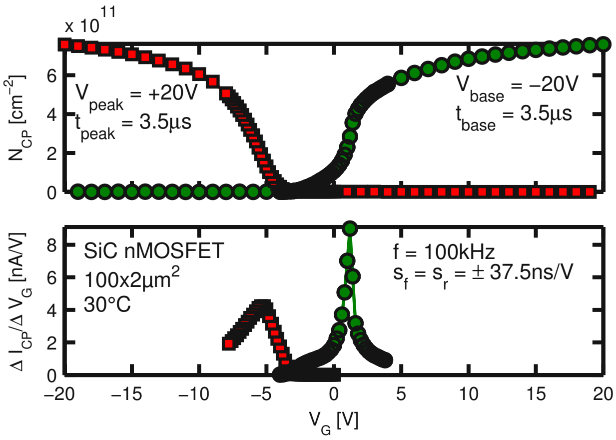

Fig. 6.15: Constant base (green) and constant peak (red) level $I_{\mathrm{CP}}(V_{\mathrm{G}})$ (top plot) and its derivative (bottom plot). The region of interest is measured a second time with higher point density.

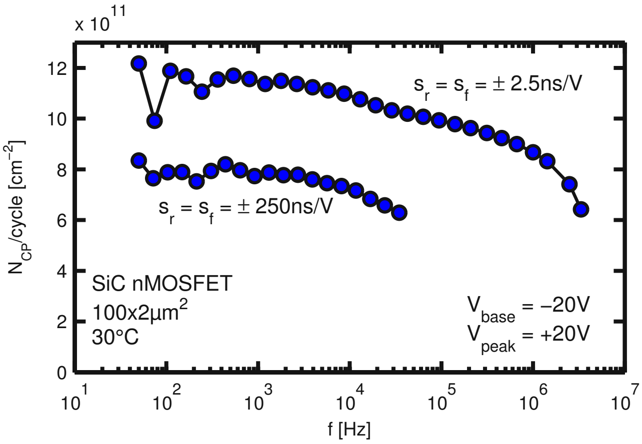

Fig. 6.16: Frequency dependent CP measurement for two different rising and falling slopes s_{r} and s_{f}, respectively.

lent is true for the CP flat-band voltage of the constant peak level measurement. The temperature dependence of the in this way extracted CP V_{TH} and V_{FB} values is shown later in Fig. 6.19.

Next, as shown in Fig. 6.16, the frequency dependence of the CP current is inspected. Two different rising and falling slopes are shown to reveal either insufficient base or peak times or measurement errors due to the finite current resolution limit of about 10 pA. The number of charges pumped per cycle N_{CP} is supposed to stay fairly constant over a few decades of frequency. This indicates that mainly the transition from accumulation to inversion and vice versa is responsible for the measured CP current, as expected for fast interface traps [Gro+84; Aic07]. However, there exists a small but evident increase of I_{CP} with decreasing frequency which is usually attributed to border traps which charge during the peak time of the pulse and discharge during the base time (and vice versa) [Fle92; Pau+92; PW94]. Still, their number is roughly one decade smaller ($\approx 10^{11}\,\mathrm{cm}^{-2}$) than the number of interface traps ($\approx 10^{12}\,\mathrm{cm}^{-2}$).

Furthermore, it can also be seen that decreasing the rising and falling slopes increases N_{CP}, consistent with the standard model for CP (1.4) [Gro+84] which states that smaller rise/fall times increase the accessible energy range within the band gap ΔE_{CP}. This is investigated in more detail in Fig. 6.17. There, N_{CP} is fairly independent of the transition time from accumulation to inversion (rise time). In contrast, a large dependence on the fall time is seen (going from inversion to accumulation). In detail: During the peak voltage period an interface trap has captured an electron which originated from the source or the drain. During the peak phase the interface trap

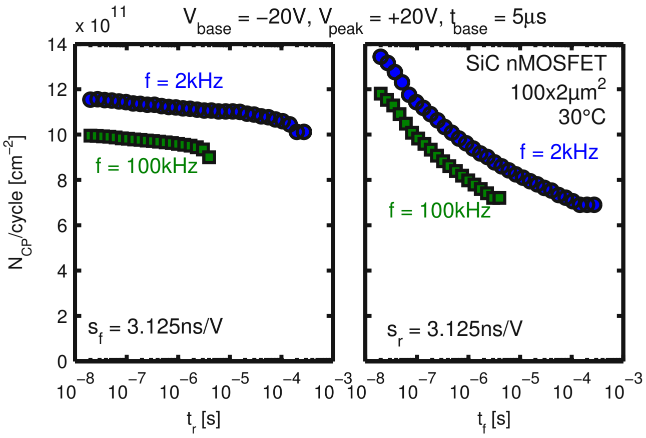

Fig. 6.17: Varying rise time (left plot) and varying fall time (right plot) CP measurement for two different frequencies. The base and peak voltage levels as well as the base time are kept constant for both measurements.

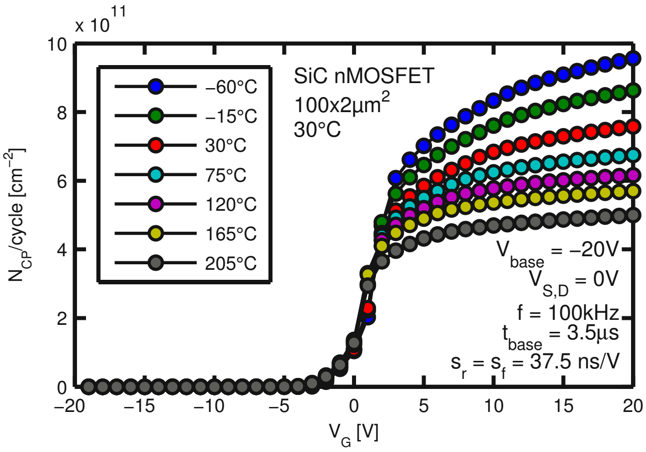

Fig. 6.18: Impact of the temperature on the N_{CP} in a constant base level CP measurement.

may re-emit its electron to the conduction band if the trap is close to the conduction band edge. If the negative charge is kept in the interface trap, two possible processes may occur during the transition from inversion to accumulation: First, the electron is emitted towards the conduction band where it returns to source or drain. Or, secondly, it is emitted towards the valence band where it is gathered by the bulk contact and contributes to I_{CP}. The latter process is initiated by the change of the gate voltage because of the dependence of the hole capture process on the Fermi level as

$$\tau_{\mathrm{cp}} = \frac{1}{v_{\mathrm{th},p}\sigma_p n_{\mathrm{i}}} \exp\left(\frac{E_{\mathrm{F}} - E_{\mathrm{V}}}{k_{\mathrm{B}}T}\right). \tag{6.11}$$

That is to say, the faster the Fermi level is changed towards the valence band edge (smaller falling time), the sooner holes from the valence band can be captured. So if a large density of interface traps is present in the upper half of the band-gap, a strong dependence on the fall time is observed. Consequently, this measurement suggests a larger interface trap density close to the conduction band edge, which is in accordance with results from CV measurements [SMA00].

6.2.2 Temperature dependence

In Fig. 6.18 the impact of the temperature on N_{CP} in a constant base level CP measurement is shown. Consistent with the standard model for CP [Gro+84] and the results on Si based MOSFETs

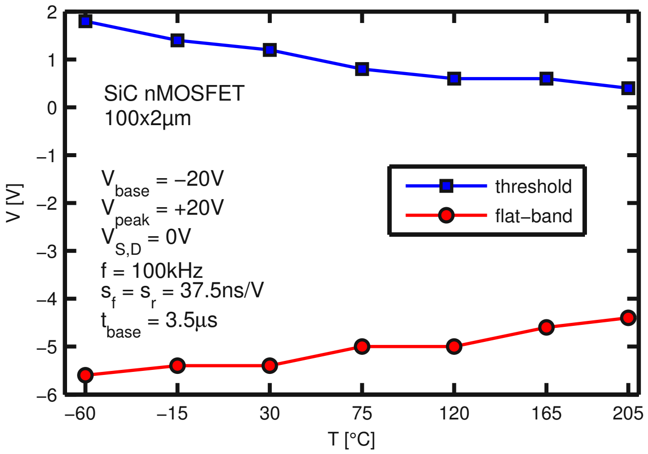

Fig. 6.19: Temperature dependence of the CP flat-band and threshold voltage. Extracted from the maximum change of the I_{CP} with V_{G} as shown in Fig. 6.15.

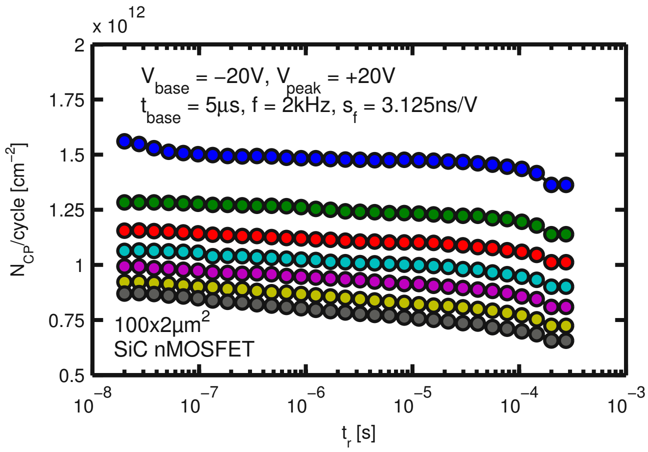

Fig. 6.20: Rise time dependence of the CP current for chuck temperatures ranging from −60 °C to 205 °C. See Fig. 6.21 for the coloring of the markers.

[ANG08], the I_{CP} decreases with increasing T. The decrease is thereby due to the decrease of the active CP energy region as given in (1.4).

Consequently, also for SiC-MOSFETs it is beneficial to perform CP experiments at the lowest possible temperature to maximize the active ΔE_{CP}. The increasing energy range is also visible by an analysis of the dependence of the CP flat-band and threshold voltages on the chuck temperature as shown in Fig. 6.19. The difference between V_{FB} and V_{TH} decreases with increasing temperature, again similar to Si based MOSFETs [Gro+84; ANG08].

For the sake of completeness, also the dependence of N_{CP} on the rise and fall times for different temperatures is shown in Fig. 6.20 and Fig. 6.21, respectively. The number of charges pumped per cycle is fairly independent of the rise time for the whole investigated temperature range from −60 °C to 205 °C. From this follows that the density of interface traps is uniformly distributed in the lower half of the band-gap. In contrast, the increase of N_{CP} with decreasing fall time, which was already evident for the 30 °C measurement in Fig. 6.17, is even larger for −60 °C. This indicates a large density of interface traps close to the conduction band edge [Gro+84], consistent with other results based on CV measurements [Cio05; Roz08; Est11].

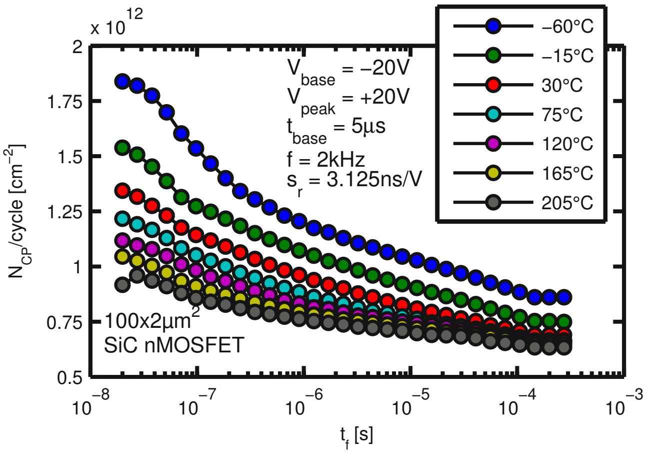

Fig. 6.21: Fall time dependence of the CP current for different chuck temperatures. The increase for colder temperatures and short fall times is emphasized.

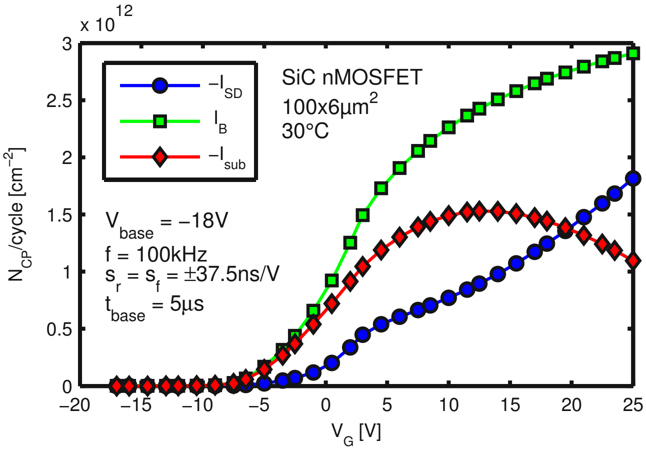

Fig. 6.22: Constant base level CP measurement on a device with a large parasitic substrate current I_{sub}. This current adds to the source/drain current I_{SD} to form the bulk current I_{B}.

6.2.3 Parasitic substrate current

Earlier publications reported a large geometrical component which interferes with the CP current and makes the technique less reliable [SM98; Oka+08a; KTL96]. On a few of the SiC devices investigated in this thesis, which have not been optimized for CP measurements, a geometrical component was observable as well. This effect is visible as a substrate current on nMOSFET devices as shown in Fig. 6.22. The current has a polarity which indicates that electrons are injected from the substrate towards the p-well of the nMOSFET. The current dependents strongly on the base and peak times of the pulse (not shown). A possible reason for the occurrence of the substrate current could be a large density of traps in the space charge region between the p-well and the substrate. However, this effect has vanished with a re-design of the test structures where the following was ensured:

- The p+ contact of the p-well was positioned as closely as possible to the channel such that the low conductive p-well has less impact.
- The p-channel implantation of the device was optimized for a homogeneous ion depth distribution.
- The metal contact to the gate poly was improved to ensure a low ohmic connection to the gate such that the pulse signal reaches the gate to the largest possible extent.

7

SiC-SiO$_2$ degradation mechanisms

Charge pumping (CP) for SiC-MOSFETs, as introduced in the previous Chapter, allows to investigate degradation at the SiC-SiO$_2$ interface precisely. With this, the reliability of SiC based MOSFETs is investigated in the following. Since only limited information regarding BTI and HCD is available for 4H-SiC MOSFETs [Ban+00; Lel+08; ALP13], the basic effect of BTS and HCS on the transistor parameters is investigated. The results presented in this Chapter have been previously published in [Pob+ pb].

7.1 Bias temperature stress

Compared to the virgin threshold voltage instability treated in Section 6.1, a larger stress bias of $V_G = 50\,\mathrm{V}$ ($\approx 6\,\mathrm{MV\,cm^{-1}}$) is used, which is close to the breakdown of the 80 nm thick SiO$_2$ layer. This ensures that the instability caused by the stress phase is larger than the impact of the V_{TH} bias phase. Both stress polarities are tested to identify the type of created charges.

First, positive BTS (PBTS) is performed at 200 °C chuck temperature. The PBTS causes the transfer characteristic of the device to shift in parallel along the voltage axis towards larger V_G values as shown in Fig. 7.1. This indicates the creation of $1.9 \times 10^{11}\,\mathrm{cm^{-2}}$ negatively charged traps after 1 ks stress assuming the charges at the SiC-SiO$_2$ interface. The readout bias independence indicates that the charges created through PBTS are only in weak contact with the carriers in the channel during the transfer characteristic measurement. That is to say, charge exchange with these defects occurs on larger timescales. In accordance, the I_{CP} from a CP measurement within a few seconds after termination of stress is almost independent of the stress time, as shown in Fig. 7.2.

Also negative BTS (NBTS) at $V_G = -50\,\mathrm{V}$ causes the creation of readout-bias-independent charges as shown in Fig. 7.3 [ALP13]. The magnitude of the drift is, however, smaller than after

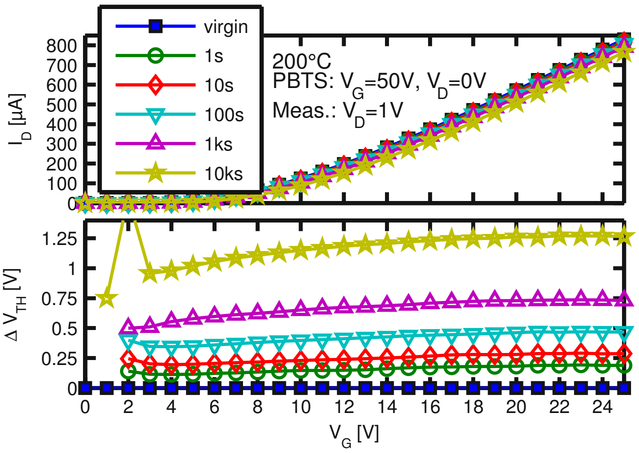

Fig. 7.1: Transfer characteristics (top) and corresponding drift plots (bottom) for nMOSFETs subjected to PBTS [Pob+ pb].

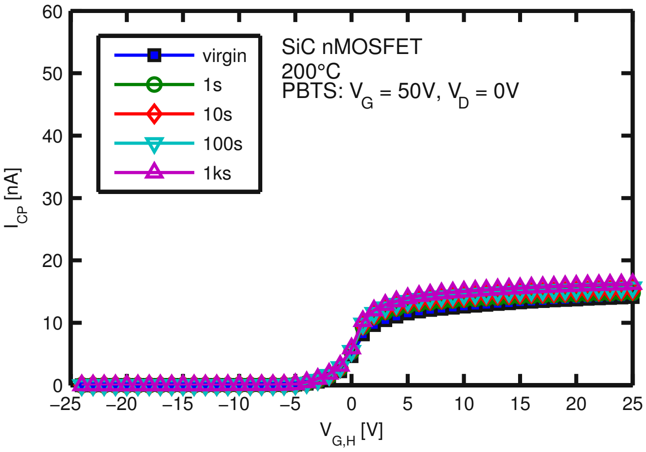

Fig. 7.2: Constant base level CP measurement results after PBTS with different duration. Details of the CP measurement are given in Section 6.2.

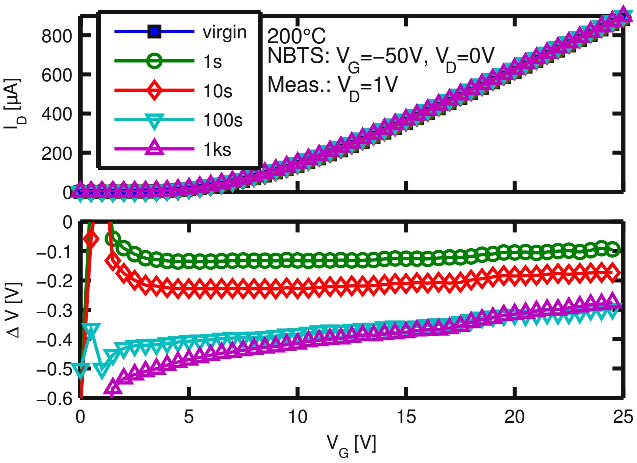

Fig. 7.3: The same as Fig. 7.1 but for NBTS.

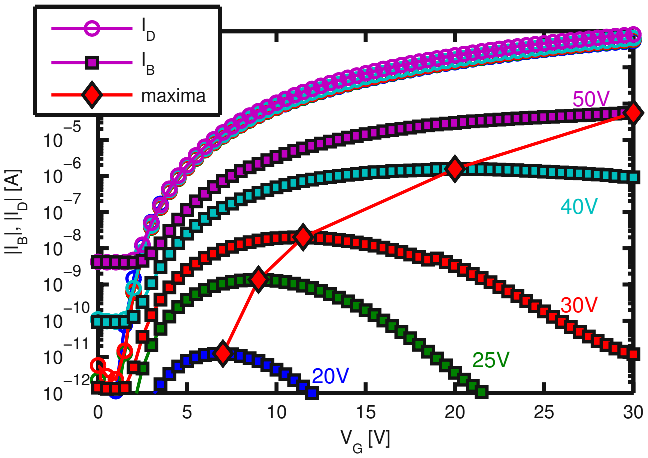

Fig. 7.4: Drain and substrate current dependence on the gate voltage for large drain bias [Pob+ pb]. The substrate current measurements are labeled with the corresponding drain voltage.

PBTS with the same absolute gate voltage value. The CP current stays constant as well (not shown).

To conclude, consistent with the results obtained for Si based MOSFETs described in Chapter 2, PBTS causes negative, and NBTS positive, gate bias independent charges, respectively. Due to the independence of the charges on the particular readout bias and the missing impact on the CP current, which would have indicated the creation of bias-dependent interface traps, it is suggested that the created charges reside within the oxide [She+11].

7.2 Hot carrier degradation

Hot carrier degradation (HCD), as described in Section 1.1.2, is the instability of a MOSFET due to large lateral electric fields during operation and the accompanying acceleration of carriers in the channel. To verify the impact of HCS on 4H-SiC-MOSFETs, test devices were subjected to large drain voltages and the change of the transfer characteristics or the CP current was investigated.

7.2.1 Bulk current

Previous work on HCD in SiC-MOSFETs [Ban+00; Yu+09] reported efficient photon emission at the drain side of the transistor indicating impact ionization of the energetic carriers. However, the impact ionization of carriers penetrating into the space charge region at the drain side can also be measured electrically on an nMOSFET via the substrate current [Sch06; BH10; OE10]. For illustration, the bulk current is measured as a function of V_G for high drain bias as shown in Fig. 7.4. Indeed, a bulk current is measured with a maximum at a certain gate voltage, which depends on the drain bias. The position of the maximum is $V_\mathrm{G} = 1/\alpha \times V_\mathrm{D}$ with $\alpha = 2\ldots3$. This is consistent with micrometer long Si MOSFETs which as well show a maximum at $V_\mathrm{G} = 1/\alpha \times V_\mathrm{D}$ [BH10]. The reason for the maximum is that the substrate current increases in the beginning with the gate voltage as an increasing number of carriers can reach the drain as the channel opens. For larger V_G the device enters its linear mode and the lateral electric field decreases [Sch06]. The bias conditions where the maximum of the substrate current occurs is considered to be a bias point for efficient HCD. Consequently, the subsequent HCS phases are conducted at $V_\mathrm{G} = 25\,\mathrm{V}$ and $V_\mathrm{D} = 50\,\mathrm{V}$.

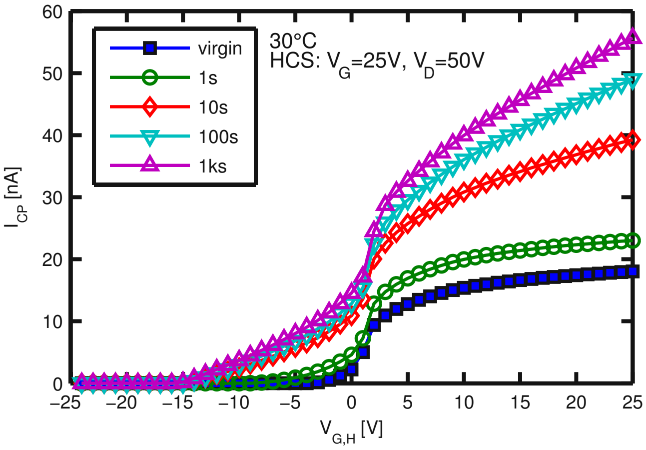

Fig. 7.5: CP measurements before and after HCS of increasing duration [Pob+pb].

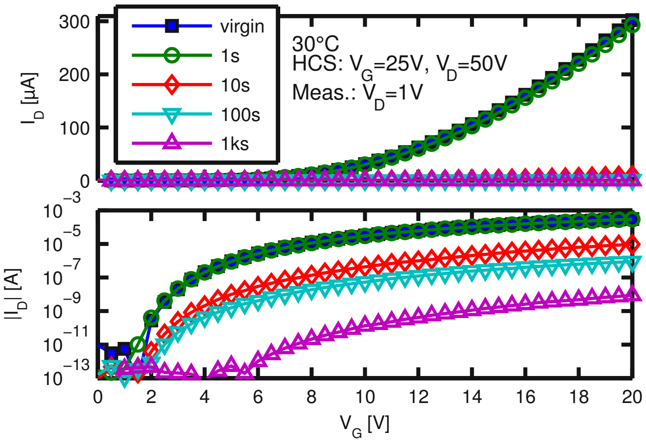

Fig. 7.6: Change of the transfer characteristic with HCS on a linear (top) and logarithmic (bottom) scale.

7.2.2 Stress impact

As shown in Fig. 7.5, the CP current increases considerably due to HCS. The particular form of the stressed CP characteristics, especially the non-saturating behavior at high $V_{G,H}$, was attributed in Si devices to an increased number of border traps [Heh+09]. However, for SiC devices this increase indicates newly created interface traps because of an simultaneous large decrease of the drain current of the device, see Fig. 7.6. The induced threshold voltage shift depends strongly on the readout bias, as shown in Fig. 7.7. From all these results follows that the high energetic carriers existent during HCS cause interface degradation.

7.3 Comparison and conclusions

Fig. 7.8 directly compares the increase of the density of interface traps after PBTS and HCS. The difference in the virgin D_{IT} is either due to device-to-device variations or because the temperature dependence of the material parameters of σ and v_{th} is neglected. However, it is evident that only HCS increases the density of interface traps measurable with CP. This indicates that HCS creates interface traps while PBTS creates only oxide traps. This is further supported by the voltage dependent shift in the transfer characteristics evident only after HCS, as compared directly in Fig. 7.9.

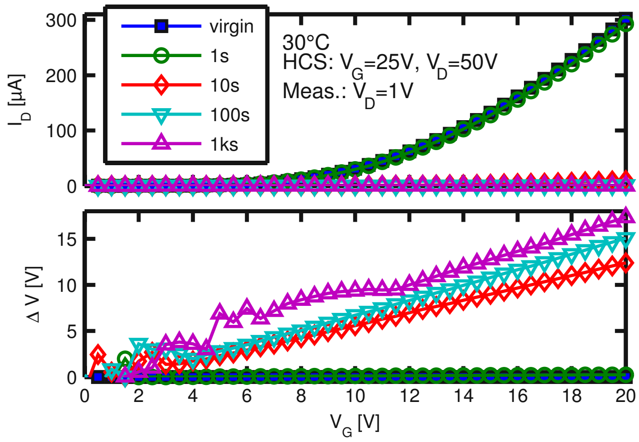

Fig. 7.7: Change of the transfer characteristic as a gate voltage dependent drift (bottom plot) with HCS [Pob+pb].

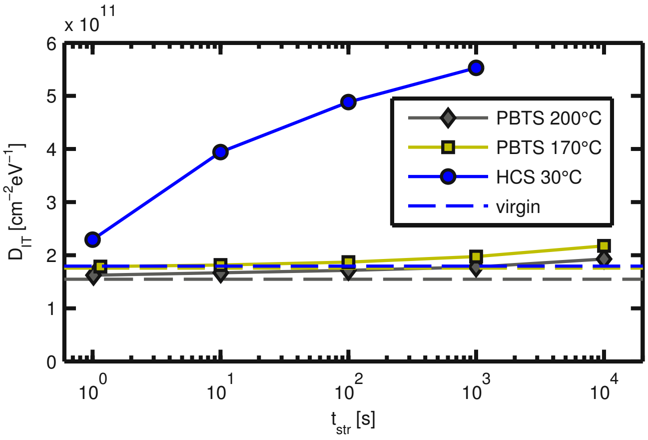

Fig. 7.8: Increase of the density of interface traps for HCS and PBTS [Pob+pb]. The characteristic labeled “PBTS 170 °C” was performed at 30 °C chuck temperature using the poly-heater only during the stress phase. All other measurements are performed at the chuck temperature indicated in the legend.

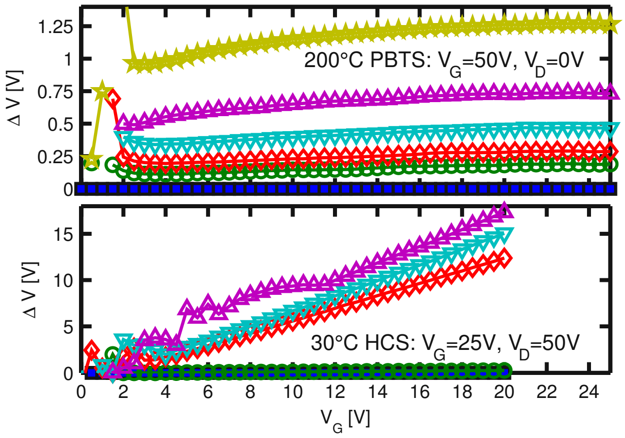

Fig. 7.9: Gate voltage dependent shift of the transfer characteristics after PBTS (top) or HCS (bottom).

The results are explained in the following way: Interface traps at the SiC-SiO_2 interface have been reported to be passivated by nitrogen (N) atoms [McD+03]. Other work states that N bonds strongly to Si or carbon (C) atoms [Dar70; Nau+93]. It is therefore speculated that only the high energetic carriers during HCS are capable of dissociating an Si-N or Si-C bond. BTS, in contrast, causes a field and temperature dependent dissociation of precursor defects within the SiO_2 which could be very similar to the mechanism in Si-MOSFETs.

8

Conclusions and Outlook

In the present thesis the degradation mechanisms in silicon (Si) and silicon carbide (SiC) based MOSFETs are investigated with an emphasis on the bias temperature instability (BTI). A unique research approach is the application of an on-chip heating structure to temperatures far above conventionally accessible ranges. The fast and reliable temperature switches possible with the poly-heater allow separating the impact of temperature on the bias stress from the subsequent recovery. This approach reveals that the degradation a device experiences under use conditions during its lifetime activates only the low energy fraction of a broad distribution of precursor defects. A main result of the present thesis is the measurement of the normal distribution of activation energies for the electrical activation of the precursor defects responsible for BTI. This normal distribution is presumably due to variations in the atomic compositions of the individual defect sites because of the amorphous structure of the thermally grown silicon dioxide (SiO_2).

Further results include a detailed assessment of the influence of the bias polarity on BTI, the investigation of the influence of process adjustments on the reliability of MOSFETs and the peculiarities regarding MOSFETs based on SiC instead of Si.

Although considerable progress in the understanding of the aforementioned topics could be accomplished, large room for improvement is left. Major points are the following:

- The determination of the distribution of activation energies for the charging of precursor has been carried out for a few representative devices with thermally grown SiO_2. The method is in principle applicable to every MOS system with different dielectric layers. However, the poly-heater needs to be appropriately designed to allow for switches to very high temperatures. Such test structures were not available for this thesis which caused the lack of corresponding data for different technologies.
- The microscopic composition of the precursor defect responsible for BTI is still largely debated. The investigations towards the impact of hydrogen on BTI presented in this thesis

do not unambiguously identify the type of defect. The answer to this question may not be found with electrical measurements alone.

- The treatment of charge pumping (CP) for SiC based MOSFETs merits a detailed comparison to the results of other methods.
- The continuing analysis of the exact difference for Si and SiC based MOSFETs regarding the investigated degradation mechanisms implies manifold output of utmost importance for the development of reliable power MOSFETs based on SiC.

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Acronyms

$I_\mathrm{D}V_\mathrm{G}$	drain current–gate voltage.
E' center	dangling bond on a Si atom bonded to three O atoms within the SiO_2.
P_b0 center	first P_b center variant at the (100)Si-SiO_2 interface.
P_b1 center	second P_b center variant at the (100)Si-SiO_2 interface.
P_b center	dangling bond on a Si atom at the Si-SiO_2 interface.
1D	one-dimensional.
2D	two-dimensional.
3D	three-dimensional.
4H-SiC	four layer hexagonal SiC.
6H-SiC	six layer hexagonal SiC.
AG	Aktiengesellschaft (german, incorporated company).
Al	aluminium.
Ansys	analysis system.
B	boron.
BEOL	back end of line.
BTI	bias temperature instability.
BTS	bias temperature stress.
C	carbon.
CET	capture-emission time.
cf.	confer (latin, read as *compare*).
CMOS	complementary MOS.
CP	charge pumping.
Cu	copper.
CV	capacitance voltage.
DCIV	direct current–current voltage.
DUT	device under test.
e.g.	exemplī grātiā (latin, read as *for example*).

EOT	SiO_2 equivalent oxide thickness, EOT $= \varepsilon_{\mathrm{SiO_2}}/C_{\mathrm{ox}}$.
EPR	electron paramagnetic resonance.
ESR	electron spin resonance.
FEM	finite element method.
Fig.	Figure.
GaN	gallium nitride.
H	neutral hydrogen atom.
H^+	positively charged hydrogen ion.
H_2	molecular hydrogen.
H_2O	water.
HCD	hot carrier degradation.
HCS	hot carrier stress.
HDL	Harry–Diamond–Laboratories.
HPSMU	high power SMU.
i.e.	id est (latin, read as *that is to say*).
ILD	inter level dielectric.
KAI	Kompetenzzentrum für Automobil- und Industrieelektronik GmbH (german, competence center for automotive and industrial electronics limited liability company).
lin	linear.
LPCVD	low-pressure chemical vapor deposition.
MOS	metal oxide semiconductor.
MOSCAP	MOS capacitor.
MOSFET	MOS field effect transistor.
MSM	measurement–stress–measurement.
N	nitrogen.
N_2	molecular N.
NBTI	negative BTI.
NBTS	negative BTS.
NH_3	ammonia.
nMOSFET	n-channel MOSFET.

O	oxygen.
OTF	on-the-fly.

P	permanent component.
PbH	H passivated P_b center.
PBTI	positive BTI.
PBTS	positive BTS.
PhD	Doctor of Philosophy.
pMOSFET	p-channel MOSFET.
poly	polycrystalline silicon.

R	recoverable component.
RD	reaction–diffusion.

sat	saturation.
Si	silicon.
Si–H	H passivated silicon dangling bond.
SiC	silicon carbide.
SiH_4	silane.
SiN	silicon nitride.
SiO_2	silicon dioxide.
SiON	silicon oxynitride.
SMU	source measurement unit.
SRH	Shockley–Read–Hall.

TCAD	technology computer aided design.
TDDB	time dependent dielectric breakdown.
TDDS	time dependent defect spectroscopy.
Ti	titanium.
TU Vienna	Vienna University of Technology.

Symbol list

Symbol	**Description**	**Unit**
A	Effective area of a MOS structure or MOSFET	cm^2
C_{ox}	Oxide capacitance	$\mathrm{F\,cm^{-2}}$
D_{IT}	Density of interface traps	$\mathrm{cm^{-2}\,eV^{-1}}$
E_{A}	Activation energy in an Arrhenius equation	eV
E_{C}	Conduction band edge energy	eV
E_{F}	Fermi level energy	eV
E_{T}	Energy level of an interface trap	eV
E_{V}	Valence band edge energy	eV
E_{g}	Band gap energy	eV
E_{i}	Energy level of the intrinsic semiconductor	eV
I_{B}	Current at the bulk connection of a MOSFET	A
I_{CP}	Charge pumping current	A
I_{D}	Current through the drain contact of a MOSFET	A
I_{SD}	Combined current at the source and drain of a MOSFET	A
I_{sub}	Substrate current of a lateral MOSFET measured at the backside of the wafer	A
N_{CP}	Number of charges pumped per cycle in an CP measurement	cm^{-2}
N_{C}	Effective density of states in the conduction band	cm^{-3}
P_{PH}	Electrical power supplied to the poly-heater	W
$R^{\mathrm{th}}_{\mathrm{FOX}}$	Apparent thermal resistance of the field oxide between the poly-heater and the device	$\mathrm{^\circ C\,W^{-1}}$
$R^{\mathrm{th}}_{\mathrm{sub}}$	Apparent thermal resistance of the substrate	$\mathrm{^\circ C\,W^{-1}}$
R^{th}	Apparent thermal resistance	$\mathrm{^\circ C\,W^{-1}}$
T_{PH}	Temperature of the poly-heater wires measured by the change of its resistance	°C
T_{chuck}	Temperature of the thermo chuck	°C
T_{dev}	Estimated temperature of the device under test	°C
T_{rec}	Recovery temperature after BTS	°C
T_{str}	Stress temperature during BTS	°C
T	Temperature	°C,K
V_{D}	Voltage applied to the drain of a MOSFET with respect to the source	V
V_{FB}	Voltage at which the energy band edges in the semiconductor are not bended	V
V_{G}	Potential difference between the gate contact and the bulk of the semiconductor in MOS structures and between the gate and the source in MOSFETs	V

Symbol	**Description**	**Unit**
V_{TH}	Threshold voltage	V
V_{rec}	Value of the bias applied to the gate during recovery after BTS	V
V_{str}	Value of the stress bias applied to the gate during BTS	V
ΔE_{CP}	Electrical active energy region within the band gap during CP	eV
ΔI_{D}	Change of the drain current of a MOSFET	A
$\Delta V_{\mathrm{TH}}^{\mathrm{max}}$	Maximum achievable threshold voltage drift	V
$\Delta V_{\mathrm{TH}}^{\mathrm{norm}}$	Normalized change of the threshold voltage considering the influence of the oxide thickness	V
ΔV_{TH}	Change of the threshold voltage	V
$\mathcal{E}_{\mathrm{ox}}$	Electric field in the oxide	$\mathrm{V\,cm^{-1}}$
μ_{FET}	Mobility of a MOSFET	$\mathrm{A\,V^{-1}}$
σ	Capture cross section	$\mathrm{cm^{2}}$
τ_0	Constant scaling factor in the temperature-time approach	s
τ_{c}	Capture time constant of a single defect	s
τ_{e}	Emission time constant of a single defect	s
τ	Emission/capture time constant	s
ε_0	Vacuum permittivity $\varepsilon_0 = 8.854\,188 \times 10^{-14}\,\mathrm{F\,cm^{-1}}$ [SN06]	$\mathrm{F\,cm^{-1}}$
$\varepsilon_{\mathrm{SiO_2}}$	Permittivity of $\mathrm{SiO_2}$ $\varepsilon_{\mathrm{SiO_2}} = 3.9 \times \varepsilon_0 = 34.531\,333\,2 \times 10^{-14}\,\mathrm{F\,cm^{-1}}$ [SN06]	$\mathrm{F\,cm^{-1}}$
ϑ	Abstract temperature-time following an Arrhenius-like temperature dependence of defect time constants	s
d_{ox}	Effective oxide thickness	cm
f	AC signal frequency	Hz
k_0	Frequency factor in the distributed activation energy model	$\mathrm{s^{-1}}$
k_{B}	Boltzmann constant $k_{\mathrm{B}} = 8.6174 \times 10^{-5}\,\mathrm{eV\,^{\circ}C^{-1}}$ [SN06]	$\mathrm{eV\,^{\circ}C^{-1}}$
n_{i}	Intrinsic carrier density	$\mathrm{cm^{-3}}$
n	Free electron density	$\mathrm{cm^{-3}}$
q	Elementary charge $1.602\,18 \times 10^{-19}\,\mathrm{C}$ [SN06]	C
s	Rising or falling slope of trapezoidal pulse	$\mathrm{ns\,V^{-1}}$
t_{e}	Emission time of a single emission event of a single defect	s
t_{f}	Fall time of a trapezoidal pulse	s
t_{rec}	Time since the termination of the stress	s
t_{r}	Rise time of a trapezoidal pulse	s
t_{str}	Stress duration	s
t	Time	s
v_{th}	Thermal drift velocity	$\mathrm{cm\,s^{-1}}$

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Education

08/2010–12/2013	**Doctoral program technical sciences**, *Vienna University of Technology, Institute for Microelectronics*, Vienna, Austria.
09/2007–06/2010	**Master program technical physics**, *Graz University of Technology, Faculty of Technical Mathematics and Technical Physics*, Graz, Austria.
09/2008–12/2008	**International student exchange program**, *Montana State University*, Bozeman, Montana, United States of America.
09/2007–02/2008	**Erasmus–European exchange program**, *Universitat Autónoma de Barcelona*, Bellaterra, Spain.
10/2004–07/2007	**Bachelor program technical physics**, *Graz University of Technology, Faculty of Technical Mathematics and Technical Physics*, Graz, Austria.
09/1998–06/2003	**Higher college telecommunications and computer engineering**, *HTL Mössingerstraße*, Klagenfurt, Austria.

Theses

Master thesis

Title	*Advance electrical characterization of NBTI induced gate oxide defects*
Supervisor	Prof. Peter Hadley, Institute of Solid State Physics, TU Graz, Austria

Bachelor thesis

Title	*Anwendungen höherer Mathematik in der Physik*

Supervisor	Prof. Wolfgang Bulla, Institute of Theoretical and Computational Physics, TU Graz, Austria

Experiences

08/2010–12/2013	**Industrial PhD thesis**, *Kompetenzzentrum für Automobil- und Industrieelektronik GmbH*, Villach, Austria.
08/2009–06/2010	**Industrial master thesis**, *Kompetenzzentrum für Automobil- und Industrieelektronik GmbH*, Villach, Austria.
07/2008–08/2008	**Internship**, *Carinthian Tech Research AG*, Villach, Austria.
07/2007–09/2007 07/2006–09/2006 08/2005–09/2005	**Internship**, *Infineon Technologies AG*, Villach, Austria.
07/2005–08/2005	**Internship**, *AT&S*, Klagenfurt.
10/2003–10/2004	**Alternative civilian service**, *Chamber of Agriculture*, Klagenfurt, Austria.
08/2003–09/2003 07/2002–08/2002 07/2001–08/2001	**Internship**, *Active photonics AG*, Villach, Austria.
07/2000–08/2000	**Internship**, *Waltronic*, Villach, Austria.

Languages

German	**Mothertongue**.
English	**C2**, *Common European Framework of Reference for Languages level, self-assessment.*
Spanish	**A2**, *Common European Framework of Reference for Languages level.*
Catalan	**A1**, *Common European Framework of Reference for Languages level.*

Interests and Miscellaneous

Hobbies	Sports, mountaineering
Driving license	Cars, motorcycles and agricultural vehicles: Austrian category A, B and F