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A MASTER THESIS ON

Development of a Low-Noise CV Measurement Module for Defect-Spectroscopy of MOS Transistors

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Abstract

The metal oxide semiconductor (MOS) transistor is one of the essential devices in modern electronic applications. In recent years, the performance and geometry of MOS transistors have been continuously improved. For instance, modern devices are only a few tens of nanometer small. Due to the miniaturization of electronic devices, even single defects in the physical structure can significantly influence the stable operation of individual devices. One widely used method for the characterization of MOS transistors is performing capacitance-voltage (CV) measurements. The resulting CV characteristics can be used to estimate fundamental physical properties of MOS field-effect transistors (MOSFETs), like oxide thickness, substrate doping, and oxide charge at given gate bias [1]. With decreasing device geometry, the capacitances are also reduced. Therefore, this thesis aims to develop the hard- and software for a low-noise CV measurement unit that can measure the small capacitance at high resolution in the femtofarad (fF) range.

The main parts of the developed CV module are an ADA4530-1 that is used in a trans-impedance amplifier (TIA) configuration followed by an ADA2200 used as a lock-in amplifier. The output voltage of the lock-in stage is sampled by a 24-bit Delta-Sigma analog-to-digital converter (ADC) (ADS1247). After calibration, this voltage can be used for calculating the measured capacitance, as demonstrated in this work.

Kurzfassung

Der MOS Transistor zählt zu einem der wichtigsten Bestandteile in modernen elektronischen Schaltungen. Aufgrund der anhaltenden Miniaturisierung können mittlerweile selbst einzelne Defekte im Oxid bzw. Oxid-Halbleiter-Übergang, die Eigenschaften eines Bauteiles deutlich verändern. Es ist daher von großer Bedeutung diese Bauteile möglichst exakt charakterisieren zu können. Eine weitverbreitete Methode um MOSFETs charakterisieren zu können ist die Kapazitäts-Spannungs-Messung (engl. capacitance-voltage (CV) measurement). Das Ergebnis einer CV-Messung ist die Kapazität dargestellt in Abhängigkeit zu der Spannung. Diese Daten können verwendet werden um auf physikalische Eigenschaften des MOSFET, wie etwa Oxiddicke, Substratdotierungsprofil und Oxidladung, rückzuschließen. Je kleiner die physikalischen Strukturen der Transistoren werden desto kleiner wird auch die Kapazität, die gemessen werden muss. Ziel dieser Diplomarbeit ist die Entwicklung der Hard- und Software für eine rauscharme CV-Messeinheit. Diese muss selbst kleinste Kapazitäten mit einer Auflösung im Femtofaradbereich (fF) messen können.

Die Hauptkomponenten bilden ein ADA4530-1, der als Transimpedanzverstärker beschalten ist, gefolgt von einem ADA2200 als Lock-in Verstärker. Die Ausgangsspannung des Lock-in Verstärkers wird von einem 24-bit Delta-Sigma Analog-Digital-Wandler (ADS1247) digitalisiert und kann in eine entsprechende Kapazität umgerechnet werden. Nach erfolgter Kalibrierung kann mit der in dieser Arbeit entwickelten Hardware die Kapazität von Transistoren sehr präzise gemessen und ausgewertet werden.

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Acronyms

ADC analog-to-digital converter. iii, 12, 13, 17, 19, 21, 24, 29, 30, 31, 32, 34, 37, 38, 42, 55, 56
ASCII American Standard Code for Information Interchange. 30

BTI bias temperature instability. xvii, xviii, 6, 48

CET capacitance equivalent thickness. 5
CMOS complementary MOS. 17
CSV comma-separated values. 32
CV capacitance-voltage. iii, v, xi, xiii, 1, 5, 6, 7, 13, 16, 21, 24, 32, 34, 37, 38, 39, 42, 44, 45, 46, 47, 48, 49, 54, 55, 56

DAC digital-to-analog converter. 15, 17, 21, 24, 31
Dit interface defect state density. xiii, 37, 54
DLTS deep-level transient spectroscopy. 34, 55
DUT device under test. xi, xii, 6, 7, 8, 13, 14, 15, 16, 21, 37, 38, 39, 42, 45

EEPROM electrically erasable programmable read-only memory. 19, 24
EOT equivalent oxide thickness. 4
ESR electron spin resonance. 5

GBP gain bandwidth product. 19
GPIO general-purpose input/output. 24, 25, 26, 27

HTML hypertext markup language. 29

I^2C inter-integrated circuit. 17, 19, 21, 24, 27
IC integrated circuit. xii, 16, 17, 18, 19, 28, 56
IuE Institute for Microelectronics. 26, 55

JTAG Joint Test Action Group. 25

LED light-emitting diode. 24

MCU microcontroller unit. 17, 19, 24, 25, 26, 27, 28, 30, 32, 55
MIS metal-insulator semiconductor. 1
MOS metal oxide semiconductor. iii, xi, xvii, 1, 2, 3, 5, 6, 17, 42, 55
MOSFET MOS field-effect transistor. iii, xi, 1, 4, 5, 6, 26, 37, 42, 45, 48, 54
MSM measure-stress-measure. 37, 48, 54

NBTI negative BTI. 6

opamp operational amplifier. xii, 6, 13, 21

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PBTI positive BTI. 6
PCB printed circuit board. v, xii, 13, 14, 15, 16, 17, 21, 28, 30, 55
poly polycrystalline silicon. 42

SDRAM synchronous dynamic random-access memory. 24
SMT surface-mount technology. 57
SNR signal-to-noise ratio. xiii, 8, 34, 42, 45, 46, 47
SPI serial peripheral interface. 17, 19
SPS samples per second. 13, 42

THT through-hole technology. 57
TIA trans-impedance amplifier. iii, xii, xiii, 6, 13, 14, 16, 18, 19, 21, 26, 37, 38, 42, 45, 47, 55

UART universal asynchronous receiver transmitter. 27
USB universal serial bus. 24, 25, 27, 30, 55

VCP virtual COM port. 28, 30, 32

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Chapter 1

Introduction

Semiconducting materials are commonly used as substrates for a large set of modern electronic devices. A decisive advantage of devices fabricated on Si substrates is that they can be produced extremely miniaturized and exhibit a characteristic length of a few tens of nanometers. However, high quality interfaces between different layers, i.e. the interface between the substrate and the insulator, pose a challenge for the fabrication. Even though lots of research and development has been put into optimizing device manufacturing, a considerable number of defects at interfaces and oxide materials cannot be avoided. It has to be noted that the role of such defects gets more important in scaled transistor nodes. As a consequence of miniaturization, single defects can influence the performance of such devices. The capacitance-voltage (CV) measurement is one method for characterizing the energetic distribution of defects, but it also enables the estimation of the defect density. There are different measurement approaches to obtain the CV characteristic of a metal oxide semiconductor (MOS) structure. The CV measurement unit developed in this thesis is especially suitable for low-frequency CV measurements below 15 kHz. It is based on an auto-balancing bridge circuit in conjunction with a lock-in amplifier. As will be demonstrated, a measurement resolution down to several femtofarad can be achieved, which is beneficial for high-resolution CV measurements and deep-level transient spectroscopy investigations.

1.1 MIS/MOS capacitor

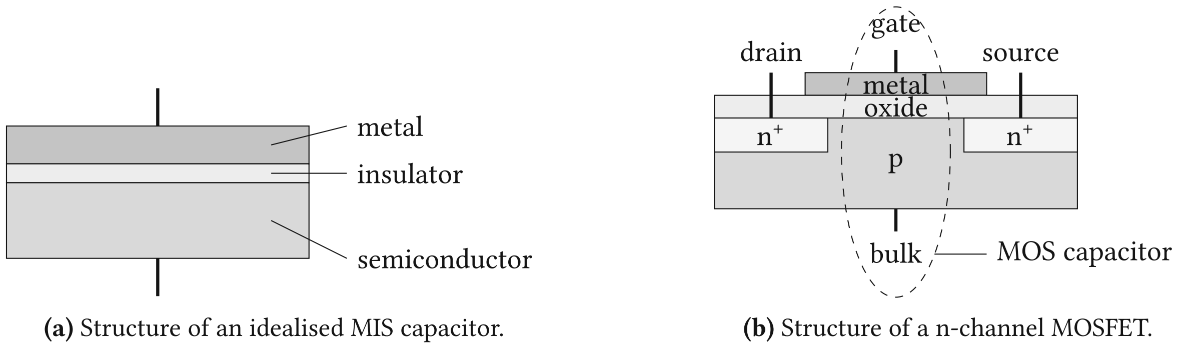
The structure of a metal-insulator semiconductor (MIS) capacitor is not used as a component in circuits, but it is an important device used to study semiconductor surfaces. These surface conditions are of great importance for nearly every semiconductor device because they are directly related to the reliability and stability of the operating of these devices [9, 10]. Therefore, this section contains a short introduction of the basic structure and the different operating ranges of the MIS capacitor.

Figure 1.1a shows the basic structure of an MIS capacitor. In the past, the most common configuration for an MIS capacitor was: metal for the gate, silicon dioxide (SiO_2) as an insulator, and silicon (Si) as a semiconductor. In modern devices, the metal gate was replaced with highly doped polysilicon. Although nowadays most transistors use polysilicon as the gate material, they are still called MOS devices.

The study of the MOS capacitor also helps to understand the physics of the MOS field-effect transistor (MOSFET), the most prominent device in modern electronics. The connection between the MOS capacitor and the MOSFET can be seen in fig. 1.1b.
There are three different operating regions of a MOS capacitor:

- accumulation
- depletion
- inversion

For these three regions and the flat band condition, the band diagrams of an idealized MOS capacitor are shown in fig. 1.2. The flat band condition occurs between accumulation and depletion. It is called



(a) Structure of an idealised MIS capacitor.

(b) Structure of a n-channel MOSFET.

Figure 1.1: Structure of a MOS capacitor (left) and a MOSFET (right). A MOS capacitor is formed between the gate and the bulk of the MOSFET.

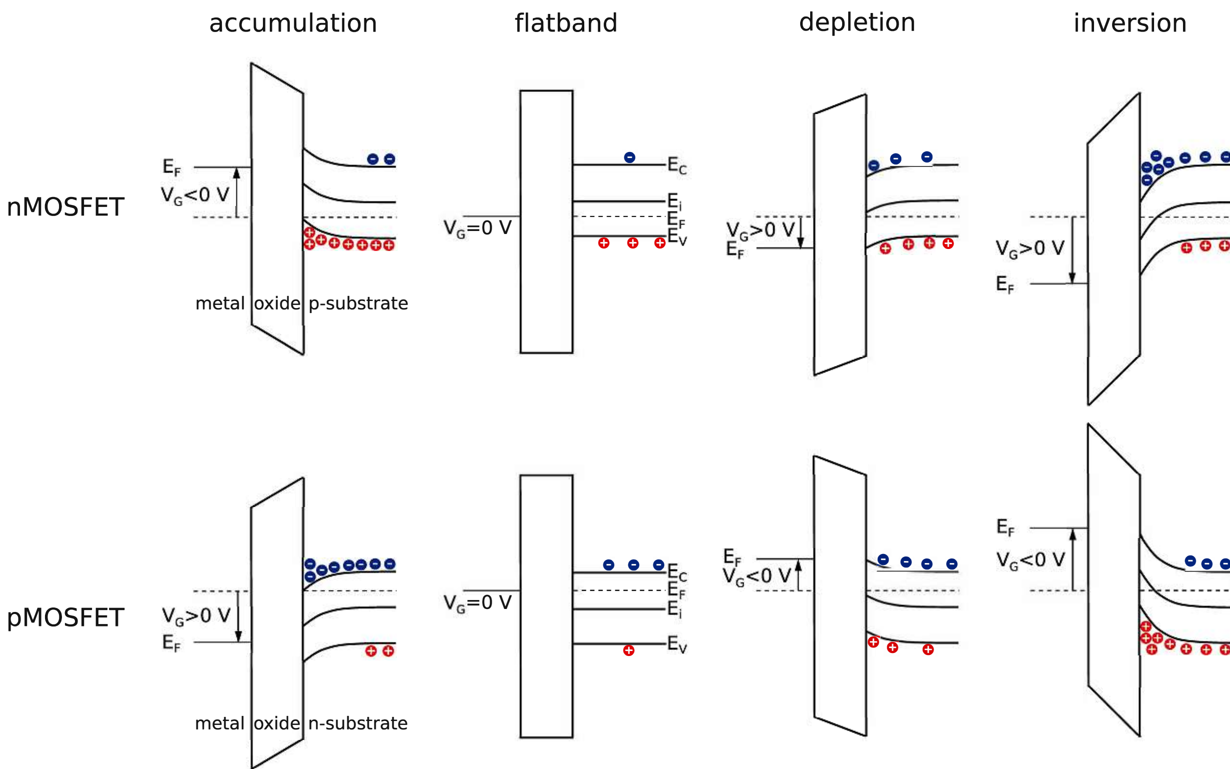


Figure 1.2: Energy band diagrams for an ideal MOS capacitor, taken from [2]. The work function of the metal and the semiconductor are the same. Therefore the flat band voltage $V_{FB} = 0\,\mathrm{V}$.

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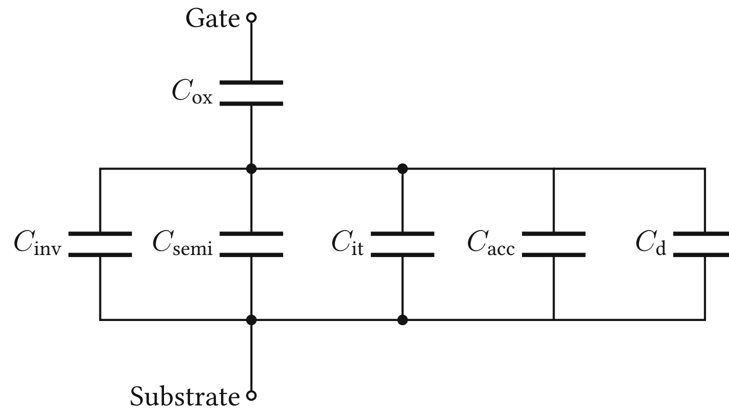

Figure 1.3: Simplified equivalent circuit for a MOS capacitor [1, p. 62].

a flat band because there is no band bending at the semiconductor/insulator junction. For the flat band condition, the surface potential Φ_s has to be zero volts. The surface potential is the difference between the intrinsic energy level at the surface (E_{i_int}) and the intrinsic energy level in the semiconductor (E_{i_semi}) [10]:

$$\Phi_s = \frac{E_{i_int} - E_{i_semi}}{q} \tag{1.1}$$

The external gate voltage V_G is calculated as the sum of the potential across the insulator V_i and the surface potential Φ_s:

$$V_G = V_i + \Phi_S \tag{1.2}$$

The potential across the insulator V_i is calculated with the total charge in the insulator Q_s and the oxide capacitance C_{ox} as:

$$V_i = \frac{|Q_s|}{C_{ox}} \tag{1.3}$$

For an idealized MOS capacitor with no oxide charges and the same work function for the metal and the semiconductor ($\phi_{ms} = 0$), the flat band voltage V_{FB} will be $0\,V$. A gate with another work function as the semiconductor will have a flat band voltage V_{FB} of greater or lower than $0\,V$ depending on the work function difference ϕ_{ms}. For example, if polysilicon is used as the gate material, the work function can be adjusted depending on the doping of the polysilicon. Figure 1.4 shows that a MOS capacitor with n-type polysilicon as gate and p-type silicon as bulk has a negative flat band voltage V_{FB}.

For an n-type MOS capacitor (p-type substrate) the semiconductor surface is heavily accumulated if the gate voltage is more negative than the flat band voltage (V_{fb}). The accumulation capacitance (C_{acc}) is very high compared to all other capacitance. The resulting total capacitance (C_m) is approximately equal to the gate dielectric capacitance (C_{ox}). The MOS capacitor is in the depletion region if the gate voltage is between the flat band (V_{fb}) and the threshold voltage (V_{th}). In this region, the total capacitance (C_m) will be the lowest. C_{ox} will be in series with the depletion capacitance (C_d) parallel to the interface state capacitance (C_{it}). For gate voltages higher than the threshold voltage (V_{th}) the MOS capacitor is in the inversion region. The total capacitance (C_m) will depend on the measurement frequency. For

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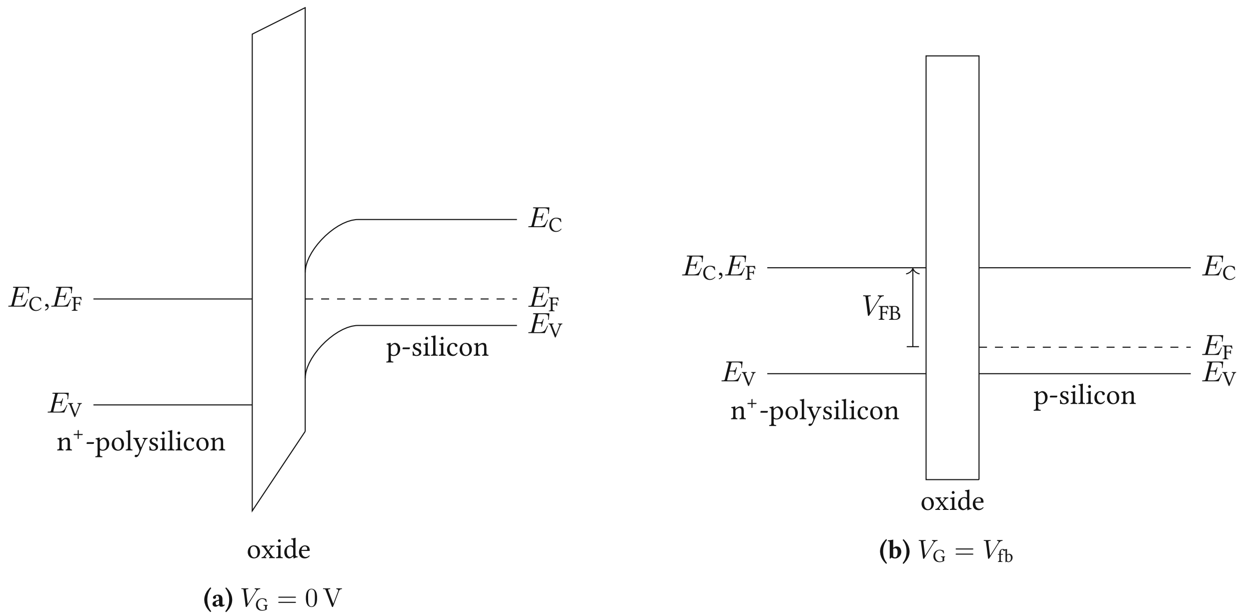

Figure 1.4: Band diagrams of an MOS capacitor with an n^+-polysilicon gate and a p-silicon semiconductor. Without an external gate voltage ($V_G = 0\,V$) there is band bending. To achieve the flat band condition, an external gate voltage that is equal to the flat band voltage V_{FB}, has to be applied.

low frequencies, the inversion layer capacitance (C_{inv}) is very high, and the total capacitance (C_m) is approximately C_{ox}. However, at high frequencies, the inversion layer charge can not follow the applied test signal, and therefore C_{inv} is lower.

The gate dielectric capacitance (C_{ox}) depends on the static dielectric constant of the insulator (ε_{ox}), the oxide thickness (C_{ox}), and the device gate area (A_g):

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} A_g \tag{1.4}$$

However eq. (1.4) assumes a homogeneous oxide thickness with a constant static dielectric constant over the full gate area. ε_{ox} is assumed to be $3.9\varepsilon_0$ for silicon dioxide. If the oxide thickness is calculated with this assumption, it is called equivalent oxide thickness (EOT) because the real dielectric constant could be different. Therefore, there will be a difference between the physical oxide thickness and the EOT.

1.2 Defects in field-effect transistors

During the manufacturing of a MOSFET the introduction of defects into the device cannot be avoided. These defects will negatively affect the performance of the device. Therefore, it is important to get a physical understanding of how they are created and what impact they will have during operation. Three different types of defects can be classified, depending on the physical location [3].

- Interface defects
- Oxide defects
- Semiconductor bulk defects

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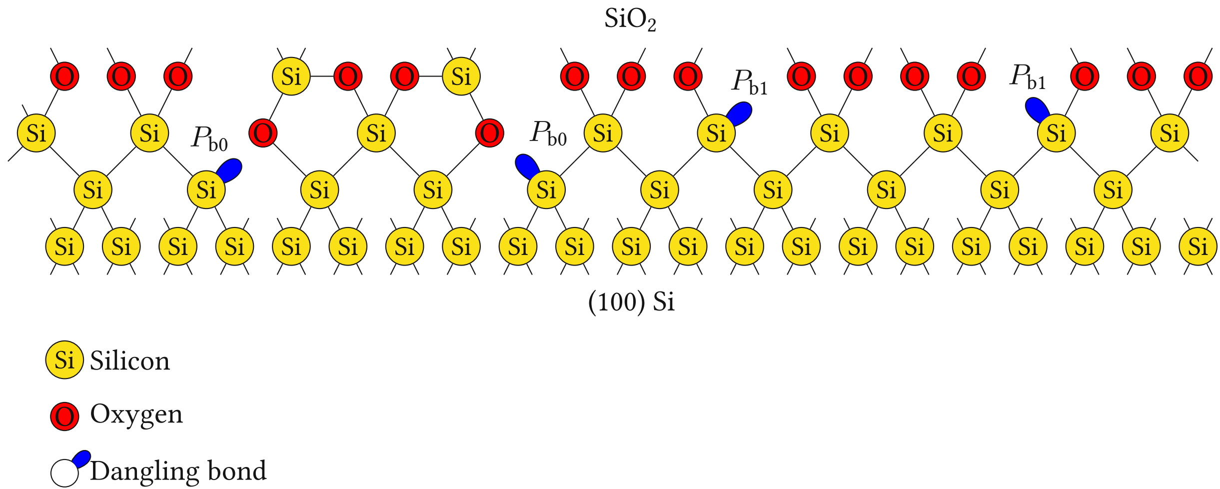

Figure 1.5: (100) Si-SiO_2 interface structure with deposition of P_{b0} and P_{b1} centers. Redrawn from [3]. Originally based on [4].

With the help of electron spin resonance (ESR) three distinct paramagnetic centers named P_a, P_b, and P_c can be found in Si-SiO_2 structures [11]. These three centers can be linked to trapped electrons in the oxide (P_a), trivalent Si centers in the oxide near the interface (P_b), and trapped holes in the Si (P_c) [4]. Figure 1.5 shows the P_{b0} and P_{b1} interface defects between Si and SiO_2.

1.3 CV characteristics of a transistor

The CV measurement can be used, among other things, for determining the oxide thickness, substrate doping and oxide charge of MOS transistors [1, p. 59]. During the CV measurement, the capacitance is measured while the gate bias voltage V_G is swept. For the measurement, a small AC signal ($\approx 100\,\text{mV}$) with a variable DC offset is applied to the gate of the MOSFET. The drain, source, and bulk of the MOSFET are connected to the ground. The AC current through the gate is measured and is used for calculating the capacitance. A typical result of a CV measurement is shown in fig. 1.6 (d).

In section 1.1 it was already shown in eq. (1.4), that the oxide capacitance (C_{ox}) is inversely proportional to the oxide thickness (t_{ox}). Equation (1.4) can be rearranged to calculate t_{ox} from C_{ox}, ε_{ox}, and A_g:

$$t_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} A_g \tag{1.5}$$

Normally ε_{ox} and A_g are known, and C_{ox} will be approximated from the CV curve at the accumulation region. For low measurement frequencies, the inversion region can also be used for approximating C_{ox}. If one of these values is used for calculating the oxide thickness, it is called capacitance equivalent thickness (CET). Because an approximation is used, there will be a difference to the real physical thickness [1].

The CV curve can also be used for determining substrate doping. For uniformly doped substrates the maximum-minimum capacitance technique can be used. For non-uniform doping concentrations, only the average doping concentration can be calculated [1]. With the maximum-minimum capacitance technique, the doping concentration can be approximated as:

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$$N_A \approx \frac{4(kT/q)\ln(N_A/n_i)}{q\varepsilon_{Si}A_G^2}\left(\frac{C_{min}}{1-(C_{min}/C_{ox})}\right) \tag{1.6}$$

1.4 Bias temperature instability

The bias temperature instability (BTI) phenomenon describes the generation of charge at a Si-SiO_2 interface or in the oxide if a strong electrical field is applied at the gate terminal of the transistor. The effect gets amplified if the device is held at an elevated temperature. This phenomenon was originally discovered and described in 1966 by Miura et. al [12]. BTI was in the past not a big concern, but because of the miniaturization of modern MOS transistors, BTI has become a significant reliability issue today [13–16]. If the gate voltage of a MOSFET is held constant under an elevated temperature, the performance will decrease over time because of BTI. This decrease in performance manifests in a shift of the threshold voltage V_{th} and a reduction of carrier mobility [17–20]. Figure 1.7 shows that these impacts are visible as changes in the CV characteristic. The interface traps will manifest in a stretch-out of the CV curve in the x-axis and a higher interface state capacitance C_{it} [21].

The BTI can be further classified in positive BTI (PBTI) and negative BTI (NBTI), depending on the polarity of the stress voltage. NBTI stress conditions applied to p-MOSFETs lead to the most degradation. Whereas PBTI on n-MOSFETs has practically no effect [20].

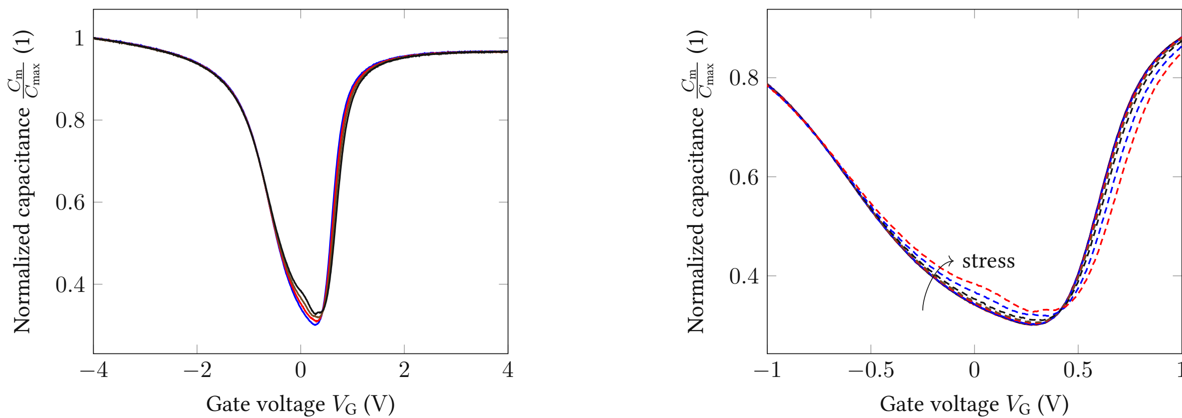

Figure 1.7: Change in the CV characteristic of an NMOS / NPOLY MOSFET because of BTI. The left diagram shows the full CV characteristic. The right diagram shows a detailed view of the change in capacitance due to an external stress voltage. A stretch-out in the x-axis and a higher interface state capacitance C_{it} can be observed. The longer the stress voltage is applied, the stronger these effects will be.

1.5 Auto-balancing bridge

An auto-balancing bridge can be used to indirectly measure the current through a DUT. A voltage signal is applied to one side of the DUT, and the other side has a virtual ground connection. This virtual ground could be achieved with an operational amplifier (opamp) in a trans-impedance amplifier (TIA) configuration. The difference voltage on the opamp inputs is near 0 V. So if the positive input of the opamp is connected to the ground, the negative input is virtual ground when a feedback resistor is

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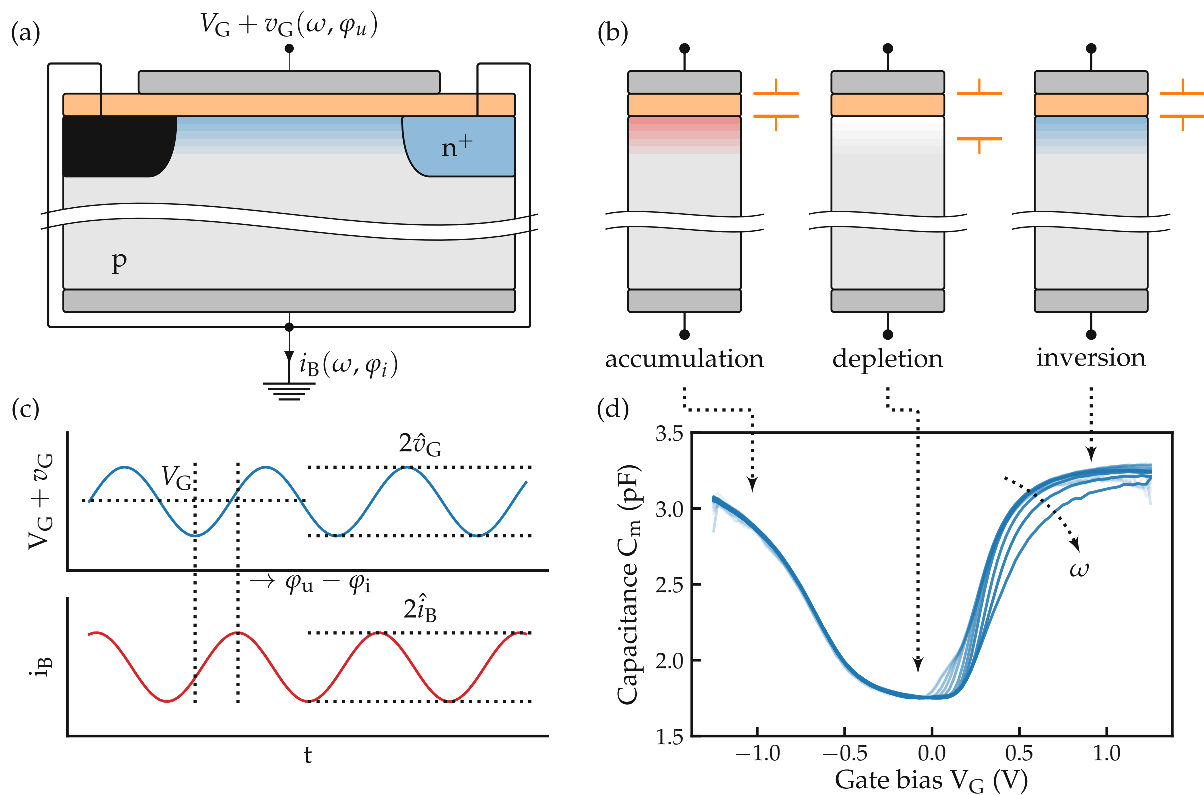

Figure 1.6: CV measurement. **(a)** the device under test (DUT) is connected for measurement. **(b)** DUT in the various operation schemes with illustrated equivalent capacitance. In the depletion regime, there are no free charges close to the interface. This can be interpreted as an increase in spacing between the plates of the equivalent capacitor. This, in turn, lowers the capacitance and gives the CV curve its characteristic shape. **(c)** Voltage and current signals during measurement. The phase and amplitudes of the voltage and current signals give the sought-after impedance. The offset voltage is swept in a staircase-like manner during the measurement. **(d)** Exemplary results of a CV measurement at multiple frequencies. The accumulation and inversion branches almost reach the oxide capacitance, while the capacitance in depletion is much lower. The inversion branch is generally steeper than the accumulation branch. Taken from [3].

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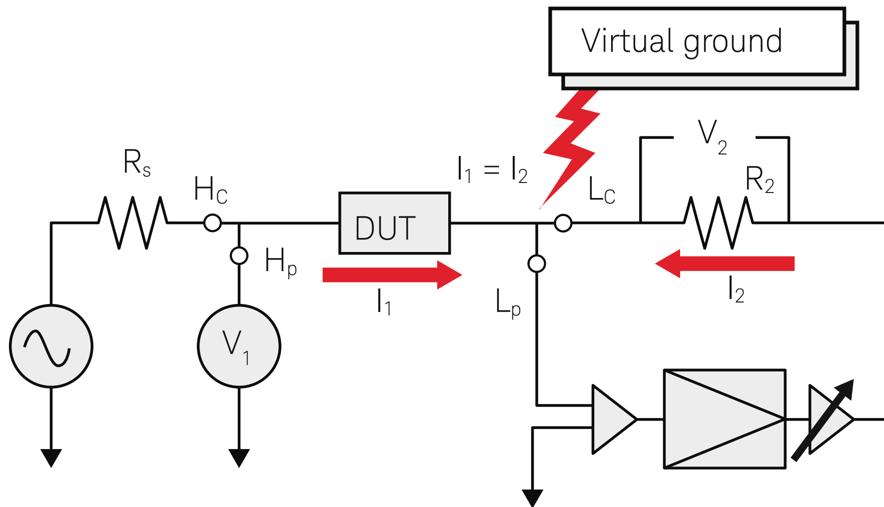

Figure 1.8: The auto-balancing bridge capacitance measurement method [5]. An excitation signal is applied to the H (high) terminal of the DUT. The L (low) terminal is virtual ground and is held at the ground through an error amplifier. The current I_1 thought the DUT is the same as the current I_2 through the feedback resistor R_2.

connected between the output and the negative input. In fig. 1.8 a simplified circuit of the auto-balancing bridge is shown. Equation (1.7) describes the connection between the output voltage of the bridge V_2 and the current through the DUT I_2. With eq. (1.8) the impedance can be calculated with the measured voltages V_1 and V_2 when R_2 is known. If the phase difference between the voltages is also measured, it is possible to calculate a complex impedance.

$$V_2 = I_2 R_2 \tag{1.7}$$

$$Z = \frac{V_1}{I_2} = \frac{V_1 R_2}{V_2} \tag{1.8}$$

1.6 Lock-in amplifier

A lock-in amplifier is a synchronous demodulator used to increase the signal-to-noise ratio (SNR) of a narrow bandwidth signal [6]. Figure 1.9 shows the basic principle of a dual-phase lock-in amplifier. The input signal gets multiplied by a reference signal with the same frequency. If two reference signals are used, 90 degrees out of phase, an in-phase and a quadrature signal can be extracted. This lock-in amplifier type is called a dual-phase lock-in amplifier. It can measure the input amplitude and the phase difference between the reference signal and the input at the same time.
The input signal without noise is assumed to be:

$$V_{IN}(t) = \hat{V}_{IN} \cdot sin(\omega \cdot t + \Phi) \tag{1.9}$$

The in-phase reference signal is:

$$V_{REF}(t) = \hat{V}_{REF} \cdot sin(\omega \cdot t) \tag{1.10}$$

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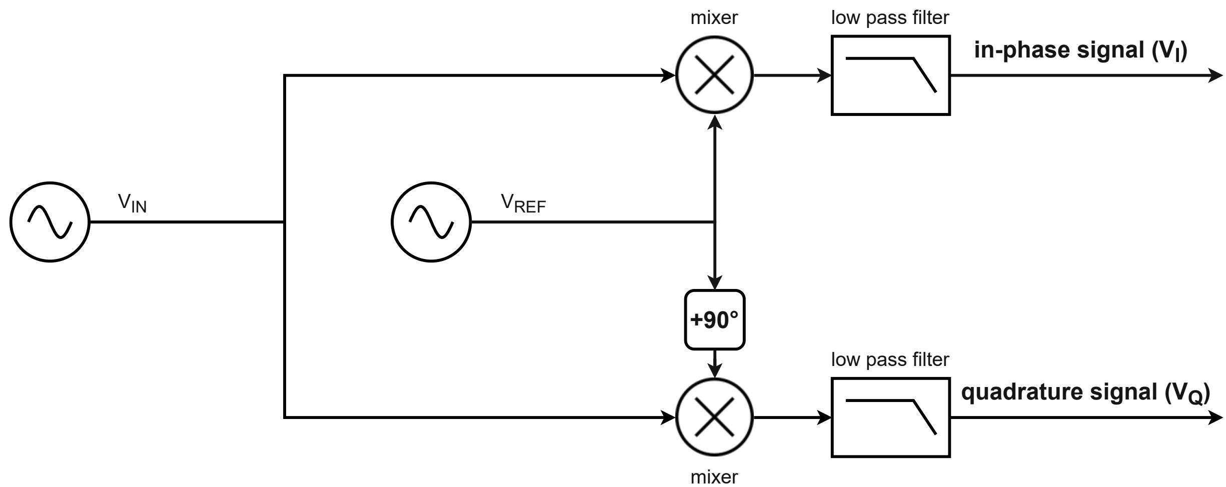

Figure 1.9: Block diagram of a dual-phase lock-in amplifier.

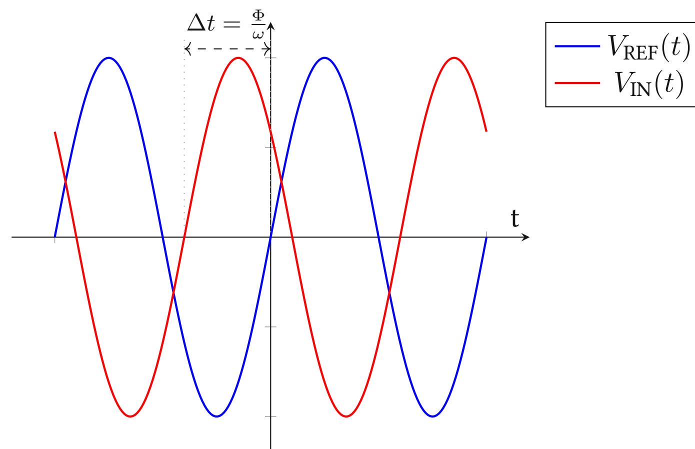

Figure 1.10: Phase difference between reference and input signal,

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The quadrature reference signal is the same as the in-phase reference signal but with a 90-degree phase shift:

$$V_{REF90}(t) = \hat{V}_{REF} \cdot cos(\omega \cdot t) \tag{1.11}$$

In fig. 1.10 the relation between the time difference Δt and the phase difference Φ between the input and the in-phase reference is shown.

The in-phase output is the multiplication of the input signal with the in-phase reference:

$$V_I(t) = V_{IN}(t) \cdot V_{REF}(t) = \frac{1}{2} \cdot (\hat{V}_{IN} \cdot \hat{V}_{REF} \cdot cos(\Phi) - \hat{V}_{IN} \cdot \hat{V}_{REF} \cdot sin(2 \cdot \omega \cdot t + \Phi)) \tag{1.12}$$

The quadrature output is the multiplication of the input signal with the quadrature reference:

$$V_Q(t) = V_{IN}(t) \cdot V_{REF90}(t) = \frac{1}{2} \cdot (\hat{V}_{IN} \cdot \hat{V}_{REF} \cdot sin(\Phi) + \hat{V}_{IN} \cdot \hat{V}_{REF} \cdot sin(2 \cdot \omega \cdot t + \Phi)) \tag{1.13}$$

The DC components of the output signals are:

$$V_I = \frac{1}{2} \cdot \hat{V}_{IN} \cdot \hat{V}_{REF} \cdot cos(\Phi) \tag{1.14}$$

$$V_Q = \frac{1}{2} \cdot \hat{V}_{IN} \cdot \hat{V}_{REF} \cdot sin(\Phi) \tag{1.15}$$

Equation (1.14) shows that if the input signal is in phase ($\Phi = 0°$) a DC voltage is present at the in-phase output (V_I) that is proportional to the amplitude of the input signal. In this case, according to eq. (1.15), the quadrature output will be zero. However, if the in-phase and quadrature signals are measured simultaneously, the amplitude of the input signal can be determined independently from its phase difference to the reference signal:

$$V = \sqrt{V_\mathrm{I}^2 + V_\mathrm{Q}^2} \tag{1.16}$$

With an in-phase and a quadrature signal, it is also possible to calculate the phase between the input signal and the reference:

$$\Phi = \arccos\left(\frac{V_\mathrm{Q}}{V}\right) = \arcsin\left(\frac{V_\mathrm{I}}{V}\right) \tag{1.17}$$

For synchronous demodulation, it is not necessary that the reference signal is sinusoidal. Many practical implementations of lock-in amplifiers use a square wave as a reference signal. This leads to the block diagram as seen in fig. 1.11. The benefit of this structure is that no analog multiplier circuit is needed. Instead of the analog multiplier, a simple switch can be used. The input, reference, and output signal can be seen at different phase differences in fig. 1.12. Figure 1.13 shows the mean value of the output of a switching multiplier lock-in amplifier as a function of the phase difference. At zero phase difference ($\phi = 0°$) between the reference and the input, the output is the same as for a normal rectifier. The mean value for a rectified sinusoidal signal is $\frac{2}{pi} \approx 0.64$ times the amplitude of the input signal. In fig. 1.13 this value can be seen at $\phi = 0°$

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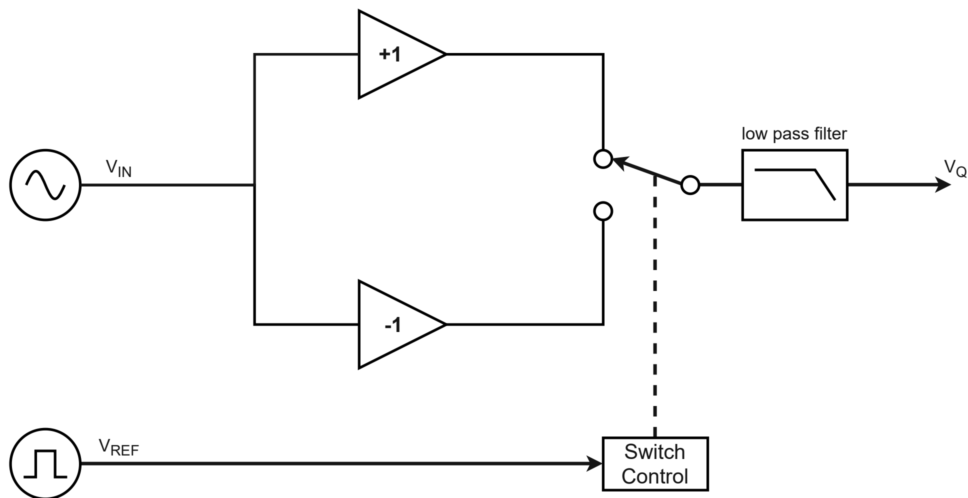
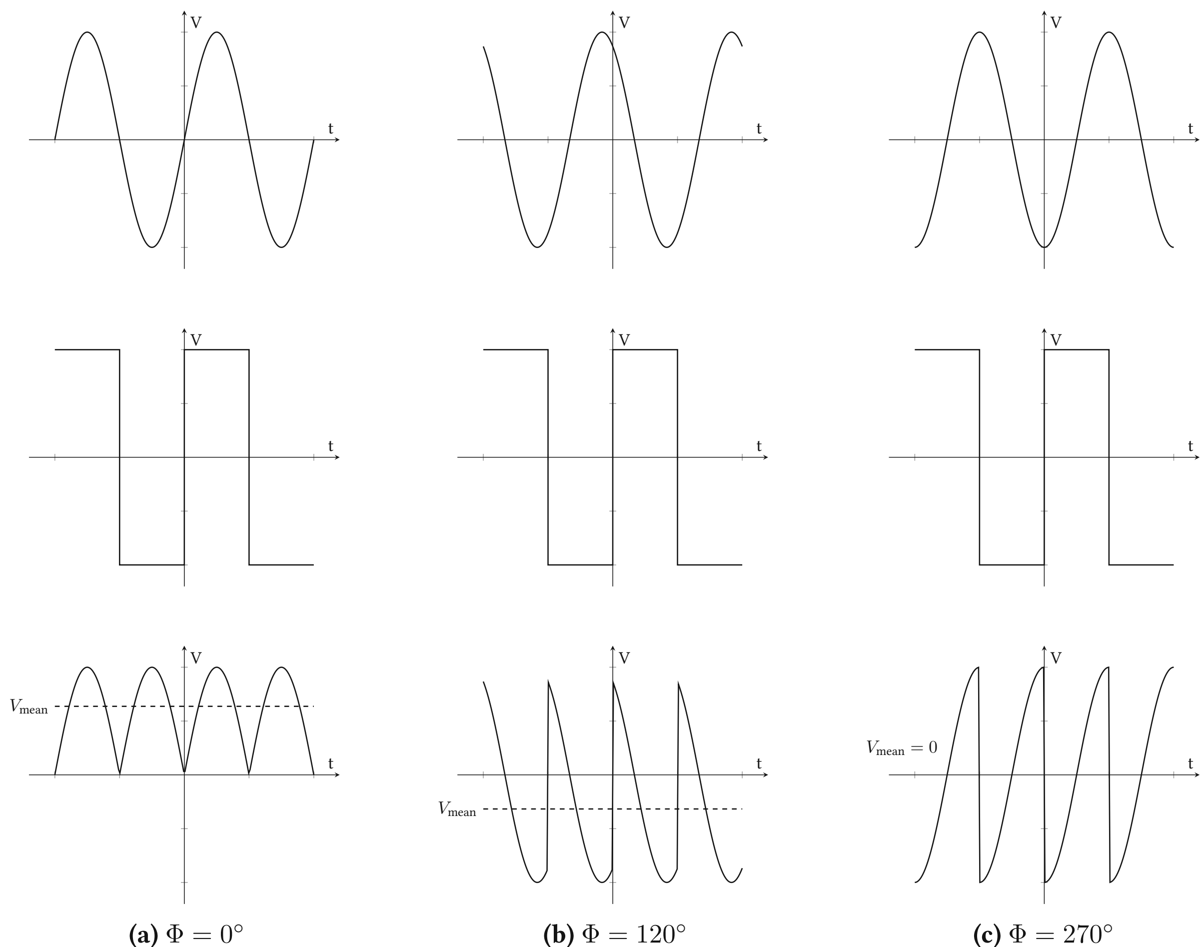


Figure 1.11: Block diagram of a switching multiplier lock-in amplifier. Modified from [6].



(a) $\Phi = 0°$ **(b)** $\Phi = 120°$ **(c)** $\Phi = 270°$

Figure 1.12: Input, reference, and output signal (from top to bottom) of a lock-In amplifier with a square wave as a reference at different phase angles (Φ) between input and reference. Modified from [6].

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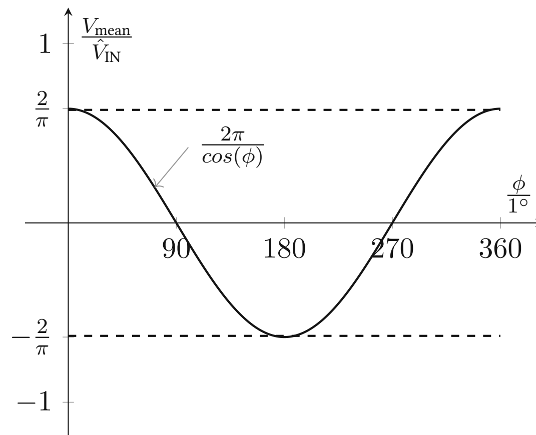

Figure 1.13: Mean output voltage V_{mean} of a synchronous rectifier, depending on the phase difference ϕ between the measured signal and the reference signal.

1.6.1 Digital lock-in amplifier

It is also possible to use a lock-in amplifier in the digital domain. The input signal has to be sampled with a high-speed analog-to-digital converter (ADC). The clock jitter needs to be very low. The demodulation and low-pass filtering can then happen entirely in the digital domain. However, the performance requirements for the clock signal and the ADC are more significant in comparison to an analog lock-in amplifier

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Chapter 2

Implementation

This chapter describes the implementation of the hard-, soft-, and firmware. The CV measurement module is in principle a capacitance meter with a a variable DC bias. There are multiple possible ways to implement a capacitance measurement device. In this thesis the current through the DUT is measured to determine the capacitance. The excitation voltage amplitude and frequency are known and fixed. With these values the impedance, and therefore the capacitance can be calculated. The current through the DUT is in the picoampere range, and can therefore not be directly measured with a shunt. Instead an active amplification is needed to raise the small signal to a useful level. The auto-balancing bridge concept, as described in section 1.5, is used to convert the small input current into a proportional output voltage. The practical implementation with an ADA4530-1 opamp is shown in section 2.2.5. To amplify the signal further a single-ended-to-differential amplifier is used. The implementation of the single-ended-to-differential amplifier is described in section 2.2.7. The two output signals are wired with coaxial cables from the TIA printed circuit board (PCB) to the lock-in PCB. The coaxial cabling and the differential signaling ensure a high immunity against external noise. It would be possible to directly connect this signal to an ADC to determine the amplitude. However, in this case the ADC sample frequency needs to be at least the double of the excitation frequency. In the end, the only important value for the current measurement is the amplitude of the fundamental wave. A lock-in amplifier, as described in section 1.6, can be used to get a DC signal which is proportional to the amplitude of the fundamental wave. All other frequency components, for example due to harmonics or noise, are attenuated. The output of the lock-in amplifier is a DC voltage. It can be measured at low sample rates and high resolutions. Therefore, as described in section 2.2.3, a 24-bit Sigma-Delta ADC is used at a sample rate of 5 samples per second (SPS).

2.1 Architecture

The CV measurement unit is implemented with two different plug-in units for a 19-inch rack according to EN 60297-3-101. The lock-in amplifier module contains a digital part as well as an analog part. The TIA module contains the highly-sensitive analog input circuitry. This physical separation ensures that no noise from the digital part can couple into the analog input circuitry. A bock diagram of both modules and the backplane is shown in fig. 2.1.

There are two possible ways of using the CV measurement unit. Either a two channel signal generator is used for generating two output signals that are phased locked. This signal path is shown in fig. 2.2a. Alternatively, as in fig. 2.2b shown, only a single square wave signal is used, and the excitation signal is generated internally in the CV measurement unit. This has the drawback that only two different measurement frequencies can be used because it is only possible to switch between two different low pass filters for the reference signal. Also, the excitation signal amplitude can only be changed if resistors are swapped on the PCB. An advantage of the internally generated excitation signal is that it is always perfectly phase-locked with the reference signal because it is directly derived from the reference signal.

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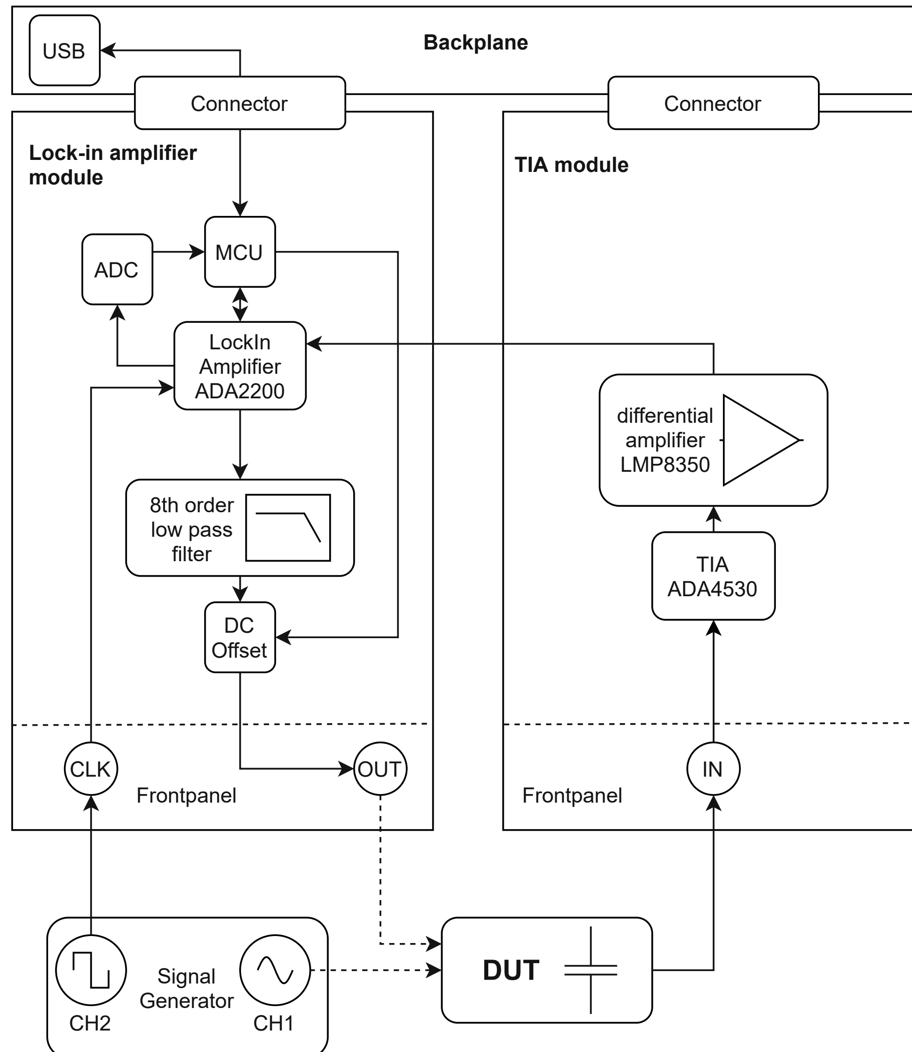
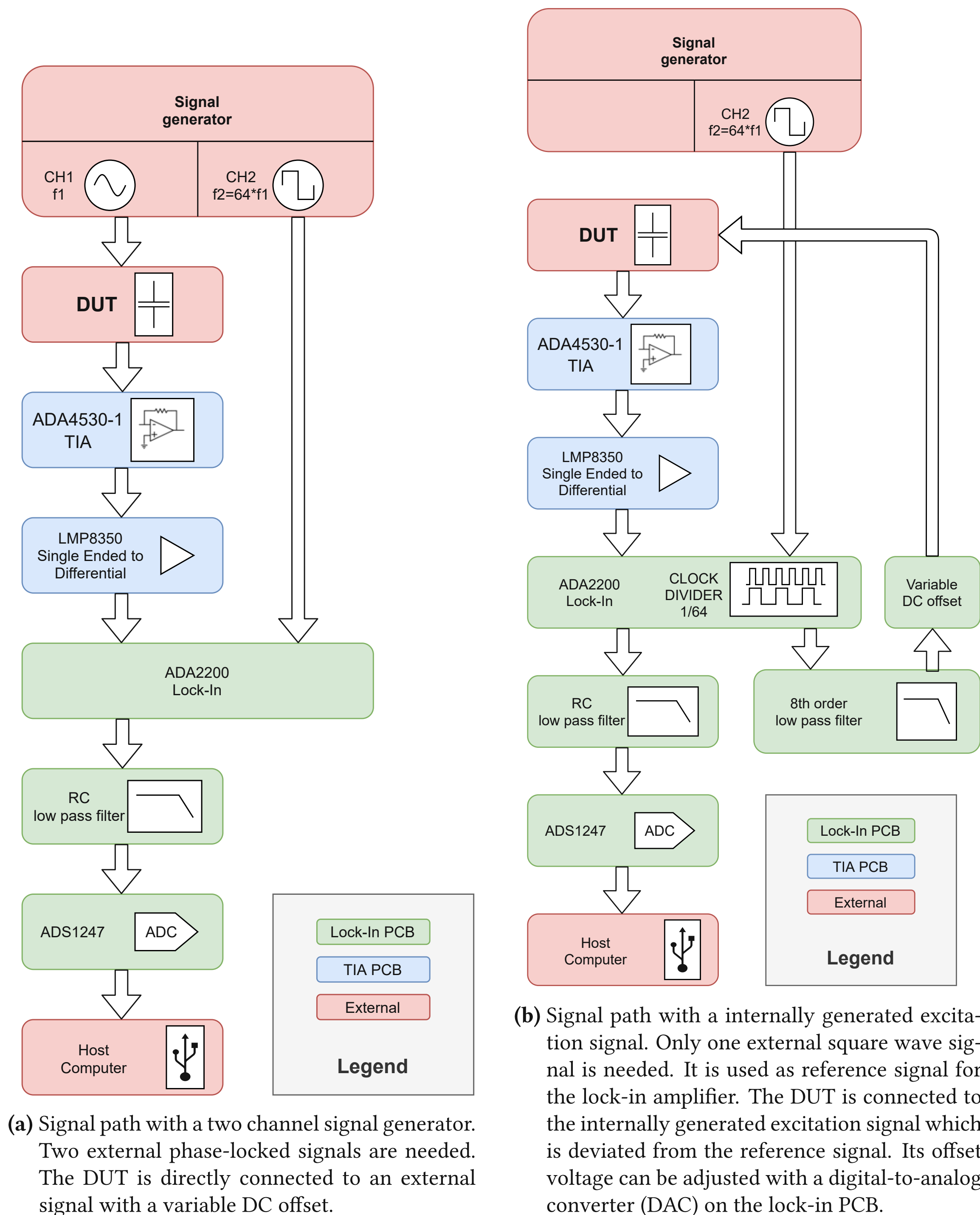


Figure 2.1: Block diagram of the lock-in amplifier module and the TIA module. It shows on which PCB each functional block is located. The dashed lines indicate that the DUT can be either excited by a signal generator, or by the internally generated output signal. For clarity, only the signal flow is indicated by arrows. Power supplies are not visible.



(a) Signal path with a two channel signal generator. Two external phase-locked signals are needed. The DUT is directly connected to an external signal with a variable DC offset.

(b) Signal path with a internally generated excitation signal. Only one external square wave signal is needed. It is used as reference signal for the lock-in amplifier. The DUT is connected to the internally generated excitation signal which is deviated from the reference signal. Its offset voltage can be adjusted with a digital-to-analog converter (DAC) on the lock-in PCB.

Figure 2.2: Signal path diagrams for internal and external excitation signal.

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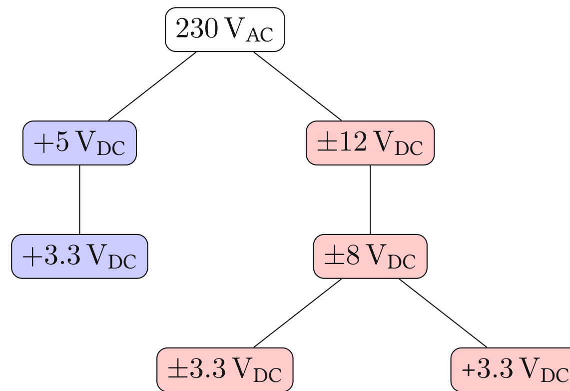

Figure 2.3: Dependencies between the different supply voltages. Voltages with a red background are for analog circuitry, and voltages with a blue background are for digital circuitry.

2.2 Hardware

2.2.1 Power supply

The whole rack is powered by 230 V mains voltage. Digital and analog circuitry have separate power supplies. The digital part used a 230 V to 5 V AC/DC plug-in module. On the lock-in PCB a UA78M33DCY linear regulator is used to convert the 5 V to 3.3 V. For the analog circuitry a 230 V to ±12 V AC/DC plug-in module is used. A low-noise converter plug-in module is used for stepping down the voltage further to ±8 V. On the lock-in PCB only +3.3 V are needed for the analog part. On the TIA PCB a bipolar ±3.3 V power supply is needed. These lower voltages are generated with a LT3045/LT3094 voltage regulator board on each PCB. In fig. 2.3 the dependencies between the different voltage supplies are shown. Table 2.1 shows the needed supply voltages for each integrated circuit (IC).

Table 2.1: Used supply voltages for the different parts.

Part	Reference designator	Supply voltages
ADA2200	N1	+3V3_A
ADA4530-1	U1	+3V3_A / -3V3_A
ADS1247IPW	U3	+3V3_A
CAT24C256SN	U15	+3V3
Display header	X2	+5V
LMP8350	N1	+3V3_A / -3V3_A
OPA2227D	IC5, IC6, IC11, IC12	+8V_A / -8V_A
PCA9600	U2	+5V / +3V3
STM32F746IGT6	U35	+3V3

2.2.2 Signal generator

The CV measurement unit requires two external signals from a signal generator if the connection scheme from fig. 2.2a is used. One sinusoidal signal is necessary as the excitation signal for the DUT. The other signal is needed as the reference for the lock-in amplifier. It should be a square wave with 64 times the frequency of the excitation signal. For this, a custom-developed signal generator provided by the Institute for Microelectronics, TU Wien, is used [22].

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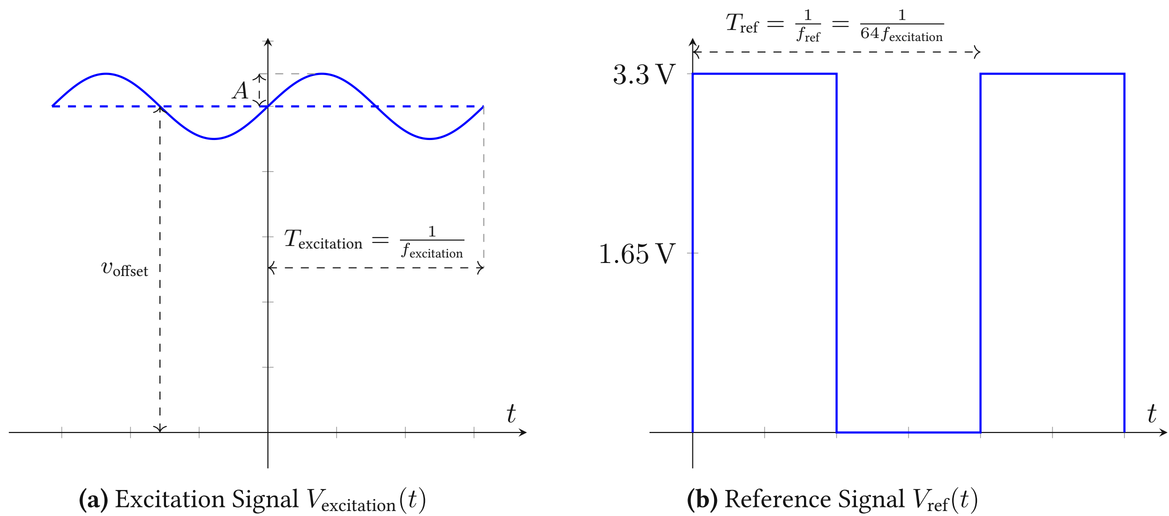

(a) Excitation Signal $V_{excitation}(t)$ **(b)** Reference Signal $V_{ref}(t)$

Figure 2.4: Description of the excitation and reference signal.

Figure 2.4a shows how the excitation signals should look like. The excitation signal can be described with:

$$V_{excitation}(t) = V_{offset} + Asin(2\pi f_{excitation}) \tag{2.1}$$

The reference signal is shown in fig. 2.4b. It is a simple 3.3 V complementary MOS (CMOS) signal, which can be described with:

$$V_{ref}(t) = 1.65\,\mathrm{V} + 1.65\,\mathrm{V} \cdot sgn(sin(2\pi f_{ref})) \tag{2.2}$$

2.2.3 ADS1247 24-bit ADC

The ADS1247 is a 24-bit Delta-Sigma ADC with an internal 2.048 V reference [23]. It gets configured through a serial peripheral interface (SPI). The SPI bus is only clocked at 843.75 kHz because of the bandwidth limitation of the used isolator ICs (see section 2.2.4). Although the ADS1247 has four channels, only one of them is used. The purpose of this ADC is to measure the DC output of the lock-in amplifier. The data ready signal of the ADC is connected to the microcontroller unit (MCU) and can issue an interrupt when a new measurement is ready.

2.2.4 Galvanic isolation

The digital and analog parts of the circuit a fully galvanic isolated from each other. This ensures that no noise from the digital part couples into the analog part. For unidirectional signals, ADUM1400AR isolators are used. This variant has a maximum allowed data rate of 1 Mbps according to the datasheet. For the bidirectional inter-integrated circuit (I^2C) signals between the MCU and the DAC the ADUM1250 isolator is used. The physical locations of the analog and digital parts on the lock-in PCB are shown in fig. 2.5.

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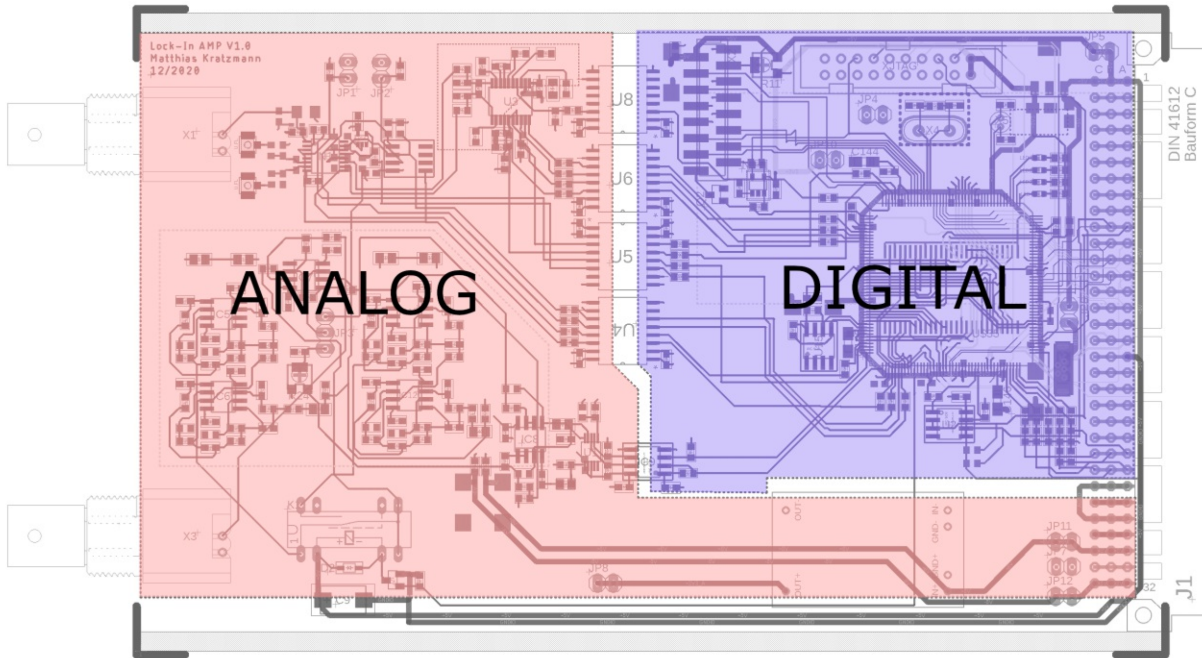

Figure 2.5: Analog and digital separation of the layout. The red part contains analog circuitry, like the ADA2200 lock-in amplifier, ADS1247 ADC, AD5693R DAC, and two 8th order low-pass filters. The STM32 MCU and its peripheral circuitry are part of the blue digital part. All signals between the analog and the digital part are separated with ADUM1400 or ADUM1250 isolator ICs.

2.2.5 ADA4530-1 TIA

The ADA4530-1 is a femtoampere input bias current electrometer amplifier. It can be used as an ultra-low noise TIA [24]. The circuit was mainly reused from the ADA4530-1R-EBZ-TIA evaluation board [25]. For the highly sensitive input path, a guard ring is used. For further reduction of external noise, a shielding case can be mounted. A schematic of the TIA circuit is shown in fig. 2.6. The relationship between input current and output voltage of the circuit is given by:

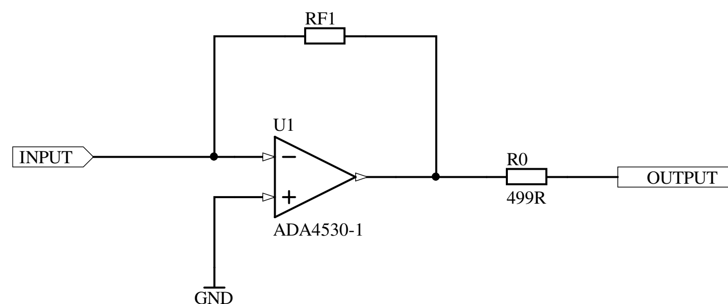

Figure 2.6: Simplified TIA circuit with the ADA4530-1.

$$V_{\text{OUT}} = -I_{\text{IN}} \cdot RF1 \tag{2.3}$$

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With the feedback resistor $RF1$ the gain can be adjusted. The bandwidth is limited by a gain bandwidth product (GBP) of 2 MHz.

2.2.6 ADA2200 lock-in amplifier

The ADA2200 is an IC for synchronous demodulation [7]. An internal block diagram of it is shown in fig. 2.7. It is used in a lock-in amplifier configuration in conjunction with the ADA4530-1 as a TIA. There are two possibilities for configuring the ADA2200. The configuration can be loaded from an external I^2C electrically erasable programmable read-only memory (EEPROM) on start-up. Or, it is loaded by the MCU via SPI. For more flexibility, the latter option is used.

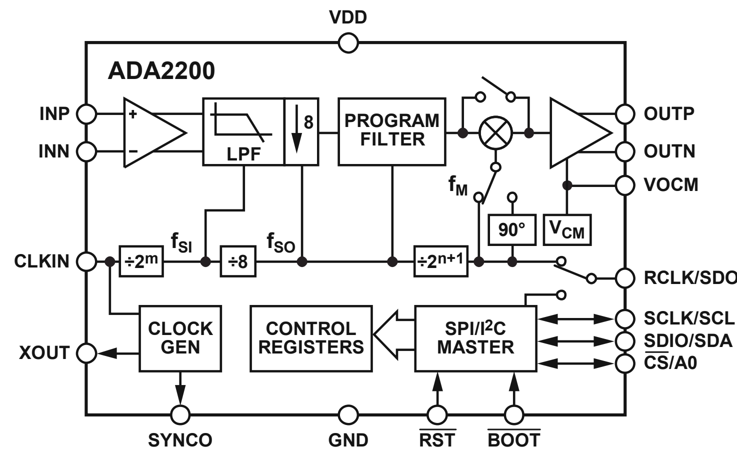

Figure 2.7: Internal block diagram of the ADA2200 [7].

The signal processing of the ADA2200 happens entirely in the analog domain. This has the benefit of no quantization noise or rounding errors. Internally charges are shared between capacitors for signal processing. The device features a time-discrete output signal which can be synced with an ADC. However this feature is not implemented yet. Instead, a low-pass filter is used and at the output to get a steady DC signal, and therefore no synchronization between ADA2200 and ADC is needed. The maximum allowed input clock frequency is 1 MHz. With an internal divider of 64, the maximum allowed excitation frequency is, therefore $\frac{1\,\mathrm{MHz}}{64} = 15.625\,\mathrm{kHz}$.

2.2.7 LMP8350 differential amplifier

The LMP8350 device is an ultra-low distortion fully differential amplifier designed for driving high-performance precision ADCs [8]. It is used for converting the single-ended output of the ADA4530-1 to a differential output for driving the ADA2200. Figure 2.8 shows the recommended circuit for using the LMP8350 as a single-ended-to-differential amplifier. The gain A_V was set to 1. $R_\mathrm{S} = 499\Omega$ is the output resistor of the TIA. The feedback resistors R_F are set to $1\,\mathrm{k}\Omega$. The two output resistors R_O keep the amplifier output stable when connected to the ADA2200 input, which input impedance is represented in fig. 2.8 with C_L and R_L. Equations (2.4) to (2.7) are from the datasheet and are used for calculating the needed resistor values in table 2.2.

$$R_\mathrm{M} = \frac{R_\mathrm{T} R_\mathrm{S}}{R_\mathrm{T} + R_\mathrm{S}} \tag{2.4}$$

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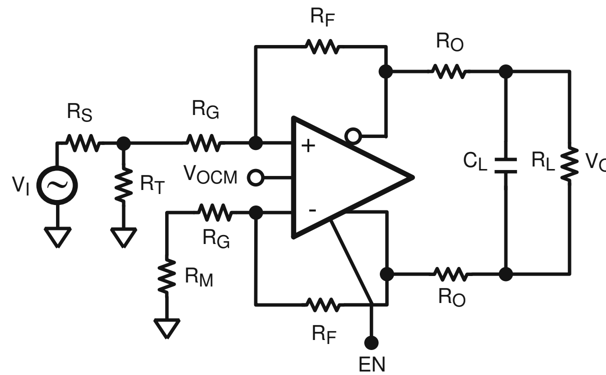

Figure 2.8: Recommended circuit for a single-ended-to-differential amplifier from the LMP8350 datasheet [8].

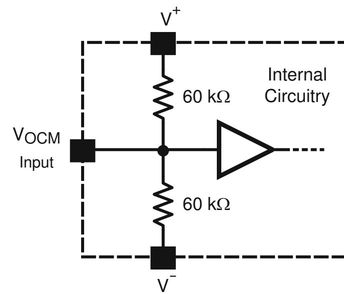

Figure 2.9: Internal bias circuit for the output common-mode voltage V_{OCM} of the LMP8350 [8].

$$R_{\mathrm{T}} = \frac{1}{(\frac{1}{R_{\mathrm{S}}} - \frac{1}{R_{\mathrm{IN}}})} \tag{2.5}$$

$$R_{\mathrm{IN}} = \frac{R_{\mathrm{G}}}{1 - (\frac{R_{\mathrm{F}}}{2\cdot(R_{\mathrm{F}}+R_{\mathrm{G}})})} \tag{2.6}$$

$$A_{\mathrm{V}} = 0.5\frac{R_{\mathrm{F}}}{R_{\mathrm{G}}} \tag{2.7}$$

Figure 2.9 shows the internal circuit for the output common-mode voltage of the LMP8350. Internally

Table 2.2: Calculated resistor values for LMP8350 single-ended-to-differential circuit.

Reference Designator	Calculated	Chosen
R_{S}	-	499 Ω
R_{T}	1667 Ω	1650 Ω
R_{G}	500 Ω	470 Ω
R_{F}	-	1000 Ω
R_{M}	384 Ω	383 Ω
R_{O}	-	10 Ω

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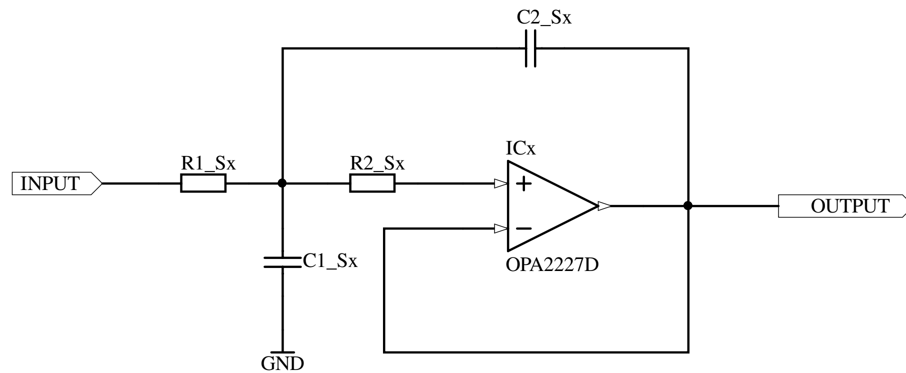

Figure 2.10: A single stage of a 2nd order Butterworth active low pass filter with an OPA2227D opamp. Four of these stages are cascaded to form the 8th order low pass filter.

the LMP8350 uses a resistor divider which sets $V_{OCM} = \frac{V^+ - V^-}{2}$ if the V_{OCM} input pin is left floating. The used supply voltage for the LMP8350 is $\pm 3.3\,\mathrm{V}$. The input common-mode voltage of the ADS1247 ADC should be half of the analog supply voltage. Therefore, the output common-mode voltage of the LMP8350 has been programmed to $1.65\,\mathrm{V}$. An external $30\,\mathrm{k\Omega}$ resistor between V^+ and the V_{OCM} input pin is used to shift the voltage up to $1.65\,\mathrm{V}$.

2.2.8 Internal excitation signal generation

The two low pass filters on the lock-in PCB are only needed if the excitation signal should be generated internally from the ADA2200 clock input. Each filter has a different cut-off frequency. A relais is used to select which filter is active.

The ADA2200 can generate a square wave which is in phase with the input clock signal but divided by 64. This signal is then filtered with an active low pass filter and can be used as an excitation signal for the DUT. Theoretically the square wave could be used directly as excitation signal and the harmonics are filtered out by the lock-in amplifier. However, in the case of a capacitive DUT, the harmonics would lead to a high current through it and the TIA output would clip. To prevent the clipping, a 8th order active Butterworth filter with OPA2227D opamps was implemented. The filtered signal has a fixed amplitude of around $60\,\mathrm{mV}$. For calculating the needed feedback network, the filter designer[1] from Texas Instruments was used. For implementing an 8th order active low pass filter, four stages of 2nd order Butterworth filters with a Sallen-Key topology were cascaded. As a reference, a single stage is shown in fig. 2.10. Table 2.3 shows the calculated component values for a filter with a cut-off frequency of $10\,\mathrm{kHz}$. Figure 2.13 shows the measured bode plot of the actual filter. The cut-off frequency is visible, as expected, at $10\,\mathrm{kHz}$ in the bode plot.

With the AD5693R 16-bit I²C DAC, the DC offset can be set. The DAC can only output voltages from $0\,\mathrm{V}$ to $2.5\,\mathrm{V}$. This voltage range is not suitable for CV measurements. Therefore, the opamp circuit in fig. 2.11 is used to shift the output range from $(0 \text{ to } 2.5)\,\mathrm{V}$ to $(-12 \text{ to } 12)\,\mathrm{V}$. The DC offset is subsequently added to the filtered reference signal, using an inverting summing amplifier, as shown in fig. 2.12. The output voltage can be calculated as:

[1] https://www.ti.com/design-resources/design-tools-simulation/filter-designer.html

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Table 2.3: Calculated resistor values for the 8th order active low pass filter.

Reference Designator	Value	Reference Designator	Value
R1_S1	10 kΩ	R1_S3	7.68 kΩ
R2_S1	21 kΩ	R2_S3	10 kΩ
C1_S1	1 nF	C1_S3	1 nF
C2_S1	1.2 nF	C2_S3	3.3 nF
R1_S2	10.7 kΩ	R1_S4	2.61 kΩ
R2_S2	15.8 kΩ	R2_S4	3.57 kΩ
C1_S2	1 nF	C1_S4	1 nF
C2_S2	1.5 nF	C2_S4	27 nF

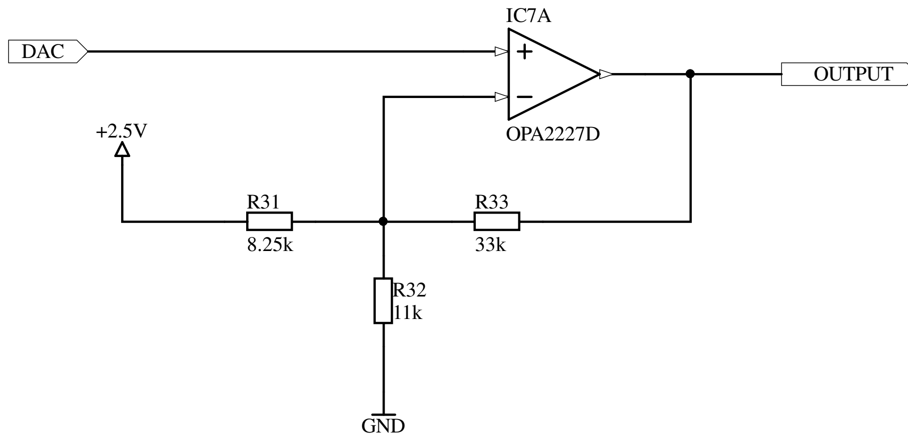

Figure 2.11: Voltage shifting circuit from (0 to 2.5) V to (−12 to 12) V.

$$V_{\text{OUT}} = (\frac{V_{\text{DC_OFFSET}}}{R25} + \frac{V_{\text{AC_SIGNAL}}}{R26}) \cdot (-R27) = -V_{\text{DC_OFFSET}} - 0.0409 V_{\text{AC_SIGNAL}} \tag{2.8}$$

The AC signal is generated from a low-pass filtered square wave with 3.3 V_{pp}. According to the Fourier series of a square wave function with an amplitude of one, the first harmonic has an amplitude of $\frac{4}{\pi}$. The amplitude of the first harmonic of the 3.3 V_{pp} input signal is:

$$A_{1\text{rst}} = \frac{3.3 \cdot 4}{2\pi} \text{V} \approx 2.1 \text{V} \tag{2.9}$$

With the factor 0.0409 from eq. (2.8) and the calculated amplitude of the first harmonic from eq. (2.9) the resulting excitation voltage is:

$$\hat{V}_{\text{excitation}} = 0.0409 \frac{3.3 \cdot 4}{2\pi\sqrt{2}} \text{V} \approx 60.7 \text{mV} \tag{2.10}$$

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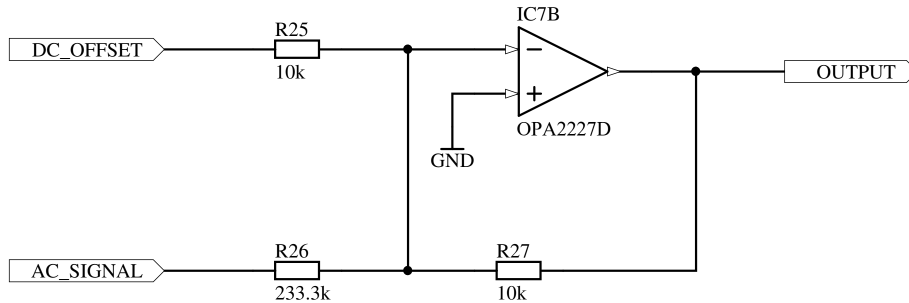

Figure 2.12: Inverting summing amplifier circuit. The AC_SIGNAL input is weighed with a factor of 0.0409.

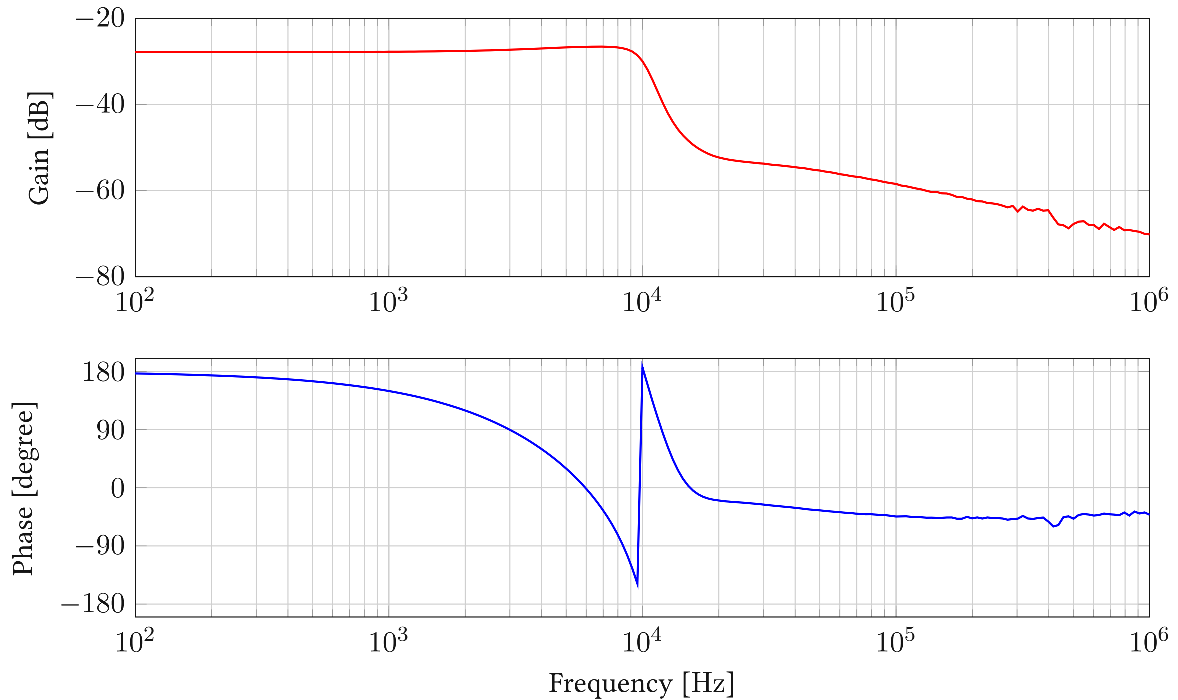

Figure 2.13: Measured Bode plot of the 8th order active Butterworth filter. The cut-off frquency is visible at 10 kHz.

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2.2.9 Microcontroller base system

The STM32F746 is used as the main controller for the CV measurement module. It controls the universal serial bus (USB) communication with the host computer and interacts as a bridge between the peripheral devices. For storage of settings, an I^2C EEPROM is used. An external 64 Mbit synchronous dynamic random-access memory (SDRAM) is connected to the MCU, but it is not yet used in the firmware. The mapping between general-purpose input/output (GPIO) pins and the on-board peripherals is shown in table 2.4.

Table 2.4: STM32F746 connection to the on-board peripherals.

Device	Peripheral	Signal	GPIO port
ADA2200 (lock-in)	SPI2	SDIO/SDA	PB15
		RCLK/SDO	PB14
		SCLK/SCL	PB13
	GPIO	$\overline{\text{CS}}$/A0	PB13
		ADA2200_$\overline{\text{RST}}$	PH7
		SYNCO	PH9
ADS1247 (ADC)	SPI1	ADC_SPI_SCLK	PA5
		ADC_SPI_MOSI	PA7
		ADC_SPI_MISO	PA6
	GPIO	ADC_SPI_$\overline{\text{CS}}$	PA4
		ADC_$\overline{\text{DRDY}}$	PA0
		ADC_START	PA1
		ADC_$\overline{\text{RST}}$	PA2
AD5693R (DAC)	I2C4	DAC_SCL	PH11
		DAC_SDA	PH12
Debug LEDs	GPIO	DBG_LED1	PE5
		DBG_LED2	PE4
		DBG_LED3	PE3
		DBG_LED4	PE2
CAT24C256SN (EEPROM)	I2C2	I2C2_SCL	PB10
		I2C2_SCL	PB11
relais	GPIO	SIGNAL_SWITCH	PD11

2.2.10 Debug interfaces

The lock-in board contains several different options for debugging the STM32F746 MCU.

Debug LEDs

Four green light-emitting diodes (LEDs) are connected to the GPIO pins of the MCU. These LEDs can be used for debugging purposes and are not visible if the lock-in board is in an enclosure.

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Table 2.5: Debug LEDs connection to the GPIOs of the MCU.

LED number / Signal name	GPIO port
DBG_LED1	PE5
DBG_LED2	PE4
DBG_LED3	PE3
DBG_LED4	PE2

Programming header

A standard 20-pin Joint Test Action Group (JTAG) header is used for programming the MCU. It is used for flashing the MCU with a STLINK/V2[2].

Table 2.6: Pinout of the 20-pin 2.54mm programming header XJTAG.

Pin number	ST-LINK/V2 signal	Board signal
1	Target VCC	+3V3
2	Target VCC	+3V3
3	JTAG TRST	NJTRST_PB4
4	GND	GNDIO
5	JTAG TDO	JTDI_PA15
6	GND	GNDIO
7	JTAG TMS, SW IO	JTMS-SWDIO_PA13
8	GND	GNDIO
9	JTAG TCK, SW CLK	JTMS-SWCLK_PA14
10	GND	GNDIO
11	Not connected	Not connected
12	GND	GNDIO
13	JTAG TDI, SWO	JTDO/TRACESWO_PB3
14	GND	GNDIO
15	NRST	PROC_RESET
16	GND	GNDIO
17	Not connected	Not connected
18	GND	GNDIO
19	VDD (3.3V)	Not connected
20	GND	GNDIO

Debug micro-USB connector

A micro-USB connector is populated on the lock-in board. It can be used to connect a host computer to the USB interface of the MCU in a standalone configuration. This connector should not be used if the lock-in board is connected to the backplane. Otherwise, the USB signals between the host computer and the USB switch on the backplane get short-circuited. The jumper JP6 connects the 5V supply of the lock-in board with the USB bus voltage of the connected host computer. It should never be populated if an external 5V supply, for example, through the backplane, is already connected to the board.

[2] https://www.st.com/en/development-tools/st-link-v2.html

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Display header

There is a 16-pin Micro-MaTch header for an external HD44780 compatible display on the lock-in board. It is only used for debugging purposes. It can be used for displaying status information during the development of the firmware. It is not necessary to connect any display to this connector during a measurement. The connection between the HD44780 compatible display and the MCU is shown in table 2.7. It is used in 4-bit mode. This reduces the number of GPIO pins that are needed between the display and the MCU. The read/write (R/W) signal is directly connected to the ground. Therefore only a unidirectional communication is possible. The drawback of this unidirectional connection is that there is no possibility to detect if a display is connected.

Table 2.7: Pinout of the 16-pin Micro-MaTch debug display header X2.

Micro-MaTch pin number	Display signal	Board signal	GPIO port
1	VSS	GNDIO	-
2	VDD	+5V	-
3	V0	Contrast voltage †	-
4	RS	LCD_RS	PH2
5	R/W	GNDIO	-
6	E	LCD_E	PH3
7	D0	GNDIO	-
8	D1	GNDIO	-
9	D2	GNDIO	-
10	D3	GNDIO	-
11	D4	LCD_D4	PC0
12	D5	LCD_D5	PC1
13	D6	LCD_D6	PC2
14	D7	LCD_D7	PC3
15	A	+5V	-
16	K	LCD_BL +	PH3

† Contrast voltage can be adjusted with the potentiometer R11.
+ LCD_BL controls the MOSFET Q2, which can connect the anode of the backlight to ground.

2.2.11 Backplane interface

The TIA board uses the backplane connector only for its power supply, whereas the lock-in board uses it for power and communication between other modules and the host computer. The backplane connector on the lock-in board follows the standard pinout at the Institute for Microelectronics (IuE) for plug-in modules. The signal connections of the backplane connector J1 are shown in table 2.8.

2.3 Firmware

The firmware for the STM32F476 was written in C. The PlatformIO[3] framework with VisualStudioCode[4] as editor was used during development. At startup, all peripherals get initialized. Afterward the MCU

[3] https://platformio.org
[4] https://code.visualstudio.com

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Table 2.8: Pinout of the lock-in board backplane connector J1.

Pin	Signal	GPIO port	Pin	Signal	GPIO port	Pin	Signal	GPIO port
A1	+5V	-	B1	+5V	-	C1	+5V	-
A2	GNDIO	-	B2	GNDIO	-	C2	GNDIO	-
A3	NC	-	B3	NC	-	C3	NC	-
A4	NC	-	B4	NC	-	C4	NC	-
A5	NC	-	B5	NC	-	C5	NC	-
A6	NC	-	B6	NC	-	C6	NC	-
A7	NC	-	B7	NC	-	C7	NC	-
A8	NC	-	B8	NC	-	C8	NC	-
A9	NC	-	B9	NC	-	C9	NC	-
A10	INT0_0	PC9⁺	B10	INT4_0⁺	PA8	C10	INT8	PG11
A11	INT1	PG6	B11	INT5	PG7	C11	INT8	PG11
A12	INT2	PG2	B12	INT6	PG9	C12	INT9	PG12
A13	INT3	PG3	B13	INT7	PG10	C13	INT10	PG13
A14	INT12	PF6	B14	INT13	PF7	C14	INT11	PG14
A15	INT15	PF9	B15	INT16	PF10	C15	GNDIO	-
A16	GNDIO	-	B16	GNDIO	-	C16	GNDIO	-
A17	USB_D_P	PA12	B17	USB_D_N	PA11	C17	GNDIO	-
A18	GNDIO	-	B18	GNDIO	-	C18	GNDIO	-
A19	NC	-	B19	NC	-	C19	NC	-
A20	NC	-	B20	GNDIO	-	C20	GNDIO	-
A21	NC	-	B21	NC	-	C21	NC	-
A22	NC	-	B22	NC	-	C22	NC	-
A23	NC	-	B23	NC	-	C23	NC	-
A24	LAYER0	PI1	B24	LAYER1	PI2	C24	ADDR0	PH13
A25	ADDR1	PH14	B25	ADDR2	PH15	C25	ADDR3	PI0
A26	AGND	-	B26	AGND	-	C26	AGND	-
A27	+48V	-	B27	+48V	-	C27	+48V	-
A28	AGND	-	B28	AGND	-	C28	AGND	-
A29	-48V	-	B29	-48V	-	C29	-48V	-
A30	+8V	-	B30	+8V	-	C30	+8V	-
A31	AGND	-	B31	AGND	-	C31	AGND	-
A32	-8V	-	B32	-8V	-	C32	-8V	-

⁺ The I^2C backplane signals are routed through a PCA9600 bus buffer to the MCU. (INT0_0 = I2C3_SDA, INT4_0 = I2C3_SCL)

waits in interrupt mode for incoming commands through USB. The program logic for measurements happens on a host computer which sends the commands to the MCU. This approach has the benefit that different measurement schemes can be implemented as Python scripts on the host computer without updating the MCU firmware.

2.3.1 Unit tests

Unit tests are a well-established workflow in software development for testing independent functional units of code. The PlatformIO framework supports unit tests for firmware. By default, it uses a universal

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asynchronous receiver transmitter (UART) as a communication channel for the STM32 MCUs. Because there is already a virtual COM port (VCP) for communication, PlatformIO has been configured to use this channel for unit tests. For running the unit test, a special firmware has to be compiled and flashed to the MCU. Then the test is executed on the board, and the results are communicated back to the host computer. The unit test can not only detect errors in the code but also hardware-related errors. For example, if there is no communication possible with a peripheral IC, the unit test for this IC will fail. So these tests will not only ensure that code changes will not break any functionality, but they will also be useful for detecting soldering errors in new PCBs early on.

```
$ platformio test
```

Listing 2.1: Command for running the unit tests.

```c
/* main function for unit tests */
int main()
{
        /* Reset of all peripherals, Initializes the Flash interface and
            the Systick. */
        HAL_Init();

        /* Configure the system clock (216MHz)*/
        SystemClock_Config();

        /* Initialize delay functions */
        TM_DELAY_Init();

        /* Initialize the LCD Display with 16 columns and 2 rows (1602) */
        TM_HD44780_Init(16, 2);
        TM_HD44780_Puts(0, 0, "   UNIT TEST    ");

        UNITY_BEGIN();

        /* 2 second delay needed for establishing connection */
        /* https://docs.platformio.org/en/latest/plus/unit-testing.html#
            workflow */
        Delayms(2000);

        DEBUG_PRINTF("Start Unit Test");

        RUN_TEST(test_eeprom);
        RUN_TEST(test_config);
        RUN_TEST(test_sdram);
        RUN_TEST(test_ada2200);
        RUN_TEST(test_ads1247);
        RUN_TEST(test_ad5693r);
        RUN_TEST(test_crc32);
        RUN_TEST(test_ads1247_burst);

        UNITY_END();

        TM_HD44780_Puts(0, 1, " ...FINISHED... ");

```


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```
38          while (1)
39          {
40          };
41  }
```

Listing 2.2: Main function for the unit test.

2.3.2 Doxygen comments

The firmware is documented with Doxygen comments. This allows for automatically generated code documentation. For generating the hypertext markup language (HTML) documentation files, it is only necessary to run doxygen in the root project directory. All generated files will be saved in the Doxygen folder.

```
1  $ doxygen
```

Listing 2.3: Command for generating the Doxygen documentation.

```
1  /**
2    * @brief  This function caclulates the CRC-32.
3    *
4    * @param[in] data Pointer to the data which is used for the CRC-32
         calculation.
5    * @param[in] len Number of bytes which will be processed.
6    * @retval CRC-32 checksum value
7    */
8  uint32_t crc32_caclulate(uint8_t *data, uint32_t len)
9  {
10 ...
```

Listing 2.4: Example of a Doxygen comment.

2.3.3 Burst measurements

For sampling the ADC as fast as possible, a burst measurement function is implemented in the firmware. Three static variables are used in the ads1247.c file.

sample_buffer is an 32 bit integer array that will store the 24 bit ADC samples.

number_of_samples is a unsigned 32 bit integer value. Its value define how many samples per burst will be measured.

sample_index is a unsigned 32 bit integer value. This variable keeps track of how many samples are already taken.

```
1  /* Internal variables */
2  static int32_t sample_buffer[ADS1247_BURST_MAX_BUFFER_SIZE] = {0};
3  static uint32_t number_of_samples = 100;
4  static uint32_t sample_index = 0;
```

Listing 2.5: Internal variables and their initialization values from ads1247.c.

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First, the buffer size has to be set with the `ads1247_burst_set_size` function. This will set the `number_of_samples` variable. Then a burst measurement can be started manually with the `ads1247_burst_start` function. This will set the ADS1247 into continuous mode and enable interrupts on the DRDY pin. Every time a new measurement is available, the DRDY pin will trigger an interrupt, and the `ads1247_interrupt_drdy_callback` function gets called. In the callback function, the latest ADC sample will be saved into the sample buffer. If all samples are saved into the buffer, the interrupt will be deactivated at the last call of the `ads1247_interrupt_drdy_callback` function. Another possibility to start a burst measurement is with an external interrupt. The Signal INT7 on the backplane connector J1 is connected to PG10 on the MCU. If this signal gets pulled low by an external module and the trigger was previously armed with the `trigger_arm` function, a burst measurement will be started just like `ads1247_burst_start` was called.

2.3.4 Commands

It is possible to interact with the MCU through a USB connection. Low-level register access to all peripherals on the lock-in PCB is granted through a VCP. The communication uses American Standard Code for Information Interchange (ASCII). Therefore it is possible to debug commands with a terminal program manually. A disadvantage is an overhead in communication compared to a binary protocol. However, this should not matter because nothing time-critical should depend on the transmission from the host to the MCU.

help

Prints a list with all available commands with a short description for each command.

Example:

Command	Return Value
help	"Available commands: ... "

log

Prints all debug messages in the log buffer.

Example:

Command	Return Value
log	every message that got printed with DEBUG_PRINTF

ada2200_reset

Resets the ADA2200. This will pull the reset pin of the ADA2200 low for 1 µs. Afterward there is another delay of 1 µs to ensure that the ADA2200 is ready again for new commands.

Example:

Command	Return Value
ada2200_reset	ada2200_reset

ads1247_reset

Resets the ADS1247. This will pull the reset pin of the ADA2200 low for 10 µs. Afterward there is another delay of 1000 µs to ensure that the ADS1247 is ready again for new commands.

Example:

Command	Return Value
ads1247_reset	ads1247_reset

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trigger_arm

Arms the trigger for burst measurements with the ADS1247. After the trigger is armed, a falling edge on INT7 will generate an interrupt, and the ADS1247 starts to sample.

Example:

Command	Return Value
trigger_arm	trigger_arm

trigger_disarm

Disarms the trigger for burst measurements with the ADS1247. After the trigger is disarmed, the INT7 signal is no longer monitored. No sampling will be started, even on a falling edge on the INT7 signal.

Example:

Command	Return Value
trigger_disarm	trigger_disarm

ads1247_read_data

Returns the latest ADC value. The signed 24-bit return value can be in the range from −8 388 608 to 8 388 607.

Example:

Command	Return Value
ads1247_read_data	1234

ad5693r_send_command

Sends a command to the AD5693R DAC. The first parameter is the command number (see AD5693R datasheet [26] for available commands). The second parameter is for additional data, such as the 16-bit output code for the WRITE_DAC command.

Example:

Command	Parameter	Return Value
ad5693r_send_command	48 0	command = 0x30 value = 0x0

ada2200_write_register

Writes into a register of the ADA2200. The first parameter is the register number (see ADA2200 datasheet [7] for available registers). The second parameter is the value that will be written into the register.

Example:

Command	Parameter	Return Value
ada2200_write_register	16 10	register = 0x10 value = 0xA

ads1247_write_register

Writes into a register of the ADS1247 ADC. The first parameter is the register number (see ADS1247 datasheet [23] for available registers). The second parameter is the value that will be written into the register.

Example:

Command	Parameter	Return Value
ads1247_write_register	16 10	register = 0x10 value = 0xA

ads1247_read_register

Reads from a register of the ADS1247 ADC. The first parameter is the register number (see ADS1247 datasheet [23] for available registers). The return value is the content of the register.

Example:

Command	Parameter	Return Value
ads1247_read_register	16	register = 0x10 = 0xA

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ads1247_send_command

Sends a command to the ADS1247 ADC. The first parameter is the command number (see ADS1247 datasheet [23] for available commands).

Example:

Command	Parameter	Return Value
ads1247_send_command	16	command = 0x10

ads1247_burst_set_size

Sets the number of samples per burst for the ADS1247. The number of samples should be set before a arm_trigger or start_burst command gets issued.

Example:

Command	Parameter	Return Value
ads1247_burst_set_size	16	command = 0x10

ads1247_burst_buffer_ready

Checks if the burst measurement of the ADS1247 is finished. After a burst measurement has been started, this command can periodically be polled to check if the burst measurement is completed or still ongoing. If the burst measurement is still ongoing, the return value will be "Busy!". If it is already finished, the return value will be "Ready!"

Example:

Command	Return Value
ads1247_burst_buffer_ready	Either "Ready!" or "Busy!"

ads1247_burst_get_buffer

Prints the last burst measurement result of the ADS1247. Before issuing this command, the result of the ads1247_burst_buffer_ready command should be checked. The return value will contain all signed 24-bit ADC values separated with newlines.

Example:

Command	Return Value
ads1247_burst_get_buffer	1234 \r\n 5678 \r\n ...

2.4 Software

For controlling the CV measurement through a host computer, a Python module was written. It communicated with the VCP of the MCU. It abstracts all communication at the register level away. So no knowledge of the register level is needed for using the Python module. The module is also responsible for the correct sequencing of commands.

2.4.1 CV measurement Python script

For CV measurements, the ADS1247 gets reset and configured. Then for each offset voltage, the signal generator gets configured accordingly. After the ADA2200 has been configured, the output of the signal generator will be enabled. Then a measurement with the ADS1247 ADC is taken. In the end, the signal generator gets deactivated, and all measurements are stored in a comma-separated values (CSV) file. The entire communication sequence between the host computer (Python script), the signal generator, and the CV module can be seen in fig. 2.14.

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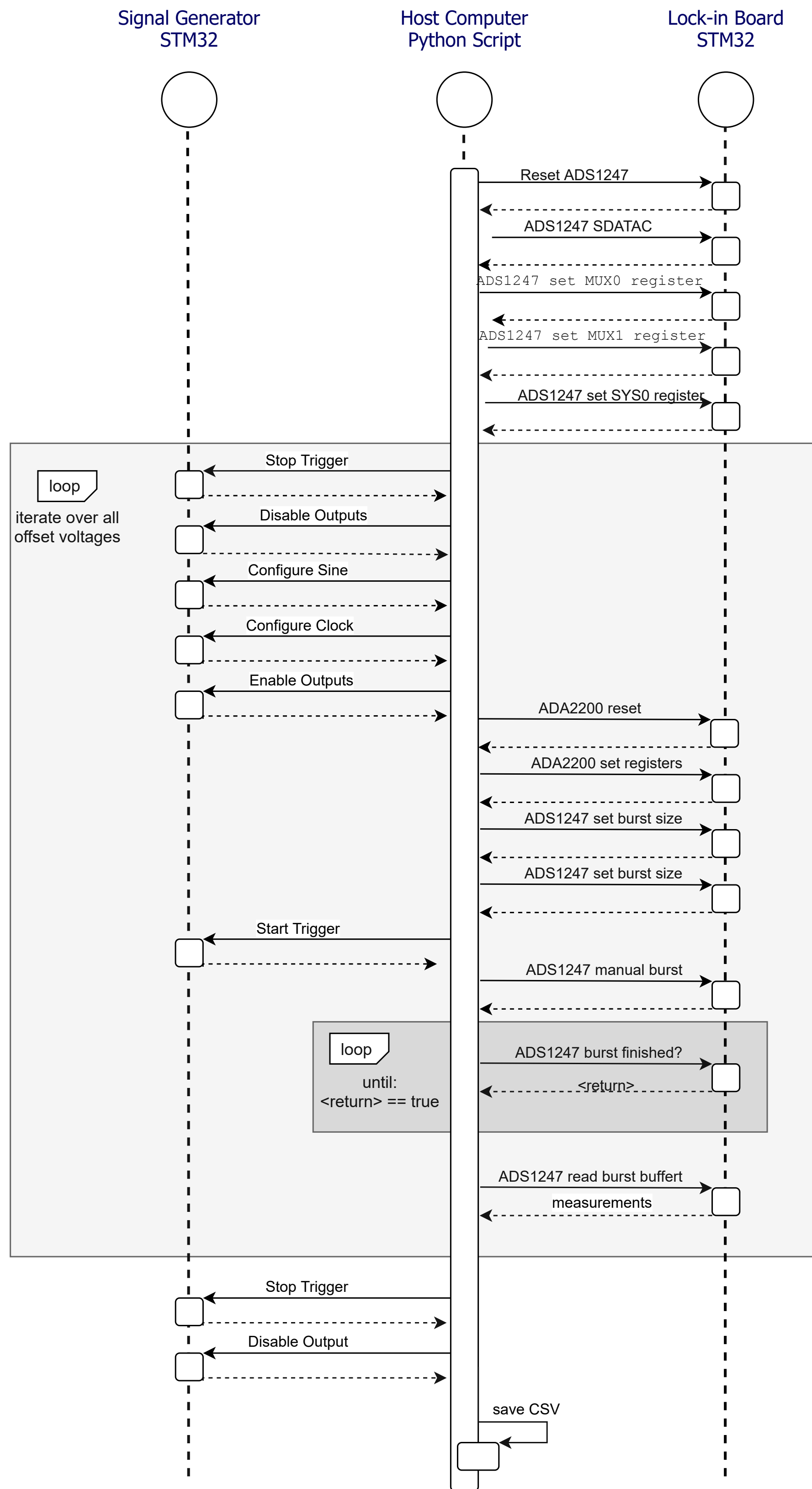

Figure 2.14: Sequence diagram of a CV measurement.

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2.4.2 DLTS measurement Python script

Although the hardware is optimized for CV measurements, it is also possible to use it for deep-level transient spectroscopy (DLTS) measurements. In contrast to the CV measurement, DLTS is a transient measurement and therefore needs a higher sample rate for the ADC. This leads to a reduced SNR, and therefore the capacitance uncertainty is higher. In fig. 2.15 the communication sequence for a DLTS measurement can be seen. This script was successfully tested for functionality, but no actual DLTS measurements were taken.

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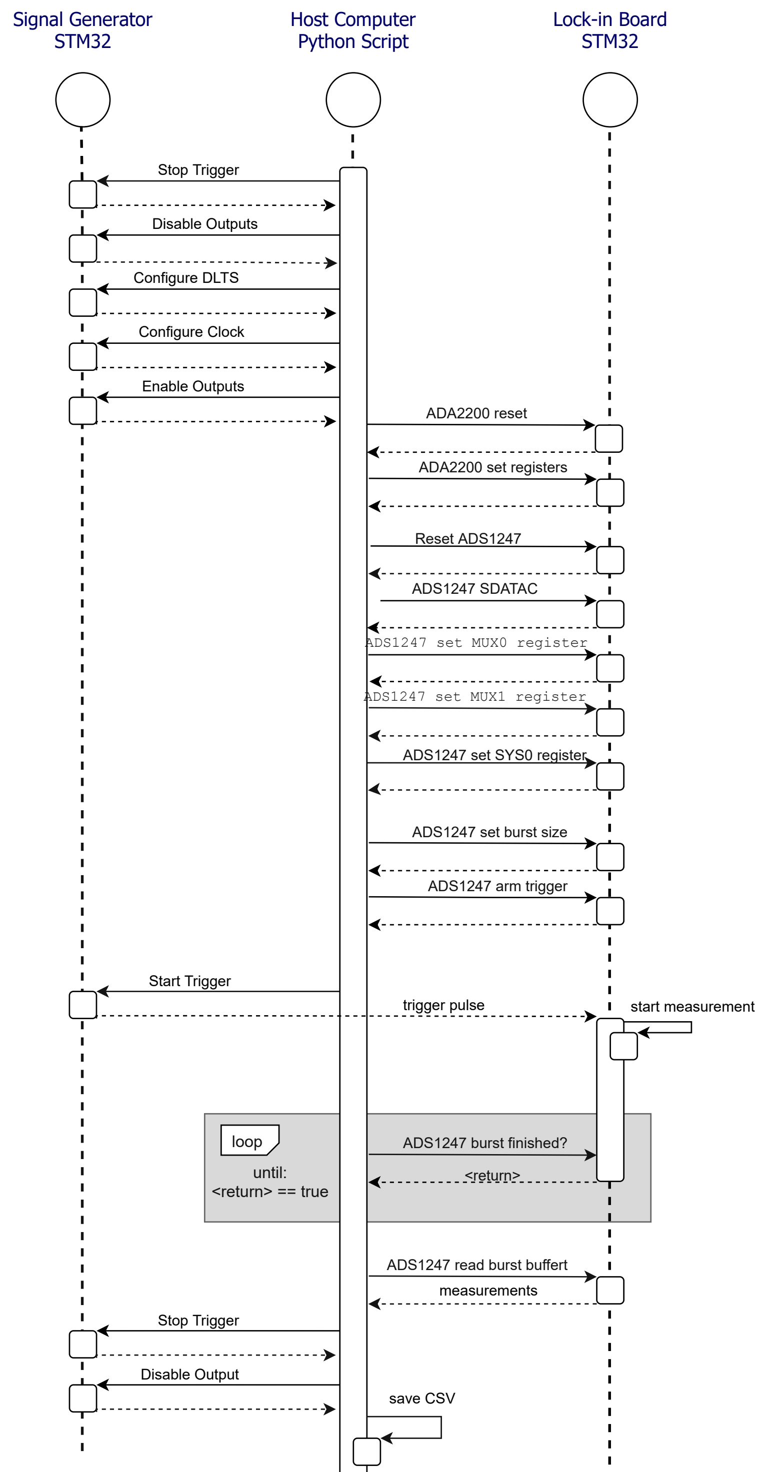

Figure 2.15: Sequence diagram of a DLTS measurement.

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Chapter 3

Measurement results

This chapter contains the calibration and characterization of the CV measurement module. The calibration procedure is described in section 3.1. For the characterisation of the CV measurement module the noise floor is measured in section 3.2 and the accuracy is determined in section 3.3. In section 3.4 different MOSFETs were measured to demonstrate the functionality of the CV measurement module based on real devices. Measure-stress-measure (MSM) results are shown in section 3.5 and are used to calculate a interface defect state density (Dit) plot.

3.1 Calibration

A calibration of the CV measurement module is needed to convert the measured ADC values to a corresponding capacitance.

There are several factors that introduce an offset error into the measurement. To name a few:

- ADA4530-1 (TIA) offset voltage
- LMP8350 (single-ended to differential amplifier) offset voltage
- ADA2200 (Lock-In amplifier) offset error
- ADS1247 (ADC) offset error
- the parasitic capacitance of the measurement setup (e.g. cabling)

It is challenging to characterize each offset error source independently. Therefore a much easier approach was taken. Three reference measurements have to be taken to be able to compensate for all these offset errors:

- Offset error measurement for determining the total offset error if no input signal is applied
- Zero capacitance measurement for determining the parasitic capacitance of the measurement setup
- Reference capacitance measurement for determining the conversion ratio between ADC values and the capacitance in Farad.

The offset error can be determined if no input signal is applied to the TIA. Ideally, the ADC should measure zero volts. The offset error of the ADA2200 can be different due to the PHASE90 bit in the Demod register. Therefore one reference measurement was taken with the PHASE90 bit reset (0) and one with the PHASE90 bit set (1). The average of 1610 measurements showed an ADC value of 61330 for PHASE90=0 and 59924 for PHASE90=1. This is equivalent to $14.97\,\mathrm{mV}$ and $14.63\,\mathrm{mV}$, respectively. The ADA2200 contributes the most to this error. According to its datasheet [7] the offset error with its inputs shorted can be as high as $\pm 39\,\mathrm{mV}$. So the measured values seem plausible.

The second reference measurement was taken with everything connected except the DUT. This measurement is used to determine the parasitic capacitance of the measurement setup as seen in fig. 3.1a. Again one measurement with PHASE90=0 and one with PHASE90=1 was taken.

For the third reference measurement, a capacitor with a known value is used as the DUT, as seen in fig. 3.1b. After these three calibrations the DUT can be connected, and the following measurements should be stored for later calculations.

- $ADC_{\text{zero-ph0}}$ =ADC value with PHASE90=0 without input signal
- $ADC_{\text{zero-ph90}}$ =ADC value with PHASE90=1 without input signal
- $ADC_{\text{setup-ph0}}$ =ADC value with PHASE90=0 with DUT disconnected
- $ADC_{\text{setup-ph90}}$ =ADC value with PHASE90=1 with DUT disconnected
- $ADC_{\text{ref-ph0}}$ =ADC value with PHASE90=0 with reference capacitor as DUT
- $ADC_{\text{ref-ph90}}$ =ADC value with PHASE90=1 with reference capacitor as DUT
- $ADC_{\text{DUT-ph0}}$ =ADC value with PHASE90=0 with real DUT connected
- $ADC_{\text{DUT-ph90}}$ =ADC value with PHASE90=1 with real DUT connected

If the DUT is purely capacitive, the capacitance of the DUT can finally be calculated as:

$$\begin{aligned} C_{\text{DUT}} = & \\ & \frac{C_{\text{ref}}}{\sqrt{ADC^2_{\text{ref-ph0}} + ADC^2_{\text{ref-ph90}}}} \\ & * \left(\sqrt{(ADC_{\text{DUT-ph0}} - ADC_{\text{zero-ph0}})^2 + (ADC_{\text{DUT-ph90}} - ADC_{\text{zero-ph90}})^2} \right. \\ & \left. - \sqrt{(ADC_{\text{setup-ph0}} - ADC_{\text{zero-ph0}})^2 + (ADC_{\text{setup-ph90}} - ADC_{\text{zero-ph90}})^2} \right) \end{aligned} \tag{3.1}$$

Each pair of measurements with PHASE90=0 and PHASE90=1 can be interpreted as a complex number:

$$ADC_{\text{X}} = ADC_{\text{X-ph0}} + j \cdot ADC_{\text{X-ph90}} \tag{3.2}$$

With eq. (3.2), eq. (3.1) can be simplified to:

$$C_{\text{DUT}} = \frac{C_{\text{ref}}}{|ADC_{\text{ref}}|}(|ADC_{\text{dut}} - ADC_{\text{zero}}| - |ADC_{\text{setup}} - ADC_{\text{zero}}|) \tag{3.3}$$

3.2 Noise

To characterize the noise floor of the CV measurement module, a DUT with a known resistance was used. Generally, the noise of the measurements depends on:

- measurement frequency
- the amplitude of the excitation signal
- feedback resistor of the TIA circuit
- shielding against external interferences

The capacitance of the DUT is measured indirectly. According to eqs. (3.4) and (3.5), the current is proportional to the capacitance if a sinusoidal voltage is applied. So the noise in the measured current is directly proportional to uncertainty in the capacitance.

$$Z_{\text{C}} = \frac{1}{j\omega C} \tag{3.4}$$

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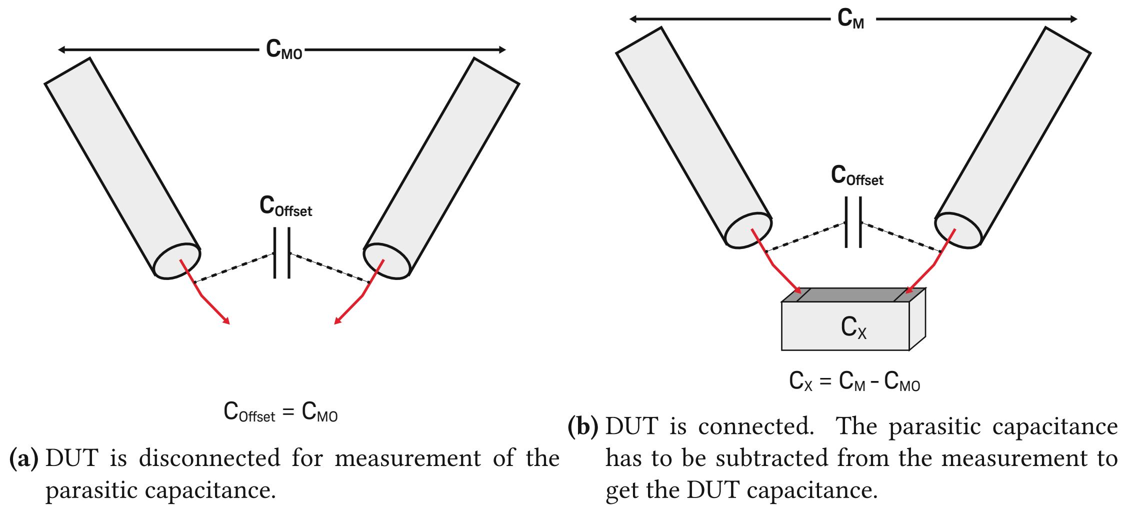

(a) DUT is disconnected for measurement of the parasitic capacitance.

(b) DUT is connected. The parasitic capacitance has to be subtracted from the measurement to get the DUT capacitance.

Figure 3.1: Offset measurement. Taken from [5].

$$V = ZI \tag{3.5}$$

For the characterization of the noise, a $1\,\mathrm{M\Omega}$ (measured: $998\,\mathrm{k\Omega}$) resistor was used as the DUT. The input voltage was measured at $V_{\mathrm{IN}} = 101.1\,\mathrm{mV_{RMS}}$ at a frequency of $10\,986.328\,\mathrm{Hz}$. The expected current is $I = 101.3\,\mathrm{nA}$. This current was subtracted from the measurement to get ΔI_{IN}. The current noise can be converted into an equivalent capacitance measurement uncertainty for a specific frequency:

$$C = \frac{I}{\omega V} \tag{3.6}$$

The current and capacitance noise is shown in fig. 3.2 with 1000 samples at unchanged conditions with a standard deviation of $534.4\,\mathrm{pA}$ or $76.6\,\mathrm{fF}$.

3.3 Accuracy

For determining the accuracy of the CV measurement module, a capacitor with a known value was used as DUT ($C = 47\,\mathrm{pF}$). Multiple capacitance measurements were taken at different frequencies. Table 3.1 shows the deviation in capacitance for different frequencies. The standard deviation of the measured capacitance decreases when the measurement frequency is increased. This means that at higher frequencies, the measurement accuracy is higher. The decrease in accuracy at lower frequencies can be explained by the measurement principle. The current is used to determine the capacitance of the DUT. This current decreases at lower frequencies. This leads to a greater impact on the measured capacitance if the current measurement uncertainty stays constant. The histograms in fig. 3.4 show the comparison between two different excitation frequencies. In fig. 3.3 the relation between the excitation frequency and the standard deviation of the measured capacitance is shown. It is clearly visible that the uncertainty is lower at higher excitation frequencies because the standard deviation of the measured current is nearly constant.

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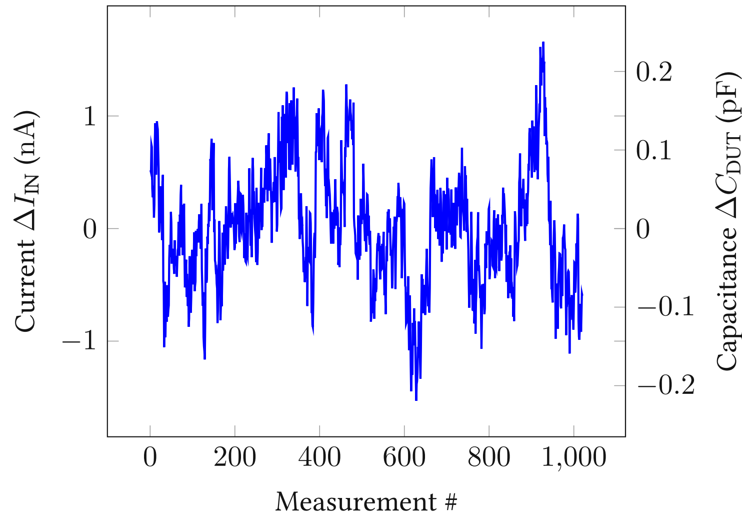

Figure 3.2: Noise measurement @ $f_{\mathrm{excitation}} = 10\,986.328\,\mathrm{Hz}$ with $R_{\mathrm{DUT}} = 998\,\mathrm{k\Omega}$ and $RF1 = 330\,\mathrm{k\Omega}$. The left y-axis shows the measured current error ΔI_{IN}. The right y-axis shows the equivalent capacitance error ΔC_{DUT}. The standard deviation of the measurement is $534.4\,\mathrm{pA}$ or $76.6\,\mathrm{fF}$.

Table 3.1: Standard deviation of the measured capacitance and current at different excitation frequencies. The mean value of the current standard deviation is $137.8\,\mathrm{pA}$.

$f_{\mathrm{excitation}}$ (Hz)	f_{clock} (Hz)	C_{mean} (pF)	C_{min} (pF)	C_{max} (pF)	$C_{\mathrm{std.deviation}}$ (pF)	$I_{\mathrm{std.deviation}}$ (pA)
85.8307	5493.1641	46.7875	43.6813	50.8426	1.1182	60.9646
171.6614	10986.3281	46.1445	39.8716	54.9986	2.7994	305.2574
343.3228	21972.6562	47.0169	46.1503	47.8548	0.3128	68.2146
686.6455	43945.3125	47.0776	46.3191	47.9021	0.3063	133.6202
1373.291	87890.625	47.0211	46.3177	47.3636	0.1489	129.8559
2746.582	175781.25	47.0262	46.8519	47.1906	0.0642	111.9545
5493.1641	351562.5	47.0321	46.9420	47.1091	0.0320	111.6393
10986.3281	703125.0	47.0323	46.9775	47.0891	0.0205	143.2185
15380.8594	984375.0	47.0326	46.9917	47.0910	0.0180	175.5373

195 measurement points were taken for each frequency.
$V_{\mathrm{excitation}} = 101.1\,\mathrm{mV_{RMS}}$
$RF1 = 453\,\mathrm{k\Omega}$

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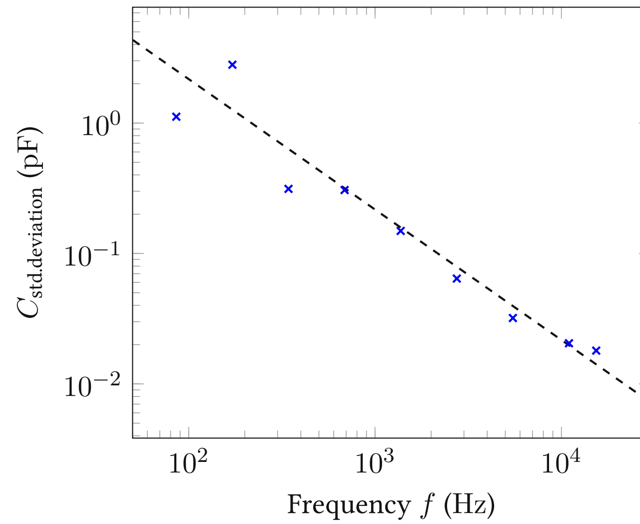
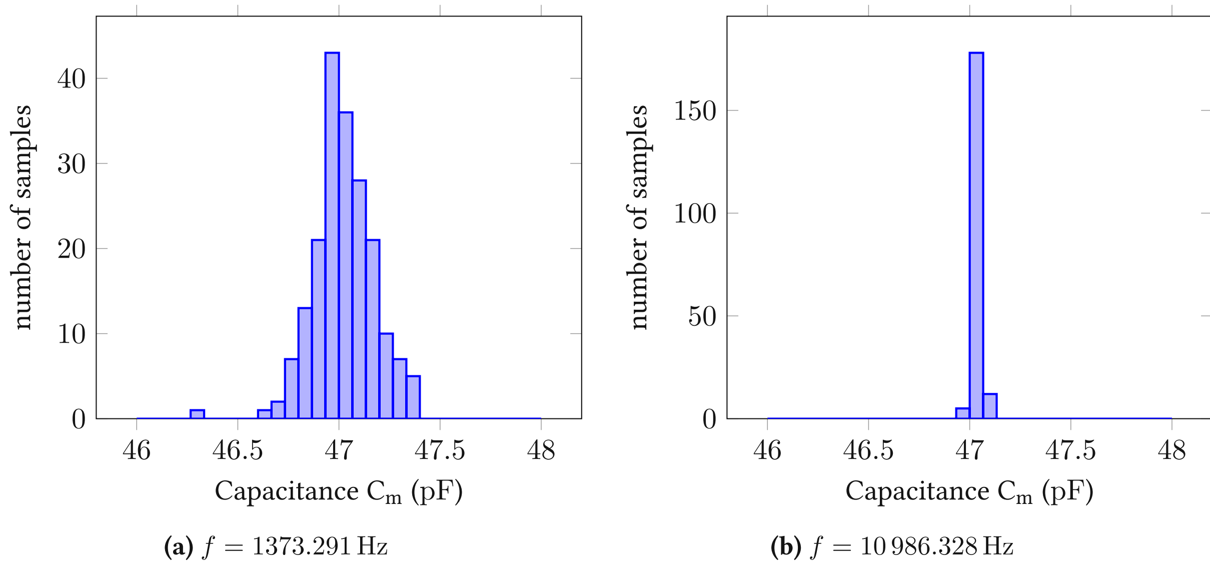


Figure 3.3: The standard deviation of the measured capacitance changes with frequency. The dashed line shows the theoretical line when the standard deviation of the measured current is constant (137.8 pA).



(a) $f = 1373.291\,\text{Hz}$ **(b)** $f = 10\,986.328\,\text{Hz}$

Figure 3.4: Histograms of a reference capacitor $C = 47\,\text{pF}$ for two different excitation frequencies. As expected the accuracy is higher at higher frequencies. 195 measurement points were taken per frequency. $RF1 = 453\,\text{k}\Omega$

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3.4 CV profiling

To determine the correct function of the developed CV measurement module, four different MOS transistors were used for CV profiling. The theorie of CV profiling is described in section 1.3. All four MOSFETs have the same gate area ($100\,\mu m \times 60\,\mu m$), oxide thickness and are rated for $3\,V$. The MOSFETs differ in the doping type of both their substrate and polycrystalline silicon (poly) gate. Thus, the DUTs measured were of the following variants:

- NMOS / NPOLY
- NMOS / PPOLY
- PMOS / NPOLY
- PMOS / PPOLY

Figure 3.5 shows two different connection schemes for an n-channel MOSFET as the DUT during a CV measurement. The source, drain, and bulk of the MOSFET were connected together and are considered as one connection of the DUT. The other terminal is the gate. When a MOSFET is connected this way, it could be seen as a MOS capacitor (see section 1.1). One of the terminals is connected to the excitation signal, whereas the other is connected as a virtual ground to the TIA. In principle, there is no difference in which connection is used as a virtual ground, besides a switch in polarity for the excitation signal. However, if external noise is considered, it has been shown that better performance can be achieved if the gate is used as a virtual ground. With this connection scheme less noise can be coupled into the large bulk area because of the lower impedance path of the signal generator output.

If not otherwise noted, an AC voltage of $100\,mV_{RMS}$ with a variable DC offset (V_G) was applied to the gate for all following measurements. V_G was swept from $-4\,V$ to $4\,V$ in $1\,mV$ steps. For the highest possible SNR, the lowest sample rate of the ADC was used (5 SPS).

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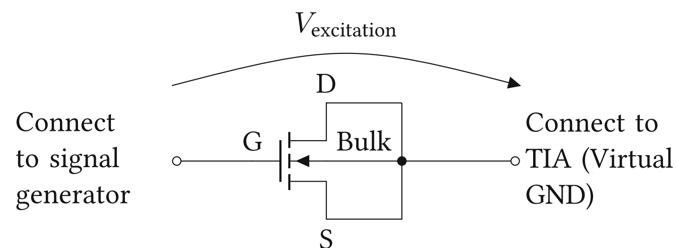
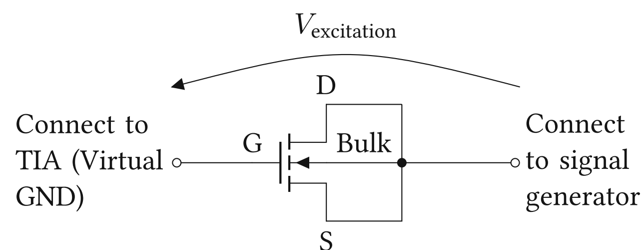


(a) Connection with bulk at virtual GND.



(b) Connection with the gate at virtual GND.

Figure 3.5: Two different connection schemes for the CV measurement with an NFET as DUT. (a) shows the regular connection. The excitation signal is applied to the gate. In (b), the excitation signal is applied to the drain, source, and bulk. This connection scheme has the advantage of reduced noise because less interference is coupled into the large bulk area. However, if the DUT is connected this way, the applied voltage has to be inverted to be in conformance with the normal connection

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3.4.1 Temperature influence on CV curves

Figure 3.6 shows the temperature influence on the CV characteristics. Each device was measured at $T = 25\,°\mathrm{C}$ and $T = 125\,°\mathrm{C}$. It can be seen that the accumulation-depletion and depletion-inversion transitions are steeper at lower temperatures.

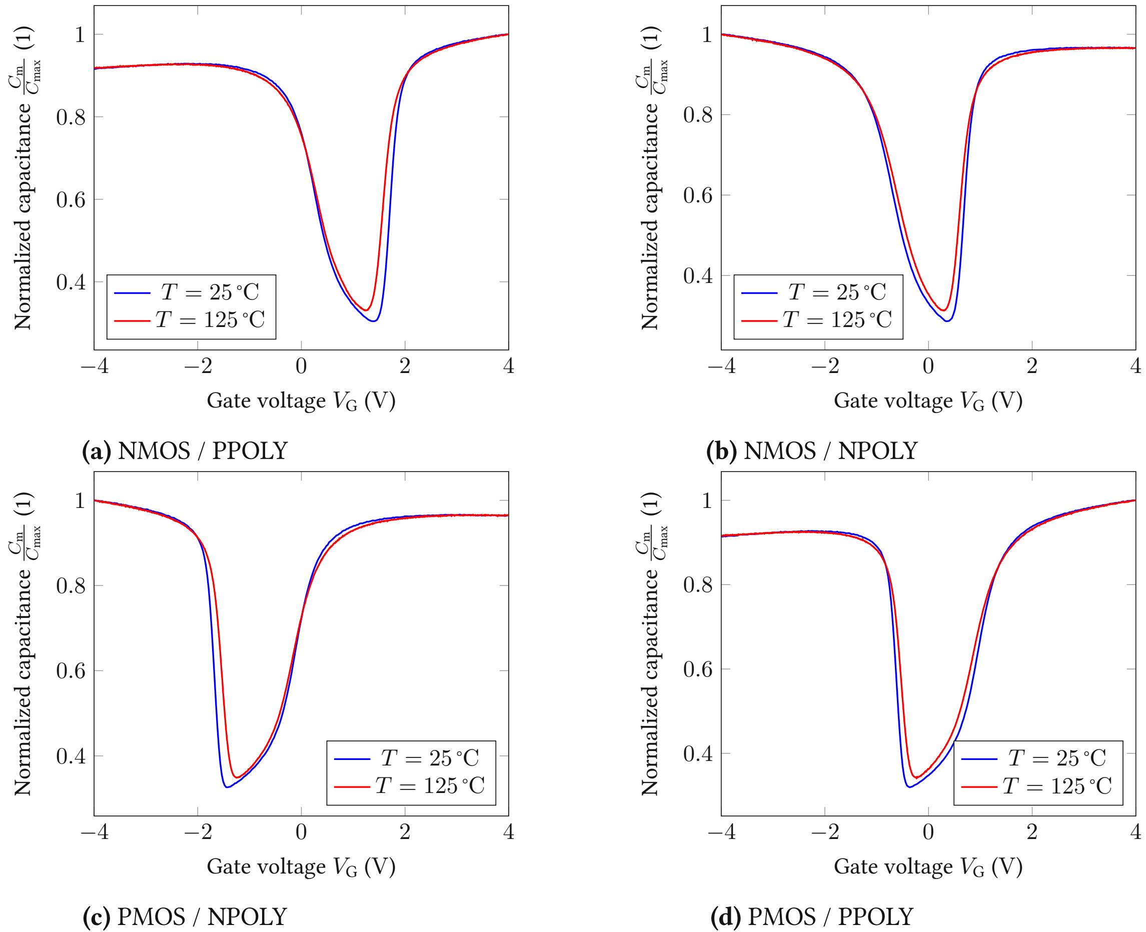

Figure 3.6: CV measurements at $T = 25\,°\mathrm{C}$ and $T = 125\,°\mathrm{C}$. The transitions between the regions are steeper at the lower temperature.
$f = 15\,380.859\,\mathrm{Hz}$
$V_{\mathrm{excitation}} = 101.1\,\mathrm{mV_{RMS}}$
$RF1 = 453\,\mathrm{k\Omega}$

3.4.2 Comparison between external and internal excitation signal

To assert if both the internal and external excitation signals give comparable results, and to compare their performance, a comparison measurement with similar parameters was taken with the internally generated excitation signal (fig. 2.2b) and one time with the excitation signal from the signal generator (fig. 2.2a). The results in fig. 3.7 show that both measurement methods work as expected. However, the use of an external excitation signal is much more flexible. An external signal can be easily varied in amplitude and frequency and thus enable better noise performance for a given measurement task, while the internally generated excitation signal is limited to a fixed amplitude and a fixed frequency.

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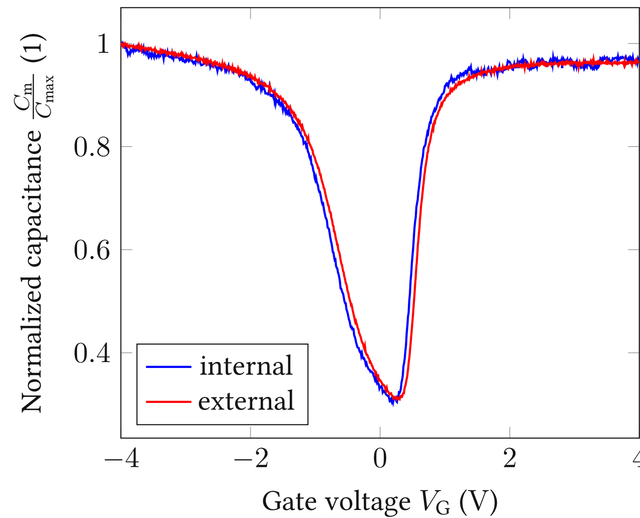

Figure 3.7: NMOS / NPOLY
Comparison between CV measurement with external excitation and internal excitation signal. Both measurement methods deliver similar results.
$f = 10\,986.328\,\text{Hz}$
$T = 125\,°\text{C}$
$V_{\text{excitation}} = 60\,\text{mV}_{\text{RMS}}$
$RF1 = 453\,\text{k}\Omega$

3.4.3 Excitation frequency influence on CV curves

Figure 3.8 shows the comparison between two different excitation frequencies for all four MOSFETs. The noise is, as expected, higher for the lower excitation frequency. It can also be seen that the higher frequency is still to low to observe a change in the inversion region, as in fig. 1.6 (d).

3.4.4 TIA feedback resistor influence on CV curves

The feedback resistor $RF1$ from eq. (2.3) determines the gain of the TIA. A higher resistor value will lead to a higher gain. The output voltage of the TIA is proportional to the current through the DUT, and the current is proportional to the capacitance of the DUT. Therefore, a higher gain will increase the SNR of the measurements. However, the output voltage of the TIA is limited to its supply voltage ($\pm 3.3\,\text{V}$). If the gain is too high, the output will be clipped. A trade-off between the measurable current range and SNR has to be taken for the gain. The influence of the feedback resistor $RF1$ on the measurements can be seen in fig. 3.9. Because of the low excitation frequency ($f = 85.831\,\text{Hz}$) the SNR is also low and a high feedback resistor value is needed to obtain a usable CV profile.

3.4.5 Connection scheme influence on CV curves

How the DUT is connected to the signal generator and the TIA can influence the measurement results. Especially which connection of the DUT is used as the virtual ground can impact the measurement noise. Figure 3.5 shows the two possible connection schemes for the DUT. In fig. 3.5a, drain, source and, bulk are connected to virtual ground. The excitation signal is applied to the gate. This connection is shown in most literature. Therefore, it will be called regular connection in this thesis. However, in practice, the reverse connection, like in fig. 3.5b is used. This has the advantage of reduced noise in the measurement

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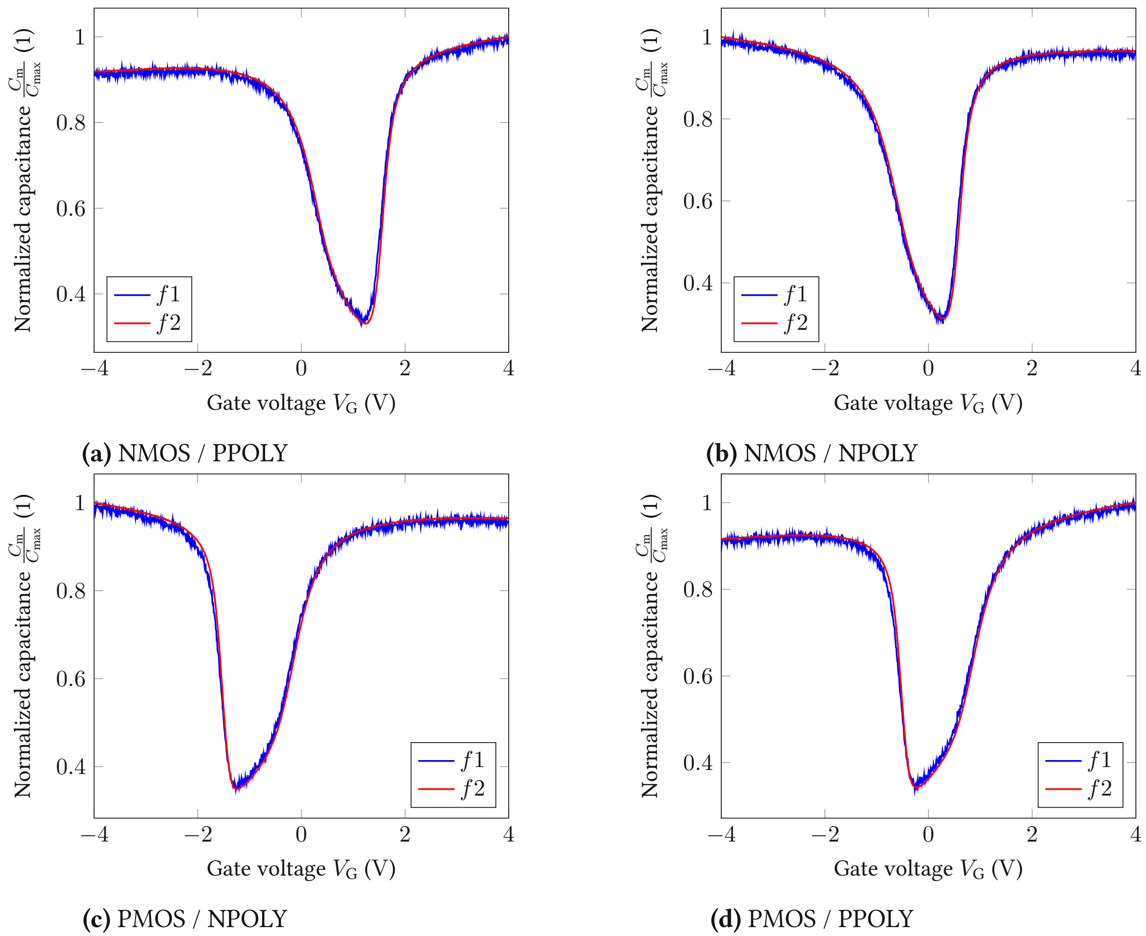

(a) NMOS / PPOLY
(b) NMOS / NPOLY
(c) PMOS / NPOLY
(d) PMOS / PPOLY

Figure 3.8: Comparison between CV measurements at $f1 = 1373.291\,\text{Hz}$ and $f2 = 15\,380.859\,\text{Hz}$. It can be seen that the SNR is higher at $f2$ than $f1$.
$T = 125\,^\circ\text{C}$
$V_{\text{excitation}} = 101.1\,\text{mV}_{\text{RMS}}$
$RF1 = 453\,\text{k}\Omega$

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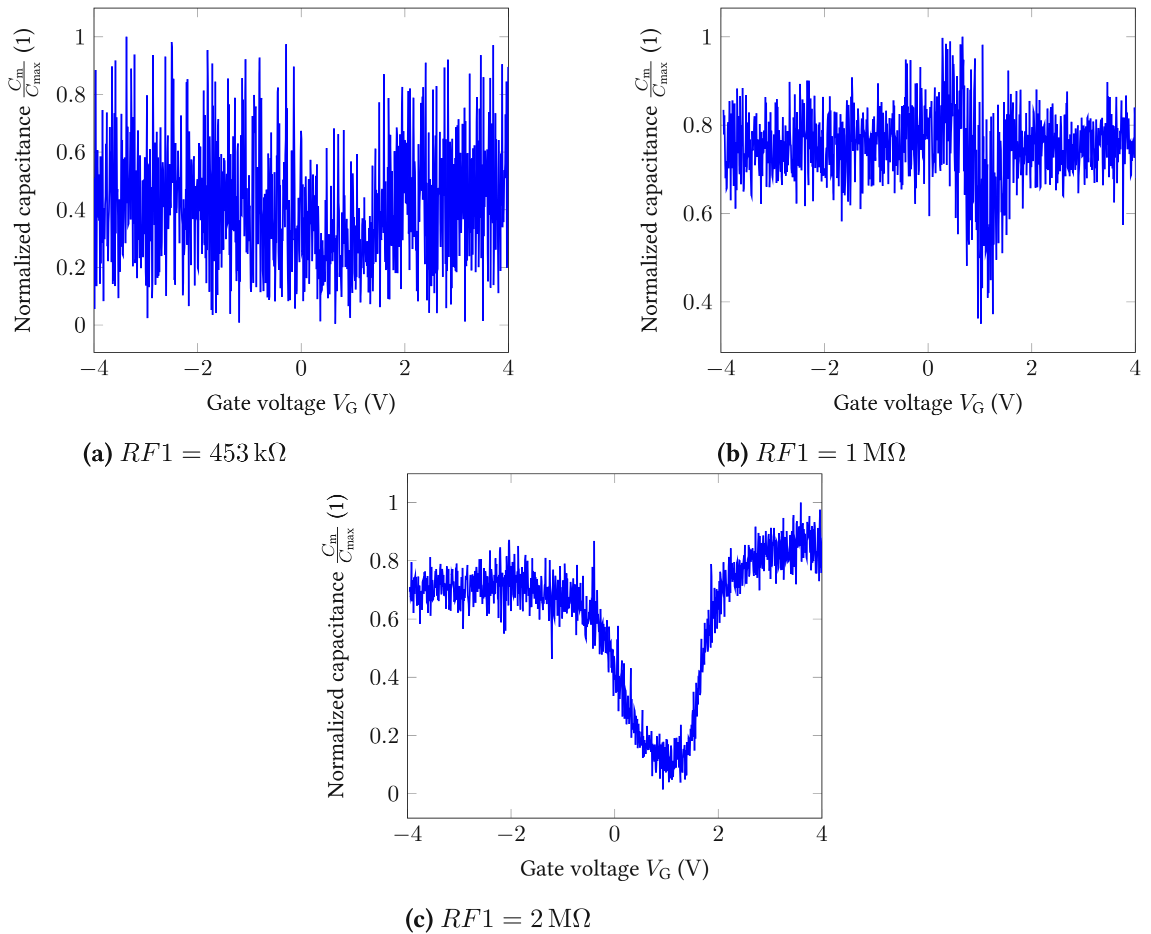

(a) $RF1 = 453\,\mathrm{k\Omega}$

(b) $RF1 = 1\,\mathrm{M\Omega}$

(c) $RF1 = 2\,\mathrm{M\Omega}$

Figure 3.9: NMOS / PPOLY
Comparison between different TIA feedback resistor values for a low-frequency CV measurement. A higher feedback resistor value leads to a higher SNR.
$f = 85.831\,\mathrm{Hz}$
$T = 125\,^{\circ}\mathrm{C}$
$V_{\mathrm{excitation}} = 101.1\,\mathrm{mV_{RMS}}$

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because less noise is coupled into the chuck. The function generator output attenuates the noise because of the lower impedance path than the virtual ground. The excitation voltage has to be inverted in this configuration to be compatible with the literature. Figure 3.10 shows a clear difference in noise between the two connection schemes.

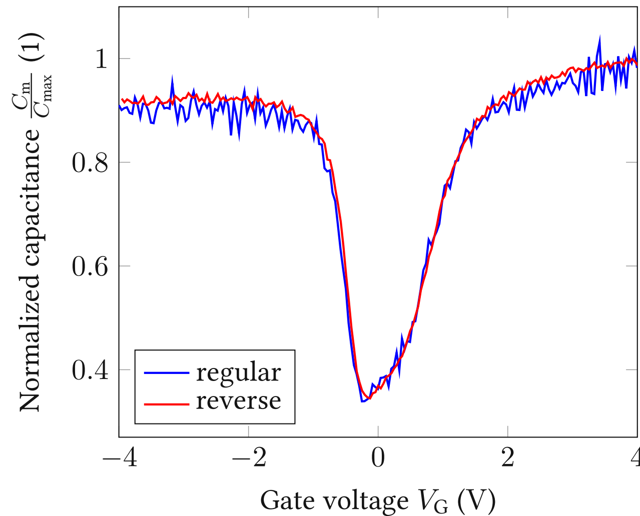

Figure 3.10: PMOS / PPOLY
Comparison between regular and reverse connection scheme. For the reverse connection, the excitation signal was inverted. A clear reduction of noise can be observed for the reverse connection.
$f = 1373.291\,\text{Hz}$
$T = 175\,°\text{C}$
$RF1 = 453\,\text{k}\Omega$

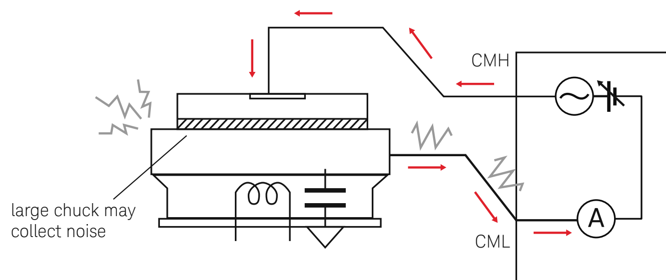

Figure 3.11: Noise can couple capacitively and inductively into the chuck [5].

3.5 MSM CV measurements

The MSM method was used to examine the effect of gate bias stress on a device and it's CV characteristics. The gate bias stress introduces or activates defects in the device and leads to BTI, as described in section 1.4. A total stress time of 10 ks was used with a stress field of $6\,\text{kV}\,\text{m}^{-1}$. After the stress phase, a recovery phase of 10 ks was used. The needed gate voltage V_G was calculated for every MOSFET in table 3.2.

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Table 3.2: Calculated stress voltages V_{stress} for an stress field of $\pm 6\,\text{MV}\,\text{cm}^{-1}$ and recovery voltages V_{recovery} for mid-gap condition ($\phi = 0\,\text{V}$).

Type	E_{stress} ($\text{MV}\,\text{cm}^{-1}$)	V_{stress} (V)	V_{recovery} (V)
NMOS / NPOLY	+6	5.3	-0.05
NMOS / PPOLY	+6	6.1	0.95
PMOS / PPOLY	-6	-5.5	0.1
PMOS / NPOLY	-6	-6.1	-0.8

V_{stress} is the gate voltage that is applied for a duration of t_{stress}.
V_{recovery} is the gate voltage that is applied for a duration of t_{recovery}.

Figures 3.12 to 3.15 show separate CV curves for the stress and the recovery phases at $T = 125\,^\circ\text{C}$ and $T = 175\,^\circ\text{C}$. As explained in section 1.4, the applied stress leads to a stretch-out of the CV curve in the x-axis and a higher interface state capacitance C_{it}. As expected these effects get stronger at higher temperatures. The most degradation can be seen for the NMOS / PPOLY transistor at $T = 175\,^\circ\text{C}$ in fig. 3.14b. The local maximum in the depletion region can be explained due to additional defects which get charged and discharged with the AC excitation frequency.

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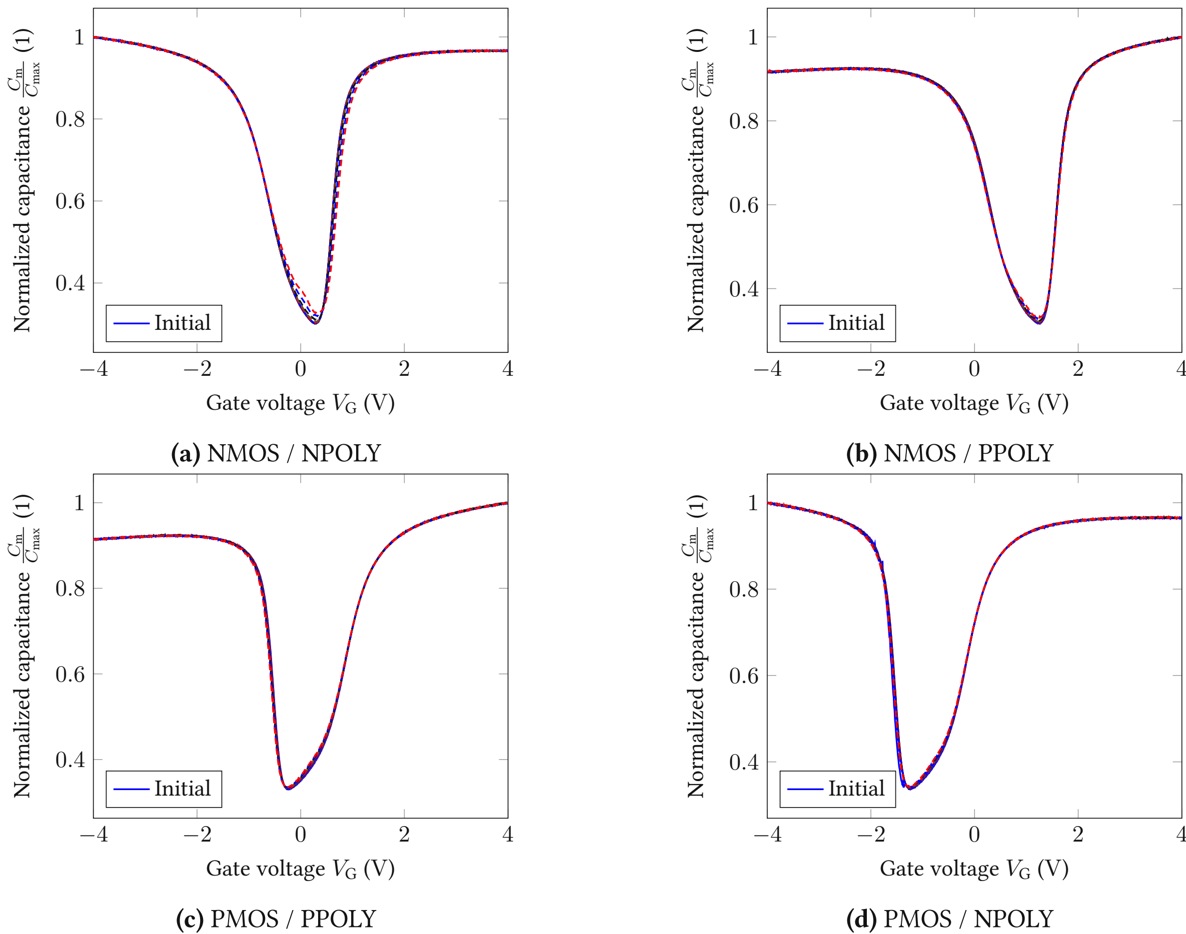

Figure 3.12: Stress change of the CV characteristic after 10 ks of stress at $T = 125\,°C$. Curves were measured at $t = 20\,s$, $t = 50\,s$, $t = 100\,s$, $t = 200\,s$, $t = 500\,s$, $t = 1\,ks$, $t = 2\,ks$, $t = 5\,ks$ and $t = 10\,ks$ after initial (unstressed) measurement. Only a small change in the CV characteristic is visible. $RF1 = 453\,k\Omega$

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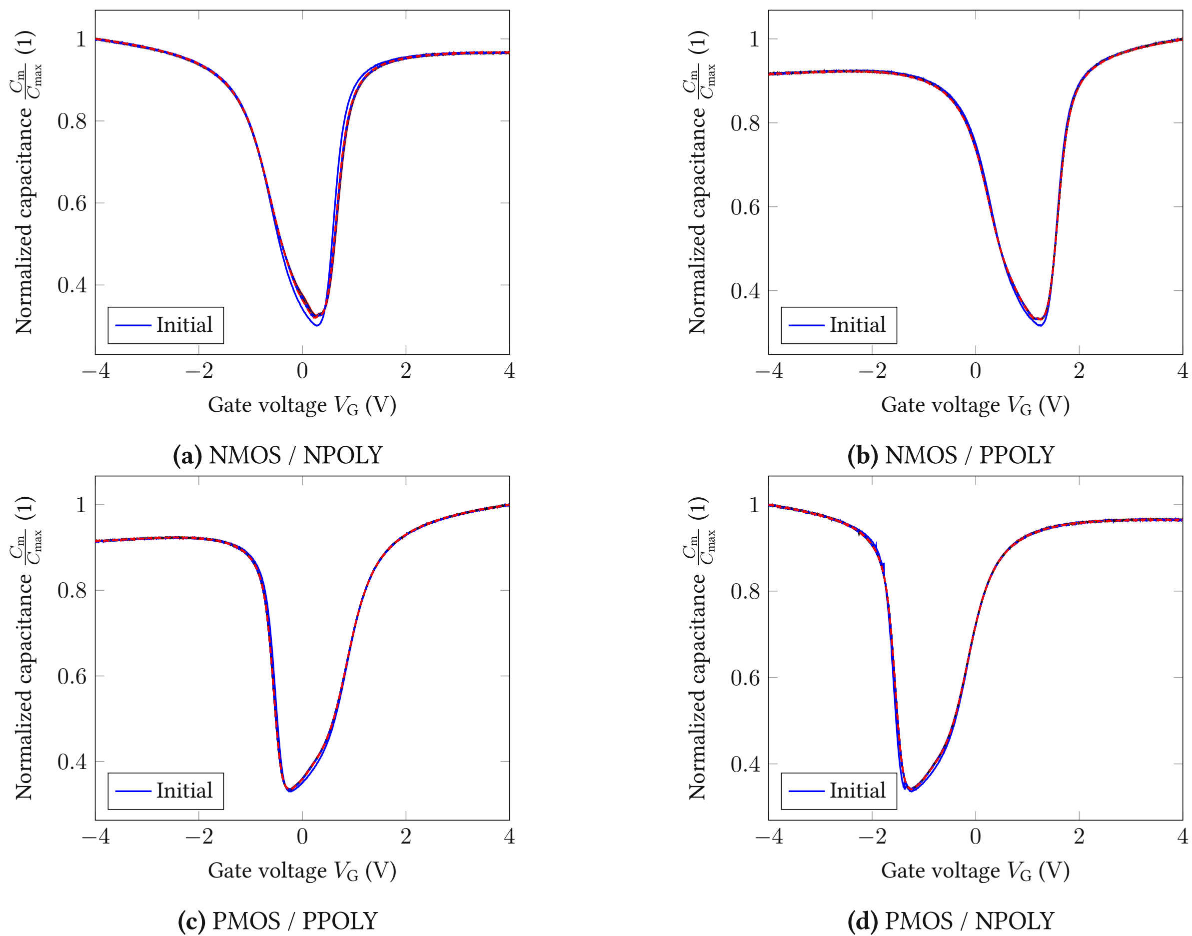

(a) NMOS / NPOLY

(b) NMOS / PPOLY

(c) PMOS / PPOLY

(d) PMOS / NPOLY

Figure 3.13: Recovery change of the CV characteristic after 10 ks of stress at $T = 125\,°C$. Curves were measured at $t = 20\,s$, $t = 50\,s$, $t = 100\,s$, $t = 200\,s$, $t = 500\,s$, $t = 1\,ks$, $t = 2\,ks$, $t = 5\,ks$ and $t = 10\,ks$ after 10 ks of stress. Even after a recovery phase of 10 ks, the CV curve will be different than the initial unstressed one. $RF1 = 453\,k\Omega$

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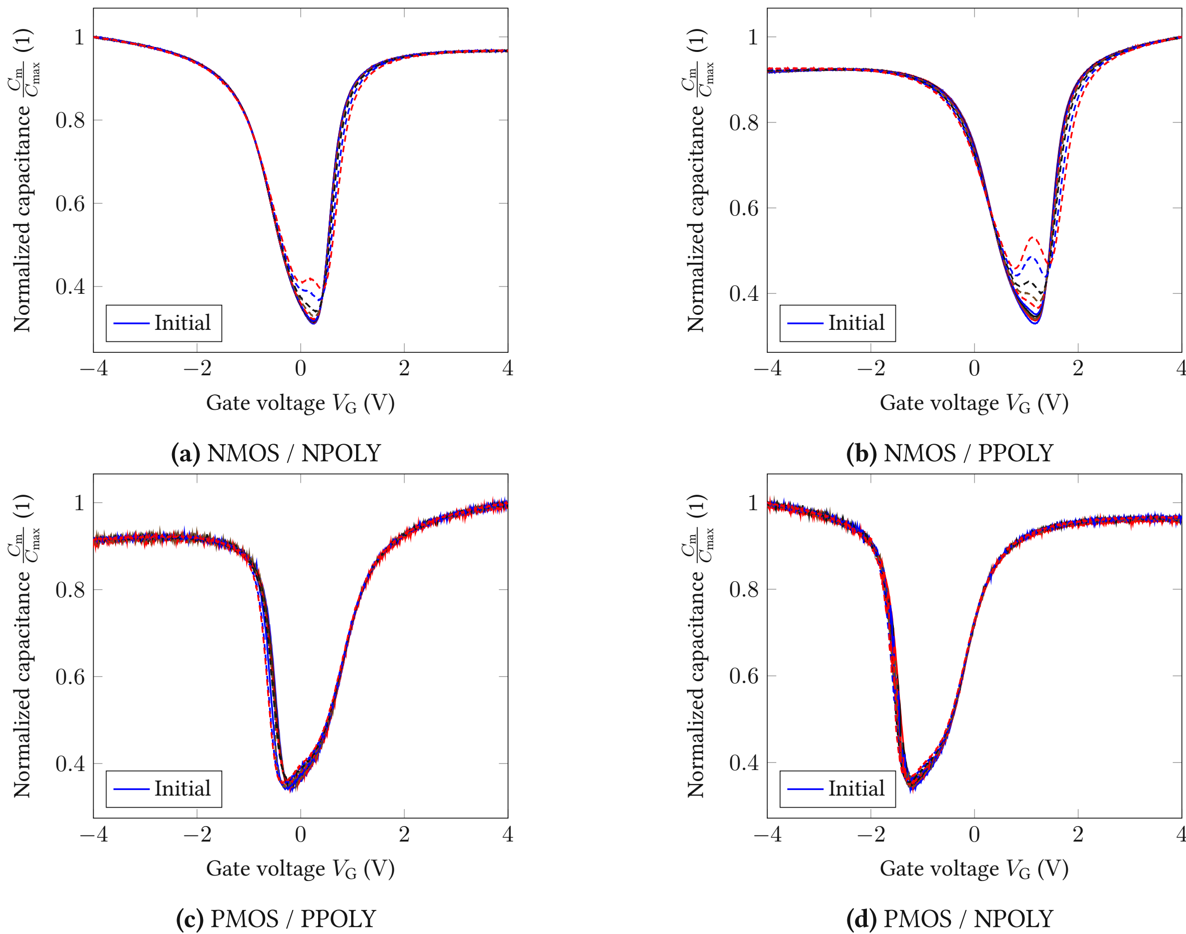

Figure 3.14: Stress change of the CV characteristic after 10 ks of stress at $T = 175\,°C$. Curves were measured at $t = 20\,s$, $t = 50\,s$, $t = 100\,s$, $t = 200\,s$, $t = 500\,s$, $t = 1\,ks$, $t = 2\,ks$, $t = 5\,ks$ and $t = 10\,ks$ after initial (unstressed) measurement. Due to the elevated temperature of $T = 175\,°C$, more effect on the CV curve is visible than at lower temperatures. $RF1 = 453\,k\Omega$

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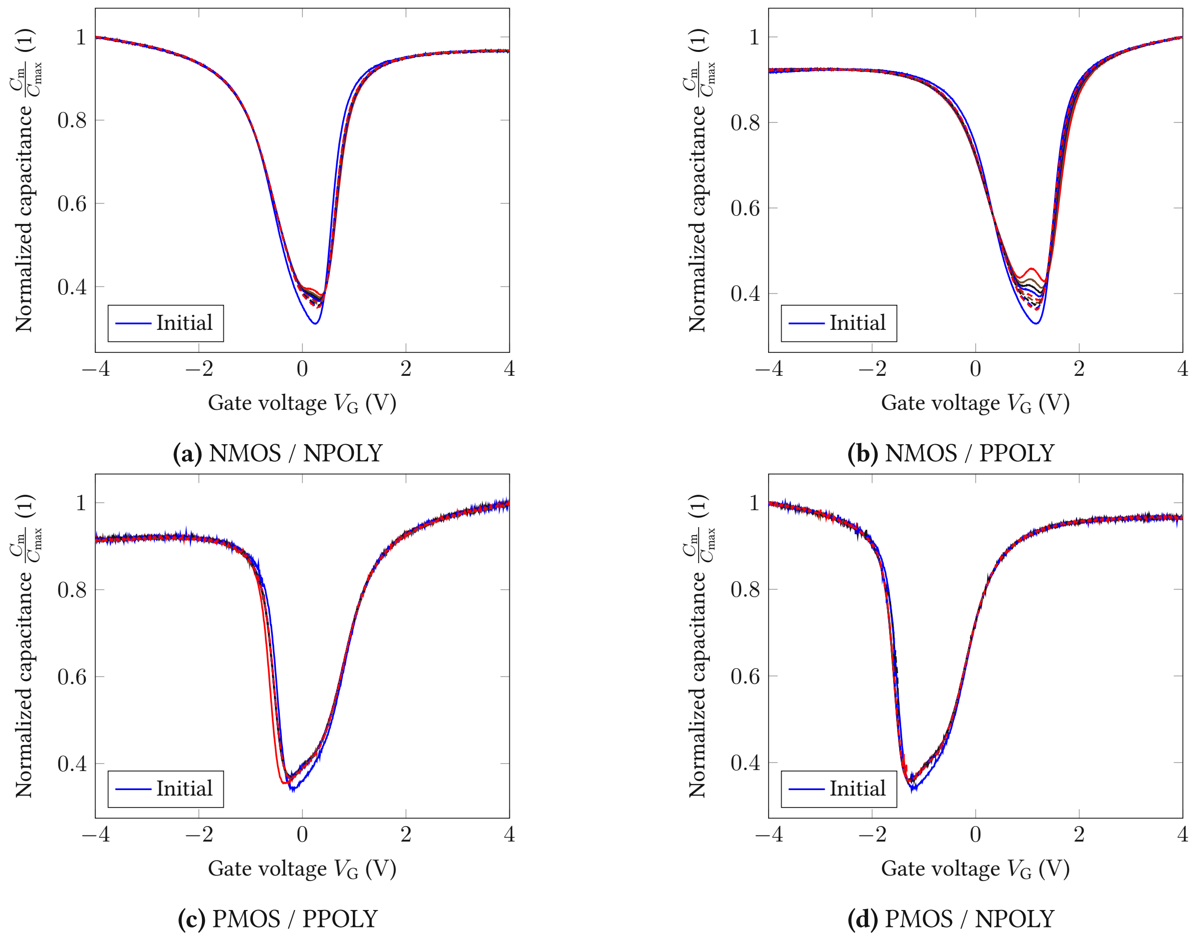

Figure 3.15: Recovery change of the CV characteristic after 10 ks of stress at $T = 175\,°C$. Curves were measured at $t = 20\,s$, $t = 50\,s$, $t = 100\,s$, $t = 200\,s$, $t = 500\,s$, $t = 1\,ks$, $t = 2\,ks$, $t = 5\,ks$ and $t = 10\,ks$ after 10 ks of stress. Even after a recovery phase of 10 ks, the CV curve will be different than the initial unstressed one. $RF1 = 453\,k\Omega$

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3.5.1 Interface state defect densities

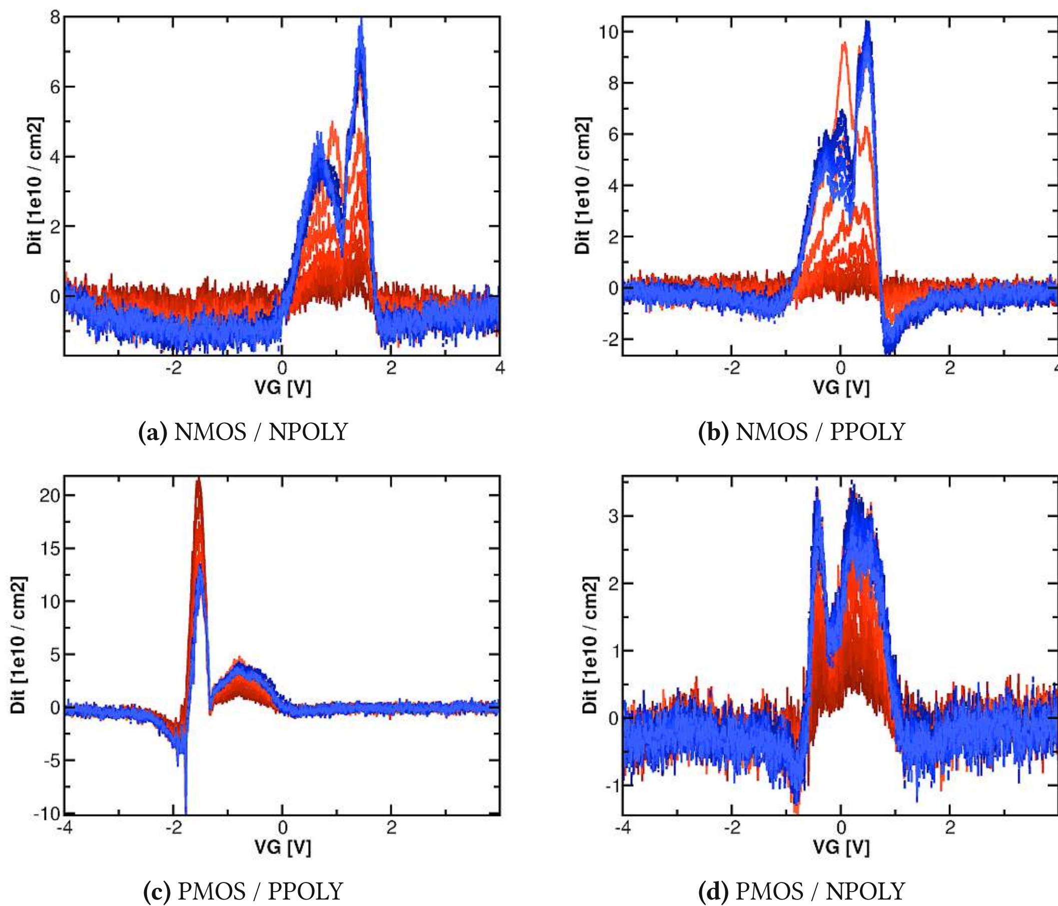
The Dit can be calculated from a high-frequency and a low-frequency CV measurement [27]:

$$D_{\text{it}} = \frac{C_{\text{ox}}}{q} \left(\frac{C_{\text{lf}}/C_{\text{ox}}}{1 - C_{\text{lf}}/C_{\text{ox}}} - \frac{C_{\text{hf}}/C_{\text{ox}}}{1 - C_{\text{hf}}/C_{\text{ox}}} \right) \tag{3.7}$$

If only the change of the defect density is of interest, a slightly modified formula can be used and only two low-frequency measurements are needed [3]:

$$\Delta D_{\text{it}} = D_{\text{it}} - D_{\text{it,ref}} = \frac{1}{qA} \left(\frac{C_{\text{ox}} C_{\text{lf}}}{C_{\text{ox}} - C_{\text{lf}}} - (\frac{C_{\text{ox}} C_{\text{lf,ref}}}{C_{\text{ox}} - C_{\text{lf,ref}}} \right) \tag{3.8}$$

With eq. (3.8) the change in the defect density between the unstressed and stressed MOSFETs can be calculated. With the data from the MSM CV measurements in section 3.5, the Dit of the four different MOSFETs has been calculated. The results are shown in fig. 3.16



(a) NMOS / NPOLY

(b) NMOS / PPOLY

(c) PMOS / PPOLY

(d) PMOS / NPOLY

Figure 3.16: Interface defect state density (Dit) dependent on the gate voltage (V_{G}) at 125 °C. This data was calculated from the stress CV measurements in fig. 3.12 with eq. (3.8).

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Chapter 4

Conclusion and future work

This thesis shows how to develop a low-noise CV measurement unit with an analog lock-in amplifier. It has been successfully used for creating CV curves for MOS transistors. It was possible to use either the internally generated excitation signal or an external excitation signal. However, there are still opportunities for further enhancements. DLTS measurements are theoretically possible with this hard- and software. However, more tests are needed to determine the accuracy of the results at higher sampling rates.

4.1 Possible improvements

4.1.1 Automatic range switching

In the current state of the TIA PCB there is only a fixed feedback resistor.
This limits the measurement range. An improvement would be to switch between different feedback resistors. This would need change at the TIA PCB and the firmware.

4.1.2 Combine TIA and lock-in PCB

At the moment, the TIA circuitry has its own PCB. This was a design choice to minimize interference between the noisy digital part and the highly sensitive TIA circuitry. A future improvement would be to integrate the TIA circuit onto the lock-in PCB if there is no significant performance decrease because of this change.

4.1.3 Integrate the module into the IuE framework

The IuE has a software framework for all MCU based modules. Currently, this module is not integrated into this framework. This would, for example, allow firmware upgrades through USB.

4.1.4 Optimize ADC input filter

The anti-aliasing input filter for the ADS1247 ADC can be further optimized to reduce the input noise to a minimum. The filter can be optimized for different purposes. If its cut-off frequency is too high, there could be aliasing and additional noise. If it is too low, the settling time is too high, and the sample rate needs to be decreased. Because this CV measurement module should be used at different excitation frequencies, there is no single optimum filter configuration. For a new revision, it would be possible to add relais which can change the filter.

4.1.5 4-wire voltage measurement

At the moment, the excitation voltage is not monitored. It is assumed that the output voltage from the signal generator does not change significantly during a CV measurement. It would be possible to

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monitor the excitation voltage with a 4-wire setup during the measurement to compensate for voltage fluctuations.

4.1.6 Increase measurement speed

It is possible to optimize the measurement flow to increase the measurement speed. The settling time could be reduced between excitation and measurement. Another possibility is to increase the sample rate of the ADC. However, if there are changes, the measurement accuracy should be monitored to ensure there is no significant performance decrease because of these changes.

4.1.7 Signal generator

The excitation signal and the clock signal greatly influence the overall accuracy of the CV measurements. Therefore, improvements to the signal generator would also benefit the CV measurement unit. Signal properties such as clock jitter, noise, and phase accuracy could be further improved.

4.1.8 Increase maximum possible measurement frequency

The maximum allowed input clock of the ADA2200 lock-in amplifier is 1 MHz. With the internal clock divider of 1/64 the maximum frequency of the excitation signal is limited to 15.625 kHz. So the ADA2200 is the limiting factor for higher excitation frequencies. Another lock-in IC or a discrete circuit could be used to increase the bandwidth of the circuit.

4.1.9 Differential capacitance measurement

Often it is enough to measure a differential capacitance ΔC, and the total capacitance is less important. For a differential measurement, two sinusoidal excitation signals with a phase shift of 180° are needed. This would have the benefit of an increase in the possible measurement resolution [28].

4.1.10 Usage of complex impedance

The principle of the lock-in amplifier allows a separate measurement of an in-phase and a quadrature component. Both parts together result in a complex value. Right now, only the absolute value is used because a simple, purely capacitive equivalent circuit is used. For more complex equivalent circuits, the real and complex parts could be both used for determining the impedance.

4.2 Bug fixes

There are some minor bugs that need to be fixed in the next revision.

4.2.1 TIA module

LMP8350 power supply

The LMP8350-1 is supplied with ±8 V but the maximum allowed voltage is only ±6 V. As a temporary solution a ±3.3 V LT3045/LT3094 voltage regulator board was inserted between the ±8 V net and the VDD/VSS net. The resistors R4 and R9 were desoldered.

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LMP8350 VOCM voltage

Currently, the VOCM pin of the LMP8350 is not connected. Due to an internal voltage divider the output mode common voltage is $\frac{VDD-VSS}{2}$ if nothing is connected to the VOCM pin. For a symmetric bipolar power supply, this would equal to $0\,\mathrm{V}$. However, the required common-mode input voltage for the ADA2200 is $1.65\,\mathrm{V}$. A $30\,\mathrm{k\Omega}$ resistor was connected between the VOCM and the VDD pin of the LMP8350.

LMP8350 wrong part name in schematic

In the schematic, the LMP8350 is named LPM3850-1. This is a typo and should be fixed.

4.2.2 Lock-in module

Wrong package for capacitors

C2_S4 and C2_S12 are $27\,\mathrm{nF}$ 0603 C0G capacitors. Such capacitors are not available. As temporary solution through-hole technology (THT) film capacitors were soldered onto the surface-mount technology (SMT) pads. For a new revision, the layout should be changed to accommodate the THT capacitors.

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