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DISSERTATION

Statistical Analysis of Reliability and Variability Effects in CMOS Technologies Based on Single-Defect Spectroscopy

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Abstract

The metal-oxide-semiconductor field effect transistor (MOSFET) is the integral building block of modern electronic devices. Its influence has triggered substantial cultural, societal, and economic shifts over the past few decades. Recognizing the sustained relevance of MOSFET technology, there is a considerable emphasis on amplifying their performance through ongoing research and development. Nevertheless, it is crucial to acknowledge that MOSFETs contain defects at the atomic scale due to their internal structure, fabrication procedures, and operating conditions. These defects represent obstacles to the reliability and functionality of MOSFETs as they trap electric charges and degrade the performance of these transistors. The impact of these defects is increasingly prominent as the trend toward transistor miniaturization continues. This situation raises issues such as bias-temperature instabilities (BTI) and random telegraph noise (RTN).

This work aims to contribute to understanding defects' impact on the performance of MOSFETs through experimental characterization and statistical modeling. The main focus is to analyze the impact of single defects on the device performance. By leveraging the extended measure-stress-measure (eMSM) on nanoscale devices, it is possible to extract the impact of single defects on the threshold voltage shift ΔV_{th}, one of the most core parameters of a transistor. Single-defect spectroscopy, used in conjunction with the defect-centric model (DCM) to evaluate the data, enables the accurate extraction of defect characteristics. This is essential for understanding the statistically distributed nature of active defects, particularly in terms of their number and impact on ΔV_{th}. This approach is especially crucial for identifying high-impact defects, known as "killer" defects, which can lead to immediate device and circuit failures in nanoscale nodes. From the results of the statistical analysis, the impact of device geometry and body bias on average threshold shift that can be induced by a single defect can be obtained, enhancing the understanding of time-dependent variations across different technologies.

Additionally, reliability simulations are employed to calculate the cumulative response of many defects on large devices and enable a comparison of theoretical trap parameters with the measurement data. For the experiments, three distinct technologies are investigated, enabling conclusions to be drawn about their distribution and physical properties. Combining experimental measurements, statistical modeling, and compact-physics simulations can lead to understanding defects in MOSFETs and device and circuit performance and reliability.

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Contents

Contents vii

List of Figures xi

List of Abbreviations xxiii

1 Introduction 1
- 1.1 History of MOSFETS . . . 2
- 1.2 Reliability Issues . . . 4
- 1.3 Variability and Yield . . . 5
- 1.4 Single Defect Analysis . . . 6
- 1.5 Defect Centric Perspective . . . 7
- 1.6 Scope of this Work . . . 8
- 1.7 Outline . . . 9

2 Defects in Field Effect Transistors 11
- 2.1 Interface Defects . . . 11
- 2.2 Oxide defects . . . 13
  - 2.2.1 Oxide Defects in SiO_2 . . . 14
  - 2.2.2 Oxide Defects in SiON . . . 15
  - 2.2.3 Oxide Defects in HfO_2 . . . 16
- 2.3 Semiconductor substrate defects . . . 17

3 Physical Modeling of Charge Transfer Reactions Involving Defects 19
- 3.1 Modeling Defect Interactions with Markov Chains . . . 19
- 3.2 SRH-like models for the transition rate . . . 21
  - 3.2.1 Recombination through defects - SRH model . . . 21
  - 3.2.2 Kirton Uren model . . . 23
- 3.3 Non-Radiative Multi-phonon Model . . . 24
  - 3.3.1 The 2-State Non-Radiative Multi-Phonon Model . . . 25
  - 3.3.2 The 4-State Non-Radiative Multi-Phonon Model . . . 26

4 Reliability Simulations 31
- 4.1 Compact Physics Framework (Comphy) . . . 31
- 4.2 Electrostatics . . . 31

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The approved original version of this doctoral thesis is available in print at TU Wien Bibliothek.
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4.2.1 Effective Density of States 32
4.2.2 Carrier Concentrations at Thermal Equilibrium 32
4.2.3 Fermi Level at Thermal Equilibrium 32
4.2.4 Electrostatics of a 1D MOS Structure 33
4.3 Occupation Probabilities 35
4.4 Distribution of Defect Parameters 36
4.4.1 Effective Single Defect Decomposition 37
4.5 Issues Related to Charge Sheet Approximation 38

5 Single Defect Statistics **41**
5.1 Introduction 41
5.2 Statistical Distributions of Defects 41
5.3 Total ΔV_{th} Distribution 43
5.3.1 Derived Parameters 44

6 Measurement Methods **47**
6.1 Time-zero Characterization 47
6.1.1 Transfer Characteristics 47
6.1.2 Capacitance - Voltage (CV) Measurements for Characterizing MOSFET Devices 49
6.2 Time-Dependent Characterization 51
6.2.1 Measure-Stress-Measure (MSM) Methods 51
6.2.2 TDDS 52
6.2.3 RTN Measurements 53
6.3 Measurement Setup 55
6.3.1 Custom-Made Low Noise Measurement Unit for MOSFET Reliability Measurements 56

7 Edge Detection Algorithms **59**
7.1 Canny Edge Detector 59
7.2 Otsu's Algorithm 60

8 Measurements and Results **63**
8.1 Impact of Defects on SiO_2 Transistors 63
8.1.1 Devices and Measurements 64
8.1.2 Measurement Analysis 66
8.1.3 Negative BTI in pMOS Devices 67
8.1.4 Positive BTI in nMOS devices 72
8.1.5 Body Bias Dependence 75
8.1.6 Conclusions 78
8.2 Single-defect analysis of BTI employing SiON Transistors 80
8.2.1 Devices and Measurements 80
8.2.2 Positive BTI in nMOS Transistors 80
8.2.3 Negative BTI in nMOS Transistors 82

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The approved original version of this doctoral thesis is available in print at TU Wien Bibliothek.

8.2.4 Negative BTI of pMOS Transistors 83
8.2.5 Comparing NBTI and PBTI degradation 84
8.2.6 Simulation Results 85
8.2.7 Conclusions 88
8.3 Statistical Characterization of RTN in high-κ devices using Smart Arrays 90
8.3.1 Devices and Measurements 90
8.4 Extraction of Step Heights 90
8.5 Distributions of Step Heights 93
8.6 Parameter Extraction 94

9 Summary and Outlook **97**
9.1 Summary 97
9.2 Outlook 98

References **101**

List of Publications **117**

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List of Figures

1.1 Illustrating the prevailing degradation mechanisms for various bias regimes, a diagrammatical depiction of the V_G , V_D space is presented. This schematic representation highlights the crucial factors influencing device performance and reliability under different operating conditions. Recreated from [21]. 4

1.2 The defect-centric picture allows for hierarchical traversal, whereby insights into the properties of defects at the atomic level can be propagated upwards to inform circuit design decisions. Originally published in [47]. 8

2.1 At the interface of Si/SiO_2 with a (100) orientation, Pb centers can manifest in two chemical forms: the P_{b0} center, characterized by the $(\cdot Si \equiv Si_3)$ structure, and the P_{b1} center, whose atomic structure is not fully comprehended. The dangling bond without a pair of electrons is depicted by blue triangles in the figure, which has been reproduced from [58]. 13

2.2 Ball-and-stick representations of two potential hole trap candidates in amorphous SiO2: (a) the hydrogen bridge and (b) the hydroxyl E′ center. In these models, silicon atoms are yellow, oxygen atoms are red, and hydrogen atoms are gray. The blue clouds depict the spin density for neutral defects, signifying the location of the unpaired electron, while for positive defects, they illustrate the distribution of the captured hole. Both defects can exist in four configurations, with two being neutral (states 1 and 1′) and two being charged (states 2 and 2′). Figures adapted from [59, 60] 14

2.3 The various defect candidates studied in SiO_2, HfO_2 and SiON have trap levels distributed throughout the band gaps of these materials. Oxygen vacancies (OV) have trap levels distant from the silicon conduction band, thus having a limited impact on BTI and RTN. Conversely, the trap levels of hydrogen-related defects like the hydroxyl-E_k center or the hydrogen bridge, along with interface defects such as the P_b center or the KN center, are near the silicon band edges, making them significantly relevant for BTI. Moreover, intrinsic charge trapping due to polarons is a key factor for electron trapping in high-κ devices. Originally published in [51]. . . 15

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2.4 The structural arrangement of a-HfO_2 (with Hf represented by silver and O represented by red) exhibits a greater level of disorder compared to a-SiO_2 (with Si represented by yellow and O represented by red). This disparity in disorder serves as a potential cause for intrinsic charge trapping, which could provide an explanation for the PBTI behavior observed in high-κ devices. Figure taken from [49]. 16

3.1 Example of Markov chain with three discrete states. The arrows indicate the transition rates between the states. 20

3.2 The band diagram schematically represents the capture and emission mechanisms for acceptor-like traps (depicted in blue) and donor-like traps (shown in red). As electron traps transition between neutral and negatively charged states, hole traps fluctuate between neutral and positively charged states. The diagram portrays the initial states of the defects before the occurrence of the specified transition. Figure adapted from [50] 22

3.3 The configuration coordinate diagram depicts the Kirton-Uren model, where a defect interacts with the reservoir through electron exchange. The position of the parabola is determined by the energy of the carrier. The thermal activation involved in the capture process is represented by the capture barrier, denoted as ΔE_B. In the diagram, the empty defect with an electron in the conduction band is depicted in black, while the captured electron at the defect site is shown in grey. The dashed line represents the energy zero of the system, corresponding to the empty defect with an electron at the Fermi level. This diagram is based on [80, 50]. 24

3.4 Potential energy surfaces (PESs) with a parabolic shape for the charged (depicted in grey) and neutral state (depicted in black) as employed in the NMP defect model, accompanied by the model's parameters. This representation is recreated based on [50]. 25

3.5 The four-state NMP model characterizes the capture and emission times of individual defects in response to changing biases and temperatures. Broadly, the model considers two stable states, 1 (neutral) and 2 (charged), as well as two meta-stable states, 1′ and 2′. It is crucial to consider these states when trying to accurately represent the emission times and other related characteristics that are dependent on bias [76]. 27

3.6 The four-state NMP model characterizes the capture and emission times of individual defects in response to changing biases and temperatures. Broadly, the model takes into account two stable states, 1 (neutral) and 2 (charged), as well as two meta-stable states, 1′ and 2′. These states are essential for accurately depicting the bias-dependent emission times and other associated attributes [76]. 28

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4.1 Comphy employs an effective 2-state NMP model to describe the charge transition of a pre-existing oxide defect. This transition from state i to state j occurs by overcoming the energy barrier ϵ_{ij}. The model's harmonic potential energy surfaces are characterized by the trap level E_T, the relaxation energy E_R, and the curvature ratio R. For the computation of the tunneling factor, the spatial coordinate x_T is employed. Figure taken from [KTJ4] 36

4.2 A defect can be characterized by the following parameters: relaxation energy (E_R), trap level (E_T), spatial position in the oxide (x_T), curvature ratio (R), and configuration coordinate offset (ΔQ). It is important to note that R and ΔQ are associated with the energy levels, while x_T is assumed to have a uniform distribution. Additionally, the energy levels follow a normal distribution within the defect bands. Recreated from [51] 36

4.3 The use of Gaussian trap bands in the 28 nm technology, as discussed in [66], indicates that only a fraction of the distribution contributes to active defects. The greater part of the defect parameters extracted from the trap band results in charge transition times exceeding 10^7 seconds (as seen on the left), rendering them experimentally unattainable. These prolonged charge transition periods correlate with relaxation energies ER that are significantly larger than those derived from DFT calculations (as seen on the right). Therefore, they can be considered as artifacts of the Gaussian distributions. The figure is a reproduction from [KTJ3]. 38

4.4 The influence of the regularization parameter γ is significant. When γ is small, the solution necessitates an excessively high defect density, which is not physically realistic. On the other hand, excessively large values of γ result in rapidly increasing approximation errors. The ideal value for γ resides between these two unfavorable regions. Originally published in [KTJ3] 39

5.1 The left part of the figure illustrates typical measure-stress-measure (MSM) sequences obtained from 40 devices of equal dimensions ($W \times L = 135\,\mathrm{nm} \times 350\,\mathrm{nm}$). Using the Canny algorithm, integrated into the data analysis framework [113, 116] used in this work, discrete steps representing charge transition events are extracted from the recovery traces, leading to the creation of a corresponding distribution. The middle panel demonstrates that the CCDF adheres to an exponential distribution while, for comparison, a uniform distribution obtained from the charge sheet approximation (CSA) is also included. Finally, the right panel exhibits a quantile-quantile (Q-Q) plot, comparing the distribution of the number of steps per device to a Poisson distribution. This plot validates that the number of steps per device can be accurately described by a Poisson distribution. Figure taken from [KTJ5] 42

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5.2 Experimental data from the largest device in the measurement set show that discrete steps are not observable in larger devices. Therefore, the statistical averages of the defects can be determined using DCM on the ΔV_{th} traces. 45

6.1 $I_{\text{D}}(V_{\text{G}})$ measurements for a set of devices, with the channel width $W = 135\,\text{nm}$ and the length $L = 350\,\text{nm}$. Using the constant current method, the threshold voltage V_{th} is extracted at $I_D = I_{ref}\frac{W}{L}$. The reference current I_{ref} is assumed to be 100 nA in this case. The V_{th} values range between 0.8 and 1 V for the identical devices of this technology. 48

6.2 The example results from a 100 kHz C-V measurement on nMOS devices display distinct accumulation and inversion branches at the peak values of negative and positive biases, respectively. The capacitance observed during the depletion phase is significantly lower. Additionally, the inversion branch tends to exhibit a steeper slope compared to the accumulation branch. V_{th} can also be estimated by the minimum value of the plot. 50

6.3 MSM sequence applied in devices of the same technology for statistical purposes. The scheme involves an initial $I_{\text{D}}(V_{\text{G}})$ measurement followed by alternating stress (red) and recovery (blue) phases with predefined applied gate voltages for a specific duration. During the recovery phase, the drain current I_{D} is monitored and correlated to ΔV_{th} using the initial $I_{\text{D}}(V_{\text{G}})$ 52

6.4 The presented recovery traces highlight the threshold voltage drift following PBTI stress in scaled SiON nMOS transistors. These devices exhibit recovery in discrete steps. Within these traces, electron emissions are identifiable as negative steps (in blue), and hole emissions as positive steps (in red), affecting the V_{th} behavior. Originally published in [KTJ4] . 53

6.5 The eMSM-based measurement strategy is utilized to evaluate the change in the threshold voltage. Once the initial $I_{\text{D}}(V_{\text{G}})$ is measured, stress and recovery voltages are applied in alternating fashion, with increasing stress and recovery durations (t_s and t_r). During the relaxation phase, the source current is recorded and subsequently converted into an equivalent ΔV_{th}using the initially measured $I_{\text{D}}(V_{\text{G}})$ characteristics. Originally published in [KTJ5] 54

6.6 The outcomes commonly observed when implementing the eMSM sequence on SiON devices with dimensions W × L = 10 × 10 μm^2 exhibit a continuous behavior in terms of the measured drain current (I_{D}). This arises from the simultaneous emission of previously trapped charges by a multitude of defects across the large device area. The individual influence of a single defect on the device's performance is too minute to be discerned through measurements. Originally published in [KTJ3] . . 55

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6.7 Four representative RTN signals exhibit varying mean charge capture and emission times, as well as step heights. From these RTN signals, the power spectral density (depicted in the same color as the corresponding RTN signal) can be derived, adhering to a Lorentzian distribution. The corner frequency of the Lorentzian corresponds to the mean capture/emission time τ of the RTN signal. The superposition of uniformly distributed Lorentzian signals results in a $1/f$ behavior, which is widely recognized in large area devices. 56

6.8 A constant gate voltage measurement setup schematic for methods focused on channel conductivity is displayed. The drain and gate voltages of the device are controlled by DACs. The gate voltage is directly applied to the DUT, while the drain current is connected to the positive terminal of an OPAMP operating as a TIA. The negative input terminal of the OPAMP is linked to the DUT's drain connection. The TIA's voltage output, corresponding to V_{out} , is captured by an analog-to-digital converter (ADC). Recreated from [50]. 57

6.9 A diagram of a constant source current measurement configuration for channel conductivity-focused methods is presented. The drain bias of the DUT is directly controlled, while the gate bias is managed by the OPAMP. The OPAMP circuit adjusts the MOSFET gate bias such that the source current matches the reference current determined by the DAC bias. Recreated from [50]. 57

7.1 The Canny method for identifying edges is showcased using a representative measurement trace. The input signal, ΔV_{th}, is convolved with the first derivative of a Gaussian pulse with a specified variance, G. This results in a signal R, which features peaks corresponding to the initial signal steps. All peaks exceeding a predetermined threshold are identified and utilized to indicate the locations of the steps in the initial trace. The peak heights can be acquired from either the original signal or the peak heights. Recreated from [126]. 61

7.2 For an RTN signal (left), a normalized histogram (right) with L bins is computed. For each bin, the inter-class variance σ_b^2 can be determined, and the bin with the maximum σ_b^2 provides the best threshold value. The locations where the signal transitions from above to below the threshold value can be extracted, and the corresponding step heights and time constants are obtained. 62

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8.1 Schematic of the carrier densities in the channel of a scaled device and the resulting current percolation path. (a) The randomly distributed dopants lead to locally decreased carrier densities. The neutral defect does not influence the current path. (b) When the defect is charged, the restrictions on the percolation path increase, leading to a decreased drain current and a higher threshold voltage [50]. Originally published in [KTJ7] . . . 64
8.2 Recovery traces obtained from scaled pMOS and nMOS devices showing the drift of the threshold voltage after NBTI/PBTI stress over time, measured on a scaled SiO_2 technology. As can be seen, the recovery proceeds in positive discrete steps for pMOS and negative for nMOS. Increased variability is observed between nominally identical devices. Originally published in [KTJ7]. 65
8.3 Recovery traces obtained from large pMOS and nMOS devices showing the drift of the threshold voltage after NBTI/PBTI stress. The traces recover similarly in a continuous manner as the increased number of defects with reduced impact on ΔV_{th} lead to a smaller variability. Originally published in [KTJ7]. 65
8.4 The CCDFs of the extracted discrete steps are shown. The pMOS data seem to follow a unimodal exponential function, while nMOS data can be described by a bimodal exponential function. The maximum limit of the CSA is shown as vertical dashed lines. Originally published in [KTJ7]. 66
8.5 The CCDFs of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential distribution used to describe the results. A recovery bias close to V_{th} was applied during the recovery phase. Originally published in [KTJ7]. . . . 68
8.6 (Top) The η values for the unimodal fit used in Figure 8.5 are plotted against the area. The devices with the same W scale nicely, but the devices with different W deviate from this trend, showing higher step heights. (Bottom) The η values for the unimodal fit are plotted against $W \times \sqrt{L}$. The fitted line seems to accurately capture all the data obtained from different geometries. Originally published in [KTJ7]. 69
8.7 The η values are plotted against $W \times \sqrt{L}$ trend. The fitted line nicely captures both experimental and DCM values. For some geometries, the markers used for the experimental data and data from the DCM model overlap as their values are too close to see a difference on a logarithmic scale. Originally published in [KTJ7]. 69
8.8 The average number of defects per device is plotted against both dimensional trends. The marker and color of the symbols follow the same convention as previous figures. Originally published in [KTJ7]. 70
8.9 The $I_D(V_G)$ characteristics of the smallest devices of the set. The grey dashed lines indicate the measurement conditions where the recovery traces were recorded. Originally published in [KTJ7]. 70

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8.10 The η values for the on-state measurements are plotted against $W \times \sqrt{L}$. The fitted line accurately captures all the data obtained from different geometries and the DCM values for the two large geometries. Originally published in [KTJ7]. 71
8.11 Traces of the smallest device of the set measured close to Vth (red lines) and at high operating conditions. At high operating conditions, the recovery is no longer observed in a discrete manner due to the increased charge in the inversion layer. Originally published in [KTJ7]. 71
8.12 The average number of active defects for the two measurement cases plotted for all the geometries. Higher values are observed when devices are measured at the on-state. Originally published in [KTJ7]. 72
8.13 The CCDFs of step heights of electron traps extracted after PBTI stress on nMOS devices. The bimodal exponential distributions (solid lines) describe the results more accurately than the unimodal exponential distributions (dashed lines). Originally published in [KTC1]. 73
8.14 (Top) The average step heights induced by single defects (η) for the data used in Figure 8.13 are plotted against the area. The red line shows the scaling of the values following a unimodal exponential distribution, and the gray dashed line is used as a comparison to the CSA. The RMSE values were normalized to compare the two different η ranges. (Bottom) The average step heights induced by a single defect (η) for the two distributions used in Figure 8.13 are plotted against $W \times \sqrt{L}$. A smaller error is observed in the latter case for the unimodal distribution. Originally published in [KTJ7]. 74
8.15 The average step heights induced by single defects (η) is used together with calculated values from DCM for the large devices that are plotted against $W \times \sqrt{L}$. The step detection values are taken from the second branch of bimodal distribution as they are closer to DCM values than the values extracted from unimodal distribution. Originally published in [KTJ7]. 74
8.16 Probability distribution of the initial V_{th0} values across a sample set of nanoscaled devices under varying V_B conditions, conforming to normal distributions. This change is largely attributed to modifications occurring in the depletion layer thickness X_{dep} as a response to alterations in BB settings. 75
8.17 Influence of the body bias on V_{th0} variability for pMOS devices. Under FBB, a reduced standard deviation of the normal distribution is observed. The smaller geometry exhibits higher initial variance and a more pronounced slope. 75
8.18 Influence of the body bias on V_{th0} variability for nMOS devices. The standard deviation is a few times higher in nMOS devices compared to their pMOS counterparts. 76

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8.19 Exponential distributions of individual charge ΔV_{th} step heights for a consistent device sample set under varied V_{B} conditions. RBB shows a heightened variance (elevated η), whereas the FBB exhibits a diminished variance (lower η). 76

8.20 The average step heights induced by a single defects (η) against the V_{B} for pMOS devices. Increased V_{B} leads to higher η values. The smaller geometry exhibits higher η values at $V_{\mathrm{B}} = 0$ and a more pronounced slope. 77

8.21 TDDS on two different BB settings on a single device. The studied step height is heavily influenced. The larger RBB leads to an increase in the step height, an observation consistent with what has been observed in the CCDFs of multiple devices. 77

8.22 The CCDFs of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential function used to explain the results. 78

8.23 The average step heights induced by a single defect (η) for the data used in Figure 8 are plotted against the V_{B}. Increased -V_{B} leads to higher η values. The slope is less steep for the nMOS case. 78

8.24 TDDS for two different BB conditions on a selected device. The step heights at larger RBB are increased, an observation consistent with what has been observed in the CCDFs. BB impact is smaller in nMOS devices than in pMOS devices. 79

8.25 The figure presents the band diagram of nMOS devices under PBTI conditions. It illustrates the presence of electron traps (depicted in blue) and hole traps (depicted in red), along with their respective AERs for charge trapping. The blue region represents the AER for charge transitions between the defects and the channel. In contrast, the red region represents the AER for charge transitions between the defects and the gate. These regions define the energetic boundaries within which the defects can change their charge state during the experiments, thereby contributing to the drift of the measurement signal. It should be noted that the height of the AERs varies with the applied gate bias. On the right side, the distribution of step heights, measured from SiON nMOS transistors after undergoing PBTI stress, is shown for three sets of devices with different geometries. The majority of observed traps are electron traps (depicted on the left), although a certain number of hole traps (depicted on the right) can also be observed. The electron traps show a bimodal exponential distribution, while the holes traps show a unimodal exponential behavior. Originally published in [KTC2]. 81

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8.26 (Left) The band diagram of nMOS devices for the NBTI conditions. In contrast to the PBTI case, more hole traps can contribute to total ΔV_{th} now as the channel's AER covers the band-gap's lower half. The AERs for charge transitions between the defects and the channel and for charge transitions between the defects and the gate are marked in blue and red color, respectively. (Right) Distribution of step heights of defects extracted after NBTI stress. Bimodal exponential behavior can be observed for both types of traps. Originally published in [KTC2]. 83

8.27 Distribution of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential function used to explain the results. originally published in [KTJ4]. . . . 84

8.28 Extracted impact of a single defect on the ΔV_{th} (η) and the number of traps per device (N_T) considering unimodal exponential distribution. Clearly visible is the underestimation of the CSA of the impact of the defects, on the device behavior. The maximum impact of CSA is considered by considering the traps directly at the interface. Originally published in [KTC2]. 85

8.29 The extracted values for the two modes of the bimodal exponential distribution are shown. As can be seen from Figure 8.25, the distribution follows more a bimodal exponential behavior than a unimodal one. Again, the CSA significantly underestimates the impact of the defects, which leads to a too pessimistic estimation for defect density from ΔV_{th}. Originally published in [KTC2]. 86

8.30 The extracted values for the unimodal exponential distribution of the hole traps of pMOS devices. The η values seem to be proportional to the gate area. The max limit of CSA approximation is around three times smaller than values extracted from the CCDFs. Originally published in [KTC2]. 86

8.31 Extracted defect bands from eMSM measurements on the SiON devices. nMOS bands are magnified to be accurately visible in the figure. Recreated from [KTJ3]. 87

8.32 Samples are obtained from the extracted defect distributions within the band diagram. The search regions used in the ESiD algorithm are represented by shaded areas. The highest concentration of both electron (blue) and hole (red) traps is found within the IL. Originally published [KTJ3]. 87

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8.33 In the top figure MSM measurements (dots) on large-area nMOS devices are shown, as presented in [KTJ3], at $T = 100\,°\mathrm{C}$ under three different stress conditions. The lines are simulated with the BTI simulator Comphy averaged for 100 sets of sampled step heights using the CCDFs extracted in section 8.2.2. The regions marked in grey are shown in more detail in the two bottom figures. Every light line presents a BTI simulation with a sampled set of step heights, the solid line is the average of all performed simulations. Originally published in [KTJ4]. 88

8.34 In the top figure MSM measurements (dots) on large-area pMOS devices are shown, as presented in [KTJ3], at $T = 100\,°\mathrm{C}$ under three different stress conditions. The lines are simulated with the BTI simulator Comphy averaged for 100 sets of sampled step heights using the CCDFs extracted in Section 8.2.4. The regions marked in grey are shown in more detail in the two bottom figures. Every light line presents a BTI simulation with a sampled set of step heights, the solid line is the average of all performed simulations. 89

8.35 Initial $I_\mathrm{D}(V_\mathrm{G})$ measurements of the biggest geometry in the bias range to capture the RTN signals. Originally published in [51, 143]. 91

8.36 After identifying the distinctive levels of an arbitrary RTN signal (shown at the top), various parameters can be derived, such as step magnitudes (shown at bottom left) and the times for charge capture and emission (shown at bottom right and middle). However, in this particular signal, the distributions of t_e and t_c fail to meet the criteria set by the χ^2 and Kolmogorov-Smirnov tests. This exclusion ensures the avoidance of erroneous detections, thus making this particular trace unsuitable for statistical analysis. 92

8.37 After identifying the distinct steps present in an arbitrary RTN signal (depicted at the top), numerous parameters can be derived, such as step magnitudes (shown at bottom left) and the times for charge capture and emission (shown at bottom right and middle). In this particular trace, the distributions of t_e and t_c successfully pass both the χ^2 and Kolmogorov-Smirnov tests, ensuring accurate detection. As a result, this trace is suitable for utilization in the statistical analysis. 92

8.38 The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 4 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature, the exponential distribution seems unable to describe the results, also the mean values do not scale with the area but present a random behavior. 93

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8.39 The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 7 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. Similar to the T= 7 K case, the exponential distribution seems unable to describe the results and also the mean values seem to not scale with the area but present a random behavior, too. 93
8.40 The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 225 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature, the exponential distribution captures nicely the results. Also, a scaling with the area starts to exist. 94
8.41 The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 300 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature similar to the T= 225 K case, the exponential distribution captures nicely, and the area scaling is clear. 94
8.42 The number of devices exhibiting RTN versus temperature for all the different areas. Even though the results are mixed, more devices exhibiting RTN can be seen in higher temperatures. 95
8.43 The extracted η values for the T= 225 K case presented in Figure 8.40 are plotted against the area. The results follow the area trend except for a small outlier at L=170 nm. The experimental values are higher than the maximum limit of CSA, similar to the other studies presented in the thesis. 95
8.44 The extracted η values for the T= 225 K case presented in Figure 8.41 are plotted against the area. The results follow the area trend with a smaller RMSE than in the T= 225 K case. The experimental values are higher than the maximum limit of CSA, although their deviation is smaller than the T= 225 K case. 96
8.45 The extracted η values for the T= 225 K case presented in Figure 8.40 are plotted against the $W \times \sqrt{L}$ trend. The results follow the trend with the same RMSE as observed in the area trend. 96
8.46 The extracted η values for the T= 300 K case presented in Figure 8.41 are plotted against the $W \times \sqrt{L}$ trend. The results follow the trend with the same RMSE as observed in the area trend. 96

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List of Abbreviations

ADC analog-to-digital coverter

aRTN anomalous RTN

BJT bipolar junction transistor

BTI bias temperature instability

CCDF complementary cumulative distribution function

CDF cumulative distribution function

CMOS complementary MOS

CV capacitance-voltage

DAC digital-to-analog coverter

DCIV direct-current current-voltage

DFT density functional theory

DIBL drain-induced barrier lowering

DLTS deep-level transient spectroscopy

DUT device under test

eMSM extended MSM

ESR electron spin resonance

FET field-effect transistor

GIDL gate-induced drain leakage

HC hot carrier

HMM hidden Markov model

IV current-voltage

MIS metal-insulator-semiconductor

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MOS metal-oxide-semiconductor

MOSCAP MOS capacitor

MOSFET MOS field-effect-transistor

MSM measure stress measure

NMP non-radiative multi-phonon

NMR nuclear magnetic resonance

OPAMP operational amplifier

OTF on-the-fly

PDF probability density function

PES potential energy surface

PSD power spectral density

RAM random access memory

RTN random telegraph noise

RTS random telegraph signal

SILC stress induced leakage current

SIMS secondary ion mass spectroscopy

SNR signal-to-noise ratio

SPICE simulation program with integrated circuit emphasis

SRH Shockley–Read–Hall

TCAD technology computer-aided design

TDDS time-dependent defect spectroscopy

TDRC thermal dielectric relaxation current

WKB Wentzel–Kramers–Brillouin

XPS X-ray photoelectron spectroscopy

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Chapter 1

Introduction

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In the modern world, electronic devices have become an integral part of daily life. This has been mainly enabled as the electronic industry has seen rapid progress in recent years with the development of smaller, faster, and more reliable devices. At the heart of most of the electronic devices lies the metal-oxide-semiconductor (MOS) transistor as one of the main building blocks, which at a first glance seems like a simple stack of three material layers [1]. MOS structures function by exploiting the field effect: applying voltage to their metal gate terminal modulates the conductivity between the source and drain terminals. This creates a channel at the semiconductor-insulator interface, allowing for the switching of electronic signals, making them essential to reproduce the binary logic necessary for logic gates of computer architectures. Due to the usage of the field effect these structures are commonly called metal-oxide-semiconductor field-effect transistors (MOSFETs). Beyond the realm of digital electronics, transistors are also extensively used in analog applications, functioning as amplifiers due to their high input impedance, low output impedance, and minimal power consumption. Their significance is particularly noteworthy in amplifying weak signals from sensors, microphones, and other low-level input sources, a function critical to the communication applications in the current era [2].

However, the continuous improvements and evolution of MOS devices are limited by parameters such as the speed and power consumption amongst other reliability issues. These constraints primarily stem from defects in the structure, either located in the oxide or at the interface between the oxide and the semiconductor. These defects can alter the electrical properties of the MOSFET by capturing and releasing charges in response to applied biases or temperature changes. This phenomenon can cause fluctuations in the threshold voltage, subthreshold slope, and transconductance of the device, leading to performance degradation and reduced reliability [3, 4]. In the worst-case scenario, single defects can cause catastrophic device failure. The impact of single defects is particularly significant in advanced nanoscale MOSFETs where the margin for variability in the device's electrical characteristics decreases. Therefore, any defect causing even slight deviations in these characteristics can have a substantial impact on the device's operation. Improving the reliability of MOS devices is a critical challenge that needs to be addressed to ensure the smooth operation of electronic systems.

This thesis aims to contribute to a better understanding of MOS device degradation phenomena and their mechanisms related to single defects, focusing on their impact on threshold voltage (V_{th}) of devices and circuits. The research presented in this thesis highlights the challenges associated with describing the impact of defects statistically and provides an overview of modeling efforts to capture the essence of the physical mechanism behind charge capture. By investigating these phenomena, the goal is to provide valuable insights that researchers and practitioners can leverage to improve the reliability and lifetime of MOS devices and, ultimately, the electronic systems that depend on them.

1.1 History of MOSFETS

The invention and evolution of the MOSFET have played a critical role in shaping the modern electronics industry. Before its invention in the 1960s, the electronic industry relied on bipolar junction transistors (BJTs) for amplification and switching applications. However, BJTs had several limitations, including high power consumption, high input capacitance, and poor thermal stability.

Julius Edgar Lilienfeld, an Austrian physicist, was the first to conceptualize the idea of using the field effect to modulate conductivity in a semiconductor triode structure, which he filed for a patent in 1928 [5]. The idea of a MOS device, which would eventually lead to the development of the MOSFET, was first proposed in the late 1950s. Although Lilienfeld filed for a patent on the idea in 1925, it was not until the invention of the MOS capacitor in the late 1950s that the possibility of a MOS transistor became a reality [6]. This marked a significant milestone in the electronic industry, as it offered several advantages over BJTs, including low power consumption, low input capacitance, and high thermal stability. These advantages paved the way for the widespread use of MOSFETs in modern electronics.

The first devices were developed in the late 1960s and early 1970s, which were relatively simple compared to the advancements of today. In 1963 the researchers Sah and Wanlass from Fairchild suggested a new type of MOSFET logic combining both nMOS and pMOS, and filed a patent which was granted in 1967. This combination was called complementary MOS (CMOS) [7], an idea which is behind on most of the electronics of today. The main reliability issue during this period was the limited lifespan of the devices, as they were prone to breakdown over time due to high electric fields at the oxide-semiconductor interface.

During the 1970s and 1980s, advancements were made in the processing techniques used to manufacture MOSFETs, resulting in improved device reliability. The use of new materials, such as silicon dioxide and nitrided oxides, allowed for the creation of more robust and reliable devices. However, the major reliability issue during this period was the limited power handling capability of the devices, as the high temperatures generated by high current levels could cause permanent damage.

During the 1990s and early 2000s, there was a shift in focus towards making MOS-

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FETs smaller and improving their power handling capabilities, following the principles of Moore's Law [8]. This law predicts that transistor density will approximately double every two years, leading to better performance and lower production costs. To ensure this continuous growth, semiconductor manufacturers began reducing the dimensions of transistors, such as their width, length, and insulating layer thickness. However, this aggressive downsizing resulted in several challenges. One of these challenges was the difficulty in scaling down supply voltages without affecting the on/off current ratio. Additionally, it became necessary to maintain a minimum thickness for the insulating layer to prevent excessive leakage currents.

These challenges prompted the exploration of alternative materials for gate stacks. High-k materials, like Hafnium oxide (HfO_2), combined with metal-gate contacts, emerged as a solution for cutting-edge devices [9, 10]. These materials enabled the reduction of the effective oxide thickness (EOT) while maintaining the necessary insulating properties. As a result, high-k gate stacks are now commonly utilized in high-performance CMOS applications. Apart from incorporating high-k materials, another strategy to enhance CMOS performance is the utilization of high mobility channels [11, 12]. For example, replacing the conventional silicon channel with a silicon-germanium (SiGe) channel allows for higher mobility, leading to larger on currents. Recent research has focused on gate-all-around (GAA) transistors, a cutting-edge design where the gate material surrounds the channel from all sides, offering enhanced control over the channel and significantly reducing leakage currents. This innovation represents a key evolution from FinFET architecture. Additionally, Forksheet devices, an advanced offshoot of the GAA design, have been explored for their potential to further reduce short-channel effects and increase drive current, showcasing a promising path for scaling beyond the limitations of traditional MOSFETs [13, 14]. Lastly, it should be noted that 2D materials are being explored for novel MOS devices. One advantage of using these materials is that the interface between the 2D material and the insulator does not have interface defects since their connection relies on van der Waals bonds, in contrast to the covalent bonds found in Si/SiO_2 interfaces. However, the development of these devices is still in its early stages and requires substantial advancements in fabrication processes to establish this technology [KTJ1].

However, the continuous process of scaling faces inherent limitations imposed by atomic dimensions. In 2016, the International Technology Roadmap of Semiconductors (ITRS) [15], responsible for establishing development standards and outlining future advancements, published its final roadmap. This decision was prompted by the imminent boundaries of the classical scaling approach, which were expected to be reached in the 2020s. Consequently, the IEEE International Roadmap for Devices and Systems (IRDS) [16] was introduced in 2016 as a successor to the ITRS, focusing on a wider range of future developments. Within this context, every year's version of IRDS mentions the importance of further development in the oxides of the devices.

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1.2 Reliability Issues

The reliable and stable operation of electronic devices can be compromised by various reliability issues that arise from harsh electrical stress, elevated temperature, radiation, and mechanical stress, negatively impacting the transfer characteristics of the device and affecting the reliability of interconnects [17, 18]. In the worst case, oxide breakdown can occur, leading to an increase in oxide leakage currents [19, 20]. Among the different types of device performance degradation mechanisms, this work focuses on the electrical issues caused by defects in the atomic structure of the device. Defects can change their charge state by charge capture and emission, thereby leading to changes in device performance. To comprehend the intricacies of charge trapping mechanisms, it becomes imperative to discern between different degradation mechanisms that prevail under distinct bias conditions, as depicted in Figure 1.1.

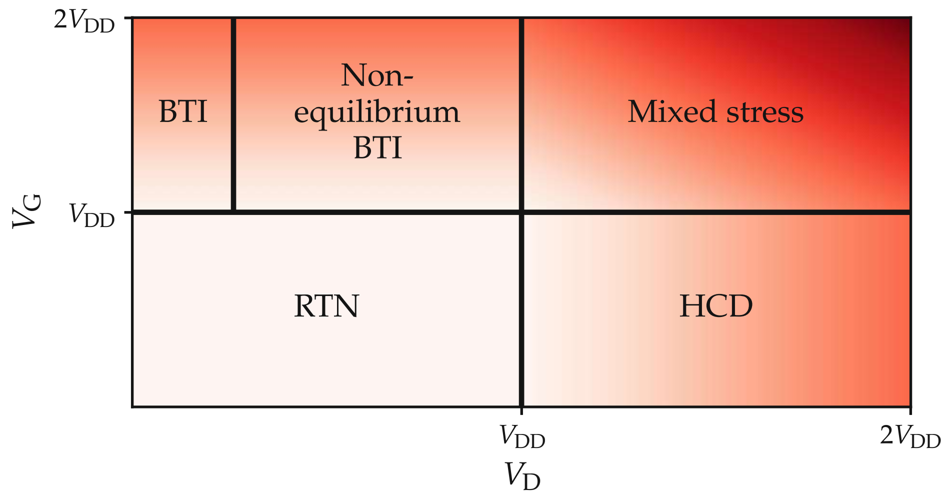

Figure 1.1. Illustrating the prevailing degradation mechanisms for various bias regimes, a diagrammatical depiction of the V_G , V_D space is presented. This schematic representation highlights the crucial factors influencing device performance and reliability under different operating conditions. Recreated from [21].

The Bias Temperature Instability (BTI) is a widely investigated mechanism responsible for performance degradation in electronic devices. This phenomenon is primarily characterized by variations in device parameters, such as threshold voltage (V_{th}) and channel mobility (μ), which result from charge trapping within the oxide layer when a bias is applied to the device's gate. Charge trapping is accelerated by elevated temperatures (T) and gate biases (V_G), but it can be partially reversed when the gate bias is reduced. Both positive BTI (PBTI) and negative BTI (NBTI) can occur in nMOS and pMOS devices. The general focus is on NBTI in pMOS devices and PBTI in nMOS devices, as these are associated with the typical bias conditions under operation. In silicon, the pMOS/NBTI combination receives greater attention since it often exhibits the most substantial degradation due to defects and the energetic alignment of the hole defect band [22, 23, 4].

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An additional phenomenon stemming from the same defects that cause BTI is Random Telegraph Noise (RTN), which occurs when the energy level of defects is situated near the Fermi level of the channel at a given operational point. RTN represents a state of dynamic equilibrium for the channel/gate dielectrics system, while BTI represents the disturbed system reverting to this equilibrium state [24]. This effect is characterized by the random capture and release of charges by the defects, leading to noise in the channel current. The magnitude of the RTN effect escalates with device scaling and is linked to various challenges in integrated circuits, such as increased failure probabilities in SRAM and jitter in ring oscillators [25, 26, 27, KTJ1].

Stress-Induced Leakage Current (SILC) or trap-assisted tunneling is another mechanism that allows defects in the oxide to facilitate charge tunneling between the channel and the gate, resulting in elevated gate leakage currents. This rise in device power consumption can lead to thermal failure and reduced retention time for EEPROM and FLASH memory cells following numerous write and erase cycles [28, 29].

Finally, Hot Carrier Degradation (HCD) is caused by carriers with high kinetic energy that cause damage close to the interface, where they can break Si-H bonds or become trapped, leading to the creation of interface states. The highest energy carriers are typically observed close to the end of the channel, where most of the damage is typically observed. The interface states can charge and affect the channel conduction similarly to BTI defects [30, 31].

Even though this work predominantly emphasizes BTI and RTN, it's crucial not to overlook the substantial impact of the other two degradation mechanisms, SILC and HCD. These mechanisms are vitally essential and contribute extensively to ensuring a reliable, consistent functionality of both devices and circuits, forming an integral part of the broader picture of device reliability and stability.

1.3 Variability and Yield

Another critical issue with modern electronic devices is the variability in scaled nodes. MOSFETs are subject to various sources of variability, including time-zero device variability and time-dependent variability, commonly referred to as device reliability. During the manufacturing process, process variations inevitably occur, causing deviations from the ideal characteristics of seemingly identical devices. This variability can have a detrimental impact on the performance of single devices and circuits and also affects the yield of the devices.

Time-zero device variability, which is a result of limited control over the fabrication process, can be classified as local and random variations within a die, variations across a single wafer due to inhomogeneities during processing, and variations between different wafers in a lot due to changing processing conditions during manufacturing [32, 33]. Other factors contributing to variability include fluctuations in surface roughness and thickness of patterned structures, metal grain roughness, and random discrete dopants.

Variations in surface roughness and thickness of patterned structures contribute

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to line edge roughness (LER), leading to stochastic fluctuations in device geometry [34]. In high-k transistors, metal grain roughness (MGR) must be considered, as these devices necessitate a metal gate contact on top of the high-k dielectrics. The metal layer's work-function depends on metal grain's orientation, introducing random variations in the threshold voltage [35]. Random discrete dopants (RDDs) play a crucial role in scaled transistors as the arbitrary placement of the limited number of dopant atoms in such devices results in threshold voltage fluctuations exceeding tens of millivolts [36, 37]. The influence of RDD fluctuations on the standard deviation of the threshold voltage ($\sigma_{V_{\mathrm{th}}}$) can be approximately represented by an analytic function [38]:

$$\sigma^2_{V_{\mathrm{th}}} \approx \sqrt{4q^3\varepsilon_{\mathrm{Si}}\phi_B}\left(\frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\right)^2 \frac{\sqrt{N_{\mathrm{tot}}}}{W \times L} \tag{1.1}$$

where ϕ_B denotes the surface potential and N_{tot} represents the doping concentration. Importantly, $\sigma_{V_{\mathrm{th}}}$ depends on the oxide thickness (t_{ox}) and the total dopant concentration (N_{tot}). Other examples of process variations include annealing effects and lithographic limitations [38, 39].

Besides time-zero device variability, MOSFET devices may undergo time-dependent variability, which pertains to changes in device characteristics over time due to aging and environmental factors. BTI and HCD are two prevalent sources of time-dependent variability. Consequently, the overall variability of deeply-scaled devices arises from a combination of time-zero and time-dependent variability. Accurately describing the time-dependent and overall statistical distributions is thus essential for reliably predicting the performance of future deeply downscaled technologies.

To mitigate the impact of variability, various techniques have been developed, including using high-quality gate oxide materials, optimizing device structures, and implementing stress and recovery cycles to counteract BTI effects. Additionally, circuit-level design strategies such as redundancy and error-correction codes can also help improve MOSFET-based circuits' reliability in the presence of variability.

1.4 Single Defect Analysis

To describe time-dependent variability and the statistics of defects influencing nanoscale technologies, extracting the impact of individual defects in electrical measurements is crucial. Single defect spectroscopy [40, 41, 42] is an advanced characterization method focusing on the study of the behavior and properties of individual defects in semiconductor materials and devices. This potent technique offers researchers a unique opportunity to investigate single defect characteristics, such as charge state dynamics and energy levels. Examining these properties allows scientists to optimize device performance, improve reliability, and deepen the understanding of defect-related phenomena in semiconductors [43].

In recent years, single defect spectroscopy has become a vital tool for examining gate dielectrics in MOSFETs. Specifically, it has been applied to investigate high-k

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dielectric materials, like hafnium oxide (HfO_2) [44, 45], which are extensively used in modern semiconductor devices due to their capacity to mitigate short-channel effects and maintain low leakage currents at state-of-the-art supply voltages.

Through single defect spectroscopy, researchers can reveal the following aspects of individual defects in semiconductor materials and devices:

- **Charge Trapping Dynamics:** The technique enables scientists to explore the charge trapping and de-trapping processes of defects in gate dielectrics. Comprehending these dynamics is essential for optimizing device performance and identifying potential reliability concerns.

- **Energy Level Characterization:** Single defect spectroscopy allows the determination of defect energy levels, which is crucial for understanding the impact of defects on device operation and devising strategies to alleviate their effects.

- **Spatial Localization:** Analyzing individual defects provides insights into their spatial distribution within the semiconductor material. This information is valuable for determining defect origins and identifying methods to reduce their occurrence during the fabrication process.

- **Temporal Behavior:** Single defect spectroscopy also elucidates the temporal behavior of defects, including their stability and lifetime. This knowledge is critical for evaluating the long-term reliability of semiconductor devices and developing strategies to prolong their operational lifetimes.

The utilization of single defect spectroscopy can contribute significantly to the comprehension of the behavior exhibited by individual defects in semiconductor materials and devices [46, 43]. This technique offers intricate insights into the properties and conduct of single defects, holding great promise for driving advancements in semiconductor device performance, reliability, and manufacturing processes.

1.5 Defect Centric Perspective

The results extracted from single defect analysis can create the framework to describe defect reliability based on their statistics. Given that only a limited number of defects have an impact on the time-dependent effects observed in deeply-scaled devices, it is crucial to understand the degradation mechanisms at the individual defect level to simulate time-dependent variability in circuits accurately [47, 48]. This concept forms the foundation of the defect-centric approach, as depicted in a hierarchical manner in Figure 1.2. The initial step is defining fundamental terms related to variability and proceeds to examine the characteristics of individual defects, explaining how these properties can be propagated to higher hierarchical levels. A commonly used statistical framework, known as Defect-Centric Model (DCM), is used to describe the distribution of devices over time through simple equations. The model is based on the statistics of

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the number of defects per device which follows a Poisson distribution with a mean value of N_T and the statistics of the effect of a single defect on the threshold voltage which is assumed to be exponentially distributed with an average value of η [24]. To accurately estimate the parameter distributions of devices and circuits at the end of their useful lifetime, it is important to combine both time-zero and time-dependent statistics. Lastly, it is crucial to propagate and simulate the combined variability at the circuit level.

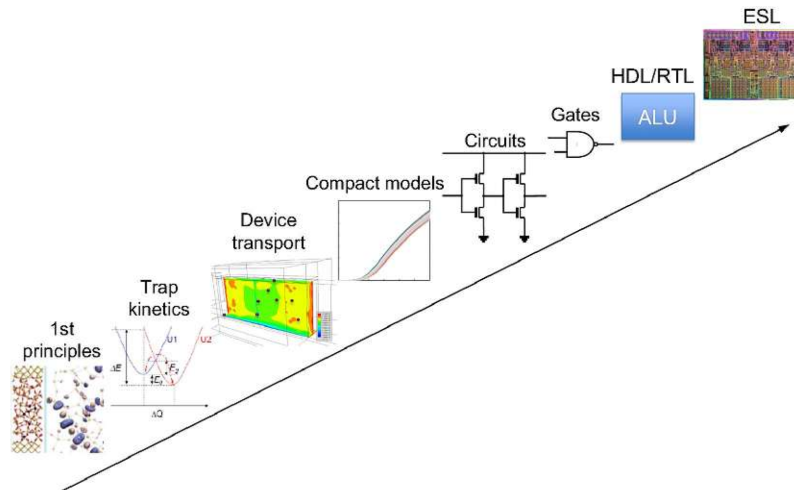

Figure 1.2. The defect-centric picture allows for hierarchical traversal, whereby insights into the properties of defects at the atomic level can be propagated upwards to inform circuit design decisions. Originally published in [47].

1.6 Scope of this Work

The purpose of this thesis is to investigate the impact of defects within the oxide and at the semiconductor/oxide interface on the operating characteristics of MOS transistors. As the lateral dimensions of MOS transistors have been reduced, their switching speed and power consumption have improved. However, with the reduction of lateral dimensions, defects within the oxide and at the semiconductor/oxide interface have an enhanced impact on the device characteristics. This leads to increased variability in device characteristics such as threshold voltages, sub-threshold swing, and carrier mobility, even when comparing devices that are nominally identical.

In order to investigate the impact of defects in semiconductor devices, a series of measurements were conducted on numerous commercial pMOS and nMOS devices. Based on the data collected, statistical distributions of defect properties were created to explore the relationship between statistical quantities, like the link between the average threshold shift of a single emission event and the lateral device dimensions. To achieve a more accurate understanding of the effect of charge traps on device behavior and to gather valuable information for the entire technology, a combined approach involving single-defect extractions and the use of the DCM was employed. This approach enables

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a more precise assessment of the impact of charge traps on device behavior, which is vital for the improvement of the layout and performance of circuits.

The focus of this thesis is to study the variability of MOS transistors by analyzing the contributions of defects on the device behavior. The findings from this research provide helpful insights into designing more reliable circuits [KTJ2], and can be used to gain a deeper understanding of the impact of defects on MOS transistors. The approach taken in this work is also applicable to the study of other technologies and can be used as a useful tool for improving the reliability of electronic devices.

1.7 Outline

The study presented here offers a comprehensive exploration of the impact of defects on MOSFETs, encompassing both experimental and theoretical aspects. The thesis is structured into several chapters discussing the characterization and modeling of defects.

The introductory chapter sets the stage by providing background information and context for the study. Subsequent chapters focus on specific aspects of defect characterization and modeling.

Chapter 2 provides an overview of the primary types of electrically active defects commonly found in MOSFETs. The chapter explains their origins and interactions with the devices, featuring relevant oxides specific to silicon technology such as the SiO_2, SiON , and HfO_2.

Chapter 3 discusses various mathematical modeling approaches for defects and their effects on device behavior. It introduces key concepts, such as employing a Markov chain with capture and emission rates to represent defects. The chapter covers different modeling techniques and outlines the mathematical tools essential for defect modeling.

Chapter 4 discusses the simulation framework utilized in the study, based on electrostatics and the non-radiative multiphonon (NMP) model. The chapter addresses the impact of the charge sheet approximation in simulations and highlights the need to describe the average impact of defects.

Chapter 5 centers on the statistical characterization of defects, exploring the distributions used to explain their behavior. It introduces the defects-centric model, which provides a framework for describing the behavior of single defects based on the distributions of their amplitude and concentration.

Chapter 6 explores experimental techniques employed in defect characterization, discussing various methods such as capacitance-voltage (C-V) measurements, conductance techniques, and noise measurements. The chapter also outlines the equipment and setups utilized for experimental defect characterization.

Chapter 7 focuses on extracting defect parameters from measurements, bridging the gap between experimental defect characterization and defect modeling. The chapter examines different approaches for extracting information about defects from measurements, emphasizing the importance of accurate parameter extraction for effective defect

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modeling.

Finally, Chapter 8 presents defect characterization studies conducted on three different technologies, incorporating combinations of the methods discussed in previous chapters. The chapter describes the experimental setups and provides a detailed analysis of the results. The data obtained from these experiments serves to validate the models and methods discussed earlier in the study.

Collectively, this work offers a comprehensive examination of defects in MOSFETs, encompassing both theoretical and experimental aspects. The study provides a deeper understanding of how defects impact MOSFET performance by exploring different defect types, their mathematical modeling, and experimental characterization methods.

The implications of this study are stimulating for the development of improved defect management strategies in MOSFETs. By identifying and comprehending the mechanisms underlying various defect types, researchers and engineers can work towards minimizing their impact and enhancing device reliability.

The inclusion of defect characterization studies conducted on multiple technologies demonstrates the practical relevance of this research. These experiments offer valuable insights into defect behavior in different materials and device structures, thereby informing the future development of more robust and reliable MOSFETs.

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Chapter 2

Defects in Field Effect Transistors

The presence of electrically active defects in the oxide or at the interface between the oxide and semiconductor of an MOS transistor can cause reliability issues, such as BTI, HCD, and RTN, that negatively impact device performance and can lead to device and circuit failure. Even though manufacturing processes have improved, defect formation cannot be fully avoided during fabrication or operation, making it crucial to understand the physical processes behind these issues to model them and consider the possible alterations on the device performance for circuit designs.

Various theoretical and experimental approaches are used to identify and study specific defect candidates. These include Density Functional Theory (DFT) and Technology Computer-Aided Design (TCAD) simulations for theoretical analysis, electrical examination tools, and physical characterization methods such as Electron Paramagnetic Resonance (EPR) spectroscopy and X-ray Photoelectron Spectroscopy (XPS). Thereby, researchers study the trapping properties of these defects to understand their impact on device performance better.

As technology advances to each new node, emerging requirements necessitate a comprehensive understanding of the effects of defects to ensure proper design and manufacturing processes. Continuous research is crucial as new materials and device structures emerge, and novel defect types may arise, further expanding the limits of electronics technology. In this chapter, the most significant known defect candidates for interface and oxide defects to date will be discussed.*Parts of this chapter have been previously published in the work of Waldhoer et al. [49] and the PhD theses of Stampfer [50] and Michl [51].*

2.1 Interface Defects

The process of manufacturing devices often leads to defects in the interfacial layer between the semiconductor substrate and insulating layer due to the structural mismatch between the materials. The density and configuration of these defects are highly influenced by the semiconductor and insulator materials used, the processing parameters, and the presence of other species during processing that may passivate these

defects. Limiting the formation during fabrication or passivation of these interface defects is a significant challenge in developing new material systems. For instance, the application of in-situ oxidation and hydrogen passivation has resulted in a low interface defect density of approximately $10^{10}/(\mathrm{cm}^2\mathrm{eV})$ in silicon devices [52]. This process optimization, combined with the high quality of the oxide, is a major factor in the continued success of the Si/SiO_2 material system in modern electronics.

The study of interface defects in silicon-based MOSFETs has a long-standing background. Characterization methods, such as electron spin resonance (ESR) also frequently referred to as electron paramagnetic resonance (EPR), have been extensively used to examine the nature of point defects in semiconductors and insulators. These techniques analyze the interaction between microwave absorption or carrier generation/recombination processes and a magnetic field, thereby enabling the investigation of the composition of these defects. Specifically, the interaction occurs with unpaired electrons found in unsaturated atomic bonds. In the case of a semiconductor-insulator system, these paramagnetic point defects can function as trapped charges, thereby altering the device's parameters. As a result, ESR investigations play a crucial role in the study of device degradation.

The inherent mismatch in crystal structure between silicon (Si) and the amorphous layer of thermally grown silicon dioxide (SiO_2) gives rise to unsaturated bonds at the interface of these two materials [53]. These unsatisfied bonds can be observed using ESR and are referred to as dangling bonds on a silicon atom at the Si/SiO_2 interface (referred to as *P*b center), distinguished by their anisotropy and Landé g-factor [54]. The orbitals associated with these bonds can accommodate up to two electrons and exhibit two trap levels within the substrate bandgap. A schematic of "dangling" bonds can be seen in Figure 2.1. These specific point defects have been linked to interface traps that can be electrically measured.

In the 1960s, Nishi et al. [55] conducted a pioneering study and discovered three distinct types of defect signatures on (111) interfaces. Later, similar P_b centers were identified on (110) and (100) surfaces [56, 57]. The original P_b center ($\cdot Si \equiv Si3$) is now known as the P_{b0} center on (110) surfaces, while chemically different P_{b1} centers, which are suspected to be oxidized P_b centers ($\cdot Si \equiv Si_2O$), were also found on (100) surfaces [58]. The centers which are known to occur in various chemical variations, include the P_{b0} center in the form of ($\cdot Si \equiv Si_3$) and the P_{b1} center. However, the atomistic structure of the latter still needs to be fully understood.

High densities of interface defects pose a significant challenge, as they can negatively impact the controllability of carrier density in the channel and increase noise in the channel current. The trapped charges at interface defects can perturb the electrostatic surface potential, reducing the channel's mobility due to Coulomb scattering and leading to long-term degradation of device parameters. This issue can be exacerbated by hot carrier stress, which can cause the depassivation of previously passivated interface defects, thereby increasing the number of electrically active interface defects.

In addition to ESR measurements, other techniques are used to study interface

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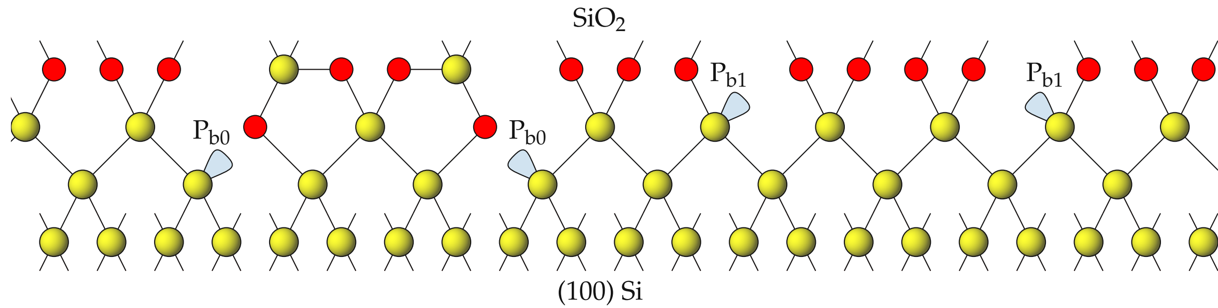

Figure 2.1. At the interface of Si/SiO_2 with a (100) orientation, *P*b centers can manifest in two chemical forms: the P_{b0} center, characterized by the $(\cdot\mathrm{Si} \equiv \mathrm{Si}_3)$ structure, and the P_{b1} center, whose atomic structure is not fully comprehended. The dangling bond without a pair of electrons is depicted by blue triangles in the figure, which has been reproduced from [58].

defects include capacitance-voltage (CV) measurements, charge pumping (CP) measurements, deep-level transient spectroscopy (DLTS), and direct-current current-voltage (DCIV) measurements. While these techniques provide information on the average properties of the defects, they do not allow the study of the impact of charge capture and emission at individual interface states on device behavior.

2.2 Oxide defects

In earlier research on MOSFET reliability, interface defects were the primary focus of the investigation, but as the understanding of device degradation advanced, defects in the bulk oxide were also considered as part of a more comprehensive analysis. The defects located within a device's insulating oxide layer can seriously impact its performance. These oxide defects, also known as border states, can form naturally during oxide growth or as a result of impurities or distorted chemical bonds within the oxide. Oxide defects can exchange charges with both the gate and channel, although the process is typically slower compared to interface defects. This is due to the spatial separation between the defect and the charge reservoirs, the large structural relaxation that occurs at the defect site of commonly studied oxide defect candidates. The energy level of oxide defects shifts with the applied gate bias, leading to a strong dependence of their charge capture and emission rates on the gate bias. A charged oxide defect can interact with carriers in the inversion layer, reducing the local carrier density and affecting the mobility in the subthreshold regime and the threshold voltage of the device. Despite the variations among these oxide traps, they have all been associated with BTI, as they can exchange charge carriers with the substrate. Current research is focused on the precise physical description of this process, including its dependence on the oxide field and temperature.

In small gate area devices, the impact of charge trapping at oxide defects can be particularly significant. This is because the smaller capacitance of these devices leads to each defect having a larger impact on the surface potential and ,thus, the threshold voltage shift. The magnitude of the perturbation of a charged defect on the channel

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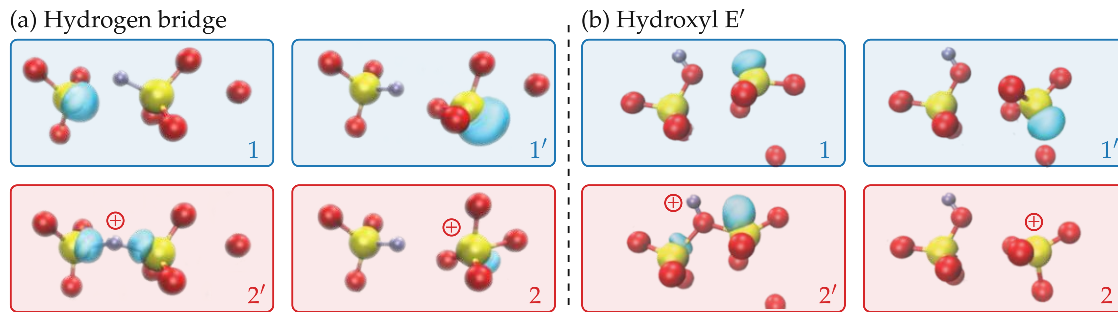

Figure 2.2. Ball-and-stick representations of two potential hole trap candidates in amorphous SiO2: (a) the hydrogen bridge and (b) the hydroxyl E′ center. In these models, silicon atoms are yellow, oxygen atoms are red, and hydrogen atoms are gray. The blue clouds depict the spin density for neutral defects, signifying the location of the unpaired electron, while for positive defects, they illustrate the distribution of the captured hole. Both defects can exist in four configurations, with two being neutral (states 1 and 1′) and two being charged (states 2 and 2′). Figures adapted from [59, 60]

current depends on its distance from the channel and its position relative to random dopants. In these devices, even a single charged oxide defect can significantly reduce in the source-drain current due to its effect on the percolation path in the channel.

2.2.1 Oxide Defects in SiO_2

Silicon dioxide (SiO_2) is a dielectric material that has been extensively studied in MOSFET devices. Recent research suggests that hydrogen-related defects, such as hydrogen bridges (HB) and hydroxyl-E′ centers (H-E′), are responsible for degradation phenomena like BTI and RTN [61].

During device processing, hydrogen is commonly used to passivate dangling bonds at the interface between the semiconductor and SiO_2. As a result, it is highly likely that defects involving hydrogen are formed [61]. Furthermore, hydrogen can easily diffuse in the SiO_2 layer, where it can form electrically active defects. Figure 2.2 shows the neutral (1) and positive (2) charge states of the two defect candidates containing hydrogen.

When the H atom binds to a Si atom, the resulting defect configuration that involves two Si atoms is called a hydrogen bridge (HB). The HB can capture a hole and form a stable positive configuration known as a puckered state, which can transit between unpuckered and puckered states through metastable states. Hydrogen atoms can also bind with the oxygen atom and form a hydroxyl-E′ center. These defects can only occur in a-SiO_2 and require strained Si-O bonds to form. In contrast to oxygen vacancies, hydrogen-related defects have trap levels close to the Si band edges, as shown in Figure 2.3 and are, therefore, more important for understanding the mechanisms behind RTN and BTI.

Most defect studies have focused on charge trapping resulting from known defect candidates. However, there have been some experimental studies that require the

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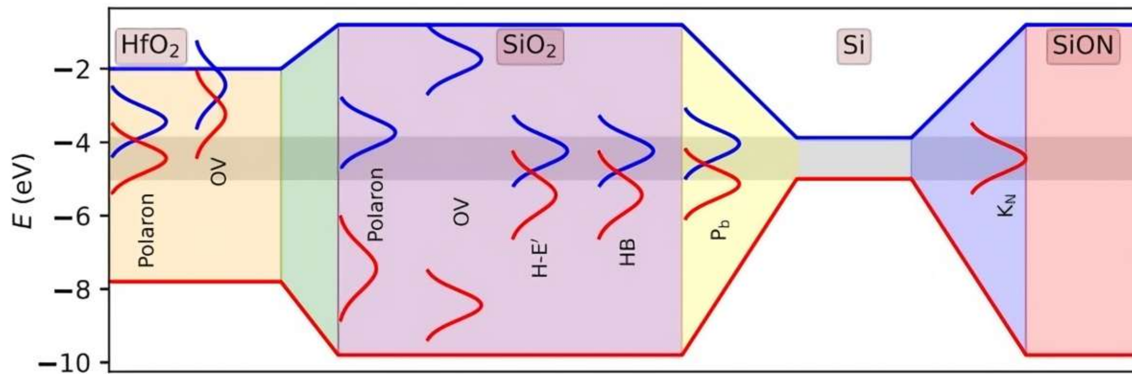

Figure 2.3. The various defect candidates studied in SiO_2, HfO_2 and SiON have trap levels distributed throughout the band gaps of these materials. Oxygen vacancies (OV) have trap levels distant from the silicon conduction band, thus having a limited impact on BTI and RTN. Conversely, the trap levels of hydrogen-related defects like the hydroxyl-E_k center or the hydrogen bridge, along with interface defects such as the P_b center or the KN center, are near the silicon band edges, making them significantly relevant for BTI. Moreover, intrinsic charge trapping due to polarons is a key factor for electron trapping in high-κ devices. Originally published in [51].

existence of trap bands that cannot be directly linked to any known defects [62]. This type of charge trapping can have a significant impact on wide bandgap devices, such as Silicon Carbide (SiC). It can also occur spontaneously in a-SiO_2 and is caused by structures with elongated Si-O bonds, which facilitate the localization of an additional electron at a certain Si atom. The trap band of these structures lies close to the conduction band edge of Si, as shown in Figure 2.3.

Unlike interface defects, oxide defects have a more complex atomic structure that enables them to exist in multiple configurations with the same net charge. Typically, the transition from one stable configuration to another via a metastable state occurs when one of the silicon atoms transitions through the triangle formed by three oxygen atoms, resulting in a so-called puckered configuration. Due to the amorphous nature of SiO_2, these defects exhibit a wide range of properties, such as their trap levels and transition barriers, which contribute to the observed variety in time constants mentioned earlier.

2.2.2 Oxide Defects in SiON

Plasma-nitrided oxides (PNO) are commonly used in silicon technology to reduce gate leakage current [63]. However, a high concentration of nitrogen atoms at the oxide-semiconductor interface can result in a large amount of K_N centers. The K_N centers are characterized by silicon dangling bonds, where silicon is bonded to three nitrogen atoms, potentially with oxygen as second-nearest neighbor atoms [64]. These K_N centers are situated within the amorphous silicon oxynitride layer and exhibit electrical properties as interface states and bulk dielectric defects. They serve as sites for recombination and tunneling. Notably, the negative bias temperature instability observed in these plasma-nitrided gate stacks does not involve the formation of P_{b0}, P_{b1}, or E' centers

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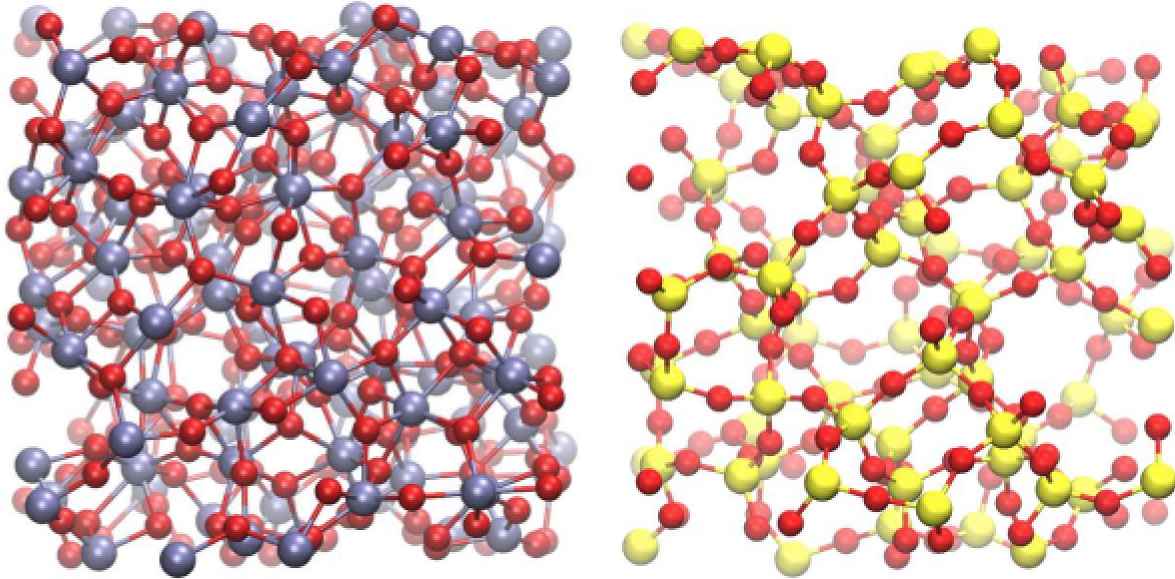

Figure 2.4. The structural arrangement of a-HfO_2 (with Hf represented by silver and O represented by red) exhibits a greater level of disorder compared to a-SiO_2 (with Si represented by yellow and O represented by red). This disparity in disorder serves as a potential cause for intrinsic charge trapping, which could provide an explanation for the PBTI behavior observed in high-κ devices. Figure taken from [49].

[63]. Although the defect candidates of near-interface defects change, hydrogen-related defects can still play a major role in nitrided oxides, as H atoms are used for passivating P_b centers [65]. K_N centers have a much narrower distribution of their energetic trap levels than P_b centers, which are broadly distributed with at least two peaks, one directly above and one directly below the midgap. The energetic trap level distribution of K_N centers is very close to the Si midgap, as seen in Figure 2.3 [66].

2.2.3 Oxide Defects in HfO_2

The scaling of MOSFETs has led to the physical thickness of insulator to be a few nm to maintain channel control. However, as the thickness of the insulator decreases, leakage currents increase, leading to several problems, such as higher of-state power consumption, heat dissipation, and a decrease in insulator reliability. Therefore, alternative insulators with larger dielectric constants, such as HfO_2 (ε_r = 25), ZrO_2 (ε_r = 25), or Al_2O_3 (ε_r = 9.1), have become necessary to increase gate capacitance without introducing leakage effects, as SiO_2 (ε_r = 3.9) is no longer sufficient.

Compared to SiO_2, HfO_2 exhibits a higher degree of disorder, as depicted in Figure 2.4, and intrinsic charge trapping is suspected to be a central reliability issue in HfO_2-based oxides [67]. HfO_2 is a non-glass-forming oxide, resulting in varying coordination numbers depending on the oxide phase, and it can partially crystallize during annealing, introducing additional structural uncertainties [68]. These factors result in various defect candidates, making the modeling of HfO_2 insulators extremely challenging. It has been suggested that HfO_2 can form electron polarons [69], which can be stable at room

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temperature and could be responsible for positive bias temperature instability (PBTI). Uncoordinated Hf ions, capable of trapping electrons, drive the formation of electron polarons. An electron trapped in this manner can localize at multiple Hf sites, forming a ring where the Hf atoms are drawn towards the center, while the O anions are pushed outward [70].

Certain defect types discovered in amorphous silicon dioxide (a-SiO_2) have been identified in amorphous hafnium dioxide (a-HfO_2). One such example is the occurrence of oxygen vacancies (OV) in HfO_2, which can exist in neutral, positive, and negative states [71]. In HfO_2, due to the presence of ionic bonding, oxygen vacancies exhibit behavior similar to F-centers in ionic crystals. This means that any additional charges are concentrated within the vacancy, resulting in strong localization of the charges [72]. It has been suggested that the negative states of OV might be responsible for the abundance of electron traps observed in high-κ devices [73]. Previous studies have reported trap levels ranging from 1.2 eV to 1.8 eV below the conduction band of HfO_2 [73]. However, recent investigations utilizing first-principle calculations propose that the energy level of oxygen vacancies is located just below the conduction band of HfO_2 [74] and is therefore oxygen vacancies cannot be directly used to explain the experimental results [49] based on the optical [74] and electrical measurements [66].

In addition to their potential function as charge traps, the presence of oxygen vacancies in hafnia-based RRAM devices is being studied as a potential cause of resistive switching. It has been observed that when electrons are injected into HfO_2, oxygen vacancies and interstitial 0^{-2} ions can form Frenkel-pairs. Additionally, preexisting oxygen vacancies can act as electron traps, which can facilitate the formation of these Frenkel-pairs nearby, resulting in a stable divacancy [75]. This process suggests that oxygen vacancies may aggregate, leading to a significant reduction of resistivity due to the formation of a conductive filament.

2.3 Semiconductor substrate defects

Defects of the semiconductor substrate can be introduced intentionally during device manufacturing through the introduction of dopants to control conductivity and other parameters or unintentionally due to contamination resulting in deep-level impurities. Bulk defects have a secondary role in inversion layer devices and are only significant in systems where proper operation requires a certain minority lifetime, such as CMOS optical sensors, RAM, or photodiodes. The presence and concentration of bulk defects can be quantified using DLTS and various physical or chemical methods. However, as this thesis focuses on the reliability issues related to oxide and interface defects, bulk defects will not be examined.

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Chapter 3

Physical Modeling of Charge Transfer Reactions Involving Defects

Detailed modeling is essential to comprehend the impact of defects on the function of devices. For this purpose, two different approaches are mainly utilized, empirical and physics-based. Empirical models rely on simplistic analytical formulas to describe measurement data, whereas physics-based models aim to explain the device behavior based on the superposition of the impact of single defects. To facilitate reliability studies of MOSFETs and simulate this process, it is crucial to mathematically describe the physical process and statistical distribution of properties of trapping and de-trapping. It is important to note that charge trapping is a dynamic process influenced by several factors, including the defect's applied biases, temperature, and intrinsic properties, such as its trap level and relaxation energy. Therefore, developing a comprehensive theoretical model that considers all aspects of charge trapping poses a significant challenge. In this chapter, the focus is on physical-based models that describe the charge-trapping kinetics of defects and their interaction with a device. The statistical models will be discussed later in this work. *Parts of this section are based on the work of Grasser et al. [76, 23] and the PhD thesis of Stampfer [50].*

3.1 Modeling Defect Interactions with Markov Chains

Charge trapping models have been developed to describe the dynamic charging and discharging processes in individual defects. In the context of this research, various defect models have been discussed, all of which utilize a continuous-time Markov chain [77] to mathematically represent the charged state of defects. However, the fundamental differences among these models lie in how they interpret the transition rates between different states and the number of possible states within the Markov chain.

The core principle of using Markov chains to model defects is based on the Markov property assumption. This property posits that defects have no memory of past states and their future behavior is determined exclusively by their current state. Consequently, defects exhibit a memoryless nature in this modeling framework.

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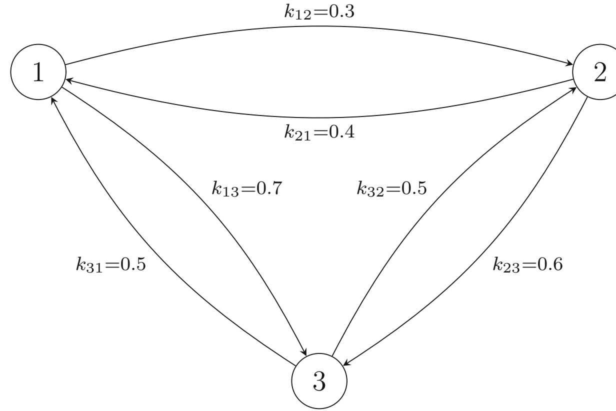

Figure 3.1. Example of Markov chain with three discrete states. The arrows indicate the transition rates between the states.

Markov chains are characterized by a finite set of states, with a defect always existing in one of these states at any given time. The behavior of a Markov chain can be described in terms of probabilities. The probability of a defect being in any of the n states at time t is represented by the state vector $\vec{P}(t)$. This model requires that the sum of the probabilities P_i for each state i equals one:

$$\sum_i P_i(t) = 1 \tag{3.1}$$

Following conventional Markov process theory the transition probabilities from state i to state j can be written as:

$$P\{X_j(t+h) = 1 \mid X_i(t) = 1; i \neq j\} = k_{ij}h + O(h), \tag{3.2}$$

with h being an infinitesimally small time step, $\lim_{h\to 0} \frac{O(h)}{h} = 0$, and k_{ij} as the transition rate. The probability that the defect stays in state i can be written as:

$$P\{X_i(t+h) = 1 \mid X_i(t) = 1\} = 1 - h\sum_{\substack{j \\ i\neq j}} k_{ij} + O(h) \tag{3.3}$$

The transition rates from state i to j are denoted as k_{ij} and can be expressed as the $n \times n$ transition matrix K. An example of a Markov chain in equilibrium is shown in Figure 3.1. The temporal evolution of $\vec{P}(t)$ can be described by the so-called master equation [78]:

$$\frac{dP_i(t)}{dt} = \sum_{i\neq j}(P_j(t)k_{ji} - P_i(t)k_{ij}) \tag{3.4}$$

This equation contains the individual transition rates k between the states, which are described by the physical defect model. The diagonal elements in matrix K are assigned to represent the dwelling times, which refers to the duration during which no transitions

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occur,

$$k_{ii} = 1 - \sum_{i \neq j} k_{ij}, \tag{3.5}$$

the master equation can be expressed in the form of a vector:

$$\frac{d\vec{P}}{dt} = K\vec{P}, \tag{3.6}$$

where K represents the the matrix of connections. The transition rate matrix K for the Markov chain depicted in Figure 3.1 is as follows:

$$K = \begin{pmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{pmatrix} = \begin{pmatrix} 0 & 0.3 & 0.7 \\ 0.4 & 0 & 0.6 \\ 0.5 & 0.5 & 0 \end{pmatrix}$$

After this general mathematical framework is established, it is important to link these parameters with the physical properties of defects. The following sections examine the physical models that define the states within the Markov chain and the transition rates between these states.

3.2 SRH-like models for the transition rate

In the early 1950s, William Shockley, William T. Read, and Robert N. Hall developed the Shockley-Read-Hall (SRH) model, also known as trap-assisted generation/recombination [79]. This model provides a theoretical framework for studying how excess carriers and defects in semiconductor materials interact. The SRH model, which was originally developed for recombination centers situated within the bulk of a semiconductor where both the defect and carrier reservoirs are positioned at the same location, has been expanded to include trapping within oxides.

3.2.1 Recombination through defects - SRH model

According to the SRH, defects can exhibit both charged and neutral states. Acceptor-like defects, for example, capture an electron during charge trapping and subsequently acquire a negatively charged state. On the contrary, donor-like defects release an electron, resulting in a positively charged state. Typically, the SRH model applies to bulk defects within the semiconductor substrate material and does not encompass oxide defects.

The SRH model defines four separate processes, as demonstrated in Figure 3.2, to calculate the carrier transition rates between defects and a reservoir, such as a channel and gate in a MOS transistor.

The SRH model outlines four possible scenarios concerning trap levels:

- An electron in the conduction band may get trapped within an intragap state.

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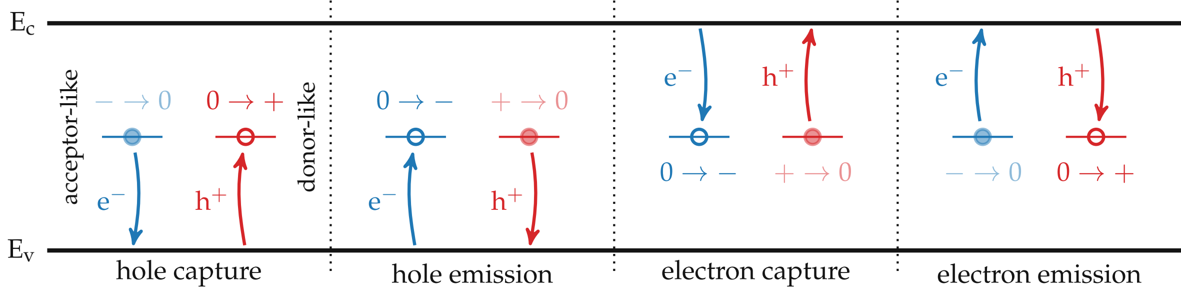

Figure 3.2. The band diagram schematically represents the capture and emission mechanisms for acceptor-like traps (depicted in blue) and donor-like traps (shown in red). As electron traps transition between neutral and negatively charged states, hole traps fluctuate between neutral and positively charged states. The diagram portrays the initial states of the defects before the occurrence of the specified transition. Figure adapted from [50]

- An electron can be released from a trap level and enter the conduction band.
- A hole located in the valence band may get captured by a trap, similar to an occupied trap releasing an electron into the valence band.
- A trapped hole can also be released into the valence band, equivalent to an electron being captured from the valence band.

It is assumed that a defect is in one of its two states, 1 for neutral and 2 for positive. The expectation values for the defect to be in either state are f_1 and f_2, with $f_1 + f_2 = 1$. We consider a system consisting of a defect plus an electron that can be moved back and forth between the defect and the reservoir. When the electron is at the defect site, its energy is E_1, when it is moved to the reservoir, the energy changes to E_2.

The capture rate is obtained by integrating the differential transitional rates over the interacting band:

$$dk_{12}(E) = c_p(E) f_p(E) g_p(E) dE \tag{3.7}$$

$$k_{12} = \int_{-\infty}^{E_v} c_p(E) f_p(E) g_p(E) \mathrm{d}E \tag{3.8}$$

where f_p is the hole occupancy probability given by the Fermi-Dirac distribution, g_p is the density of states and c_p is the capture coefficient.

The emission rate is given by:

$$dk_{21}(E) = e_p(E) f_n(E) g_p(E) dE \tag{3.9}$$

$$k_{21} = \int_{-\infty}^{E_v} e_p(E) f_n(E) g_p(E) \mathrm{d}E \tag{3.10}$$

where $f_n(E) = 1 - f_p(E)$ is the electron occupancy probability and e_p the emission coefficient.

Assuming thermal equilibrium, the probability of the defect being neutral, $p_1 = f(E_1)$, and capturing a carrier at a specific energy must be balanced with the probability

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of it being charged, p_2, and emitting a carrier at that energy:

$$p_1 c_p(E) f_p(E) = p_2 e_p(E) f_n(E) \tag{3.11}$$

Assuming that the hole capture from the valence band occurs without a barrier, the probability of charge capture is given by:

$$c_p \approx v_{\mathrm{th}} \sigma \tag{3.12}$$

where $v_{th} = \sqrt{\frac{8k_{\mathrm{B}}T}{\pi m^*}}$ is the thermal velocity of the carriers in the reservoir, k_B is the Boltzmann constant, T is the lattice temperature, m^* is the effective mass of the carrier, and σ is the capture cross section, that is, the effective area within which a charge has to pass to be captured by a defect [80].

The emission probability e_p can be related to the capture probability c_p and the energy of the captured carrier E_1:

$$e_p(E) = c_p(E) \frac{p_1}{1-p_1} \frac{1-f_n(E)}{f_n(E)} = c_p(E) e^{\left(-\beta(E_1-E_f)\right)} e^{\left(\beta(E-E_f)\right)} \tag{3.13}$$

where $\beta = (k_B T)^{-1}$ and E_f is the Fermi energy. Assuming Boltzmann statistics, the probability p can be expressed as:

$$p = N_{\mathrm{v}} e^{(\beta(E_{\mathrm{v}}-E_{\mathrm{f}}))} \tag{3.14}$$

where N_{v} is the valence band weight.

By approximating all carriers to be concentrated at the band edges, which is known as band edge approximation [66], the capture and emission rates can be expressed as:

$$k_{12} = p v_{\mathrm{th}} \sigma \tag{3.15}$$
$$k_{21} = N_v v_{\mathrm{th}} \sigma e^{(\beta(E_v - E_1))} \tag{3.16}$$

Capture and emission rates can be extended to oxide defects by including a Wentzel-Kramers-Brillouin tunneling coefficient λ in σ to account for elastic tunneling between the defect and the carrier reservoirs. However, this model cannot accurately describe the bias-dependence or temperature-dependence of defects observed during BTI characterization experiments, and modified equations must be used to model defects located energetically above or below the band gap.

3.2.2 Kirton Uren model

Due to its limited ability to explain the temperature dependence observed in measurements related to oxide defects, the SRH model does not provide an accurate framework to describe the experimental measurements related to charge trapping processes. This suggests the presence of a non-radiative multi-phonon (NMP) process. In response,

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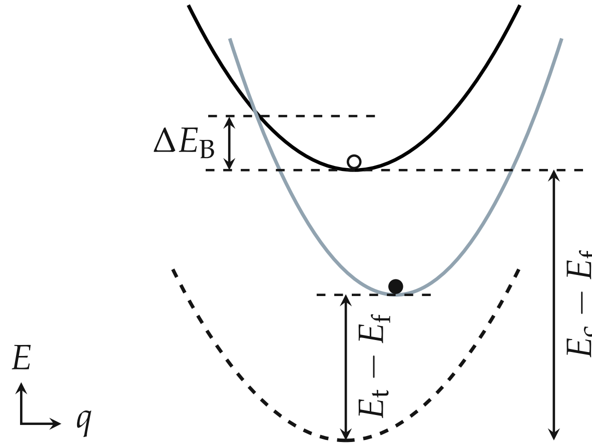

Figure 3.3. The configuration coordinate diagram depicts the Kirton-Uren model, where a defect interacts with the reservoir through electron exchange. The position of the parabola is determined by the energy of the carrier. The thermal activation involved in the capture process is represented by the capture barrier, denoted as ΔE_B. In the diagram, the empty defect with an electron in the conduction band is depicted in black, while the captured electron at the defect site is shown in grey. The dashed line represents the energy zero of the system, corresponding to the empty defect with an electron at the Fermi level. This diagram is based on [80, 50].

Kirton and Uren [80] developed an improved approach that considers structural relaxation of defects. They recognized that multi-phonon processes were involved in the charge trapping reactions to explain the temperature dependence of charge trapping at oxide defects. To take this into consideration, they introduced a phenomenological Boltzmann factor into the effective capture cross section [80]:

$$\sigma = \sigma_0 \lambda e^{(-\beta \Delta E_\mathrm{B})}. \tag{3.17}$$

In this equation, ΔE_B represents the energetic capture barrier between the two equilibrium positions of the defects charge states, as shown in Figure 3.3. By introducing this additional term, the Kirton-Uren model is capable of modeling the temperature dependence of 1/f noise and the average charge transition times. However, it should be noted that the Kirton-Uren model introduces a correlation between the capture rate and the emission rate, which is not observed during BTI characterization experiments. Additionally, the barrier is independent of gate bias and, therefore, fails to describe the bias dependence of charge trapping accurately.

3.3 Non-Radiative Multi-phonon Model

The NMP model [81, 82, 76] has been developed to extend the limitations of the aforementioned models in describing bias-dependent phonon-assisted charge transfer from and to oxide defects. Kirton Uren model is inadequate for describing the bias dependence, as it does not consider the shift of the trap level of the defect due to the

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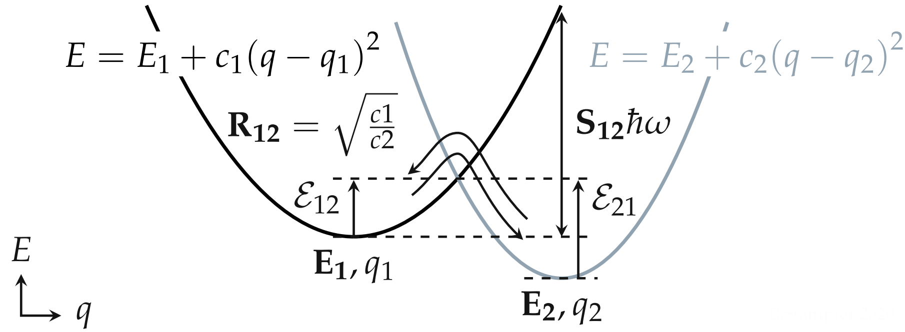

Figure 3.4. Potential energy surfaces (PESs) with a parabolic shape for the charged (depicted in grey) and neutral state (depicted in black) as employed in the NMP defect model, accompanied by the model's parameters. This representation is recreated based on [50].

gate bias, which is observed in measurements.

3.3.1 The 2-State Non-Radiative Multi-Phonon Model

The process of charge transition in a physical system involving electrons and nuclei can be described using the NMP model. The model divides the transition into an electronic part and a vibrational part, since electrons move much faster than the nuclei, using the Born-Oppenheimer approximation [83]. To accurately describe the entire system in the physical defect model surrounding phonon bath needs to be included with all the involved electrons and nuclei. This enables an accurate description of the structural reconfiguration that occurs at the defect site as a result of changing charge states and the electrostatic shift of the trap level due to the oxide field. The process of deformation involves the emission and absorption of phonons, which must be taken into account in the model to ensure an accurate representation of the system.

The transition from one state to another is associated with an energetic barrier, which is determined by a transition state on the potential energy surface (PES), i.e. the highest point along the minimum energy transition path. PES is a complex 3N-dimensional surface for a system with N atoms. Accurate PES of the charge states of a defect structure can be computed by employing DFT, but to obtain a usable model, the multidimensional PES is reduced to one dimension along a reaction coordinate, described by the lowest energy path between the states. Finally, in this approach, PES is substituted with a Taylor expansion centered around the minimum, and this expansion is limited to the quadratic term. This method allows for the depiction of defect states as harmonic oscillators. Consequently, a configuration coordinate diagram is created, featuring parabolic potential energy curves, as illustrated in Figure 3.4.

The Born-Oppenheimer approximation, Frank-Condon principle, and Fermi's golden rule allow the transition rate from one state to another to be expressed as $k_{ij} = A_{ij} f$ [84, 85, 86]. Here, A is the electronic matrix element between the initial and final electronic states, and f is the line shape function. However, since the electronic matrix element cannot be calculated for the systems of interest, it is commonly approximated using a WKB tunneling factor and a prefactor. The line shape function can be calculated,

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but is often simplified by neglecting nuclear tunneling [87] below the highest point in the minimum energy path. This leads to transitions occurring at the intersection point of the PES, and the line shape function is written as a Dirac function at the energy of intersection in the classical limit [88]. The energy barrier between the two states can be determined from the intersection of the two PESs. In the semiclassical regime, the transition can be modeled using a Boltzmann factor based on this barrier energy, provided tunneling below the barrier can be ignored.

To model the system, it is necessary to parameterize the two parabolas. Standard parameterization involves the ratio of curvatures $R = \sqrt{c1/c2}$, the relaxation energy $S\hbar\omega$, the Huang-Rhys factor S, and the ground state energies E_1 and E_2. Note that this parameterization eliminates the reaction coordinate between the states, which is necessary for nuclear tunneling calculations, but not required in the semi-classical approximation. Using these parameters and $E_{21} = E_2 - E_1$, it is possible to calculate the energy barrier between state 1 and state 2.

$$\mathcal{E}_{12} = \frac{S\hbar\omega}{(R^2-1)^2}\left(1 - R\sqrt{1 + \frac{S\hbar\omega + (R^2-1)E_{21}}{S\hbar\omega}}\right)^2 \tag{3.18}$$

If R = 1, there is a singularity, and the energy can be calculated using:

$$\mathcal{E}_{12} = \frac{(S\hbar\omega + E_{21})^2}{4S\hbar\omega} \tag{3.19}$$

The backward barrier can be calculated using:

$$\mathcal{E}_{21} = \mathcal{E}_{12} - E_{21} \tag{3.20}$$

For the two-state NMP defect model, the capture and emission rates can be calculated using the following equations, with the valence band and band edge approximation:

$$k_{12} = p v_{\mathrm{th}} \sigma_0 \lambda e^{(-\beta\mathcal{E}_{12})} \tag{3.21}$$

$$k_{21} = N_V v_{\mathrm{th}} \sigma_0 \lambda e^{(\beta(E_{\mathrm{V}}-E_1))} e^{(-\beta\mathcal{E}_{21})} \tag{3.22}$$

where p is the hole concentration in the channel, v_{th} is the thermal velocity, σ_0 is the capture cross-section, λ is the Debye length, β is the reciprocal of the thermal energy, E_{V} is the energy at the valence band edge, and N_{V} is the density of states at the valence band edge.

3.3.2 The 4-State Non-Radiative Multi-Phonon Model

Single defects can exhibit more than one characteristic dwelling times within the same charge state. Consequently, a single state needs to be splitted into two, as demon-

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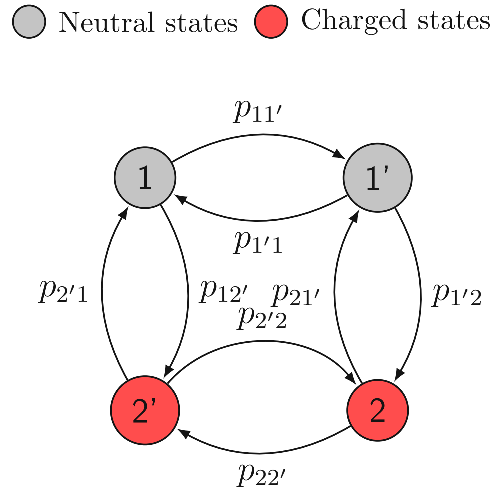

Figure 3.5. The four-state NMP model characterizes the capture and emission times of individual defects in response to changing biases and temperatures. Broadly, the model considers two stable states, 1 (neutral) and 2 (charged), as well as two meta-stable states, 1' and 2'. It is crucial to consider these states when trying to accurately represent the emission times and other related characteristics that are dependent on bias [76].

strated by single-defect measurements like RTN and time dependent defect spectroscopy (TDDS). In RTN measurements, this phenomenon is observed as anomalous RTN (aRTN), where inactive periods of the defect alternate with active periods of RTN signal [25]. Similarly, TDDS measurements have shown that individual defects may vanish for several measurements and then reappear. These empirical observations, combined with insights from DFT calculations for potential defect candidates, have led to the development of the four-state defect model [60, 89].

The four-state defect model described by a Markov chain, seen in Figure 3.5, considers defects to be both meta-stable and stable for both charged (depicted in red) and neutral charge states (depicted in grey). The transitions between the neutral and charged states, i.e., $1 \leftrightarrow 2'$ and $1' \leftrightarrow 2$, are modeled as NMP transitions. On the other hand, the transitions between states of the same charge are modeled by purely thermal reactions with energetic barriers of constant height. The resulting energy profiles along the multiple reaction paths of such a defect are schematically illustrated in Figure 3.6.

Although the 2-state NMP theory is efficient for describing BTI on large-area devices where large ensembles of defects are at the same time capturing or emitting charge, certain phenomena cannot be explained with only two states. An example of this is the observation of anomalous RTN (aRTN), in which the RTN signal is interrupted for longer periods [25]. This behavior can only be explained by introducing an additional third state [3]. A defect captures and emits a high frequency charge transitioning between states 1 and 2. After a certain time, a transition between state 2 and 2' occurs, and the defect stays for a comparably long period in state 2'. By utilizing the intricate potential energy surfaces depicted in Figure 3.6, it becomes possible to represent the two NMP and the two thermal transition rates [76]. These rates facilitate the determination of the total capture and emission time required to transition from one stable state to another.

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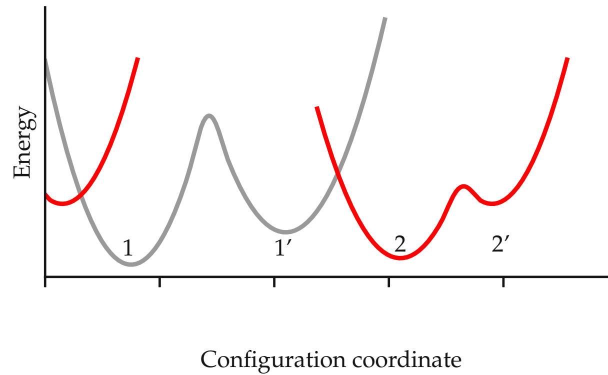

Figure 3.6. The four-state NMP model characterizes the capture and emission times of individual defects in response to changing biases and temperatures. Broadly, the model takes into account two stable states, 1 (neutral) and 2 (charged), as well as two meta-stable states, 1′ and 2′. These states are essential for accurately depicting the bias-dependent emission times and other associated attributes [76].

Applying Markov theory, the probability p_i of a defect being in state i can be calculated, which makes it feasible to conduct reliability simulations.

According to this model, a defect in a device can switch between charged and neutral states through two different routes. This helps to explain complex behaviors in defect capture and release times, as seen in RTN and TDDS measurements. This approach distinguishes between two different type of traps, namely fixed traps and switching traps [90]. Fixed traps have capture times that change with bias, but their release time might not depend on bias. This is because they use a specific pathway $(1 \rightarrow 2' \rightarrow 2)$ for both capture and release. The release time here mainly depends on a constant barrier between two states (2 and 2′). Switching traps, however, capture charges using the same pathway as fixed traps but release them through a different route $(2 \rightarrow 1' \rightarrow 1)$, resulting in bias-dependent rates for both capture and release. This approach has been used to understand the charge trapping behavior of various defects in different types of devices, including traditional silicon-based ones [76], those with high-κ gate stacks, and even 2D devices [91].

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Chapter 4

Reliability Simulations

Contemporary TCAD simulation tools, such as Minimos-NT [92, 93] and Sentaurus Device [94], incorporate a multi-state non-radiative multiphonon (NMP) model [76] to account for the influence of charge trapping on device performance and lifetime. However, these models often demand a comprehensive data set for precise modeling, rather than relying on just a few data points. Additionally, an excessively complex modeling approach might distract from the fundamental physics of charge trapping, which can often be adequately represented by a simplified 2-state NMP model [95, 96].*Parts of this chapter are based on the authors' previous publications [KTJ3, KTJ4] and the PhD thesis of Michl [51] and Rzepa [66].*

4.1 Compact Physics Framework (Comphy)

In line with this perspective, the Comphy (compact-physics) framework [66, 97, KTJ3, 95], which was jointly developed by imec and the Institute for Microelectronics at TU Wien, is used as the main simulation tool of this thesis. Comphy is a streamlined Python package aimed at simulating a range of charge-trapping related reliability concerns based on the 2-state NMP model within a concise 1D reliability simulator. It has been shown that Comphy can physically explain the average BTI degradation observed in large area MOSFETs, requiring a smaller set of defect parameters. This framework is particularly suitable for calculating BTI in SiO_2 and SiON devices which are studied in this thesis as a large number of defects can be efficiently handled, and physical defect parameters can be extracted by using established material parameters. The following section outlines the main physical models that provide the electrostatic quantities necessary to compute the charge transfer kinetics and transient ΔV_{th}.

4.2 Electrostatics

The depiction of electrostatics is crucial for every physical degradation model. This section will initially revisit the fundamentals of semiconductor modeling. Following that, these principles will be applied to resolve the electrostatics in a one-dimensional (1D) MOS device.

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4.2.1 Effective Density of States

The effective density of states in the conduction and valence bands, denoted as N_C and N_V respectively, can be expressed as follows [98]:

$$N_{\mathrm{C}} = 2\left(\frac{2\pi m_{n,\mathrm{eff}} k_{\mathrm{B}} T}{h^2}\right)^{3/2} M_{\mathrm{C}}, \tag{4.1}$$

$$N_{\mathrm{V}} = 2\left(\frac{2\pi m_{p,\mathrm{eff}} k_{\mathrm{B}} T}{h^2}\right)^{3/2}, \tag{4.2}$$

where M_C indicates the number of equivalent conduction band minima, $m_{p,\mathrm{eff}}$ is the effective mass of the valence band of silicon and $m_{n,\mathrm{eff}}$ is the effective mass of the conduction band of silicon [99].

4.2.2 Carrier Concentrations at Thermal Equilibrium

The intrinsic carrier concentration in a semiconductor n_i, is determined using the formula:

$$n_i = \sqrt{N_{\mathrm{C}} N_{\mathrm{V}}} e^{-\frac{E_{\mathrm{G}}}{2k_{\mathrm{B}}T}}, \tag{4.3}$$

the electron concentration n, is calculated from the $N_{\mathrm{C}}(E)$ across energy levels and their corresponding occupation probability $f(E)$, as follows:

$$n = \int_{E_{\mathrm{C}}}^{\infty} N_{\mathrm{C}}(E) f(E) dE, \tag{4.4}$$

where E_{C} is the conduction band minimum energy.

The occupation probability of states is given by the Fermi-Dirac distribution function $f_F(E)$, expressed as:

$$f_F(E) = \frac{1}{1 + e^{\frac{E-E_{\mathrm{F}}}{k_{\mathrm{B}}T}}}, \tag{4.5}$$

The thermal equilibrium electron concentration, n_0, with respect to the effective density of states in the conduction band, N_{C}, is represented by:

$$n_0 = \frac{N_{\mathrm{C}}}{2}\sqrt{\frac{\pi}{k_{\mathrm{B}}T}} \int_{E_{\mathrm{C}}}^{\infty} \sqrt{E - E_{\mathrm{C}}} \left(\frac{1}{1 + e^{\frac{E-E_{\mathrm{F}}}{k_{\mathrm{B}}T}}}\right) dE, \tag{4.6}$$

Since this integral cannot be evaluated analytically, approximations are generally used, with the Boltzmann and Joyce-Dixon [100] being the most common ones.

4.2.3 Fermi Level at Thermal Equilibrium

The thermal equilibrium Fermi level (E_{F_0}) in the channel of a MOS device that's been doped can be determined in the following manner : Suppose all dopants in the

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semiconductor are ionized; in this case, charge neutrality exists if

$$n_0 + N_A = p_0 + N_D, \tag{4.7}$$

where n_0 and p_0 are the intrinsic concentrations, N_A is the acceptor concentration and N_D is the donor concentration. For non-degenerate semiconductors in thermal equilibrium, where $n_{i2} = n_0 p_0$, for n-type semiconductors where $N_D > N_A$, we have [98]:

$$n_0 = \frac{(N_D - N_A)}{2} + \sqrt{\left(\frac{(N_D - N_A)}{2}\right)^2 + n_{i2}}, \tag{4.8}$$

$$p_0 = \frac{n_i^2}{n_0}, \tag{4.9}$$

$$N_D - N_A = n_i \exp\left[\frac{(E_{F_0} - E_i)}{(k_B T)}\right], \tag{4.10}$$

and similarly for p-type semiconductors, where $N_A > N_D$:

$$n_0 = \frac{n_i^2}{p_0}, \tag{4.11}$$

$$p_0 = \frac{(N_A - N_D)}{2} + \sqrt{\left(\frac{(N_A - N_D)}{2}\right)^2 + n_i^2}, \tag{4.12}$$

$$N_A - N_D = n_i \exp\left[\frac{(E_{F_0} - E_i)}{(k_B T)}\right]. \tag{4.13}$$

Hence, the intrinsic Fermi level E_i, can be used to compute E_{F_0} as:

$$E_i = \frac{(E_C + E_V)}{2} + \frac{k_B T}{2} \ln\left(\frac{N_V}{N_C}\right). \tag{4.14}$$

4.2.4 Electrostatics of a 1D MOS Structure

To determine the effective trap level of a defect relative to the carrier reservoirs in the channel, it is necessary to know the relationship between the applied gate bias and the surface potential at the interface between the channel and the oxide. Assuming that a uniform doping concentration and charge neutrality exist, deep in the bulk semiconductor (far from the interface), one can use the approximation of the surface charge Q_S as a function of the surface potential ϕ_S given by [98]:

$$Q_S = \pm\frac{\sqrt{2} k_B T}{q L_D}\sqrt{(e^{-\frac{\phi_S}{k_B T}} + (k_B T)\phi_S - 1) + \frac{n_0}{p_0}(e^{\frac{\phi_S}{k_B T}} - (k_B T)\phi_S - 1)}, \tag{4.15}$$

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where the positive sign refers to $\phi_S > 0$, while the negative sign is used for $\phi_S < 0$. The abbreviation $L_D = \sqrt{k_B T \epsilon_0 \epsilon_{r,chan} / p_0 q^2}$ is the Debye length for holes, where $\epsilon_{r,chan}$ is the relative permittivity of the channel. The channel concentrations for electrons n and holes p are calculated using the Joyce Dixon approximation [100]. The temperature dependence of the Si bandgap is computed using the model proposed by Bludau [101]. The effective masses for the valence band and the conduction band are taken from the models proposed by Lang et al. [102] and Green [99], respectively.

One can derive an equation for surface potential ϕ_S by using electrostatic considerations [97]. The equation for an ideal, defect-free, MOS device can be written as:

$$\frac{Q_S(\phi_S)}{C_{ox}} + \phi_S - V_G + \Delta E_W/q = 0, \tag{4.16}$$

Here, ΔE_W represents the work function difference defined as:

$$\Delta E_W = \Delta E_{W,gate} - E_{W,chan} \tag{4.17}$$

In this approach, while ΔE_W is an input parameter, it simultaneously depends on $E_{W,chan}$, which is clearly determined by the doping concentrations, also considered as input quantities. Consequently, the intrinsic work function difference $\Delta E_{W,0}$ is given by:

$$\Delta E_{W,0} = \Delta E_W - E_{F,0} \tag{4.18}$$

to derive ϕ_S, the following equation is solved through an iterative approach:

$$\frac{Q_S(\phi_S)}{C_{ox}} + \phi_S - V_G + \Delta E_{W,0}/q + E_{F,0}/q = 0, \tag{4.19}$$

The capacitance of the oxide is given by:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{r,ox} W L}{d_{ox}}, \tag{4.20}$$

where $\epsilon_{r,ox}$ denotes the relative permittivity of the oxide, W and L are the channel width and length, and d_{ox} is the thickness of the oxide. Equation (4.16) can be solved by using an iterative method like a Newton solver method, to obtain ϕ_S.

The trapped charges in the oxide can also be considered in the equation, which leads to the extension of Equation (4.16) as:

$$\frac{Q_S(\phi_S)}{C_{ox}} + \phi_S - V_G + \Delta E_{W,0}/q + E_{F,0}/q + V_{traps} = 0, \tag{4.21}$$

In this context, V_{traps} signifies the voltage shift due to oxide charge presence. Determining the surface potential ϕ_S is vital for surface potential-focused compact models, as it facilitates the calculation of the potential curve throughout the defect-free insulator. Using this data, the change in trap levels can be computed, and charge capture and

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emission rates can be assessed through the 2-state NMP theory. For a collection of defects, an average captured charge can be determined at each time interval, contingent on defect occupancy and density. The aggregate of all charge states results in a threshold voltage shift, producing a transient ΔV_{th} feature that can be contrasted with experimental findings. Evaluating the surface potential ϕ_{S} is a crucial component in the precise modeling of MOSFET behavior.

4.3 Occupation Probabilities

The previous section was dedicated to discussing the computation of device electrostatics. Each defect has a probability of being in either a charged or neutral state, as dictated by the transition rates derived from 2-state NMP theory. These rates enable the calculation of each trap's occupancy by solving master equations. These equations consider the interaction of each defect with various charge reservoirs r, including the valence and conduction bands of the channel and the gate in a MOSFET. The probabilities of a defect being in the initial or final state are represented as $p_{i,j}$, and the corresponding differential equations are as follows:

$$\frac{dp_{i(t)}}{dt} = -p_i \sum_{r=1}^{N_{\mathrm{R}}} k_{ij,r} + p_j \sum_{r=1}^{N_{\mathrm{R}}} k_{ji,r}, \tag{4.22}$$

$$\frac{dp_{j(t)}}{dt} = p_i \sum_{r=1}^{N_{\mathrm{R}}} k_{ij,r} - p_j \sum_{r=1}^{N_{\mathrm{R}}} k_{ji,r}. \tag{4.23}$$

The equations must satisfy the condition $p_i + p_j = 1$. In this context, $k_{ij,r}$ represents the electron emission rate, while $k_{ji,r}$ signifies the electron capture rate of the defect as it interacts with carrier reservoir r. For a defect, the total rates $k_{ij,r}$ and $k_{ji,r}$ are the cumulative sum of the rates across all N_{R} carrier reservoirs. In the Comphy framework, these carrier reservoirs include the valence band of the channel, the channel's conduction band, and the metal gate.

The solution to the differential equation system is expressed as:

$$p_j(t) = \frac{k_{ij}}{k_{ij} + k_{ji}} + \left(p_j(0) - \frac{k_{ij}}{k_{ij} + k_{ji}} \right) e^{-t(k_{ij}+k_{ji})}, \tag{4.24}$$

$$p_i(t) = 1 - p_j(t). \tag{4.25}$$

These equations can be employed to compute the perturbation of the electrostatic potential across the gate stack the impact of the defects on the potential, as demonstrated by the charge sheet approximation (CSA) [103, 104]:

$$V_{\mathrm{traps}} = -\frac{q}{C_{\mathrm{ox}} N_{\mathrm{T}}} \sum_{n=1}^{N_{\mathrm{T}}} p_{\mathrm{j}}(t)(1 - \frac{x_{\mathrm{T},n}}{d_{\mathrm{ox}}}) \tag{4.26}$$

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Subsequently, the device's surface potential is determined through Equation 4.19, which facilitates the computation of potential shift relative to the initial time step, thus determining the threshold voltage shift. The total threshold voltage shift is dependent on the probability of a charge transition, which is affected by factors like defect parameters, the applied gate voltage, and temperature, as illustrated in Figure 4.1.

4.4 Distribution of Defect Parameters

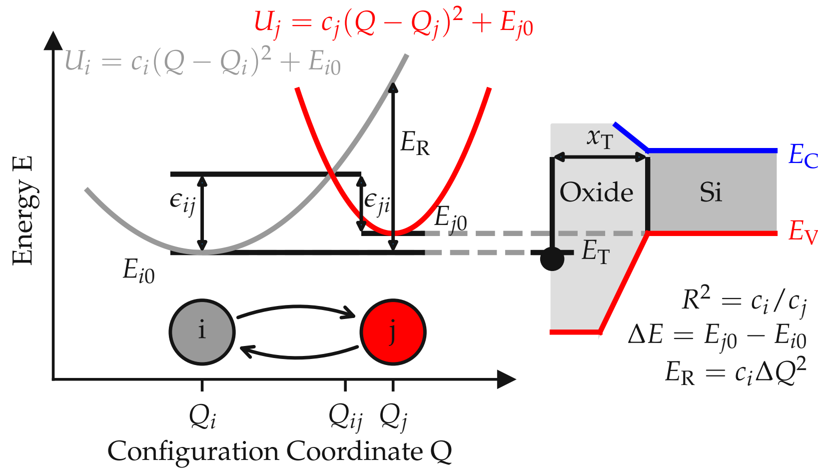

Figure 4.1. Comphy employs an effective 2-state NMP model to describe the charge transition of a pre-existing oxide defect. This transition from state i to state j occurs by overcoming the energy barrier ϵ_{ij}. The model's harmonic potential energy surfaces are characterized by the trap level E_T, the relaxation energy E_R, and the curvature ratio R. For the computation of the tunneling factor, the spatial coordinate x_T is employed. Figure taken from [KTJ4]

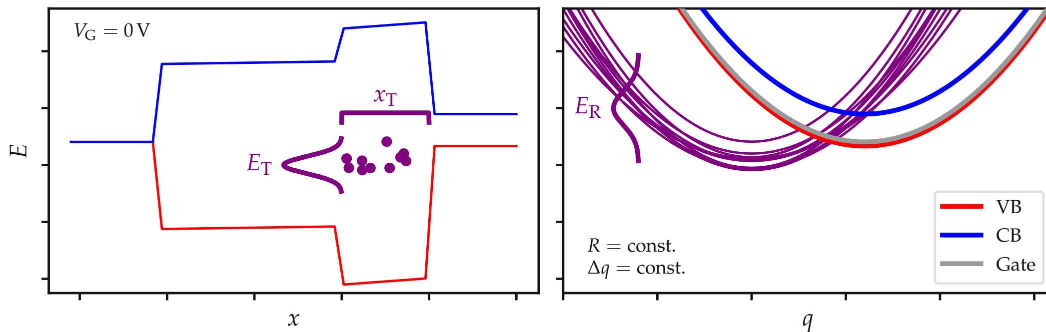

Figure 4.2. A defect can be characterized by the following parameters: relaxation energy (E_R), trap level (E_T), spatial position in the oxide (x_T), curvature ratio (R), and configuration coordinate offset (ΔQ). It is important to note that R and ΔQ are associated with the energy levels, while x_T is assumed to have a uniform distribution. Additionally, the energy levels follow a normal distribution within the defect bands. Recreated from [51]

Each defect is described by a set of model parameters, including the relaxation

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energy E_R, curvature ratio R, trap level E_T, spatial position inside the oxide x_T, and the configuration coordinate offset ΔQ (if a quantum mechanical 2-state NMP transition rate is used). In devices with large surface areas, a group of defects is typically assumed to be spread across a defect band. The trap levels of the defects are assumed to follow a normal distribution, while the relaxation energies and spatial positions are assumed to follow normal and uniform distributions, respectively [66]. Since the curvature of the potential energy curves (PECs) is correlated with the relaxation energy, R need not be treated as a stochastically distributed unit. Furthermore, a uniform spatial defect concentration N_T across parts of the dielectric is assumed. The relevant parameters are illustrated in Figure 4.2. Defect sampling can be carried out through Monte-Carlo sampling or a more efficient approach involving the computation of the mean degradation of the defect band by sampling the parameters on a grid and introducing a weighting scheme.

4.4.1 Effective Single Defect Decomposition

The utilization of Gaussian trap bands has been successful, but it requires larger relaxation energies than those obtained from DFT calculations of appropriate oxide defect candidates, which is a disadvantage. This can lead to unreasonably long charge transition times, as exemplified by the shallow SiO_2 trap band of the 28 nm technology described in [66]. In Figure 4.3, the majority of all sampled defects exhibited transition times exceeding 10^7 s, which is not experimentally accessible. The smaller time constants are associated with the low-energy end of the relaxation energy distribution. To address this problem, an alternative method called effective single defect decomposition (ESiD) has been developed, which calibrates the model to experimental data without assuming any defect parameter distributions, as outlined in [KTJ3]. The ESiD algorithm allows for an efficient extraction of trap parameters from measurement data, which can then be compared to DFT simulations.

When using the ESiD method, the total shift in threshold voltage (ΔV_th) is expressed as the sum of the threshold voltage shifts caused by each individual defect (δV_th):

$$\Delta V_\mathrm{th} = \sum_{E_\mathrm{T}, E_\mathrm{R}, x_\mathrm{T}, \Delta Q} N(t; E_\mathrm{T}, E_\mathrm{R}, x_\mathrm{T}, \Delta Q)\delta V_\mathrm{th}(E_\mathrm{T}, E_\mathrm{R}, x_\mathrm{T}, \Delta Q) \tag{4.27}$$

Here, $N(E_\mathrm{T}, E_\mathrm{R}, x_\mathrm{T}, \Delta Q)$ represents the weight of each defect. Instead of assuming Gaussian distributions for E_T and E_R, the ESiD algorithm employs a uniform parameter grid sampled for E_T, E_R, x_T, and ΔQ. These parameters form a grid that is considered in the response matrix (δV), where the response δV_th is computed at each point. Using the response matrix and defining the observation vector $(\Delta V)_j = \Delta V_\mathrm{th}(t_j)$, a non-negative linear least square (NNLS) algorithm can be employed to compute the weights $(N)_i = N(E_\mathrm{Ti}, E_\mathrm{Ri}, x_\mathrm{Ti}, \Delta Q_i)$ such that:

$$(\hat{N}) = \underset{\hat{N} \geq 0}{\operatorname{argmin}} \, ||(\delta V) \cdot \hat{N} - \Delta V||^2 \tag{4.28}$$

Since this is a mathematically ill-posed problem that can lead to solutions with

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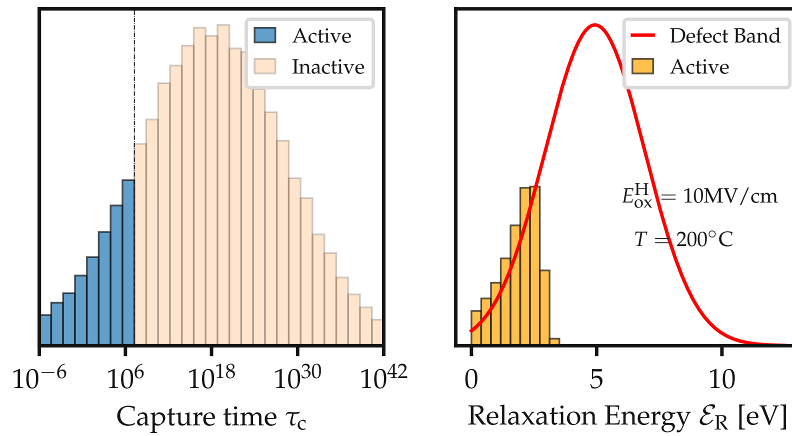

Figure 4.3. The use of Gaussian trap bands in the 28 nm technology, as discussed in [66], indicates that only a fraction of the distribution contributes to active defects. The greater part of the defect parameters extracted from the trap band results in charge transition times exceeding 10^7 seconds (as seen on the left), rendering them experimentally unattainable. These prolonged charge transition periods correlate with relaxation energies ER that are significantly larger than those derived from DFT calculations (as seen on the right). Therefore, they can be considered as artifacts of the Gaussian distributions. The figure is a reproduction from [KTJ3].

physically unrealistic high defect densities, a Tikhonov regularization [105] is added to ensure that the least-square solution results in smoother defect densities:

$$(\hat{N}) = \underset{\hat{N}\geq 0}{\text{argmin}}\, ||(\delta V) \cdot \hat{N} - \Delta V||^2 + \gamma^2 \hat{N}^2 \tag{4.29}$$

Here, γ is the regularization parameter. In practical applications, the parameter γ needs to be adjusted according to the specific problem at hand. However, as demonstrated in Figure 4.4, a reasonable value can be estimated by plotting the total defect density against the error norm to the experimental data for different γ values, resulting in an L-shaped curve. This curve provides valuable insights: for very small values of γ, the approximation error is remarkably low but at the expense of a significantly high defect concentration. Conversely, if γ is too large, the problem becomes overregularized, leading to a substantial increase in approximation error as γ is further increased. Based on the L-criterion [105], the optimal value for γ is located at the "corner" of this L-shaped curve, striking a balance between accurate representation of the experimental data and maintaining a reasonably small defect concentration.

4.5 Issues Related to Charge Sheet Approximation

Even though Comphy provides a convenient way to evaluate device reliability, the usage of a 1D geometry inherently limits its accuracy. This is due to the CSA, see Equation 4.9, used to model the impact of oxide charges on device electrostatics [104].

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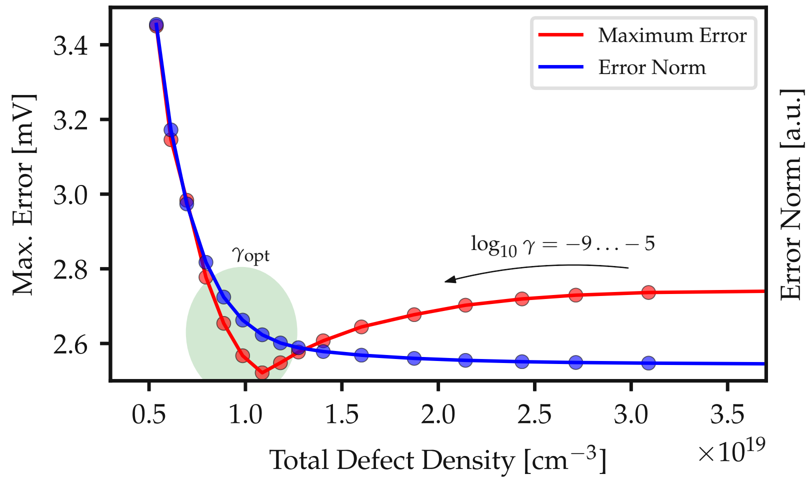

Figure 4.4. The influence of the regularization parameter γ is significant. When γ is small, the solution necessitates an excessively high defect density, which is not physically realistic. On the other hand, excessively large values of γ result in rapidly increasing approximation errors. The ideal value for γ resides between these two unfavorable regions. Originally published in [KTJ3]

CSA calculations take into consideration a uniform way of conduction, while in reality a percolative way of conduction takes place [106]. These inaccuracies become more pronounced in the subthreshold regime, where the conductivity is heavily affected by random discrete dopants (RDD) and random trapped charges. Many recent studies have demonstrated that the CSA significantly underestimates the impact of a single defect on device performance [106, 107, KTJ4], which can potentially result in a slight overestimation of trap densities. Even for ideal planar devices, this approximation does not accurately describe the distribution of threshold voltage shifts caused by individual trap charges. For more complex device geometries, such as FinFETs or gate-all-around (GAA) FETs, the modeling of transmission coefficients and the strongly inhomogeneous electric fields and carrier concentrations lead to further inaccuracies in the 1D approximation [95].

Even though CSA has proven to work pretty effectively in numerous cases, a thorough statistical analysis of single defects and their impact on device performance is needed for accurate extraction of the parameters that influence the impact of defects, like geometry and dopant concentration. Kaczer et al. [48], have proposed the following expression for the impact of a single defect in the ΔV_{th}, mentioned as η:

$$\eta \approx \frac{t_{\text{inv}} \times N_A^a}{A}, \tag{4.30}$$

where t_{inv} is the oxide thickness corresponding to capacitance in inversion, N_{A} the channel doping and A the area of the device channel. The exponent a has been observed around 0.5.

However, in references in the literature where statistical analysis is performed, it has also been observed that the area dependence used in the CSA is not valid under

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all operating conditions [26, 108]. The nature of percolative conduction appears to be the main reason for these observations [109, 110, 111]. This is especially pronounced in devices with smaller gate areas, where charge trapping at oxide defects can significantly reduce the source-drain current, even a single charged defect can have this effect due to its influence on the percolation path in the channel. In such devices, the lower capacitance means that each defect exerts a greater influence on the surface potential and, consequently, the shift in threshold voltage. Another issue with the uniform way of conduction expected by the CSA is its inability to explain the distribution of traps observed in experiments. The next chapter will delve into the details of statistical methods that to explain the impact of traps on device behavior which were also used for the work of this thesis.

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Chapter 5

Single Defect Statistics

5.1 Introduction

As discussed in the previous chapter, the influence of individual defects varies across different technologies, with factors such as random dopant fluctuations playing a significant role. Consequently, approximations like the CSA, while effective in estimating the impact in many cases, can introduce inaccuracies.

In the realm of nanoscale devices, where modern devices are scaled down, only a few defects are present in each device, and each defect significantly affects the device's operation. To better comprehend degradation mechanisms like BTI and RTN in these scaled devices, it is beneficial to analyze the impact of a small group of individual charged traps. Each device can be characterized by the active number of defects in the measurement window, denoted as N_T, and the average impact of a single defect in Δv_{th}, denoted as η. Only the occupied charged defects are assumed to affect the channel current. The occupation of each defect, determined by its voltage and temperature-dependent capture and emission times, also contributes differently to the channel current.

Due to their discrete nature, these small groups of defects can be examined, and statistical models can be developed to estimate their impact. This chapter will present the distributions primarily used to describe the quantity and influence of individual defects. Utilizing these distributions, equations that describe the overall impact of defects in a device are established, allowing the direct extraction of the means N_T and η from the measured ΔV_{th} traces, eliminating the need for separate examination of individual defects. *Parts of this chapter are based on the work of Kaczer et al. [48, 112] the authors' previous publications [KTJ5].*

5.2 Statistical Distributions of Defects

A set of MSM measurements obtained from devices with the same geometry ($W \times L = 135\,\mathrm{nm} \times 350\,\mathrm{nm}$) is displayed in Figure 5.1(left). The discrete steps (charge transition events) are extracted with the Canny edge detection algorithm [113], which

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is integrated into the data analysis framework used within the thesis. The resulting extracted step heights for different devices are collected and statistically analyzed.

These collected amplitudes of step heights, denoted as Δv_{th}, are used to construct a cumulative distribution function (CDF) for each particular geometry. The convention of a complementary CDF (CCDF) normalized to the N_{T} is employed in this work, as shown in Figure 5.1 (middle). This approach enables the direct extraction of N_{T} from the CCDF distribution, allowing for the comparison of multiple geometries within a single plot.

It is worth noting that the distributions obtained from BTI measurements have been found to approximately follow an exponential behavior in the literature [106, 24, 32]. This exponential distribution has also been repeatedly reported for RTN amplitudes and confirmed by various theoretical studies, with the responsible transition times exhibiting the same behavior [32, 114, 115]. These similarities have reinforced the link between RTN and BTI, providing a common framework to study both phenomena.

The exponential distribution of step heights can be generally attributed to the non-uniform conductive paths between source and drain, which are affected by the random dopants of the substrate and other variability sources [106].

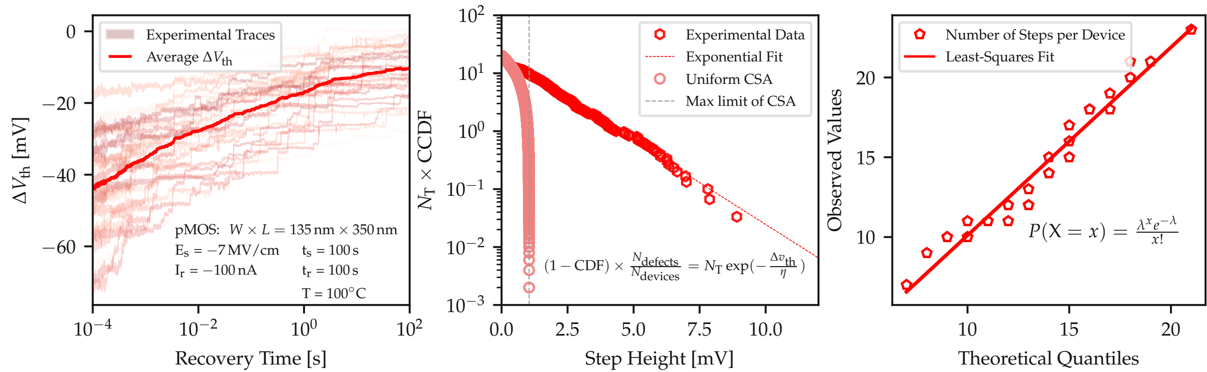

Figure 5.1. The left part of the figure illustrates typical measure-stress-measure (MSM) sequences obtained from 40 devices of equal dimensions ($W \times L = 135\,\text{nm} \times 350\,\text{nm}$). Using the Canny algorithm, integrated into the data analysis framework [113, 116] used in this work, discrete steps representing charge transition events are extracted from the recovery traces, leading to the creation of a corresponding distribution. The middle panel demonstrates that the CCDF adheres to an exponential distribution while, for comparison, a uniform distribution obtained from the charge sheet approximation (CSA) is also included. Finally, the right panel exhibits a quantile-quantile (Q-Q) plot, comparing the distribution of the number of steps per device to a Poisson distribution. This plot validates that the number of steps per device can be accurately described by a Poisson distribution. Figure taken from [KTJ5]

The respective exponential probability distribution function (PDF) can be described by [112, 48]

$$f(\Delta v_{\text{th}}) = \frac{1}{\eta} \exp\left(-\frac{\Delta v_{\text{th}}}{\eta}\right), \tag{5.1}$$

where η is the mean threshold voltage shift caused by a charge transition event of a

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defect. From the PDF, the corresponding CDF can be calculated

$$F(\Delta v_{\mathrm{th}}) = \int f(\Delta v_{\mathrm{th}}) \mathrm{d}\Delta v_{\mathrm{th}} = 1 - \exp\left(-\frac{\Delta v_{\mathrm{th}}}{\eta}\right). \tag{5.2}$$

By normalizing the complementary CDF to the average number of defects per device, the following relation can be obtained

$$(1 - \mathrm{CDF}) \times \frac{\mathrm{N_{defects}}}{\mathrm{N_{devices}}} = N_{\mathrm{T}} \exp\left(-\frac{\Delta v_{\mathrm{th}}}{\eta}\right), \tag{5.3}$$

where N_{defects} is the total number of active defects observed in the measuring time window, N_{devices} is the number of tested devices, and N_{T} is the average number of active defects per device. The impact of an individual defect on the threshold voltage of a device (Δv_{th}, denoted with a lowercase "v" and referred to as step height) depends on the position of the defect in the oxide.

The number of defects per device generally follows a Poisson distribution [112]. To verify this assumption, the number of defects per device are extracted for all the tested traces and the quantiles of the extracted distribution are evaluated, see Figure 5.1 (right). As can be seen, the results confirm that the observed number of defects per device is Poisson distributed.

Note that the higher number of electrically active defects on pMOS devices can be observed directly by the maximum value of the normalized CCDFs. The vertical dashed lines show the maximum limit the CSA would give for this device type. However, as shown, the distribution based on the CSA significantly underestimates the experimentally observed average impact of the defects η. This underestimation is casually related to the neglection of the impact of percolative conduction in weak inversion regimes, which is associated with the dopants of the substrate [24]. As a result, the CSA can lead to overly pessimistic results for defect densities when extracted from ΔV_{th}.

5.3 Total ΔV_{th} Distribution

If the lateral locations of n successively trapped charges are assumed to be uncorrelated, the overall threshold voltage shift will be [112, 48]

$$\Delta V_{\mathrm{th}} = \sum_{i=1}^{n} \Delta v_{\mathrm{th,i}}. \tag{5.4}$$

The distribution of ΔV_{th} can be expressed as a convolution of individual exponential distributions [Equation 5.1], with the PDF and the CDF respectively described by

$$f_{\eta,n}(\Delta V_{\mathrm{th}}) = \frac{n}{n!} \frac{\Delta V_{\mathrm{th}}^{n-1}}{\eta_n} \exp\left(-\frac{\Delta V_{\mathrm{th}}}{\eta}\right), \tag{5.5}$$

and

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$$F_{\eta,n}(\Delta V_{\text{th}}) = 1 - \frac{n}{n!}\Gamma\left(n, \frac{\Delta V_{\text{th}}}{\eta}\right). \tag{5.6}$$

Here, Γ is the incomplete gamma function.

The population of stressed devices typically contains a varying number n of visible oxide defects in each device, with this number following a Poisson distribution [24, 112]. Assuming that the small fraction of the device population exhibiting RTN around V_{th0} can be ignored to avoid complex statistics [117, 118], the total ΔV_{th} distribution can be determined by summing distributions F_n, weighted by the Poisson probability:

$$p_{N_{\text{T}},n} = \frac{e^{-N_{\text{T}}}(N_{\text{T}})^n}{n!}. \tag{5.7}$$

In Equation 5.7, N_{T} is the mean number of defects in the FET gate oxide and is related to the oxide trap (surface) density N_{ot} as $N_T = WLN_{\text{ot}}$ (i.e., N_T is not an integer). This line of reasoning then results in the total ΔV_{th} CDF given by [112, 48]:

$$H_{\eta,N_{\text{T}}}(\Delta V_{\text{th}}) = \sum_{n=0}^{\infty} p_{N_{\text{T}},n} F_{\eta,N}(\Delta v_{\text{th}}) = \sum_{n=0}^{\infty} \frac{e^{-N}(N)^n}{n!} \left[1 - \frac{n}{n!}\Gamma\left(n, \frac{\Delta V_{\text{th}}}{\eta}\right)\right]. \tag{5.8}$$

The corresponding PDF is

$$h_{\eta,N_{\text{T}}}(\Delta V_{\text{th}}) = e^{-N}\left[\delta(\Delta V_{\text{th}}) + \frac{N}{\eta}\exp\left(-\frac{\Delta V_{\text{th}}}{\eta}\right) {}_0F_1\left(2; \frac{N}{\eta}\Delta V_{\text{th}}\right)\right], \tag{5.9}$$

The hypergeometric function ${}_0F_1(2; x)$ can be expressed in terms of the modified Bessel function I_1 as ${}_0F_1(2; x) = x^{-1/2} I_1(2\sqrt{x})$. The Dirac delta function $\delta(\Delta V\text{th})$ accounts for the fraction of devices with zero voltage shift [114], which decreases with an increase in N_{T}.

5.3.1 Derived Parameters

The following equations provide a practical way to describe the distribution of total ΔV_{th}, which can be statistically analyzed through its mean and variance. The mean is given by the following equation:

$$\langle \Delta V_{\text{th}}(t) \rangle = \eta N_{\text{T}}(t) \tag{5.10}$$

where N_T and η are proportional and inversely proportional to the FET gate area A, respectively. The variance of the distribution is given by:

$$\sigma^2_{\Delta V_{\text{th}}}(t) = 2\eta^2 N_{\text{T}}(t)$$

The relative deviation, $\sigma_{\Delta V_{\text{th}}} / \langle V_{\text{th}} \rangle = (2/N_{\text{T}})^{1/2}$, increases with decreasing gate area and decreases with increasing N_T. The skewness of the distribution is given by:

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$$6\eta^3 N_{\text{T}}(t) \tag{5.11}$$

and the kurtosis by:

$$12\eta^4[N_{\text{T}}^2(t) + 2N_{\text{T}}(t)] \tag{5.12}$$

Expressing N_T and η in terms of more "circuit designer-friendly" parameters $\langle V_{\text{th}} \rangle$ and $\sigma^2_{\Delta V_{\text{th}}}$ gives:

$$N_T(t) = 2\langle \Delta V_{\text{th}}(t) \rangle^2 / \sigma^2_{\Delta V_{\text{th}}} \tag{5.13}$$

and

$$\eta = \sigma^2_{\Delta V_{\text{th}}} / [2\langle \Delta V_{\text{th}}(t) \rangle] \tag{5.14}$$

Hence, the first two moments of a measured total BTI V_{th} distribution are sufficient to extract both N_T and η. The time-dependent variance $\sigma^2_{\Delta V_{\text{th}}}$ can be expressed as a function of η and $\langle V_{\text{th}} \rangle$:

$$\sigma^2_{\Delta V_{\text{th}}} = 2\eta \langle \Delta V_{\text{th}}(t) \rangle \tag{5.15}$$

This equation removes the complexity of degradation kinetics and allows degradation to be solely expressed in terms of the average degradation, as seen in Figure 5.2. The technology-dependent parameter η can be obtained through single-emission measurements or measurements of total ΔV_{th} distributions or by considering links with time-zero variance.

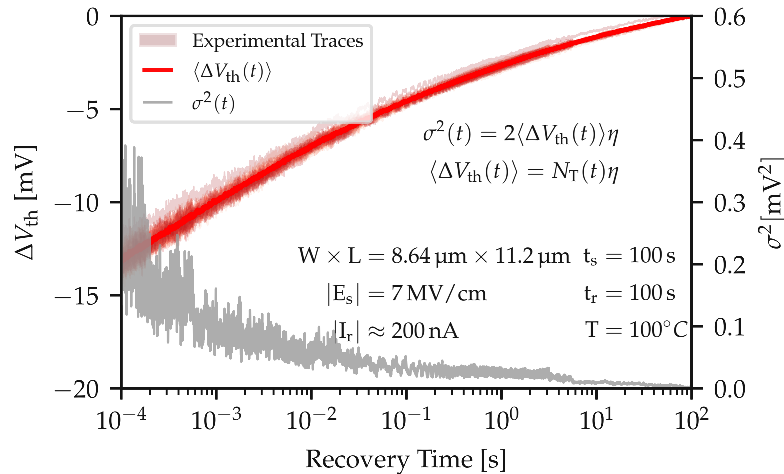

Figure 5.2. Experimental data from the largest device in the measurement set show that discrete steps are not observable in larger devices. Therefore, the statistical averages of the defects can be determined using DCM on the ΔV_{th} traces.

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Chapter 6

Measurement Methods

This chapter focuses on exploring different measurement techniques utilized to determine the reliability of MOSFET devices, with a particular emphasis on the extraction of device parameters and the evaluation of parameter degradation over time. Initially, an overview of methods for extracting important device parameters, such as the threshold voltage (V_{th}), from electrical characterization is presented. Subsequently, commonly used measurement schemes designed to evaluate device parameter degradation, especially the drift of threshold voltage (ΔV_{th}), are discussed. In addition, the custom-built measurement tools utilized in this research are examined, outlining their benefits and limitations.

6.1 Time-zero Characterization

Time zero properties of MOSFETs generally refer to their initial characteristics and performance metrics when they are manufactured or at the point of initial use. These properties are crucial because they serve as a baseline for understanding how the device will behave and how it could degrade over time under various operating conditions.

6.1.1 Transfer Characteristics

In MOSFET devices, several critical parameters are affected by device operation. The main parameter used in this thesis for device evaluation is the threshold voltage (V_{th}). It is the minimum bias condition needed for a conductive channel to form between the source and the drain. Another essential parameter is the subthreshold slope (SS), which plays a crucial role in achieving accurate switching between the ON and OFF states within a narrow gate bias range. Additionally, the transconductance (g_m), which is primarily associated with carrier mobility and correlated with interface defect scattering, is another vital parameter.

The transfer characteristics of a MOSFET device can be used to estimate the time-zero properties of a device under test as they describe the relationship between the drain current I_D and the gate bias V_G measured at a fixed drain bias V_D. This relationship can

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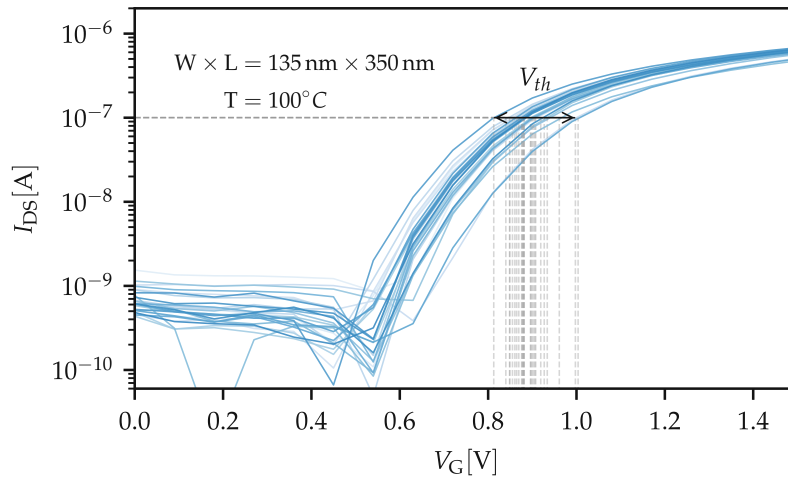

Figure 6.1. $I_D(V_G)$ measurements for a set of devices, with the channel width $W = 135$ nm and the length $L = 350$ nm. Using the constant current method, the threshold voltage V_{th} is extracted at $I_D = I_{ref}\frac{W}{L}$. The reference current I_{ref} is assumed to be 100 nA in this case. The V_{th} values range between 0.8 and 1 V for the identical devices of this technology.

be used to determine the current state of device parameters at the time of measurement. Typically, it is recommended to perform a fast sweep of the gate bias of the Device Under Test (DUT) and measure I_D at each bias point as quickly as possible. This approach aims to minimize the duration of an applied oxide stress field during the sweep, thereby reducing the impact of defects with shorter capture and emission time constants compared to the sweep duration. As a result, fast sweeps help maintain the device's pristine state. Since the theoretical definition of V_{th}, which denotes the exact equilibrium of majority and minority carriers in the conducting channel of a MOSFET [98], cannot be experimentally determined, alternative definitions of V_{th} are needed for its experimental extraction [119, 120]. One common method for determining V_{th} involves applying a constant source-drain current criterion, which is depicted in Figure 6.1. In its simplest form the V_{th} is identified as the gate voltage where:

$$I_D = I_{ref}\frac{W}{L} \tag{6.1}$$

I_{ref} is typically chosen to result in a drain current within the sub-threshold region of the transfer characteristics. Normally it depends on the studied technology and it varies between 1 nA and 200 nA. With this method, V_{th} can be continuously measured by using a feedback loop to maintain a constant I_D while tracking V_G. The constant current method proves to be beneficial in comparing MOSFETs with varying channel geometries. Due to its ease of application and low extraction variability, this method is suitable for extracting ΔV_{th} over time for wafer-scale device variations, as stated in [121].

Other methods for determining V_{th} from the I_D-V_G characteristics of a MOSFET device use the transconductance g_m. One such approach is the linear extrapolation method, which uses the gate voltage for the maximum transconductance $g_{m,max}$ to

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extrapolate to zero drain current. By subtracting $V_{D/2}$ from the resulting intersection gate bias, V_{th} can be obtained as shown in [122]:

$$V_{th,g_{m,lin}} = \frac{I_{D|g_{m,max}}}{g_{m,max}} - V_{G|g_{m,max}} - \frac{V_D}{2} \quad (6.2)$$

Another approach, known as the second derivative method, provides a more accurate comparison with the theoretical value of V_{th}. This method identifies the threshold voltage by locating the gate bias at the minimum point of the second derivative of the logarithmic drain current, as referenced in [123].

6.1.2 Capacitance - Voltage (CV) Measurements for Characterizing MOSFET Devices

Capacitance-voltage (CV) measurements are crucial in obtaining key insights into MOSFET devices, including their inherent properties and defect features. Two primary methods are employed for CV measurements: the ramp method, which involves measuring the displacement current while sweeping the gate voltage, and the impedance method, where a small AC signal is superimposed on the DC gate bias and the AC current is measured. In this section, the emphasis will be on the impedance method, which offers more flexibility in measurement parameters and allows for the observation of small signal conductance.

The impedance method is extensively utilized to gather vital information about the transistor gate stack, such as oxide thickness, doping densities, poly-Si gate-depletion, and permittivity. By altering measurement parameters and comparing the resulting changes in the CV curves' shape, one can extract defect properties. This method involves applying a DC voltage at the gate contact, overlaid with a small-amplitude sinusoidal AC signal, while grounding the bulk contact of a MOSCAP (or all terminals—source, drain, and bulk—for a MOSFET).

The core principle behind a CV measurement, the results of which os illustrated in Figure 6.2, consists of applying a small sinusoidal AC voltage (typically 50 mV at 100 kHz) combined with a discrete varying DC bias to the gate, while grounding the bulk. Simultaneously, the gate voltage and bulk current are measured. Alternatively, the roles of the gate and bulk may be switched, with the voltage applied to the bulk and the gate current measured. These measurements can be performed on either MOSCAP or MOSFET structures. MOSCAP structures offer benefits, such as being effectively one-dimensional, which allows for more straightforward and accurate models. However, MOSFETs permit faster gate bias sweeps due to the availability of minority carriers from the source and drain regions. The main distinction between the two structures concerns the supply of minority carriers for inversion.

CV measurements generally involve stepping the gate bias from accumulation to inversion or vice versa to obtain the small signal capacitance and conductance curves (C-V and G-V). The AC signal frequency, ranging from kHz to GHz, is the most critical parameter in this measurement. Typically limited to 1 MHz due to increased

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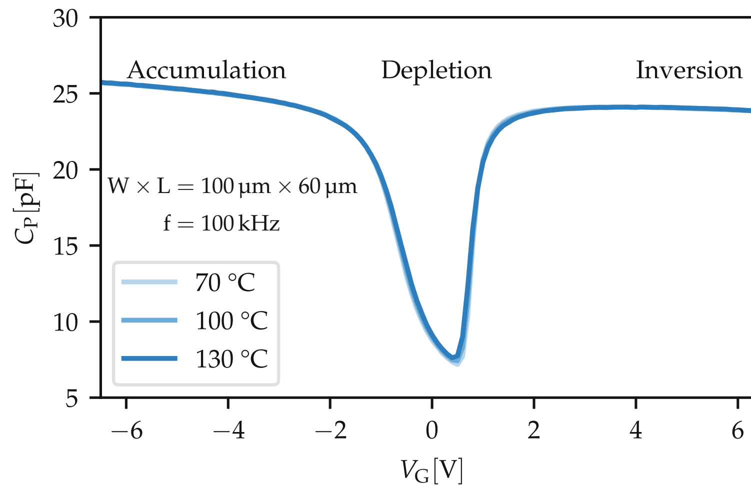

Figure 6.2. The example results from a 100 kHz C-V measurement on nMOS devices display distinct accumulation and inversion branches at the peak values of negative and positive biases, respectively. The capacitance observed during the depletion phase is significantly lower. Additionally, the inversion branch tends to exhibit a steeper slope compared to the accumulation branch. V_{th} can also be estimated by the minimum value of the plot.

measurement effort, the frequency determines how defects contribute to the measured CV curve, as defects unable to follow the signal will not affect the measured capacitance. In MOSCAP structures, the sweep rate compared to the minority response further impacts the measurement outcomes.

CV measurements can complement I_D measurements to study defect-related parameters. Initially, a reference CV curve is measured, and then the device is stressed under well-defined conditions. A second CV curve is recorded, and the variations between the pre- and post-stress CV curves enable the extraction of various defect properties. The difference between subsequent measurements can be connected to changes in the device's defect populations. This technique serves as a potent tool for reliability characterization, offering valuable information about the traps' energetic position. Several options are available for determining defects' contribution to a measurement, including the high-low frequency method, which compares low-frequency measurements to high-frequency measurements, and the single-frequency measurement method, comparing the measured curve to a simulation or calculation. Additionally, measurements can be performed in a MSM-like manner, relating the difference between subsequent measurements to changes in the device's defect populations.

In conclusion, CV measurements can be used alongside $I_D(V_G)$ measurements to offer a valuable method of characterizing MOSFET devices and their defects. Further investigation of this technique may result in the development of enhanced extraction methods and a better understanding of MOSFET device performance and reliability.

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6.2 Time-Dependent Characterization

In previous chapters it was discussed how charged defects located between the gate and the conducting channel of a MOSFET can influence the electrostatics at the channel/insulator interface from the sub-threshold region up to inversion. The Coulomb interaction between the trapped charge and the channel carriers can lower the carrier density in the vicinity of the defect, which in turn affects the drain-source conductivity of the device. The impact of a defect on the channel current depends on the resulting perturbation of the current percolation path. This effect is used in various characterization methods for defect detection. The methods discussed in this chapter are based on changes in channel conductivity, which rely on recording the drain-source current at a constant bias and temperature. The circuits used in practice incorporate additional components to switch between multiple amplification ranges, by using different resistors in the feedback loop of an operational amplifier (OPAMP) circuit. Furthermore, the SNR is improved by limiting the frequency range or for circuit stability in the case of the constant-current scheme. In addition, the gate current may also be measured to characterize single interface traps and states [KTJ6].

6.2.1 Measure-Stress-Measure (MSM) Methods

To evaluate the reliability of a technology, it is common practice to subject devices to stress conditions that exceed the nominal operating range, in order to accelerate degradation mechanisms and allow for observations within a reasonable time frame. This can include exposing the device to elevated gate and/or drain biases, temperature, or even radiation. The measure-stress-measure (MSM) method is a well-known technique for this purpose, consisting of three phases: first the measurement of a fresh device, second the application of defined stress conditions, and third the subsequent characterization of the stressed device. The results of the original and post-stress measurements are then contrasted to evaluate the effect of the stress. This process may be repeated under increasingly harsh stress conditions.

MSM on Multiple Devices

For defect-spectroscopy in multiple devices of a same batch for statistical purposes the following MSM sequence is typically used. First, an $I_D(V_G)$ sweep is measured within a narrow gate bias range before the first stress cycle is applied. After that a stress and recovery sequence of a certain duration is applied. Then to the next device, the same sequence with an $I_D(V_G)$ measurement followed by a stress-recovery sequence is applied again. The same sequence is applied for all the devices of the same batch as can be seen in Figure 6.3. A typical set of selected measured traces of nMOS devices can be seen in Figure 6.4.

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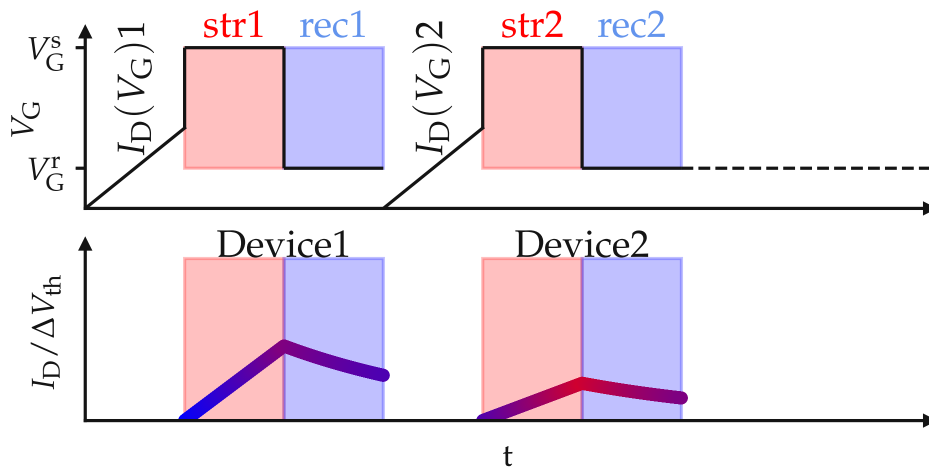

Figure 6.3. MSM sequence applied in devices of the same technology for statistical purposes. The scheme involves an initial $I_D(V_G)$ measurement followed by alternating stress (red) and recovery (blue) phases with predefined applied gate voltages for a specific duration. During the recovery phase, the drain current I_D is monitored and correlated to ΔV_{th} using the initial $I_D(V_G)$.

eMSM Method

Extended MSM (eMSM) measurements are commonly used to characterize the effects of BTI in large devices. In the eMSM scheme for measuring BTI effects, the device's drain and gate terminals are kept at ground during the stress phase, while a gate bias equal to or greater than the threshold voltage is applied. During the relaxation or recovery phase, the gate bias is set to a lower readout value while a small drain bias is applied to ensure a small channel current. The temporal behavior of the channel current, mapped to a threshold voltage shift during relaxation, is derived using an initial $I_D(V_G)$ measurement recorded before stress. The recovery behavior is monitored after the stress phase, and additional stress phases are performed with increasing stress times. The corresponding recovery phases are chosen long enough to eliminate most of the recoverable part of the degradation, and sampling is usually performed at logarithmic time instances. An illustration of eMSM can be seen in Figure 6.5. A set of selected results for both pMOS and nMOS devices of a SiON technolgy where eMSM has been applied is shown in Figure 6.4.

6.2.2 TDDS

The time dependent defect spectroscopy (TDDS) is another application that makes use of stress-recovery measurements, which aims to characterize single defects. Charging and discharging of such defects can be observed within the relaxation traces on small gate area devices. This can be used in conjunction with BTI measurements to characterize their charge trapping kinetics at various biases and temperatures to explain their behavior physically.

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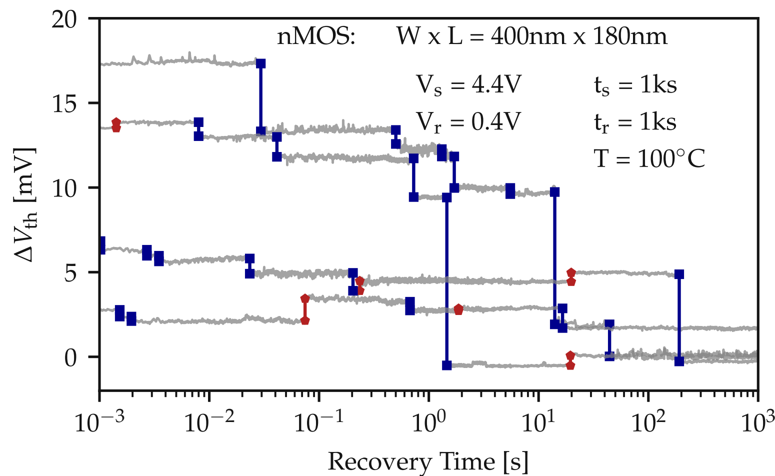

Figure 6.4. The presented recovery traces highlight the threshold voltage drift following PBTI stress in scaled SiON nMOS transistors. These devices exhibit recovery in discrete steps. Within these traces, electron emissions are identifiable as negative steps (in blue), and hole emissions as positive steps (in red), affecting the V_{th} behavior. Originally published in [KTJ4]

For TDDS, the measurement conditions are similar to those of BTI measurements on large devices. The main difference is that each stress condition is repeatedly measured to gather ample statistical data on the capture probabilities and emission times of individual defects. The characterization windows for TDDS are set by the time it takes for charge capture during stress and the charge emission duration during the relaxation phase of the defects. The measurement window in the stress phase of TDDS is determined by several factors: the range of stress times (minimum to maximum) applied, the highest gate bias that avoids causing oxide breakdown, and the lowest gate bias where the defect being studied nearly reaches full occupancy. During the recovery phase, the measurement window is defined by the initial delay after stress when the first measurement is possible, the longest relaxation time used, the highest gate bias where the defect's occupancy remains near zero, and the minimum voltage at which individual recovery steps can be measured

Applying TDDS to extract the charge transition times over wide ranges for stress and recovery bias can be time-consuming. However, TDDS measurements can be performed in conjunction with RTN measurements, which allows the capture of both close to the intersection bias while also extracting the capture and emission times of a defect over wide ranges of gate biases. TDDS data are commonly processed using step detection algorithms, similar to RTN data, but defect parameter extraction is comparatively simple as the emission probabilities for the defects increase drastically after applying the recovery conditions.

6.2.3 RTN Measurements

In MOS transistors, random telegraph noise (RTN) is frequently seen in conjunction with 1/f noise, and is also referred to as pink or flicker noise. The origin of this noise can

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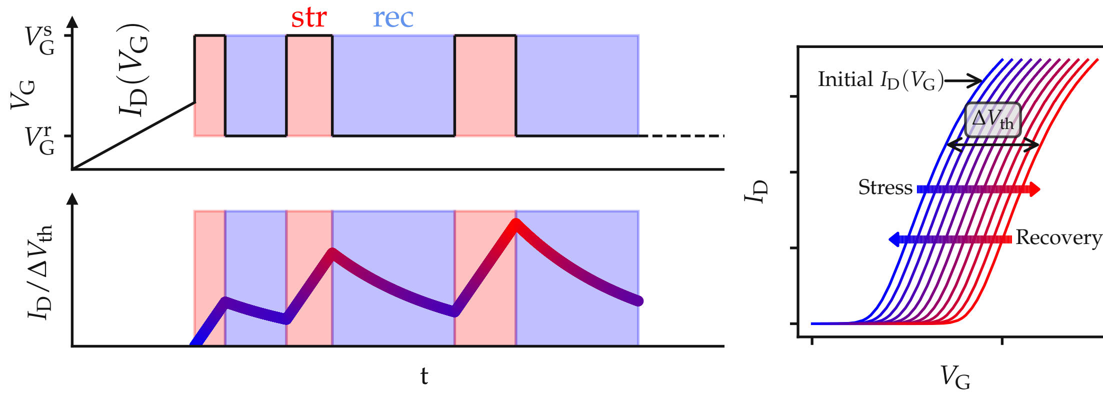

Figure 6.5. The eMSM-based measurement strategy is utilized to evaluate the change in the threshold voltage. Once the initial $I_D(V_G)$ is measured, stress and recovery voltages are applied in alternating fashion, with increasing stress and recovery durations (t_s and t_r). During the relaxation phase, the source current is recorded and subsequently converted into an equivalent ΔV_{th}using the initially measured $I_D(V_G)$ characteristics. Originally published in [KTJ5]

be attributed to individual defects that dynamically charge and discharge during device operation. As the gate area of MOSFETs shrinks, discrete steps in the channel current become noticeable, connecting 1/f noise to single defects that alter the resistance of the inversion channel.

The experimental evaluation of RTN consists of the following procedure. A constant voltage is applied to the gate of the DUT, while the drain-source current is measured over a specified duration using an equidistant sampling scheme. By initially determining the $I_D(V_G)$ curve, the current signal can be converted to a corresponding V_{th} signal. Active charge traps can capture and release charges, leading to distinct steps in the recorded current and the associated ΔV_{th} curve. For large area devices, where only the combined effect of numerous individual defects can be examined, the primary interest lies in the noise amplitude or power. In the case of small area devices, distinct steps are observable in the drain current over time at multiple gate voltages. This is shown on a few selected traces in Figure 6.7 (left).

In devices with a large gate area, a signal with 1/f noise is typically acquired, whereas in smaller area devices, distinct steps can be seen. The spectral characteristics of each individual defect's contribution can be depicted by a Lorentzian power spectral density (PSD), which exhibits a plateau beneath a specific frequency and declines proportionally to f^{-2} beyond that. When numerous defects have border frequencies loguniformly distributed across the frequency axis, this results in a 1/f PSD, which is observable in large area devices.

Defects that can be characterized by RTN are situated energetically near the Fermi level of the channel or the gate under the applied measurement conditions. These defects undergo stochastic changes in their charge state within a reasonable measurement time frame. By altering the gate bias, the region of the band diagram being scanned can be

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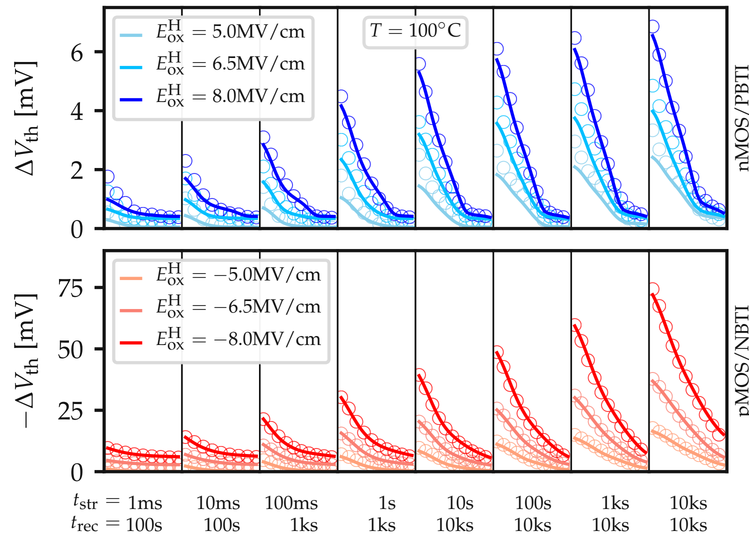

Figure 6.6. The outcomes commonly observed when implementing the eMSM sequence on SiON devices with dimensions W × L = 10 × 10 μm^2 exhibit a continuous behavior in terms of the measured drain current (I_D). This arises from the simultaneous emission of previously trapped charges by a multitude of defects across the large device area. The individual influence of a single defect on the device's performance is too minute to be discerned through measurements. Originally published in [KTJ3]

adjusted, facilitating the examination of RTN behavior under various circumstances.

To determine how the charge transition times for individual defects are influenced by bias, RTN measurements are performed at different gate voltages and temperatures. This allows us to understand how parameters like average charge capture and emission times, as well as average step heights, depend on the gate voltage V_G and temperature. By adjusting the sampling frequency, it is possible to investigate defects with both high and low capture and emission rates.

6.3 Measurement Setup

As mentioned in the previous section, measurements based on channel conductivity are vital for evaluating and characterizing defects in MOSFET devices. The two prevalent techniques for extracting channel conductance are the constant gate voltage scheme and the constant drain current method. The constant gate voltage scheme uses a transimpedance amplifier (TIA) configuration to measure the source-drain current through the channel and converts it to a voltage proportional to the current. This method is straightforward and highly stable but requires converting the recorded drain current change back to a threshold voltage shift using an initially recorded $I_D(V_G)$ characteristic. Any changes in the subthreshold-slope (SS) and trans-conductance (g_m) during the experiment may result in inaccurate ΔV_{th} measurements, although these seem to be minor [124].

In contrast, the constant drain current method implements a feedback loop from the

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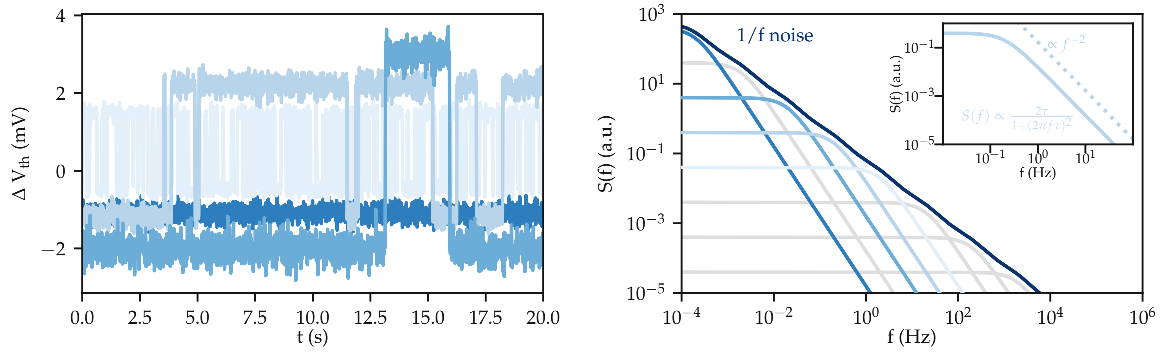

Figure 6.7. Four representative RTN signals exhibit varying mean charge capture and emission times, as well as step heights. From these RTN signals, the power spectral density (depicted in the same color as the corresponding RTN signal) can be derived, adhering to a Lorentzian distribution. The corner frequency of the Lorentzian corresponds to the mean capture/emission time τ of the RTN signal. The superposition of uniformly distributed Lorentzian signals results in a $1/f$ behavior, which is widely recognized in large area devices.

amplifier output to the transistor gate, ensuring constant conductance in the channel at a steady drain bias. This technique accounts for changes in trans-conductance and the $I_D(V_G)$ shape, removing extra error from post-processing with an initially recorded characteristic. Researchers should weigh factors like simplicity, stability, and the likelihood of threshold voltage shift errors when choosing a method.

Both constant-voltage and constant-current schemes can benefit from additional components. Relays can be added for switching between various amplification ranges, while other passive components can enhance SNR or ensure circuit stability. A combination of custom-built voltage sources, sampling circuits, commercial source units, or digital storage oscilloscopes can be used for control and measurement devices in these setups. Nonetheless, achieving the highest SNR and managing the timing of experiments continue to be significant challenges in the development of measurement tools in general.

6.3.1 Custom-Made Low Noise Measurement Unit for MOSFET Reliability Measurements

The custom-made low noise measurement solution used in this work, known as the defect probing instrument (DPI) [43], has been developed to tackle the specific needs of single defect spectroscopy in MOSFET devices, including TDDS and RTN measurements. The DPI is specially designed to offer comprehensive control over experimental parameters, such as output voltages and switching behavior, diverse data acquisition methods for current monitoring, and supplementary control outputs, all while maintaining minimal noise levels.

Initially optimized for single-defect spectroscopy in silicon and wide band-gap MOS transistors, the DPI has since been adapted to characterize large-area transistors using MSM schemes, CV characteristics, automated analysis of array structures, and

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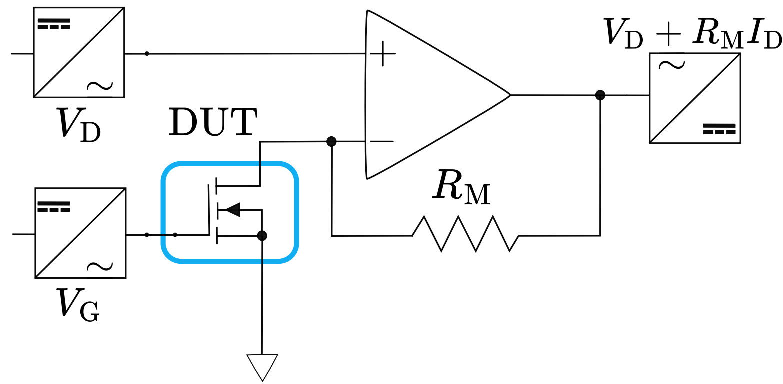

Figure 6.8. A constant gate voltage measurement setup schematic for methods focused on channel conductivity is displayed. The drain and gate voltages of the device are controlled by DACs. The gate voltage is directly applied to the DUT, while the drain current is connected to the positive terminal of an OPAMP operating as a TIA. The negative input terminal of the OPAMP is linked to the DUT's drain connection. The TIA's voltage output, corresponding to V_{out} , is captured by an analog-to-digital converter (ADC). Recreated from [50].

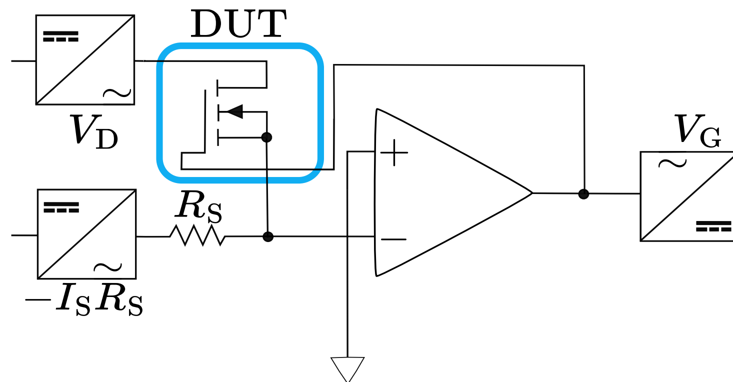

Figure 6.9. A diagram of a constant source current measurement configuration for channel conductivity-focused methods is presented. The drain bias of the DUT is directly controlled, while the gate bias is managed by the OPAMP. The OPAMP circuit adjusts the MOSFET gate bias such that the source current matches the reference current determined by the DAC bias. Recreated from [50].

devices based on 2D materials like MoS_2. Featuring a modular design concept, the DPI ensures maximum flexibility for continuously evolving requirements.

While general-purpose instruments (GPIs) are suitable for established measurement sequences, custom-made solutions like the DPI present a more versatile and adaptable option. DPI surpasses GPIs by compensating for missing features and overcoming limitations typically encountered in commercial setups. As shown in [43] the DPI's superior performance is evident when compared to GPIs supplemented with digital storage oscilloscopes, programmable pulse units, lock-in amplifiers, and other devices.

The primary configuration of the DPI comprises a three-channel pattern generator unit (PGU) to deliver programmable bias signals, a device connector unit (DCU) to convert device currents into corresponding voltages, and up to two data acquisition units (DAU) to capture voltage signals from the DCU. All units are synchronized using a backpanel bus system and can be individually configured via USB connection. This

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design approach enables ongoing independent enhancements of each unit, improving SNR and measurement resolution. Moreover, features such as fast ID(VG) or fast CV methods can be incorporated into the system with minimal effort.

- Pattern Generator Unit (PGU)

  The PGU maintains strict electrical isolation between digital and analog components, ensuring minimal noise in analog signal paths. An ARM processor manages output signals and facilitates USB communication with the measurement host. The processor also connects to an internal bus system for exchanging control information and maintaining synchronized timing behavior. Utilizing various compensation techniques, the PGU achieves smooth transitions between distinct bias levels without voltage overshoots. The compensated switching transient allows for a maximum output frequency of 1MHz, with an output bias range configurable up to ±48 V, expanding applicability to wide band-gap technologies like SiC and GaN.

- Data Acquisition Unit (DAU)

  The DAU captures analog input voltages at a high sampling rate of up to 1MHz with a resolution of approximately 75 µV. Before the analog input signal is converted into a digital word, it undergoes filtering and pre-amplification. The filter and pre-amplifier stages are calibrated to match the input bandwidth of the analog-to-digital converter stage for optimal performance. The DAU also features an analog voltage level shifter, enabling an extended measurement range without sacrificing accuracy.

- Current Converter Unit (CCU)

  The CCU centers around a TIA and aims to achieve the highest current measurement resolution for defect spectroscopy. It employs FET-input OPAMPs to minimize leakage currents. The CCU has seven single channels, each defined by a different gain, selected using mechanical relays. This design choice avoids the leakage currents often associated with integrated switches. Additional hardware components remove the source bias from the TIA output voltage signal, and a filter stage limits the signal bandwidth to the maximum sampling frequency of the DAU.

In conclusion, the custom-made low noise DPI measurement solution offers significant advantages for MOSFET reliability assessments, addressing the specific requirements of single defect spectroscopy and providing a flexible, modular design that can adapt to constantly evolving measurement needs.

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Chapter 7

Edge Detection Algorithms

In the previous chapter, it was noted that one of the greatest challenges in conducting electrical characterization measurements is maintaining controlled bias conditions, precise timing, and minimal noise on the typically encountered nano-scale currents. An additional challenge in electrical characterization is the evaluation of the data set to derive parameters related to defects, such as charge transition times and the amplitude of step heights, which are essential for accurate simulations, lifetime estimations, and predictions. This chapter discusses two of the algorithms included in the data analysis framework used for this work: the Canny algorithm for BTI and RTN traces and the Otsu algorithm specifically for the evaluation of RTN data.

7.1 Canny Edge Detector

The Canny edge detection algorithm was originally developed by John F. Canny in 1986 to detect edges in 2-dimensional images [125]. However, this algorithm can also be used to detect steps in RTN signals, which is a 1-dimensional problem. The way the Canny edge detection algorithm works can be seen in Figure 7.1. The input of the algorithm is the RTN signal (marked as ΔV_{th}) with discrete steps, which can be seen in the upper subfigure. The detected steps (η) at a specific time can be seen in the bottom subfigure.

In general, multiple steps are required to ensure the success of the Canny process. The first step involves enhancing the intensity of the RTN signal (referred to as S for the coherence of the literature) by convolving the time signal with a discretized first derivative of a Gaussian filter G, resulting in a convoluted signal $R[n]$, seen in the middle subfigure. This step is important for mitigation of the effects of noise and drift in the signal. The equation for the convoluted signal can be expressed as follows:

$$R[n] = (S * G)[n] = \sum_{k=-W}^{W} S[k] G_k[n-k], \tag{7.1}$$

where W is the width of the truncation and $G_k[t]$ is a function of the width of the Gaussian filter sigma.

The second step involves simplifying the convoluted signal $R[n]$ by applying a non-maximum suppression, resulting in a simplified signal $R_\mathrm{m}[n]$. This step is essential because it helps to identify the boundaries between adjacent regions of the signal with different properties, which is crucial to measure the signal accurately. The equation for the simplified signal can be expressed as:

$$R_\mathrm{m}[n] = \begin{cases} R[n], & |R[n]| > R[n+1] \wedge |R[n]| > R[n-1] \\ 0, & \text{else} \end{cases}. \tag{7.2}$$

The final step involves thresholding the simplified signal $R_\mathrm{m}[n]$ using a threshold value R_th, resulting in a thresholded signal $R_\mathrm{t}[n]$. This step is important as it helps to suppress responses originating from noise. The equation for the thresholded signal can be expressed as

$$R_\mathrm{t}[n] = \begin{cases} R_\mathrm{m}[n], & |R_\mathrm{m}[n]| > R_\mathrm{th} \\ 0, & \text{else} \end{cases}. \tag{7.3}$$

By analyzing the sign of the thresholded signal $R_\mathrm{t}[n]$, it is possible to detect upward or downward steps in the signal, and the amplitude of each step can be extracted from the original signal. The Canny algorithm is characterized by its high precision and low error rate, which makes it an excellent tool for edge detection in RTN and BTI measurements of MOSFET devices.

However, the Canny algorithm has some drawbacks, such as the width of the Gaussian filter sigma and the threshold value R_th, user-defined parameters that must be adjusted to detect different types of active defects. Therefore, detection quality depends on the choice of these parameters.

In summary, the Canny edge detection algorithm is a powerful tool for edge detection in RTN and BTI measurements of MOSFET devices. It involves several steps, including enhancing the intensity of the signal, simplifying the signal, and thresholding the signal. By analyzing the sign of the thresholded signal, it is possible to detect upward or downward steps in the signal, and the amplitude of each step can be extracted from the original. However, when managing a large set of RTN signals, a fully automated step detection algorithm is necessary. One example is Otsu's method, which will be discussed in the following section.

7.2 Otsu's Algorithm

The second algorithm for edge detection used in this work is Otsu's algorithm [127]. Otsu's algorithm is a widely used method for image thresholding that has been used in various fields such as computer vision, medical image analysis, and remote sensing. As mentioned earlier, it can also be applied to one-dimensional signals, such as RTN measurements. This algorithm, named after its inventor Nobuyuki Otsu in 1979, seeks to find the optimal threshold that separates the signal into two classes: one

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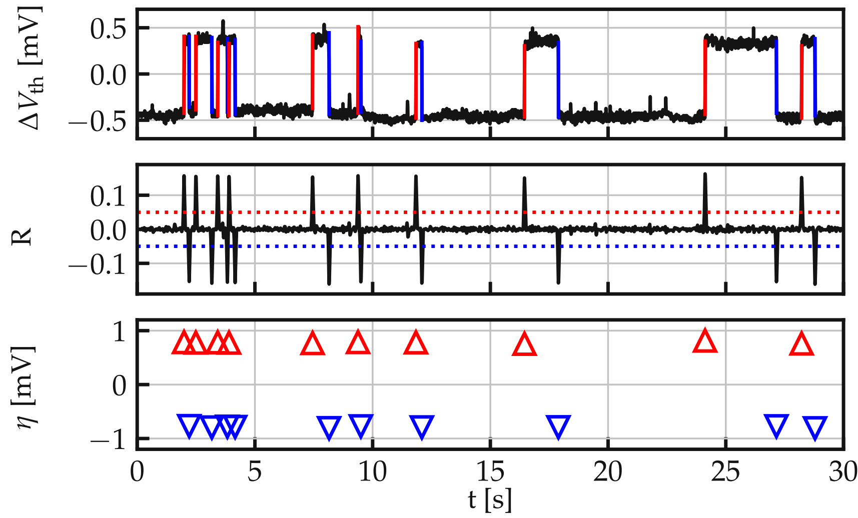

Figure 7.1. The Canny method for identifying edges is showcased using a representative measurement trace. The input signal, ΔV_{th}, is convolved with the first derivative of a Gaussian pulse with a specified variance, G. This results in a signal R, which features peaks corresponding to the initial signal steps. All peaks exceeding a predetermined threshold are identified and utilized to indicate the locations of the steps in the initial trace. The peak heights can be acquired from either the original signal or the peak heights. Recreated from [126].

corresponding to the background noise and the other corresponding to the signal of interest. The two classes are separated by a threshold value t. Values greater than or equal to t are assigned to the foreground, and those with intensity values less than t are assigned to the background. The algorithm aims to find the optimal threshold value t that minimizes the intra-class variance and maximizes the inter-class variance. In this case, background noise is the constant value of the measured signal, and the events of interest are the RTN spikes.

The algorithm works by calculating the between-class variance for all possible threshold values and then selecting the threshold value that maximizes this variance. The between-class variance is defined as the product of the probability of the two classes multiplied by the squared difference of their means. Mathematically, it can be expressed as

$$\sigma_b^2(t) = \omega_1(t)\omega_2(t)[\mu_1(t) - \mu_2(t)]^2, \tag{7.4}$$

where $\omega_1(t)$ and $\omega_2(t)$ are the probabilities of the two classes for a given threshold value t, and $\mu_1(t)$ and $\mu_2(t)$ are the means of the two classes.

To apply Otsu's algorithm to RTN signals, the first step is to calculate the histogram of the signal, which provides the frequency distribution of the signal values. The histogram is then normalized to obtain the probability distribution function, and the cumulative distribution function is calculated. Following this, the cumulative means and the total mean are computed, which are used to calculate the between-class variance for each possible threshold value.

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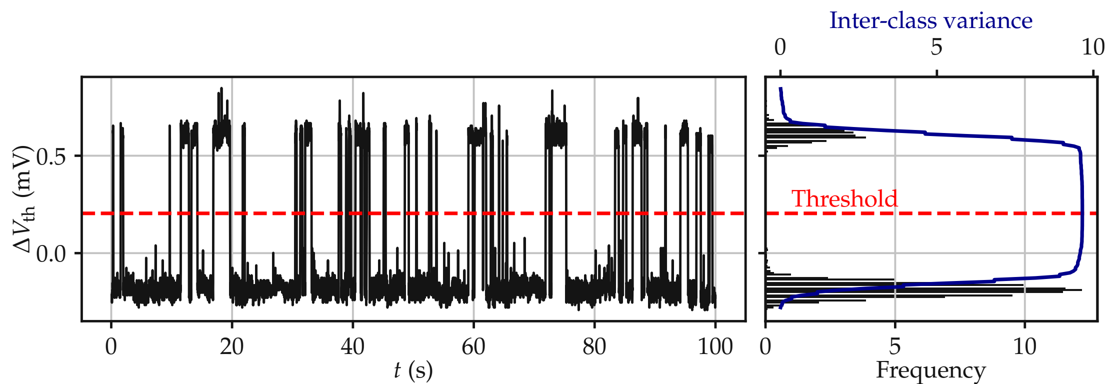

Figure 7.2. For an RTN signal (left), a normalized histogram (right) with L bins is computed. For each bin, the inter-class variance σ_b^2 can be determined, and the bin with the maximum σ_b^2 provides the best threshold value. The locations where the signal transitions from above to below the threshold value can be extracted, and the corresponding step heights and time constants are obtained.

The threshold value that maximizes the between-class variance is selected as the optimal threshold value, and the signal is then thresholded at this value to obtain a binary output image. The thresholded signal can be further analyzed to extract the positions and amplitudes of the discrete steps in the signal, which can provide valuable insights into the underlying physical mechanisms.

Compared to other edge detection algorithms, Otsu's algorithm has the advantage of being fully automated and not requiring any user-defined parameters. However, it is sensitive to noise in the signal, which can affect the accuracy of the thresholding. Therefore, it is important to preprocess the signal to remove any noise before applying the algorithm.

To enhance the accuracy of automated thresholding, it is often beneficial to apply a denoising filter beforehand to suppress measurement noise [128], although this may result in the loss of very short time constants. Nonetheless, this approach ensures a highly robust thresholding process capable of detecting small step heights. In the present study, the denoising algorithm proposed by Chambolle [128] is employed.

However, Otsu's method only applies to measurement data containing a single active defect a single active defect. When multiple active defects are present, such as in cases of multi-level RTN, it is customary to extract only the most prominent defect signal to avoid erroneous detection. Furthermore, additional sanity checks, including the Kolmogorov-Smirnov test, are employed to validate the detection results by assessing whether capture and emission times follow an exponential distribution. For a more comprehensive analysis of multi-level RTN, advanced techniques like factorial hidden Markov model analysis are necessary [129].

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Chapter 8

Measurements and Results

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This section will present the results obtained by employing the electrical measurements, data analysis techniques, and Comphy reliability simulations discussed in the previous chapters. Section 8.1 will delve into the statistical analysis of individual defect measurements, adopting the defect-centric approach and focusing specifically on Si/SiO_2 MOSFETs under BTI conditions. *The measurement results of this technology have been published in [KTJ7, KTC1, KTJ5].* In Section 8.2, BTI's characterization will be showcased through single defect measurements on Si/SiON MOSFETs. These measurements and the extracted parameters will be used to calibrate the Comphy framework to simulate MSM sequences. *The measurement results and Comphy simulations based on this technology have been published in [KTC2, KTJ4].* Finally, Section 8.3 will discuss the results of RTN measurements conducted on high-k MOSFETs integrated within smart arrays.

8.1 Impact of Defects on SiO_2 Transistors

The impact of single defects in nanoscale devices is considered a significant challenge in modern technologies [47]. When compared to larger devices with dimensions in the micrometer range, nanoscale devices exhibit a considerable level of variability in their characteristics [48]. Although the number of defects affecting the performance has decreased over the past few decades, the impact of a single defect on the drain-source current and the associated threshold voltage shift ΔV_{th} has increased [24, 46]. Because of the reduced capacitance in nanoscaled devices, on average, each defect has a more significant effect on the surface potential [106]. In devices with small gate areas, the trapping of charges at oxide defects can lead to a significant reduction in the source-drain current, even for single charged defects. The current is reduced due to the defect's effect on the percolation path, as depicted in Figure 8.1. Due to the increased impact of charge trapping, emission events appear as discrete steps in the MSM measurements [130, 40, 131, 106], and statistical analyses based on their characteristics can be conducted.

The average threshold shift induced by a single defect (η) and the average number of active defects per device (N_T) are the main parameters of interest when studying the variability of devices. The dependence of these parameters on the device geometry is

a decisive factor for optimizing device dimensions against the detrimental effects of charge trapping. Two models have been proposed for planar FETs: $\eta \propto 1/(WL)$ [112, 114] and $\eta \propto 1/(W\sqrt{L})$ [26]. For the technology studied here, results show that the defects' impact follows $\eta \propto 1/(W\sqrt{L})$ when measured close to V_{th} and $\eta \propto 1/(WL)$ when measured close operating conditions. Additionally, the DCM [112, 132] has been used to evaluate large-area devices of the same batch, and the results obtained from single-defect extraction agree with the DCM investigations. This provides a fully consistent picture and methodology to evaluate the effect of charge trapping in both large-area and scaled technology nodes.

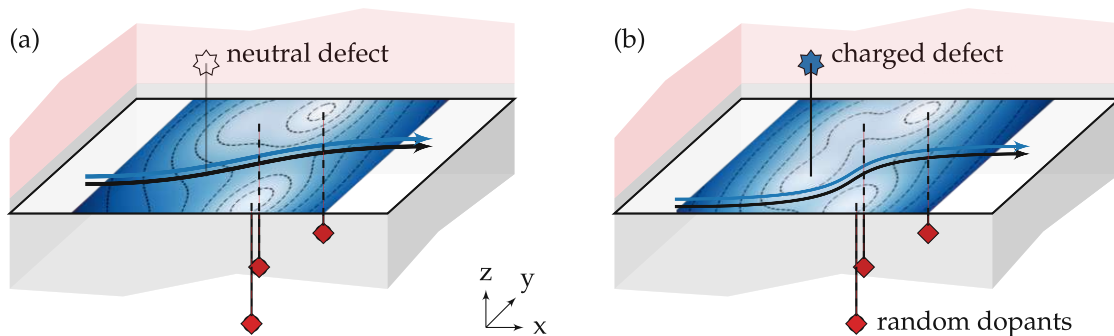

Figure 8.1. Schematic of the carrier densities in the channel of a scaled device and the resulting current percolation path. (a) The randomly distributed dopants lead to locally decreased carrier densities. The neutral defect does not influence the current path. (b) When the defect is charged, the restrictions on the percolation path increase, leading to a decreased drain current and a higher threshold voltage [50]. Originally published in [KTJ7]

8.1.1 Devices and Measurements

Electrical measurements under NBTI and PBTI stresses were conducted on pMOS and nMOS devices with a wide range of gate areas, fabricated in a commercial technology using SiO_2 as gate insulator. A MSM scheme, see section 6.2.1, was employed to study the temporal recovery of device degradation, which was monitored using DPI [43].

The MSM measurements for each device under test consisted of three phases: an initial $I_{\mathrm{D}}(V_{\mathrm{G}})$ measurement within a narrow gate bias window, a stress phase with a gate field of 7 MV/cm and a temperature of $T = 100\,^{\circ}\mathrm{C}$ for a stress time of 100 s, and a recovery phase with a recovery field corresponding to V_{th} and time of 100 s. The drain current was recorded during the recovery phase using a constant current criterion. The resulting recovery curves were mapped to equivalent ΔV_{th} traces using initially measured $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics, assuming negligible changes in SS. The V_{th} values from the constant current criterion were confirmed using the method of the second derivative of the drain current.

The stress conditions were optimized to capture a sufficient number of defects for statistical significance without needing excessively long measurement sequences or

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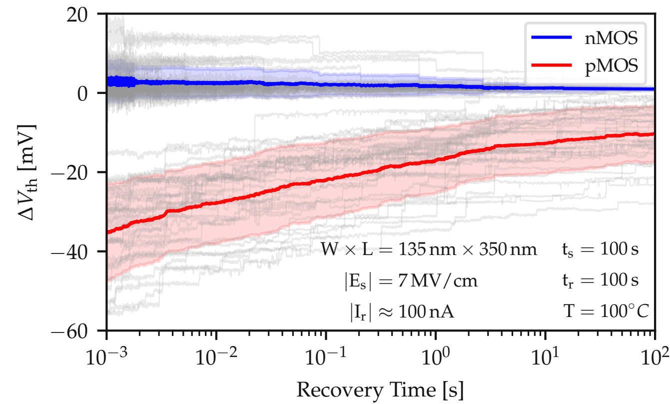

Figure 8.2. Recovery traces obtained from scaled pMOS and nMOS devices showing the drift of the threshold voltage after NBTI/PBTI stress over time, measured on a scaled SiO_2 technology. As can be seen, the recovery proceeds in positive discrete steps for pMOS and negative for nMOS. Increased variability is observed between nominally identical devices. Originally published in [KTJ7].

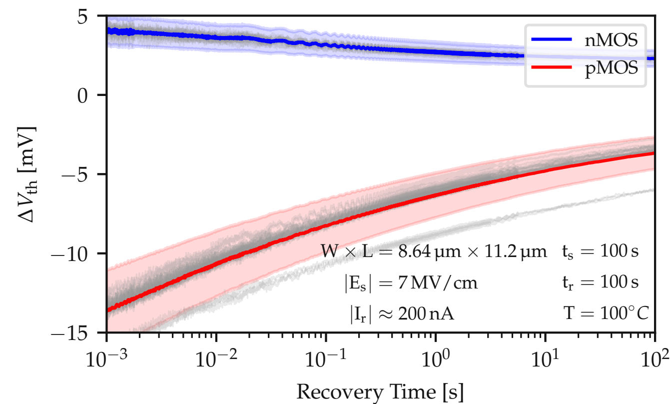

Figure 8.3. Recovery traces obtained from large pMOS and nMOS devices showing the drift of the threshold voltage after NBTI/PBTI stress. The traces recover similarly in a continuous manner as the increased number of defects with reduced impact on ΔV_{th} lead to a smaller variability. Originally published in [KTJ7].

special efforts to disentangle the signals from simultaneously occurring charge emission events at different defects. These parameters were tested on the smallest geometry, where three different batches were available to test devices with the same parameters without previous stress affecting the results. The operating conditions of the test devices were around 3 MV/cm, making the stress bias strong enough to charge a large ensemble of defects while avoiding extensive damage to the devices.

Figure 8.2 shows ΔV_{th} traces as a function of recovery time after gate stress conditions for pMOS and nMOS devices with SiO_2 as the gate insulator. These traces were obtained by converting measured drain currents to an equivalent ΔV_{th}. Typically, pMOS devices with SiO_2 insulators are more affected by BTI than nMOS devices, as evidenced by the difference in the total ΔV_{th} in Figures 8.2 and 8.3. This difference can be explained by the relative position of trap bands in the insulator with respect to the silicon band edges [133].

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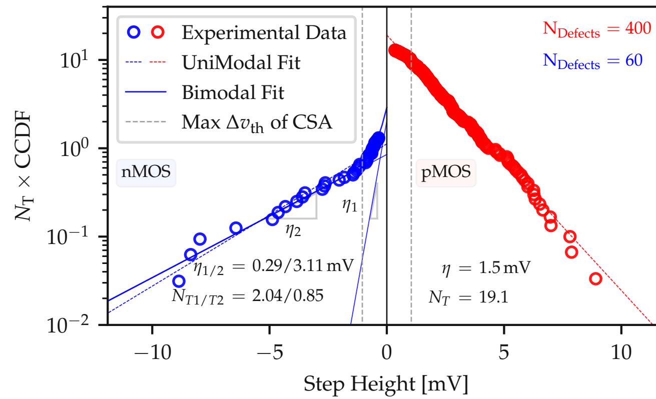

Figure 8.4. The CCDFs of the extracted discrete steps are shown. The pMOS data seem to follow a unimodal exponential function, while nMOS data can be described by a bimodal exponential function. The maximum limit of the CSA is shown as vertical dashed lines. Originally published in [KTJ7].

8.1.2 Measurement Analysis

The two primary methods used for the measurement analysis are the step height extraction of single defects and the DCM.

Single-defect Analysis

The Canny algorithm, see Section 7.1, embedded in the used data analysis framework [113, 116], is used to extract the discrete transitions of ΔV_{th} shown in Figure 8.2. To avoid measuring artifacts due to the noise of the measuring system [43], the range of extracted step heights is considered inside the noise limits of each measured time interval.

To describe the contribution of electron and hole traps on ΔV_{th}, a CCDF is created based on the collected amplitude of step heights (Δv_{th}) for each device geometry normalized to the active number of defects per device, see Section 5.2. Previous studies have observed that pMOS devices can be described by a unimodal exponential distribution [24], while both unimodal and bimodal exponential behavior has been observed for nMOS devices [45, KTC2]. The CCDFs obtained for the smallest geometry of the pMOS and nMOS set can be seen in Figure 8.4, where a unimodal exponential CCDF is observed for the pMOS data and a bimodal one for the nMOS data.

Defect Centric Model (DCM)

The number of defects per device is typically modeled by a Poisson distribution [112]. The DCM [112], see Section 5.3.1, combines the Poisson distribution of the number of defects per device with the exponentially distributed step heights to calculate the distributions of the total ΔV_{th}. The first two moments of ΔV_{th} can be used to extract the two statistical parameters of interest: the average $\langle \Delta V_{\mathrm{th}}(t) \rangle$ at a given time and its variance $\sigma^2(t)$.

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$$\sigma^2(t) = 2\langle \Delta V_{\text{th}}(t)\rangle \eta,$$
$$\langle \Delta V_{\text{th}}(t)\rangle = N_{\text{T}}(t)\eta,$$

In this work, DCM is employed to evaluate the data from both nanoscale and large-area devices. The DCM is particularly useful for evaluating device geometries where single charge transitions are obscured by measurement noise, such as large-area transistors. Therefore, the combination of both single-defect analysis and DCM provides a versatile framework for evaluating time-dependent variability in transistor technologies.

8.1.3 Negative BTI in pMOS Devices

In the following, the examination focuses on how the impact of charge traps on the threshold voltage (ΔV_{th}) is influenced by the recovery bias, as opposed to previous studies, which focused primarily on charge trapping near the sub-threshold regime. It is important to note that when utilizing this information in a circuit, understanding BTI's effect over a wide bias range is required for efficient and robust design.

Operation Regime Close to V_{th}

Specifically, the operation regime close to the threshold voltage (V_{th}) is studied, by examining the collected amplitudes of charge transitions following NBTI stress on pMOS devices with scaled geometries. These amplitudes are represented in the form of CCDFs in Figure 8.5, where the symbols represent experimentally extracted step heights and the dashed lines represent unimodal exponential functions used to describe the data. It was found that the unimodal exponential distributions provided a smaller error for the tested data set when compared to other distributions in the literature, such as lognormal or bimodal exponential distributions [134, 135, 136, 137], despite having fewer available parameters. However, it should be noted that the range of each measurement unit may influence the optimal distribution for explaining experimentally created distributions. In this particular data, a limit of 0.3 mV is used for the amplitudes, to avoid kinks at small step heights or missing steps in that range due to measurement noise.

The mean of the unimodal exponential distributions, i.e. the average threshold shift induced by a single emission event (η), determines the slope of the function. Devices of the same area are expected to have the same mean in terms of the CSA. However, in the studied geometry, it is observed that devices with the same area but different W/L lead to different η. The same slope is observed in two device sets with the same $W \times \sqrt{L}$.

To further investigate this observation, η was plotted against $W \times L$ and $W \times \sqrt{L}$ in Figure 8.6. The obtained root mean square error (RMSE) of a linear regression is around three times smaller in the $W \times \sqrt{L}$ case. The RMSE for the first case is RMSE $= 0.15$ mV while in the case of a $W \times \sqrt{L}$ dependence it is only RMSE $= 0.046$ mV. This asymmetry

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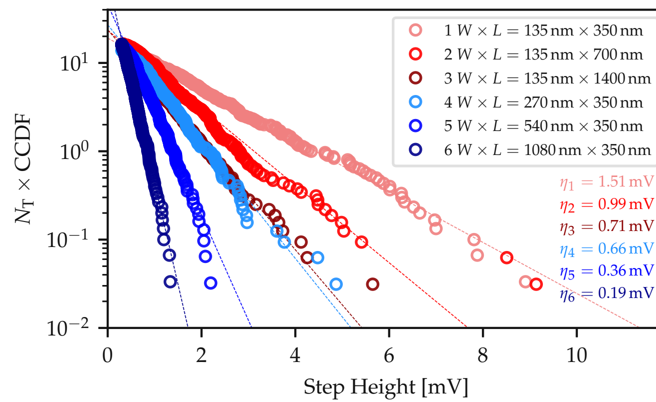

Figure 8.5. The CCDFs of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential distribution used to describe the results. A recovery bias close to V_{th} was applied during the recovery phase. Originally published in [KTJ7].

can be explained by the different impact of variations of W and L on percolative conduction [26, 108, 138]. When devices are measured close to the threshold voltage, multiple non-uniform conduction paths form due to the impact of random dopants in the substrate [110, 111]. The local potential associated with each discrete dopant acts as a barrier for the current, which consequently flows in a few narrow channels connecting the source to the drain. In this perspective, a weaker dependence on the device length can be observed, as in a narrower channel, there is a higher probability for a trap to effectively suppress a percolative conduction path [110]. Generally, any increase of W and L increases the number of charges in the inversion layer. This can lead to reduced values of η [106]. However, when considering percolative conduction, W and L will have a different impact. Increasing the area while keeping L constant, by only increasing W, will lead to a higher number of current channels between source and drain compared to a case where W is kept constant but L is increased [111]. Due to that, a single defect could have a higher impact in the latter case of a narrower channel.

The extrapolated line of the $W \times \sqrt{L}$ is extended towards larger device areas in Figure 8.7, in order to test the validity of the results for large-area devices, where the measurements are evaluated using DCM. It can be seen that the DCM values, which are depicted with the half-full symbols, are nicely captured by the $W \times \sqrt{L}$ trend. In some geometries, the markers for the experimental data and data from the DCM model overlap as their values are too close for a difference to be observed on the logarithmic scale.

Next, the number of active traps N_{T} are plotted against both geometrical trends in Figure 8.8. It should be noted that a comparison of the N_{T} values is meaningful here, as data sets for the same NBTI bias conditions are compared. Again, for the comparison of N_{T}, the $\mathrm{W} \times \sqrt{\mathrm{L}}$ dimensional scaling captures all the data more accurately. Regarding the number of defects, this trend can be explained by the generally higher number of low-impact active defects which can be detected due to the increased percolative conduction in wider devices [110, 111]. Thus, scaling the width can increase the number

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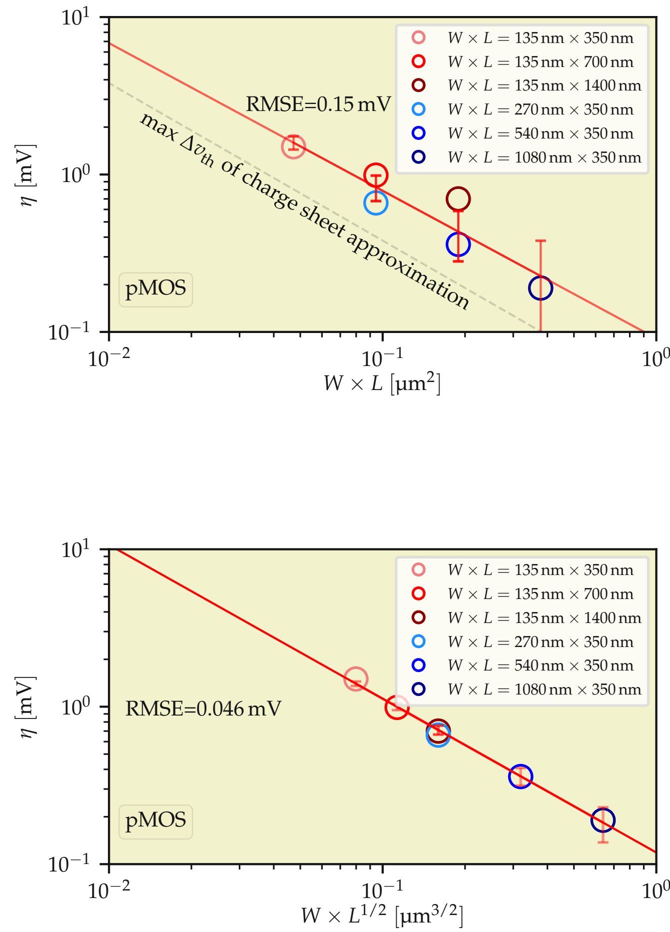

Figure 8.6. (Top) The η values for the unimodal fit used in Figure 8.5 are plotted against the area. The devices with the same W scale nicely, but the devices with different W deviate from this trend, showing higher step heights. (Bottom) The η values for the unimodal fit are plotted against $W \times \sqrt{L}$. The fitted line seems to accurately capture all the data obtained from different geometries. Originally published in [KTJ7].

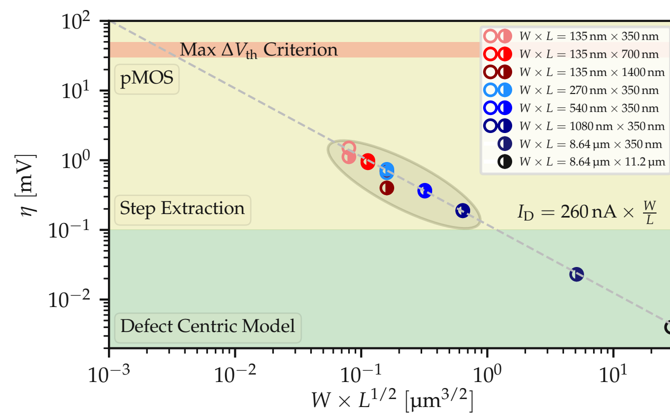

Figure 8.7. The η values are plotted against $W \times \sqrt{L}$ trend. The fitted line nicely captures both experimental and DCM values. For some geometries, the markers used for the experimental data and data from the DCM model overlap as their values are too close to see a difference on a logarithmic scale. Originally published in [KTJ7].

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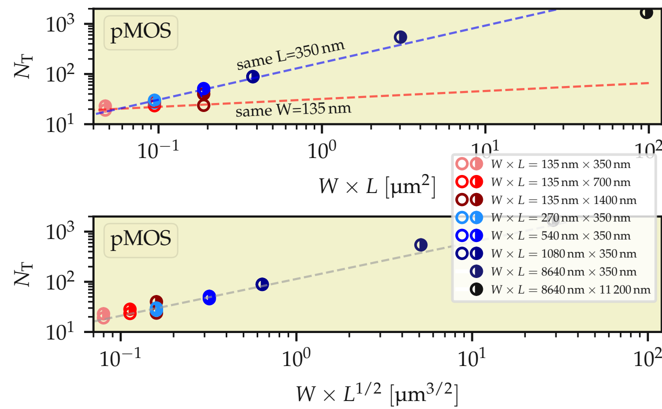

Figure 8.8. The average number of defects per device is plotted against both dimensional trends. The marker and color of the symbols follow the same convention as previous figures. Originally published in [KTJ7].

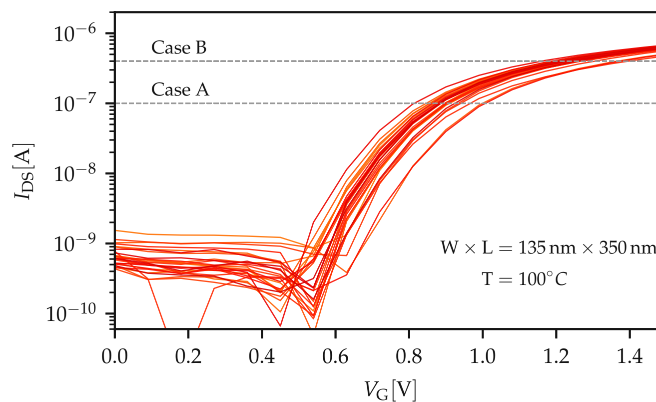

Figure 8.9. The $I_D(V_G)$ characteristics of the smallest devices of the set. The grey dashed lines indicate the measurement conditions where the recovery traces were recorded. Originally published in [KTJ7].

of defects more substantially but also decrease the impact of every single defect.

On-state Operation Regime

In order to study the impact of the percolative conduction on the average step height, the device set was measured at higher biases, corresponding to operating conditions, where a more uniform way of conduction is expected due to the increased carrier density in the inversion layer. The two different measurement conditions used in measurement cases can be seen in Figure 8.9, together with the set of initial $I_D(V_G)$ curves for the smallest device geometry. The measurements were conducted as close to the limit as possible, where the discrete nature of recovery persists. As can be seen in Figure 8.10, the plotted η seem to follow the area trend, as the η values of narrow devices are close to the values of the wider devices of the same area. The error for the area trend is around three times lower compared to what has been observed for the measurements around V_{th}. The calculated values from the DCM are also captured nicely by the same trend.

The η values are expected to decrease when measured at higher recovery biases

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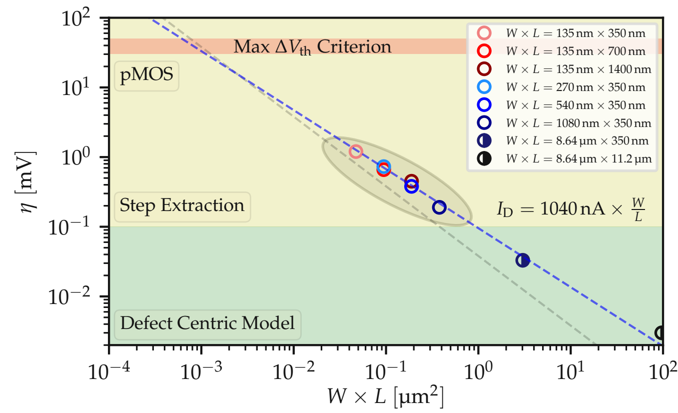

Figure 8.10. The η values for the on-state measurements are plotted against $W \times \sqrt{L}$. The fitted line accurately captures all the data obtained from different geometries and the DCM values for the two large geometries. Originally published in [KTJ7].

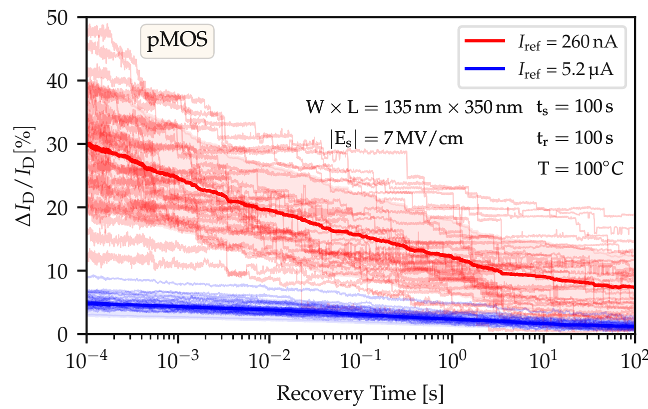

Figure 8.11. Traces of the smallest device of the set measured close to Vth (red lines) and at high operating conditions. At high operating conditions, the recovery is no longer observed in a discrete manner due to the increased charge in the inversion layer. Originally published in [KTJ7].

due to the increased screening of trapped charges from the inversion layer [106]. This can be observed clearly in Figure 8.11, where a high recovery bias, five times larger than V_{th}, is used. In this operation regime, the traces are recovering in a continuous form and discrete steps can not be distinguished anymore, as η values become smaller than the measurement noise, similar to what has been observed in large-area devices. In Figure 8.11, the convention of $\Delta I_D / I_D$ is used, to avoid comparisons of ΔV_{th} for such large differences in recovery biases, as the drain current becomes too large to allow for accurate extraction of ΔV_{th}.

The average number of active defects for measurements close to V_{th} and close to the on-state can be seen in Figure 8.12 marked with red and blue color, respectively. Interestingly, more active defects are observed in the measurement window for the higher recovery bias. The only deviation from this overall trend is observed for the largest geometry shown in Figure 8.12. A possible explanation of this deviation is that some events can be missed in the extraction process as the amplitude decreases when the area and the recovery bias increase.

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For the case of a higher recovery bias, a smaller portion of the activated defects is expected to recover due to the smaller active energy region (AER). Furthermore, the measurement window's range and the readout bias's impact on the charge transition times can affect the results. Emission times of defects are expected to have a slight dependence on the recovery bias [40, 41]. If emission times increase with higher recovery biases, events with emission times smaller than the selected measurement range for V_{th} can become accessible for the recovery conditions in the on-state. Additionally, the bias dependence of each trap differs, thus, it is plausible that more events with fast emission times fit in the measurement window in comparison to the slow emission times, which are no longer accessible.

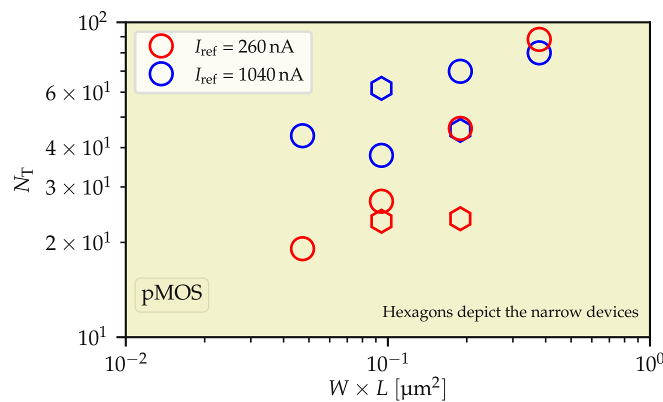

Figure 8.12. The average number of active defects for the two measurement cases plotted for all the geometries. Higher values are observed when devices are measured at the on-state. Originally published in [KTJ7].

8.1.4 Positive BTI in nMOS devices

The measurements of nMOS devices have been performed on four scaled geometries where the step extraction was possible and two large ones that have been analyzed with the DCM. The CCDFs for the scaled nMOS device can be seen in Figure 8.13. For all nMOS device geometries studied, the recovery condition was chosen close to V_{th}. In addition to the exponential unimodal distributions used in the pMOS case, bimodal distributions were used to describe the results since they appear to show more minor errors when used for nMOS devices. The solid lines depict the bimodal exponential functions, and the dashed lines depict the unimodal exponential functions.

It is worth noting that the bimodal exponential distributions have been mainly observed in the past for devices with high-κ gate stacks, where each branch of the distribution has been assigned to charge transfer interactions of defects within each of the two layers, e.g. SiO_2 and HfO_2, with the channel [45]. Recently, the bimodal exponential distributions have been reported for devices with SiON insulators [KTJ4].

In order to develop an understanding of the geometrical dependencies of the two exponential branches, the average step heights were collected and plotted against $W \times L$

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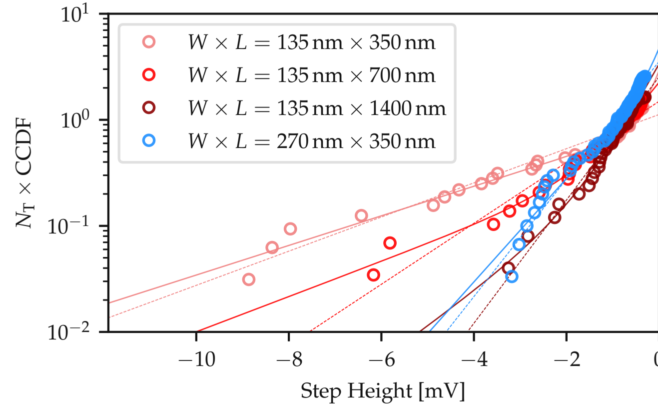

Figure 8.13. The CCDFs of step heights of electron traps extracted after PBTI stress on nMOS devices. The bimodal exponential distributions (solid lines) describe the results more accurately than the unimodal exponential distributions (dashed lines). Originally published in [KTC1].

and $W \times \sqrt{L}$, see Figure 8.14. To compare the errors of the two distributions, the root-mean-square error (RMSE) was computed and normalized (nRMSE) to the range of the values for the two cases.

The $W \times \sqrt{L}$ behavior describes the data more accurately for the unimodal case than pure area scaling. For the $W \times L$ dependence, $\mathrm{nRMSE}_{\mathrm{Unimodal}} = 0.16$ while for the case of a $W \times \sqrt{L}$ dependence is $\mathrm{nRMSE}_{\mathrm{Unimodal}} = 0.02$. In the case of the nMOS devices, a clear overall trend of the η values describing the bimodal exponential distribution cannot be observed. While the slope of the second branch scales for both cases, the first branch does not follow the trend and instead seems to be uncorrelated to the device dimensions.

The $W \times \sqrt{L}$ trend is presented in Figure 8.15 together with DCM data. The η values of step detection are taken from the second branch of bimodal distribution as they appear to be closer to DCM values. The DCM values of large-area devices deviate from the trend observed for the experimentally extracted step heights from single defect measurements. The reasons for these deviations observed for PBTI on nMOS devices are currently unclear and need to be analyzed together with the origin of the bimodal distribution in more detailed future investigations.

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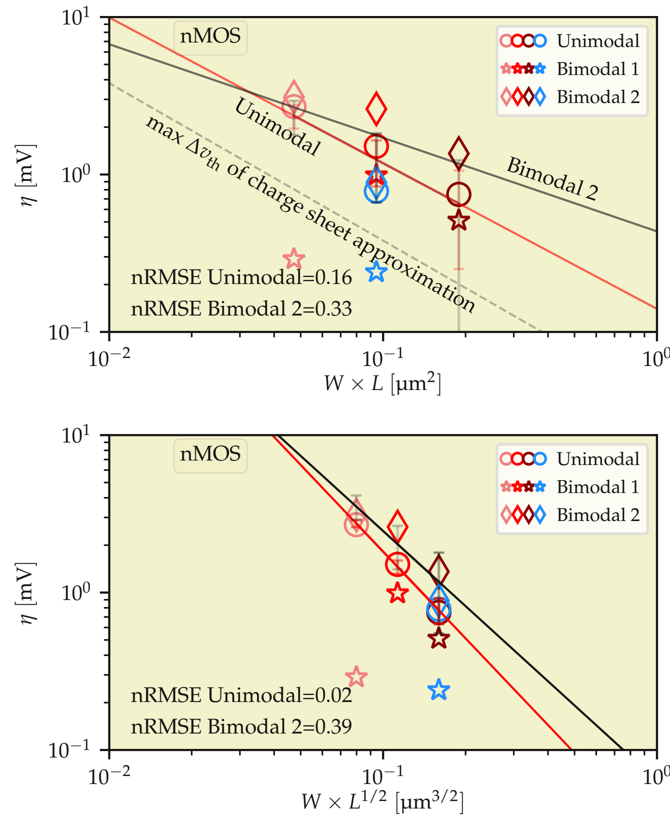

Figure 8.14. (Top) The average step heights induced by single defects (η) for the data used in Figure 8.13 are plotted against the area. The red line shows the scaling of the values following a unimodal exponential distribution, and the gray dashed line is used as a comparison to the CSA. The RMSE values were normalized to compare the two different η ranges. (Bottom) The average step heights induced by a single defect (η) for the two distributions used in Figure 8.13 are plotted against $W \times \sqrt{L}$. A smaller error is observed in the latter case for the unimodal distribution. Originally published in [KTJ7].

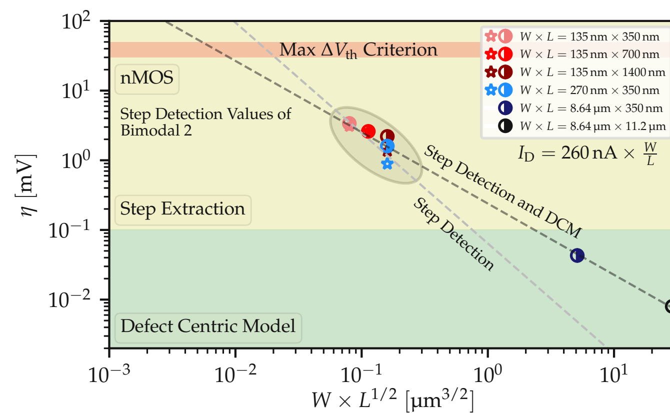

Figure 8.15. The average step heights induced by single defects (η) is used together with calculated values from DCM for the large devices that are plotted against $W \times \sqrt{L}$. The step detection values are taken from the second branch of bimodal distribution as they are closer to DCM values than the values extracted from unimodal distribution. Originally published in [KTJ7].

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8.1.5 Body Bias Dependence

In previous sections, it was examined how lateral dimensions and recovery gate conditions impact the statistical quantities related to defects such as η and N_T. Next, research focus is extended on how body bias (BB) can also play a pivotal role in shaping the effect of individual charged defects on device behavior.

Time-zero Characteristics

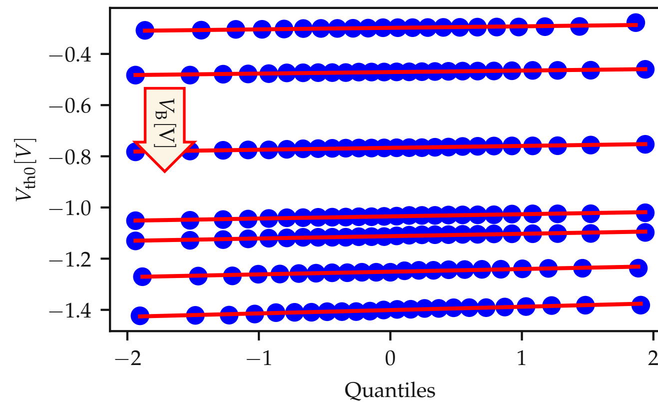

Figure 8.16. Probability distribution of the initial V_{th0} values across a sample set of nanoscaled devices under varying V_B conditions, conforming to normal distributions. This change is largely attributed to modifications occurring in the depletion layer thickness X_{dep} as a response to alterations in BB settings.

In the analysis of the $I_D(V_G)$ measurements, the extracted V_{th0} values manifested a normal distribution, see Figure 8.16. The BB impact is known to modulate the channel depletion layer thickness (X_{dep}) and, as a result, the average threshold voltage, but it seems to also influence the variability of V_{th0} [139]. With the introduction of a forward body bias (FBB), the spread of V_{th0} in the standard deviation affiliated with the distribution was reduced, as depicted in Figure 8.17 for pMOS and Figure 8.18 for nMOS devices

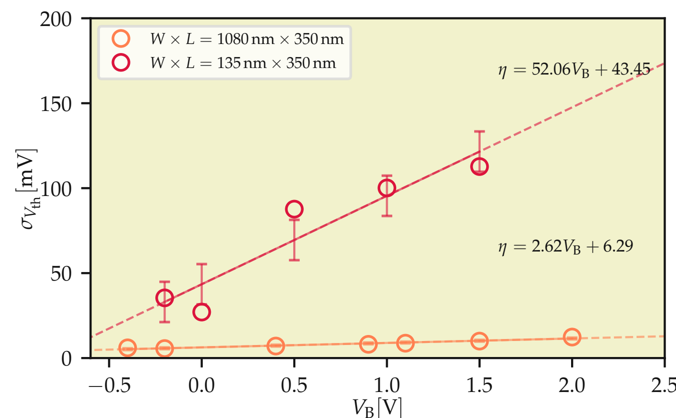

Figure 8.17. Influence of the body bias on V_{th0} variability for pMOS devices. Under FBB, a reduced standard deviation of the normal distribution is observed. The smaller geometry exhibits higher initial variance and a more pronounced slope.

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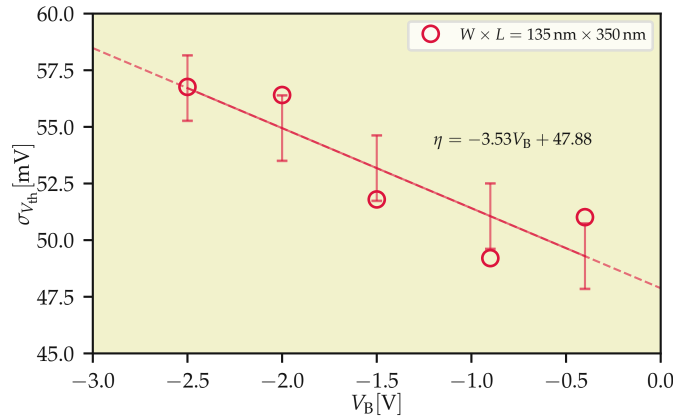

Figure 8.18. Influence of the body bias on V_{th0} variability for nMOS devices. The standard deviation is a few times higher in nMOS devices compared to their pMOS counterparts.

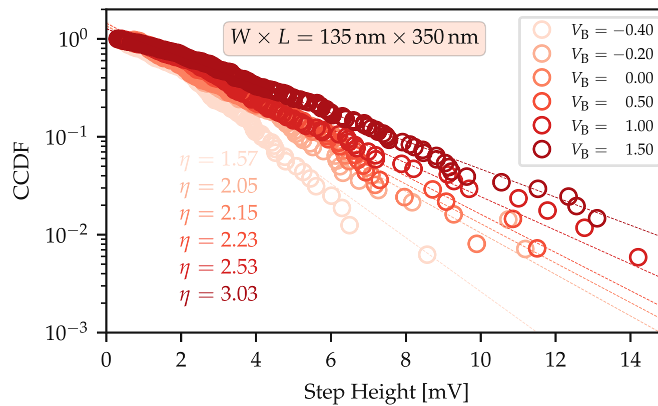

Figure 8.19. Exponential distributions of individual charge ΔV_{th} step heights for a consistent device sample set under varied V_B conditions. RBB shows a heightened variance (elevated η), whereas the FBB exhibits a diminished variance (lower η).

accordingly. This effect was more pronounced in pMOS devices with dimensions of 135 nm × 350 nm.

Reducing X_{dep} through adjustments in BB has similar positive effects as reducing the channel doping level, notably decreasing the initial variability. This observation suggests that fine-tuning of BB could emerge as a valuable strategy to control variability in device functionalities, similar to how adjustments in doping levels are used [139].

Negative BTI for pMOS devices

The CCDFs for pMOS geometries with increasing width are displayed in Figure 8.19 together with their unimodal fits depicted with dashed lines. The extracted η values are plotted against V_B values in Figure 8.20, where a linear fit approximation is used for this bias range. A rise in V_B results in greater η values. Furthermore, the smaller geometry exhibits higher η values at $V_B = 0$ and a more pronounced slope, revealing the clear influence of substrate dopants on η values together with area dependence. TDDS relaxation traces captured for two different BB conditions on a device with a dominant oxide trap can be seen in Figure 8.21. Notably, the BB seemed to impact the step heights

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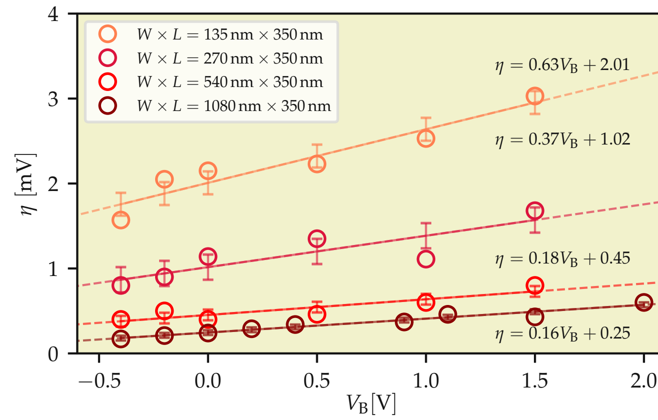

Figure 8.20. The average step heights induced by a single defects (η) against the V_B for pMOS devices. Increased V_B leads to higher η values. The smaller geometry exhibits higher η values at $V_B = 0$ and a more pronounced slope.

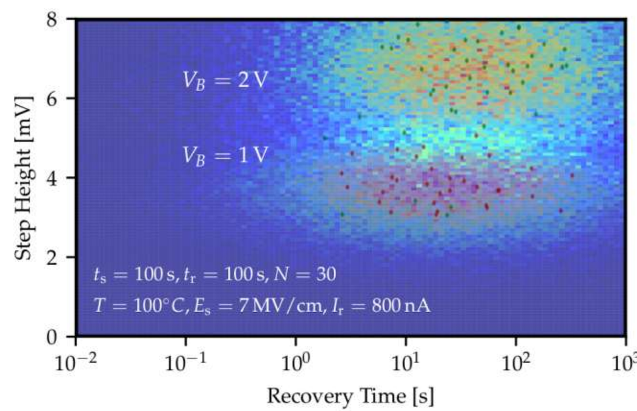

Figure 8.21. TDDS on two different BB settings on a single device. The studied step height is heavily influenced. The larger RBB leads to an increase in the step height, an observation consistent with what has been observed in the CCDFs of multiple devices.

in a similar way as in Figure 8.20, where the increase of V_B leads to higher η values. This phenomenon proved consistent, repeating in numerous devices showcasing substantial gate oxide defects.

The trends observed in the experiments have a strong connection to the adjustments in X_{dep}. RBB can expand X_{dep}, allowing the dopants in the substrate to have a more pronounced effect on the current's flow paths. Essentially, utilizing BB to manage X_{dep} emerges as a promising strategy to reduce the complications arising from RDD, enhancing bot time-zero and time-dependent variability.

Positive BTI for nMOS devices

In Figure 8.22, the CCDFs for the nMOS set of measurements are displayed. Applying a bimodal exponential function typically provides a more accurate representation of the experimental data, characterized by a reduced statistical error. Despite this, and considering the inconsistent scaling highlighted in [KTJ7], a single exponential distribution is emplyed to derive the η values. The outcomes of this process are illustrated in

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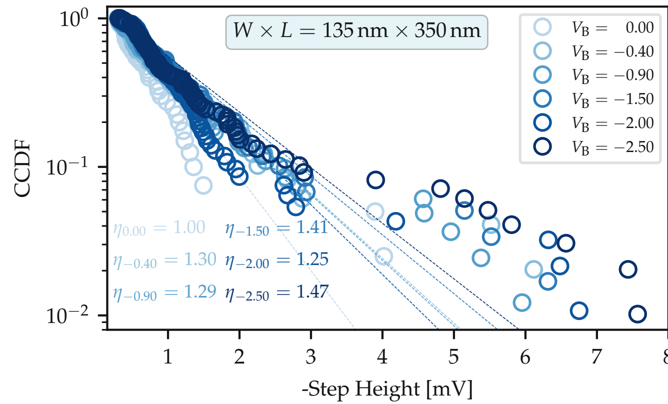

Figure 8.22. The CCDFs of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential function used to explain the results.

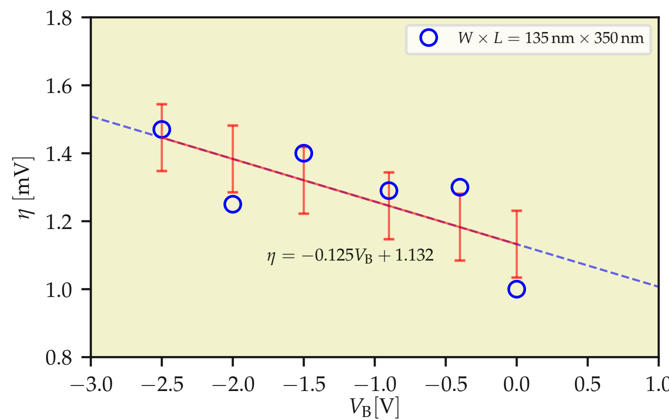

Figure 8.23. The average step heights induced by a single defect (η) for the data used in Figure 8 are plotted against the V_B. Increased -V_B leads to higher η values. The slope is less steep for the nMOS case.

Figure 8.23, where it can be observed that the extracted η values follow a similar scaling trend as those of pMOS, albeit with a slightly diminished slope.

Shifting focus to Figure 8.24, the TDDS results are presented, delineating the outcomes under the extreme settings of both FBB and RBB. Analyzing a selected defect, it was anticipated and confirmed that higher step heights are attained with RBB. Interestingly, the discrepancy between the two clusters was less pronounced than initially hypothesized, especially when compared to their pMOS counterparts. This subtler distinction may be attributed to the relatively lower concentration of dopants present in the nMOS devices, which influences the observed behaviors.

8.1.6 Conclusions

The statistical distributions of the step heights of threshold voltage drift describe the contribution of single defects. These step heights are observed by applying the MSM scheme under PBTI conditions on nMOS devices and NBTI on pMOS devices with dimensions small enough to observe discrete steps when charge transitions occur. Based

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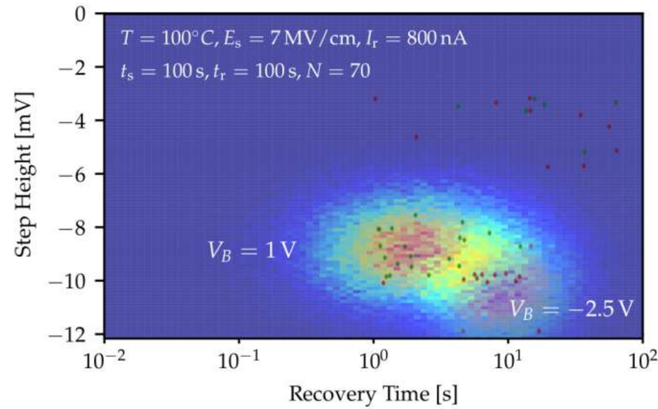

Figure 8.24. TDDS for two different BB conditions on a selected device. The step heights at larger RBB are increased, an observation consistent with what has been observed in the CCDFs. BB impact is smaller in nMOS devices than in pMOS devices.

on the detected steps, the CCDFs of the step heights are created and η values by utilizing exponential functions are extracted. The findings demonstrate that a bimodal exponential distribution can explain the results extracted from nMOS data and a unimodal exponential distribution the results from pMOS data. For the measurements close to V_{th}, it is shown that the scaling of statistical parameters is described better by a $W \times \sqrt{L}$ trend rather than the area of the devices $W \times L$ which is typically used in literature. However, if a higher recovery bias is applied η decreases, especially on devices affected more by the percolative conduction, and the $W \times L$ trends capture nicely the values for all the tested geometries. At the same time, more defects contribute to the observed degradation for higher recovery bias conditions. Nevertheless, the dimensional scaling trends for the step heights for a bimodal distribution for nMOS data can still not be fully resolved and need to be addressed in future studies.

Finally, in the results of the influence of individual charged gate oxide defects on nanoscaled pMOSFETs, the role of body bias emerged as a critical factor. Distinct changes were identified in both time-zero and time-dependent variabilities. The underpinnings of these observations lie in the alteration of unscreened dopant atoms in the channel depletion zone, which are modulated by the body bias. Using an RBB raises both X_{dep} and V_{th0}, making it useful for applications that require low leakage. On the other hand, an FBB decreases X_{dep} and V_{th0}, which can be beneficial for high-performance applications, albeit with a trade-off of higher junction leakage. These findings are of high relevance to the reliability of nanoscaled MOSFETs as they constitute a flexible electrical technique to improve the time-zero and the time-dependent variability in nanoscaled MOSFETs without involving any technological tuning.

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8.2 Single-defect analysis of BTI employing SiON Transistors

A single defect analysis has also been performed in a commercial SiON technology in addition to SiO_2, which was examined in the previous section. Furthermore, it is observed that the electron and the hole trap contributions for each device kind, indicating that trapping at both trap types is of equal importance for precise descriptions of the devices. Previous research on SiON technologies has suggested that the step heights of single defects are best described by unimodal exponential distributions. However, the investigation has uncovered evidence that suggests bimodal exponential distributions are a more accurate representation. The importance of this discovery lies in accurately assessing the tail of the distribution, which encompasses defects that can have a significant impact on the ΔV_{th} and cause device and circuit failure. To better understand the effect of these defects, their statistical distributions are analyzed and compared to values obtained using the commonly used CSA. The results indicate that the CSA significantly underestimates the true impact of the defects for the studied SiON technology. Finally, the obtained distributions are used to evaluate their impact on the variability of measure-stress-measure simulations, utilizing Comphy.

8.2.1 Devices and Measurements

For this technology, both nMOS and pMOS devices with different geometries have been investigated under both PBTI and NBTI conditions. The measurement process is the same MSM sequence as the one mentioned in the previous section. The only difference is that in this study the device set was measured with stress and recovery times of 1 ks.

8.2.2 Positive BTI in nMOS Transistors

Initially, the temporal variability and reliability of nMOS devices are examined by applying a positive stress bias. When a positive bias is applied on the gate of a MOS structure, the valence and conduction band edges bend towards lower energies. Figure 8.25 (left) presents a schematic representation of the band diagram during PBTI stress.

For a defect to impact ΔV_{th}, it must be located in the AER where charge trapping occurs. In the case of PBTI, electron traps above the Fermi level of the channel carrier reservoir and hole traps below the Fermi level at the poly-gate can acquire and release charges under specific conditions. These conditions require that the applied stress lasts longer than the time it takes to capture the charge and that the recovery time exceeds the emission time of the respective defect. Consequently, the energetic range covered by the AER, governing the charge exchange between the channel and electron traps (represented by blue triangle) and between the poly-gate and hole traps (depicted as red triangles), is determined by the bias utilized for the MSM measurement.

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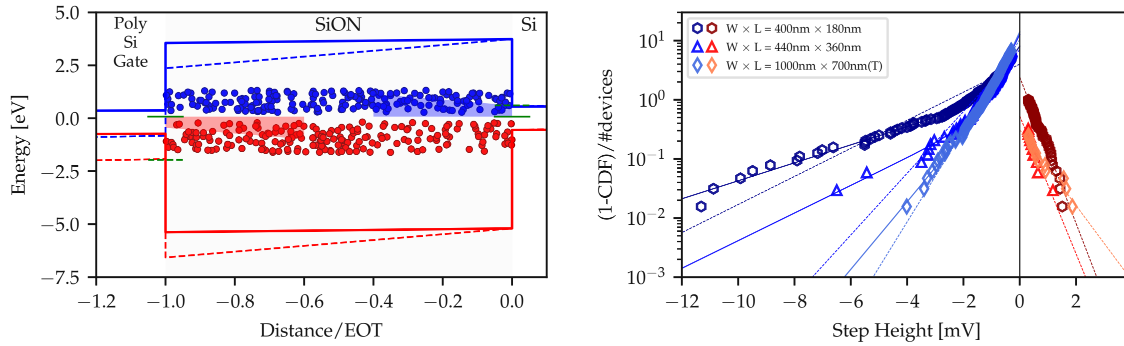

Figure 8.25. The figure presents the band diagram of nMOS devices under PBTI conditions. It illustrates the presence of electron traps (depicted in blue) and hole traps (depicted in red), along with their respective AERs for charge trapping. The blue region represents the AER for charge transitions between the defects and the channel. In contrast, the red region represents the AER for charge transitions between the defects and the gate. These regions define the energetic boundaries within which the defects can change their charge state during the experiments, thereby contributing to the drift of the measurement signal. It should be noted that the height of the AERs varies with the applied gate bias. On the right side, the distribution of step heights, measured from SiON nMOS transistors after undergoing PBTI stress, is shown for three sets of devices with different geometries. The majority of observed traps are electron traps (depicted on the left), although a certain number of hole traps (depicted on the right) can also be observed. The electron traps show a bimodal exponential distribution, while the holes traps show a unimodal exponential behavior. Originally published in [KTC2].

Figure 8.25 (right) displays the corresponding CCDFs for the PBTI scenario for three sets of devices with different geometries. The largest device (denoted as (T) in the figure legend) possesses a thicker oxide compared to the other two devices. Consequently, a higher gate bias is employed to maintain a consistent oxide field. Electron trapping, involving the interaction between the silicon channel and defects, is represented by blue shades, while red shades represent hole traps, which denote interactions between the poly-gate and defects. The CCDFs following PBTI stress exhibit a bimodal exponential behavior for electron traps and a unimodal exponential characteristic for hole traps. To fit the experimental data and extract device parameters η and N_T, the normalized CCDF (Equation 5.3) is employed. The unimodal and bimodal fits are represented by dashed and solid lines, respectively. The obtained parameters for the PBTI case are listed in Table II.

Based on the gathered parameters and the CCDF plots, it can be seen that the impact on ΔV_th during PBTI stress conditions is primarily governed by electron traps. However, a small number of active hole traps have also been identified. Out of a total of 990 recorded traps, 910 defects (92 %) have been characterized as electron-related, whereas hole trapping originates from interactions between defects and the gate, as indicated by recent research [46]. An advantageous aspect of investigating single defects is the ability to separate the contributions of electron traps and hole traps. In contrast, when examining large-area devices, only the average response of numerous defects can be

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Table 8.1. Extracted parameters of CCDF fitting on experimental data for the PBTI study case. Superscripts e and h refer to electron and hole trapping accordingly. The bimodal fit is only used for electron traps since hole traps do not exhibit two branches.

unimodal

W(nm)	L(nm)	$\eta^{e}(mV)$	N^{e}	$\eta^{h}(mV)$	N^{h}
400	180	1.8	4	0.35	2.4
440	360	0.83	7	0.37	0.5
1000	700	0.56	10.4	0.6	0.31

bimodal

W(nm)	L(nm)	$\eta_1(mV)$	N_1	$\eta_2(mV)$	N_2
400	180	0.52	6.64	2.86	1.4
440	360	0.42	11.79	1.86	0.89
1000	700	0.36	10.54	0.76	3.52

Table 8.2. Extracted parameters of CCDF fitting on experimental data for the nMOS/NBTI study case. Superscripts e,h refer to electron and hole trapping, respectively.

W(nm)	L(nm)	$\eta^{e}{}_1(mV)$	$N^{e}{}_1$	$\eta^{e}{}_2(mV)$	$N^{e}{}_2$	$\eta^{h}{}_1(mV)$	$N^{h}{}_1$	$\eta^{h}{}_2(mV)$	$N^{h}{}_1$
400	180	0.33	6.73	2.49	0.21	0.25	4.22	1.04	2.26
440	360	0.37	6.9	1.39	1.45	0.37	4.15	2.22	0.3
1000	700	0.16	18.54	0.62	1.08	0.18	26.33	0.72	1.02

measured.

The absolute contribution of a particular carrier type, such as electrons, to the overall threshold voltage shift ΔV_{th}, can be calculated using the equation [46]:

$$r_e = \frac{\sum_{i=1}^{N_e} |d_e|}{\sum_{i=1}^{N_e} |d_e| + \sum_{i=1}^{N_h} |d_h|}, \tag{8.1}$$

Here, N_{e} and N_{h} represent the numbers of electron and hole defects, respectively, while $|d_|$ and $|d_{\mathrm{h}}|$ correspond to the step heights of individual hole or electron emission events. It can be observed that hole trapping leads to a reduction in the total ΔV_{th} by approximately 5.9 % under the specific bias and temperature conditions employed for the PBTI case.

8.2.3 Negative BTI in nMOS Transistors

In addition to the previous section, the investigated device types were subjected to negative bias stress conditions. The application of a negative gate voltage leads to a reverse band bending compared to the PBTI case, hence the conduction and valence band edges are bent towards higher energies. The corresponding band diagram for the NBTI case is displayed on the left side of Figure 8.26. The AERs for hole trapping are

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indicated in red, while those for electron trapping are shown in blue. During NBTI stress, hole traps below the Fermi level can capture charges from the channel, while carriers from the poly-gate can charge the electron traps. Consequently, a more significant number of hole traps and fewer electron traps are anticipated to contribute to the threshold voltage shift compared to the PBTI case.

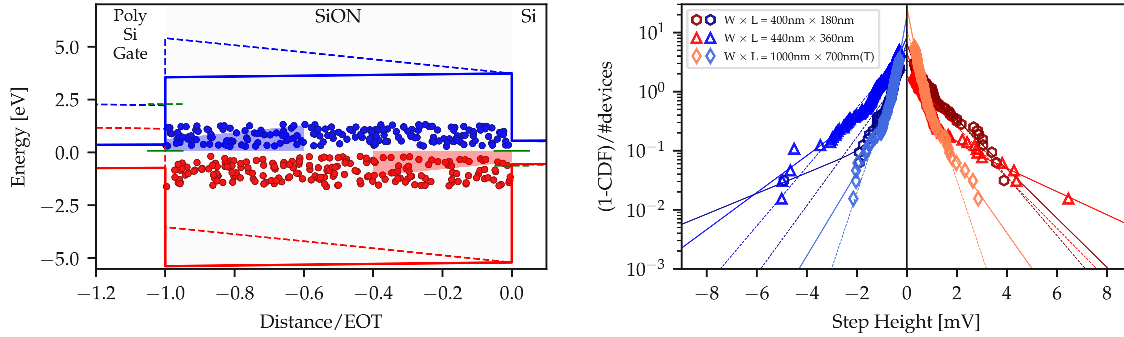

Figure 8.26. (Left) The band diagram of nMOS devices for the NBTI conditions. In contrast to the PBTI case, more hole traps can contribute to total ΔV_{th} now as the channel's AER covers the band-gap's lower half. The AERs for charge transitions between the defects and the channel and for charge transitions between the defects and the gate are marked in blue and red color, respectively. (Right) Distribution of step heights of defects extracted after NBTI stress. Bimodal exponential behavior can be observed for both types of traps. Originally published in [KTC2].

The increased prevalence of hole trapping is clearly evident in the extracted CCDFs for both electron and hole traps, presented on the right side of Figure 8.26. Each type of trap exhibits a two-branch distribution, and considering an unimodal model would underestimate the tail of these distributions. A notable distinction from the PBTI case is the presence of bimodal exponential distributions for both types of traps in this scenario. The parameters obtained from the bimodal fitting are compiled in Table 8.2. Unlike studies utilizing unimodal models, the extracted parameters from the bimodal model do not appear to be associated with the device area, as observed in previous works [24].

8.2.4 Negative BTI of pMOS Transistors

The previous section demonstrated that both electron and hole traps contribute to the ΔV_{th} shift, and that the step height distribution requires a bimodal description. To complement these results, pMOS devices under NBTI conditions are analyzed using the same device geometries as in the nMOS case. Similar to the nMOS device, the largest devices have a thicker oxide compared to the other geometries, necessitating a higher stress gate bias to maintain an equivalent oxide field.

The CCDFs of the pMOS device are presented in Figure 8.27. In contrast to the nMOS device, only hole traps are observed in the pMOS device, with electron traps having no contribution to the threshold voltage shift. This observation can be attributed to the higher effective number of defects typically found in pMOS devices, as previously

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Table 8.3. Extracted parameters of CCDFs for experimental data of pMOS devices under NBTI stress conditions.

unimodal			
W(nm)	L(nm)	$\eta^{\mathrm{h}}(mV)$	N^{h}
220	180	1.32	54.63
400	180	0.72	56.39
800	180	0.44	120.66
440	360	0.37	121.8
1000	500	0.4	42.77

reported [140]. The step heights exhibit a unimodal distribution across all geometries, and the extracted parameters can be found in Table 8.3.

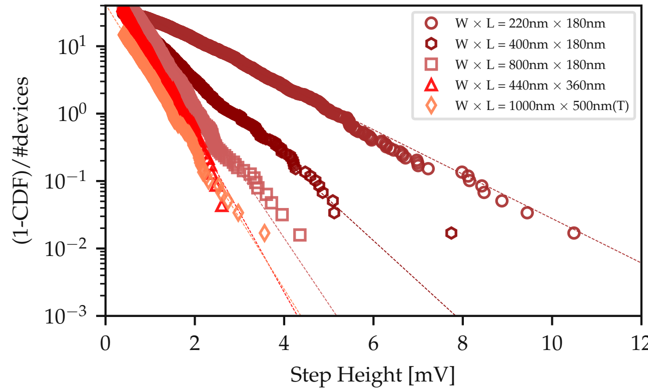

Figure 8.27. Distribution of step heights of hole traps extracted after NBTI stress on pMOS devices. The dashed lines depict the unimodal exponential function used to explain the results. originally published in [KTJ4].

8.2.5 Comparing NBTI and PBTI degradation

The step heights of electron traps extracted from nMOS devices exhibit a bimodal exponential distribution, which is distinct from what has been reported in the literature for SiON technologies, where only unimodal exponential distributions have been observed [140, 45]. bimodal distributions of single defects have been observed in technologies utilizing high-κ gate stacks [45]. In high-κ devices, each branch of the distribution is associated with charge-transfer interactions between defects residing in one of the insulating layers and the channel.

Regarding PBTI, the behavior of nMOS devices is predominantly influenced by electron traps (approximately 92 % of all traps are electron traps), while for NBTI, hole trapping becomes significantly more important. The ratio between electron and hole traps is approximately 52 % to 48 %. Therefore, it is necessary to consider both electron and hole traps in the analysis. On pMOS devices, the ΔV_{th} originates solely from hole traps. It is worth noting that a large number of traps with small average step height are more likely to be located farther from the channel [46], and thus their measurement

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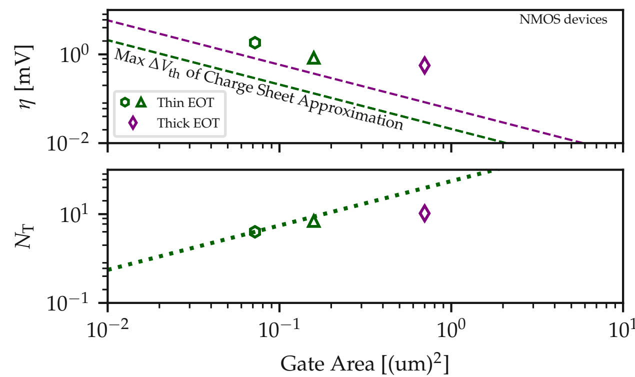

Figure 8.28. Extracted impact of a single defect on the ΔV_{th} (η) and the number of traps per device (N_T) considering unimodal exponential distribution. Clearly visible is the underestimation of the CSA of the impact of the defects, on the device behavior. The maximum impact of CSA is considered by considering the traps directly at the interface. Originally published in [KTC2].

requires optimized low-noise tools [43]. Otherwise, charge trapping might be entirely masked by the measurement noise.

Comparison to CSA

The extracted parameters for PBTI in nMOS devices, including the average step height and the number of traps per device, considering both unimodal and bimodal CCDFs, are presented in Figure 8.28 and Figure 8.29, respectively, along with the maximum limit of the CSA. The extracted parameters from measurements performed on pMOS devices are displayed in Figure 8.30. It appears that the η values are proportional to the gate area under the assumption of a unimodal distribution of step heights.

To estimate the impact of a single defect on ΔV_{th}, the CSA (4.26), is often employed in device simulators. In this work,the extracted values of the threshold voltage shift obtained from CCDFs are compared with the maximum impact predicted by the CSA, which occurs when $x_T = 0$, i.e., directly at the interface. It is evident from the dashed lines in Figure 8.28 and Figure 8.29 that, for both distributions, the CSA significantly underestimates the extracted average impact of the defects, η. As a result, defect densities derived from ΔV_{th} will yield overly pessimistic results. The findings presented here are of particular importance for improving charge-trapping models and enhancing the accuracy of simulations.

8.2.6 Simulation Results

The BTI simulator Comphy [97] is used for verification of the distributions, which were extracted in the previous sections. Comphy uses an one-dimensional gate-stack for which the surface potential is computed at a given gate voltage using several input quantities such as doping concentrations or the work-function difference for the ideal device. During the execution of a BTI simulation, defects are sampled in the oxide.

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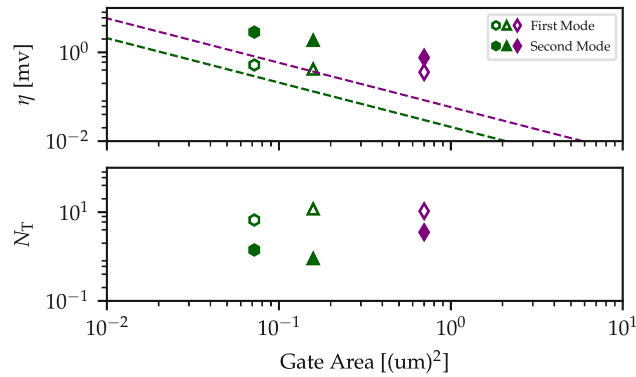

Figure 8.29. The extracted values for the two modes of the bimodal exponential distribution are shown. As can be seen from Figure 8.25, the distribution follows more a bimodal exponential behavior than a unimodal one. Again, the CSA significantly underestimates the impact of the defects, which leads to a too pessimistic estimation for defect density from ΔV_{th}. Originally published in [KTC2].

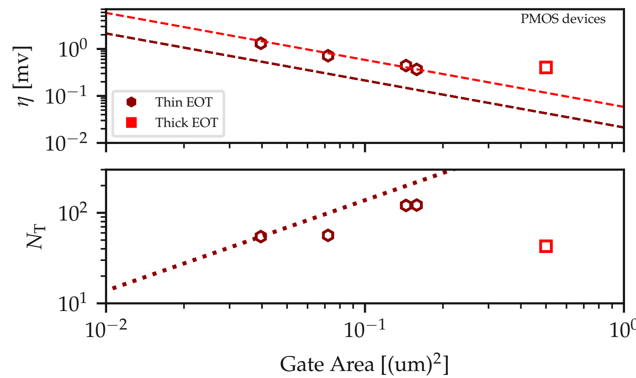

Figure 8.30. The extracted values for the unimodal exponential distribution of the hole traps of pMOS devices. The η values seem to be proportional to the gate area. The max limit of CSA approximation is around three times smaller than values extracted from the CCDFs. Originally published in [KTC2].

Capture and emission rates of these pre-existing defects can be computed using a two-state nonradiative-multiphonon model [76]. For the computation of the rates, the barrier heights ϵ_{ij} between the defect and the band edges needs to be computed.

For this, the trap level E_{T}, the relaxation energy E_{R} and the ratio of the curvatures of the potential energy surfaces R is needed. Additionally, it is necessary to know the spatial position x_{T} of the defect for computing the Wentzel-Kramers-Brillouin (WKB) factor. By sampling E_{T}, E_{R}, x_{T} for a fixed R-value, it is possible to compute the transition rates:

$$k_{ij} = n v_{\mathrm{th}} \vartheta_{\mathrm{WKB}} \sigma \exp\left(-\frac{\epsilon_{ij}}{k_{\mathrm{B}} T}\right) \tag{8.2}$$

with n being the carrier concentration, the thermal velocity v_{th}, the WKB factor ϑ_{WKB} and the capture cross-section σ [76]. The defect bands extracted in [KTJ3] are used for

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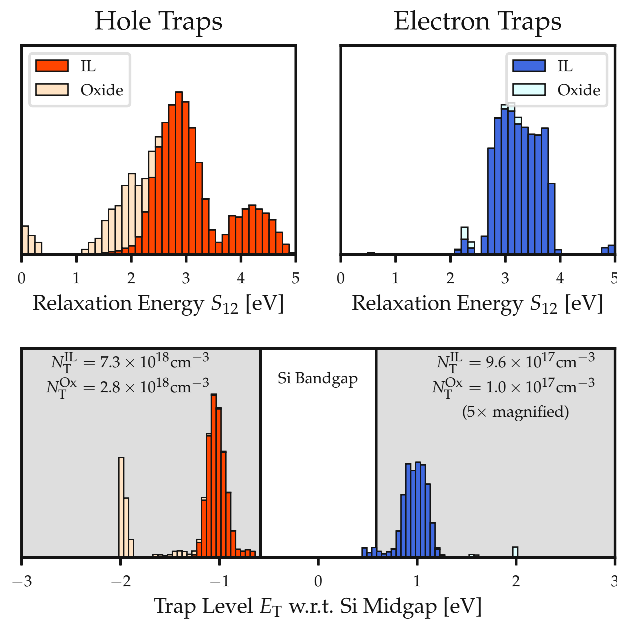

Figure 8.31. Extracted defect bands from eMSM measurements on the SiON devices. nMOS bands are magnified to be accurately visible in the figure. Recreated from [KTJ3].

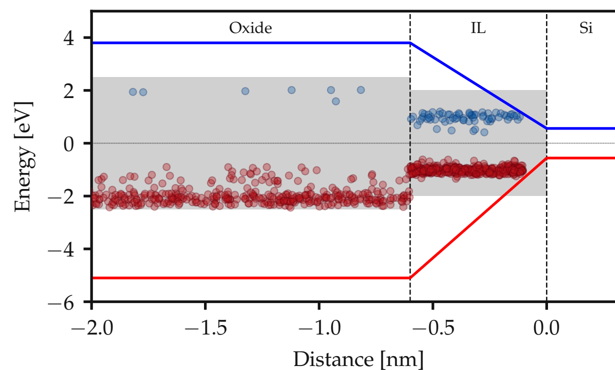

Figure 8.32. Samples are obtained from the extracted defect distributions within the band diagram. The search regions used in the ESiD algorithm are represented by shaded areas. The highest concentration of both electron (blue) and hole (red) traps is found within the IL. Originally published [KTJ3].

the simulations, which have been extracted for large-area devices using a non-negative least square approach for finding optimal defect distributions semi-automatically. The extracted defect band can be seen in Figure 8.31 and the positions of the defects in the device in Figure 8.32. Defects are randomly drawn and an η-value for every contributing defect is sampled from these defect bands using the CCDFs extracted in sections 8.2.2 and 8.2.4. Using this setup, it is possible to simulate the measured MSM-traces from large area devices presented in [KTJ3], as shown in the top part of Figure 8.33 for nMOS devices and Figure 8.34 for the pMOS ones. As can be seen, the step heights extracted from the CCDFs allow a precise simulation of the measurement data. The lower figures show recovery traces for the measurement with the highest oxide field for two selected regions (marked grey) with more detail. The solid lines show the average of all recovery

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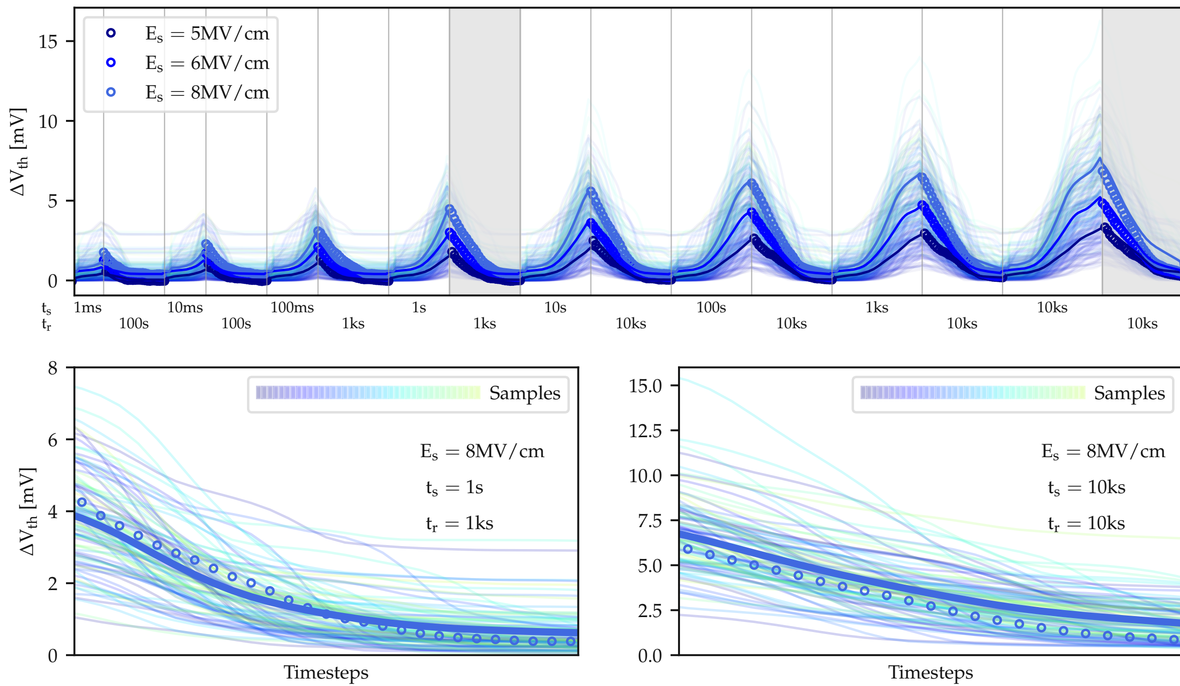

Figure 8.33. In the top figure MSM measurements (dots) on large-area nMOS devices are shown, as presented in [KTJ3], at $T = 100\,°C$ under three different stress conditions. The lines are simulated with the BTI simulator Comphy averaged for 100 sets of sampled step heights using the CCDFs extracted in section 8.2.2. The regions marked in grey are shown in more detail in the two bottom figures. Every light line presents a BTI simulation with a sampled set of step heights, the solid line is the average of all performed simulations. Originally published in [KTJ4].

traces with different sampled step heights.

8.2.7 Conclusions

The distribution of step heights is crucial in characterizing the impact of single defects in nanoscale devices. In this study, MSM measurements were conducted for both NBTI and PBTI stress conditions. Specifically, the utilized devices were of dimensions small enough to enable the detection of individual steps during charge transitions. By analyzing these detected steps, the distributions of step heights are created and demonstrated that bimodal distributions are necessary for an accurate description, particularly in the case of PBTI/nMOS. Notably, the extracted distributions yielded higher average step heights compared to the commonly used CSA employed in simulations. This discrepancy indicates that the contribution of single defects is underestimated when relying solely on the CSA.

Subsequently, CCDFs were incorporated into Comphy and successfully accounted for the measurements obtained from large-area devices. This approach highlights the significance of considering realistic step height distributions in device simulations to better capture the influence of single defects on device performance.

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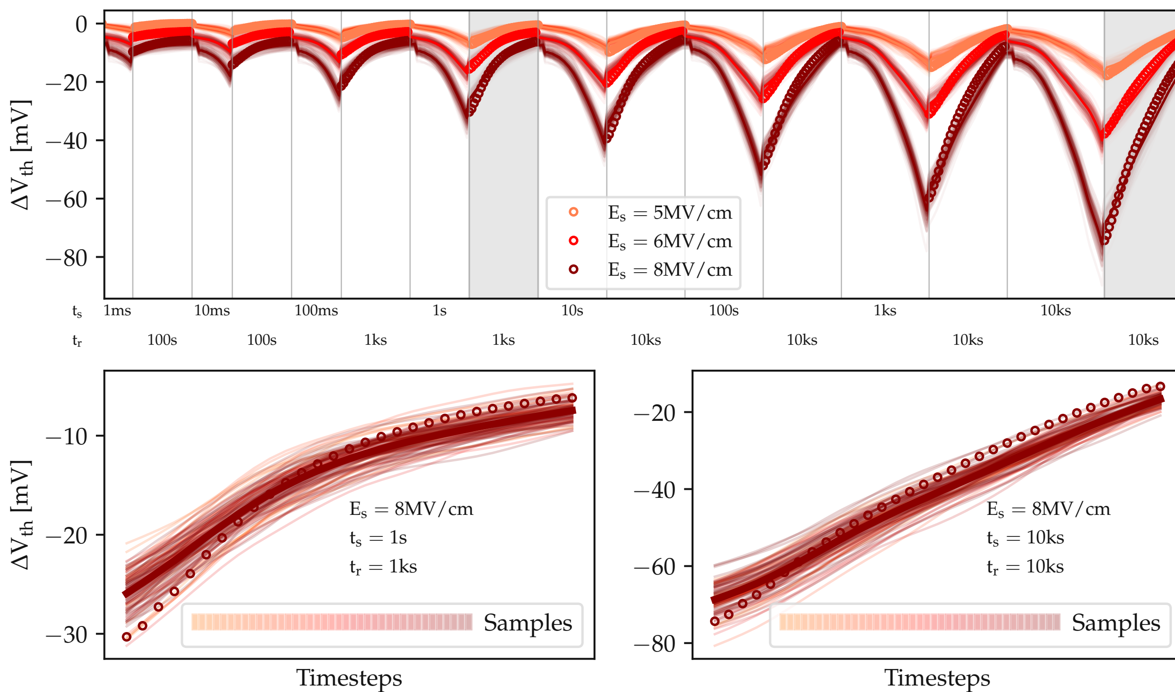

Figure 8.34. In the top figure MSM measurements (dots) on large-area pMOS devices are shown, as presented in [KTJ3], at $T = 100\,°\mathrm{C}$ under three different stress conditions. The lines are simulated with the BTI simulator Comphy averaged for 100 sets of sampled step heights using the CCDFs extracted in Section 8.2.4. The regions marked in grey are shown in more detail in the two bottom figures. Every light line presents a BTI simulation with a sampled set of step heights, the solid line is the average of all performed simulations.

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8.3 Statistical Characterization of RTN in high-κ devices using Smart Arrays

In addition to the previously discussed BTI measurements, RTN measurements provide valuable insights into the trapping kinetics of individual defects. For pMOS devices unlike BTI, which freezes out at cryogenic temperatures, RTN continues to be a persistent reliability concern even at these low temperatures, regardless of the channel materials and device geometries employed [126]. In the upcoming section, RTN measurements conducted on smart arrays [141, 142] comprising high-k devices will be explored.

8.3.1 Devices and Measurements

In this section, the RTN measurements were conducted using a commercially available bulk CMOS technology with a metal gate contact and a high-κ layer of HfO_2. The technology utilizes a thin interface layer created through rapid thermal oxidation on the substrate. The high-κ layer has an EOT of 1.41 nm. The measurements involved devices with a width of 100 nm and different lengths of 70 nm, 100 nm, 135 nm, 170 nm, and 200 nm. The measurement array consisted of 2500 transistors, including both nMOS and pMOS devices. The first 50 gate lines allowed the selection of 500 devices with the smallest geometry using ten drain lines. The subsequent drain lines corresponded to devices with progressively larger geometries.

To collect statistical data on the distribution of step heights, a standardized characterization sequence was followed for each tested device. The sequence began with an initial $I_D(V_G)$ characterization, which ensured proper device operation, determined the gate voltages for RTN measurements, and established a correlation between recorded drain-source currents and equivalent threshold voltage shifts. Figure 6.2 illustrates the initial $I_D(V_G)$ measurements of the biggest geometry and the bias range used to capture the RTN signals .

After the initial $I_D(V_G)$ curve, the sequence continued with RTN traces taken at five different constant biases near V_{th}, where the RTN measurement window is available [50]. At each gate voltage, RTN traces were recorded with a sampling time T_s of 100 µs and a duration t_r of 1 s. Each device was measured for these RTN traces. The measurements were conducted at four different temperatures: 4 K, 77 K, 225 K, and 300 K.

8.4 Extraction of Step Heights

For each recorded trace, the steps were identified using Otsu's method (see Section 7.2), allowing the extraction of distributions for τ_c, τ_e, and η. Examples of these distributions can be observed in Figures 8.36 and 8.37. By utilizing these extracted distributions, the mean values of τ_c, τ_e, and η were calculated for each V_G within the measured range.

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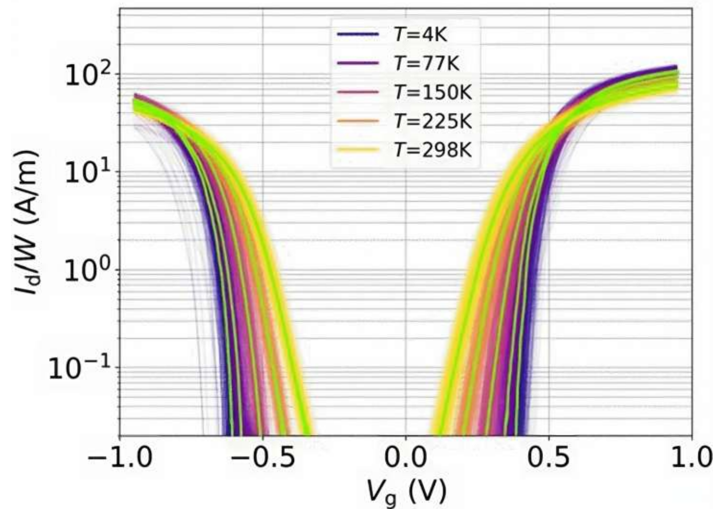

Figure 8.35. Initial $I_D(V_G)$ measurements of the biggest geometry in the bias range to capture the RTN signals. Originally published in [51, 143].

Compared to the Canny edge detector, Otsu's method offers the advantage of fully automated thresholding. It is often advantageous to apply a filter before automated thresholding to suppress measurement noise, although this may result in the loss of very fast charge transition events. However, it significantly enhances the robustness of thresholding and enables the detection of small step heights. In this study, the denoising algorithm proposed by Chambolle was employed for this purpose [128].

It is important to note that Otsu's method can only be applied to measurement data containing a single active defect. In cases where multiple active defects are detected, typically only the most prominent defect signal is extracted (referred to as multi-level RTN). To prevent incorrect detection, additional sanity checks, such as the χ^2 test and Kolmogorov-Smirnov test, are implemented to assess whether the capture and emission times follow an exponential distribution. For a comprehensive analysis of multi-level RTN, advanced techniques like factorial hidden Markov model analysis are required [129].

Figure 8.36 presents a non ideal measurement scenario for an pMOS device where even though it seems to have an appropriate RTN behavior, the two used tests lead us to reject the trace for conducting statistics. The ideal scenario of a used trace can be seen in Figure 8.37.

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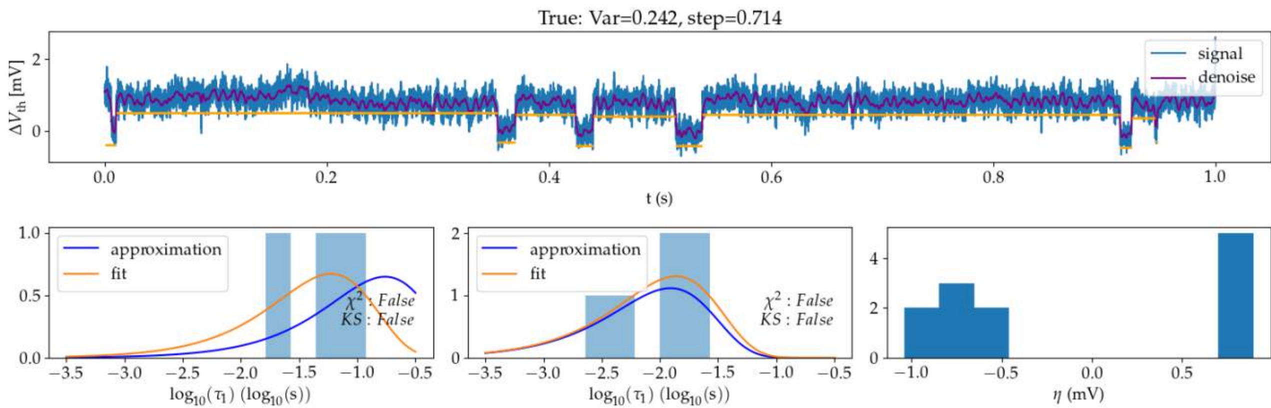

Figure 8.36. After identifying the distinctive levels of an arbitrary RTN signal (shown at the top), various parameters can be derived, such as step magnitudes (shown at bottom left) and the times for charge capture and emission (shown at bottom right and middle). However, in this particular signal, the distributions of t_e and t_c fail to meet the criteria set by the χ^2 and Kolmogorov-Smirnov tests. This exclusion ensures the avoidance of erroneous detections, thus making this particular trace unsuitable for statistical analysis.

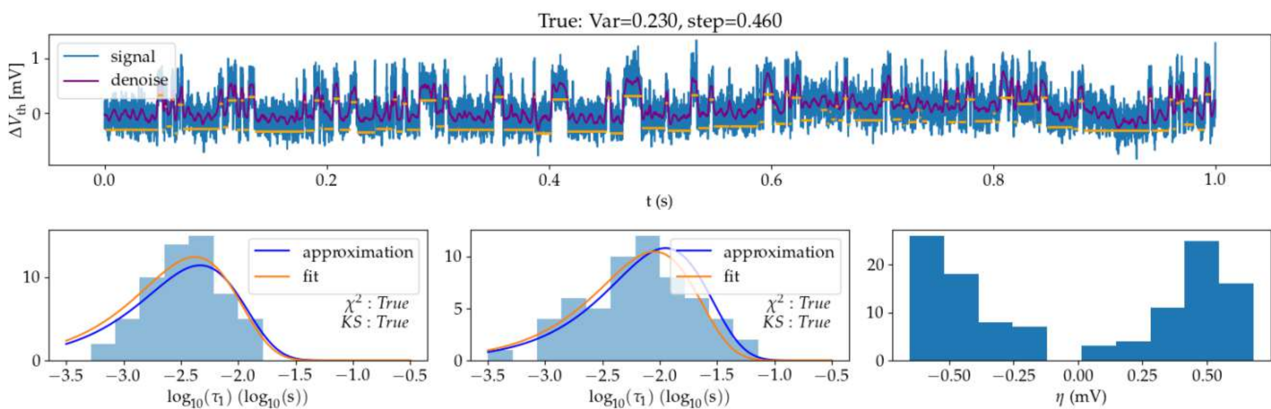

Figure 8.37. After identifying the distinct steps present in an arbitrary RTN signal (depicted at the top), numerous parameters can be derived, such as step magnitudes (shown at bottom left) and the times for charge capture and emission (shown at bottom right and middle). In this particular trace, the distributions of t_e and t_c successfully pass both the χ^2 and Kolmogorov-Smirnov tests, ensuring accurate detection. As a result, this trace is suitable for utilization in the statistical analysis.

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8.5 Distributions of Step Heights

The CCDFs of the steps extracted for the RTN traces of pMOS devices can be seen in the following Figures for each different temperature condition. In Figures 8.38 and 8.39 the CCDFs of T=4 K and T=77 K are shown. At these temperatures, the results cannot be described correctly by the commonly used exponential or lognormal distributions [144]. The step heights seem to distribute randomly, and from the lack of clear slopes, an area scaling is not possible to observe.

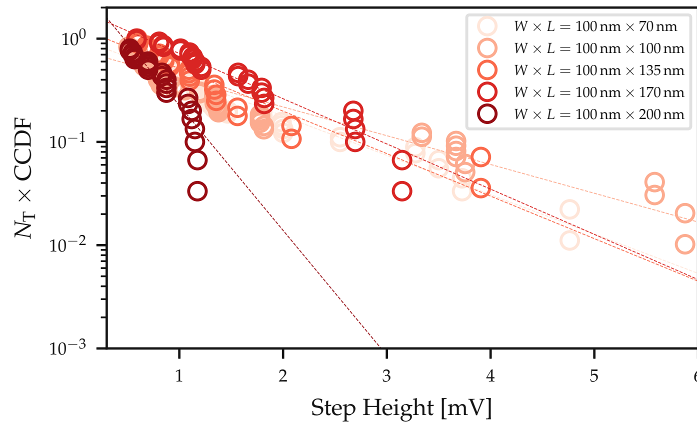

Figure 8.38. The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 4 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature, the exponential distribution seems unable to describe the results, also the mean values do not scale with the area but present a random behavior.

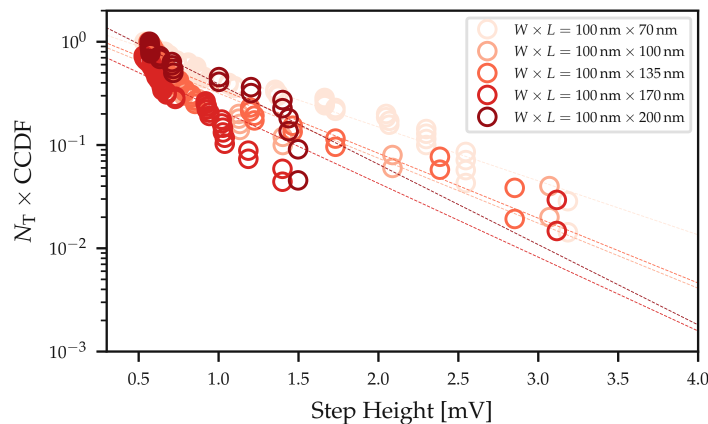

Figure 8.39. The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 7 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. Similar to the T= 7 K case, the exponential distribution seems unable to describe the results and also the mean values seem to not scale with the area but present a random behavior, too.

Contrary to that, in Figures 8.40 and 8.41 where CCDFs of T=225K and T=300K are shown, exponential distributions seem to capture the results nicely. One possible

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explanation is that the number of defects for the larger geometries is smaller in lower temperatures, see Figure 8.42 and thus accurate distributions cannot be observed.

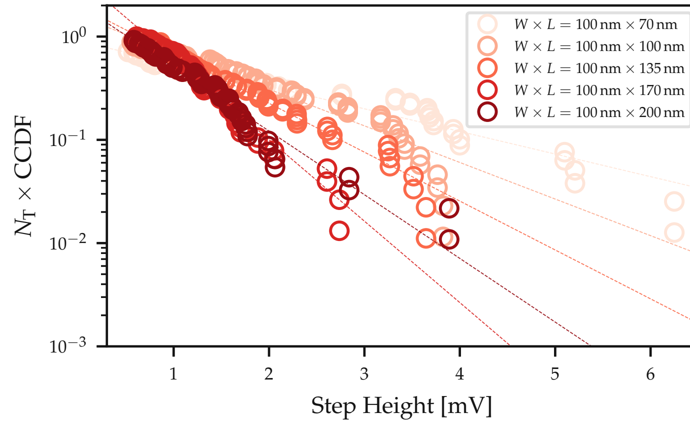

Figure 8.40. The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 225 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature, the exponential distribution captures nicely the results. Also, a scaling with the area starts to exist.

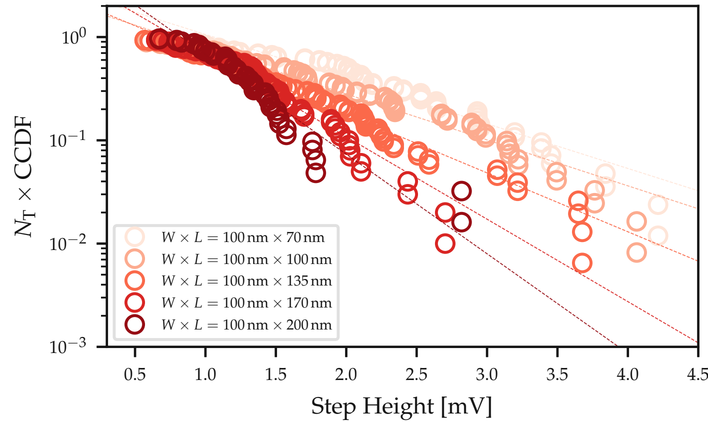

Figure 8.41. The CCDFs of step heights of hole traps extracted after RTN measurements on pMOS devices at T= 300 K. The dashed lines depict the unimodal exponential distribution that has been used to describe the results. At this temperature similar to the T= 225 K case, the exponential distribution captures nicely, and the area scaling is clear.

8.6 Parameter Extraction

Extracted η values of the CCDFs of the previous section can be seen in Figures 8.43 and 8.44 plotted against the area. The markers of red shade represent the experimental η values for each geometry. The red line is the extrapolated area trend, and the grey dashed line represents the maximum value expected from CSA for a single defect. The results seem to follow area scaling in a consistent way with RMSE $= 0.11$ and RMSE $= 0.9$ for

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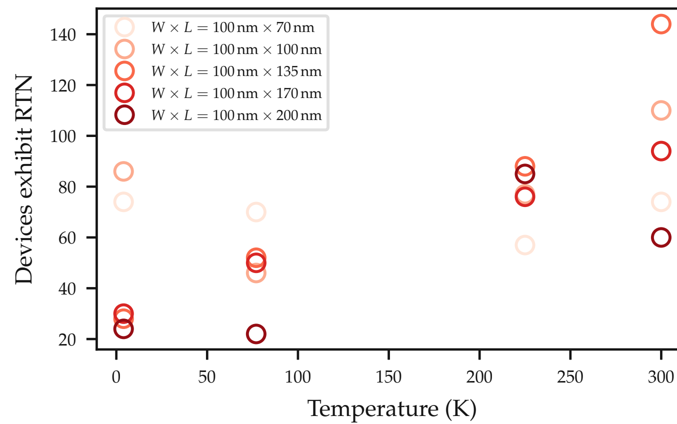

Figure 8.42. The number of devices exhibiting RTN versus temperature for all the different areas. Even though the results are mixed, more devices exhibiting RTN can be seen in higher temperatures.

temperatures T= 225 K and T= 300 K accordingly. The experimental values are higher than the maximum limit of CSA, consistent with what has been observed in the other studied geometries.

The η values are also plotted against the $W \times \sqrt{L}$ trend, which described the results of the first studied technology better than the area trend, in Figures 8.43 and 8.44 accordingly. Interestingly, the results follow the $W \times \sqrt{L}$ trend with the same RMSE values as in the area case. This observation can attributed to the small range of L in the studied geometries. To better analyze the two trends, a broader set of geometries is needed, and ideally, devices with the same area and different W/L ratios as in the SiO_2 case of the previous section.

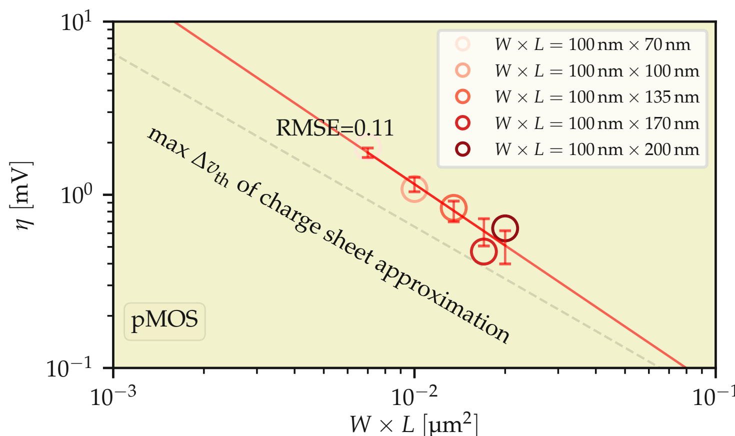

Figure 8.43. The extracted η values for the T= 225 K case presented in Figure 8.40 are plotted against the area. The results follow the area trend except for a small outlier at L=170 nm. The experimental values are higher than the maximum limit of CSA, similar to the other studies presented in the thesis.

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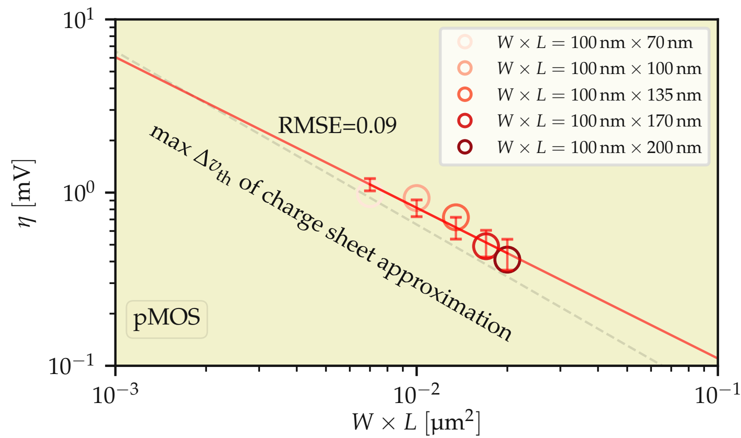

Figure 8.44. The extracted η values for the T= 225 K case presented in Figure 8.41 are plotted against the area. The results follow the area trend with a smaller RMSE than in the T= 225 K case. The experimental values are higher than the maximum limit of CSA, although their deviation is smaller than the T= 225 K case.

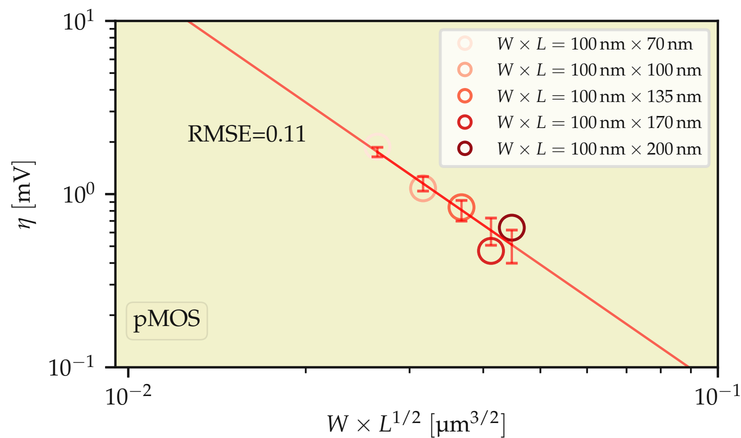

Figure 8.45. The extracted η values for the T= 225 K case presented in Figure 8.40 are plotted against the $W \times \sqrt{L}$ trend. The results follow the trend with the same RMSE as observed in the area trend.

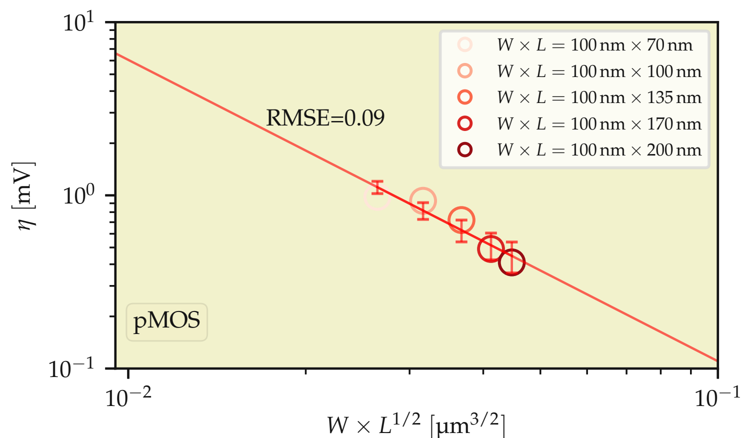

Figure 8.46. The extracted η values for the T= 300 K case presented in Figure 8.41 are plotted against the $W \times \sqrt{L}$ trend. The results follow the trend with the same RMSE as observed in the area trend.

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Chapter 9

Summary and Outlook

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9.1 Summary

The MOSFET has been critical in many technological advancements over the past decades. Ensuring their reliable function under diverse operating conditions, such as various biases and temperatures, is crucial for the consistent performance of the circuits they comprise. In this thesis, reliability issues in MOSFET devices are explored, focusing specifically on bias temperature instability (BTI) and random telegraph noise (RTN), effects arising from individual defects. These defects originate from the intrinsic device structure, from manufacturing procedures, or develop during device usage and create localized electric field fluctuations, capture charges, and form interface states, negatively impacting the device's performance.

In the studies included in this thesis, the impact of single defects on the device performance is studied by leveraging MSM measurements focusing on threshold voltage shift ΔV_{th}, one of the most critical parameters for the device reliability. The main focus is the statistical analysis of the discrete amplitudes of single defects, which can be extracted from ΔV_{th} when nanoscale devices are employed. By creating statistical distributions based on these amplitudes, essential metrics for the impact of defects can be extracted, such as the average number of active defects per device N_{T} and the average threshold shift induced by a single defect η. The investigation of devices of different technologies and geometries under various bias conditions led to insights into how parameters, such as gate width and length, affect the impact of single defects. In addition to the experimental distributions, defect-centric model (DCM) is used to validate these approaches.

More specifically, from the analysis of the SiO_2 technology on pMOS devices, it is observed that for measurements close to threshold voltage V_{th}, the scaling of η is described better by a $W \times \sqrt{L}$ trend rather than the area of the devices $W \times L$, which is typically used in literature. However, if a higher recovery bias is applied η decreases, especially on devices affected more by the percolative conduction, and the $W \times L$ trends capture nicely the values for all the tested geometries. At the same time, more defects contribute to the observed degradation for higher recovery bias conditions.

From the measurements on the same technology with varying body bias, modulations of both time-zero variability and time-dependent variability are found. These observations were explained by the modulation of the number of unscreened dopant atoms within the channel depletion region induced by the body bias. It was shown that using reverse body bias (RBB) can increase both depletion region thickness X_{dep} and $|V_{\mathrm{th}}|$, making it advantageous for applications that require low leakage. On the other hand, forward body bias (FBB) reduces X_{dep} and $|V_{\mathrm{th}}|$, which can be beneficial for high-performance applications, albeit with a trade-off of higher junction leakage.

The statistical distributions obtained for SiON technology revealed that bimodal distributions are necessary for an accurate description of the amplitudes of step heights, particularly in the case of PBTI/nMOS. Nevertheless, the dimensional scaling trends for the step heights for a bimodal distribution for nMOS data still need to be fully resolved and addressed in future studies. Subsequently, the observed distributions were incorporated into reliability simulator Comphy and successfully accounted for the measurements obtained from large-area devices. This approach highlights the importance of considering realistic step height distributions in device simulations to better capture the influence of single defects on device performance.

The knowledge gained from the studies presented in this thesis can further be applied to different technologies and device structures to determine the impact of single defects on their performance. The integration of experimental measurements, statistical modeling, and compact physics simulations lead to a comprehensive understanding of the defect nature in MOSFETs and pave the way for improved device performance and reliability.

9.2 Outlook

The findings presented in this thesis contribute to the understanding of the link between device geometry and charge trapping effects, which is essential for making circuits resilient against charge trapping. Building upon the insights gained from the current study, several key areas warrant further exploration.

Future research can involve incorporating gate current measurements in addition to the measurements presented in this thesis. The study of defect charge trapping behavior in this thesis primarily focuses on its impact on the drain-source current. However, these defects also affect the gate current, either through direct charge exchange with the gate or by affecting tunneling currents [145, 146]. Additionally, the new trap-assisted tunneling (TAT) model implemented into Comphy [KTJ6, 147] can be used to simultaneously study BTI and TAT within a single technology. To do this effectively, it is necessary to design test structures with sufficiently large gate areas to detect small leakage currents and smaller structures for detailed BTI analysis.

Furthermore, investigating the impact of the device geometry on η for different technologies and novel device structures can shed more light on the physical mechanisms of single defects. Experimental test structures with strategically placed defects

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can be used to connect the results obtained from the methods used in this thesis with the predetermined characteristics of the injected defects. Such an analysis can shed light on the relationship between device geometry and the severity of reliability issues, enabling the development of design guidelines to optimize MOSFET reliability in various configurations.

In addition to the impact of gate geometry and body bias on the impact of single defects, future research can also explore the influence of other device parameters, such as dopant concentration. Identifying how devices with different dopant concentrations can interact under different body bias conditions can give a more precise understanding of how substrate dopants affect the device performance [139].

By systematically varying these parameters, researchers can comprehensively understand their effects on the occurrence and severity of reliability issues. This knowledge can guide device manufacturers to make informed decisions during the fabrication process to enhance the reliability of MOSFETs. Finally, these ideas for future research can lead to a complete statistical model for η where various device parameters and operating conditions that affect device reliability can be included.

Finally, additional studies to address strategies to mitigate the impact of defects would naturally be a next step based on the work of this thesis. Having characterized the impact of defects, which allows the proper incorporation into a statistical modeling and simulation environment, controlling or suppressing their impact based on the affecting parameters is promising for future research.

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List of Publications

Scientific Journals

[KTJ1] M. Waltl, T. Knobloch, **K. Tselios**, L. Filipovic, B. Stampfer, Y. Hernandez, D. Waldhör, Y. Illarionov, B. Kaczer, and T. Grasser. "Perspective of 2D integrated electronic circuits: Scientific pipe dream or disruptive technology?" In: *Advanced Materials* (2022), p. 2201082. DOI: 10.1109/TED.2022.3185965.

[KTJ2] M. Waltl, D. Waldhoer, **K. Tselios**, B. Stampfer, C. Schleich, G. Rzepa, H. Enichlmair, E. G. Ioannidis, R. Minixhofer, and T. Grasser. "Impact of single-defects on the variability of CMOS inverter circuits". In: *Microelectronics Reliability* 126 (2021). Proceedings of ESREF 2021, 32nd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, p. 114275. DOI: https://doi.org/10.1016/j.microrel.2021.114275.

[KTJ3] D. Waldhoer, C. Schleich, J. Michl, B. Stampfer, **K. Tselios**, E. G. Ioannidis, H. Enichlmair, M. Waltl, and T. Grasser. "Toward Automated Defect Extraction From Bias Temperature Instability Measurements". In: *IEEE Transactions on Electron Devices* 68.8 (2021), pp. 4057–4063. DOI: 10.1109/TED.2021.3091966.

[KTJ4] **K. Tselios**, D. Waldhoer, B. Stampfer, J. Michl, E. G. Ioannidis, H. Enichlmair, T. Grasser, and M. Waltl. "On the Distribution of Single Defect Threshold Voltage Shifts in SiON Transistors". In: *IEEE Transactions on Device and Materials Reliability* 21.2 (2021), pp. 199–206. DOI: 10.1109/TDMR.2021.3080983.

[KTJ5] **K. Tselios**, J. Michl, T. Knobloch, H. Enichlmair, E. G. Ioannidis, R. Minixhofer, T. Grasser, and M. Waltl. "Evaluation of the impact of defects on threshold voltage drift employing SiO2 pMOS transistors". In: *Microelectronics Reliability* 138 (2022). 33rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, p. 114701. DOI: https://doi.org/10.1016/j.microrel.2022.114701.

[KTJ6] C. Schleich, D. Waldhör, A.-M. El-Sayed, **K. Tselios**, B. Kaczer, T. Grasser, and M. Waltl. "Single- Versus Multi-Step Trap Assisted Tunneling Currents—Part II: The Role of Polarons". In: *IEEE Transactions on Electron Devices* 69.8 (2022), pp. 4486–4493. DOI: 10.1109/TED.2022.3185965.

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[KTJ7] **K. Tselios**, T. Knobloch, D. Waldhoer, B. Stampfer, E. Ioannidis, H. Enichlmair, R. Minixhofer, T. Grasser, and M. Waltl. "Revealing the Impact of Gate Area Scaling on Charge Trapping employing SiO2 Transistors". In: *IEEE Transactions on Device and Materials Reliability* (2023), pp. 1–1. DOI: 10.1109/TDMR.2023.3262141.

Conference Proceedings

[KTC1] **K. Tselios**, T. Knobloch, J. Michl, D. Waldhoer, C. Schleich, E. Ioannidis, H. Enichlmair, R. Minixhofer, T. Grasser, and M. Waltl. "Impact of Single Defects on NBTI and PBTI Recovery in SiO2 Transistors". In: *2022 IEEE International Integrated Reliability Workshop (IIRW)*. 2022, pp. 1–5. DOI: 10.1109/IIRW56459.2022.10032748.

[KTC2] **K. Tselios**, B. Stampfer, J. Michl, E. Ioannidis, H. Enichlmair, and M. Waltl. "Distribution of Step Heights of Electron and Hole Traps in SiON nMOS Transistors". In: *2020 IEEE International Integrated Reliability Workshop (IIRW)*. 2020, pp. 1–6. DOI: 10.1109/IIRW49815.2020.9312871.

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