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Compact I-V model for back-gated and double-gated TMD FETs

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ABSTRACT

A physics-based analytical DC compact model for double and single gate TMD FETs is presented. The model is developed by calculating the charge density inside the 2D layer which is expressed in terms of the Lambert W function that recently has become the standard in SPICE simulators. The current is then calculated in terms of the charge densities at the drain and source ends of the channel. We validate our model against measurement data for different device structures. A superlinear current increase above certain gate voltage has been observed in some MoS_2 FET devices, where we present a new mobility model to account for the observed phenomena. Despite the simplicity of the model, it shows very good agreement with the experimental data.

1. Introduction

In an effort to overcome the limitations of silicon-based CMOS devices in delivering the desired performance for Very Large-Scale Integration (VLSI) circuits, there has been increasing interest in using 2D materials as the conducting channel in Field Effect Transistors (FETs) [1]. This area of research is gaining momentum as a potential alternative to traditional silicon-based technologies. The ultra-thin nature of 2D materials is making it possible to achieve the ultimate scalability in FETs, resulting in enhanced gate electrostatic control over the channel and reduced parasitic effects when compared to 3D gate structures. Additionally, 2D materials show potential for use in stacked nanosheet transistor architecture [2]. Initially, research on 2D materials was focused on graphene, which possess exceptional electronic and optical properties [3]. However, due to its lack of a bandgap, its use in electronic circuits, particularly in digital electronics, is limited [4]. As an alternative, the research community began to explore other kinds of 2D materials, specifically Transition Metal Dichalcogenides (TMDs), which can be present in nature as insulators, semiconductors, metals, and even superconductors [5]. Compared to graphene, TMDs have gained more attention due to their relatively large bandgap, making them more suitable to be used in future logic electronics. MoS_2 is the most extensively studied TMD, with high-performance MoS_2 FETs being reported in literature [6–8].

For any new device technology to be used in circuit design and simulation, compact models describing the I-V and C-V characteristics of the device need to be developed and made available to the designers. Those models work as a bridge between foundry and circuit designers. Those models will not only enable the design and simulation of circuits, but also will help interpreting experimental results. Several compact models regarding 2D FETs have been developed [9–14].

The focus of this paper is the development of a DC compact model for double and single back-gated TMD FETs. Our model utilizes a unified charge control model that stems from the formulation presented in [15]. In contrast to [15], we introduce an approximate explicit equation for the channel charge, which is expressed using a Lambert W function that is widely established in circuit simulators. Furthermore, the current is determined based on the charge densities at the source and drain. Our model is presented in the form of explicit closed equations that can be easily integrated into circuit simulators. Our model has been validated against measurement data, and we have observed a good agreement between the two, except for one kind of device technology, where a superlinear current increase was experimentally observed above a certain gate voltage. As a result, we introduced a new mobility model to account for the observed phenomena. This phenomenon might be related to the filling of traps. More details on the latter model can be found in [16]. It is worth noting that larger gate voltage sweeps were applied for this technology that we observe the superlinear current

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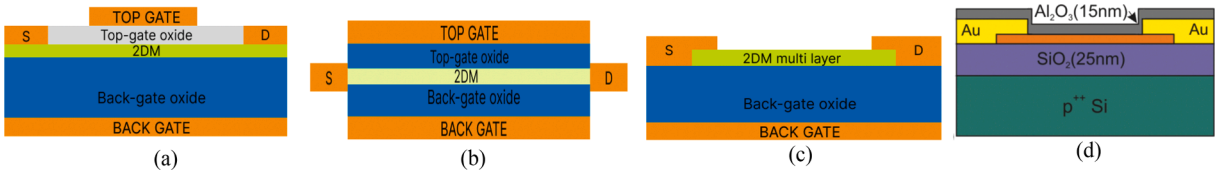

Fig. 1. 2D schematic structure for 2D TMD FETs. (a) Device 1 is a double gated monolayer MoS_2 FET [15]. (b) Device 2 is a double gated monolayer WSe_2 FET [17]. (c) Device 3 is single back-gated multilayer MoS_2 FET [18]. (d) Device 4 is single back-gated monolayer FET [19].

Table 1
Input Parameters for the 2D FET model.

Parameter	Symbol	Device (1)	Device (2)	Device (3)	Device (4)
Channel Material		MoS_2	WSe_2	MoS_2	MoS_2
Length	L	150 nm	9.4 μm	500 nm	4 μm
Width	W	10 μm	10 μm	10 μm	10 μm
Top Oxide Dielectric Permittivity	ϵ_t	9	12.5	–	
Bottom Oxide Dielectric Permittivity	ϵ_b	3.9	3.9	3.9	3.9
Top Oxide thickness	t_t	10 nm	17.5 nm	–	15 nm
Bottom Oxide thickness	t_b	285 nm	270 nm	90 nm	25 nm
Mobility	μ	21.2 cm^2/Vs	235 cm^2/Vs	21.2 cm^2/Vs	19.1 cm^2/Vs
Charge correction parameter	α	2.4 @Vds = 0.1 V 2.8 @Vds = 1 V	1	55	18
Charge correction parameter	β	0.55 @Vds = 0.1 V 0.62 @Vds = 1 V	0.35 @Vds = -0.05 V 0.44 @Vds = -1V	27	9
Mobility enhancement parameter	M	–	–	–	0.8113
Mobility enhancement parameter	V_A	–	–	–	7.48
Mobility enhancement parameter	γ	–	–	–	0.5

increase. On the other hand, the other technologies were measured over a smaller gate voltage range and that could be the reason why this phenomenon was not observed.

2. Model development

We begin the development of our physics-based compact model by modeling the device electrostatics. Our approach draws heavily on the findings of [15], which describes the electrostatics using the following equation.

$$Q_{net} + Q_{it} = -C_t\left(V_g - V_{g0} - V(x) + V_c(x)\right) - C_b\left(V_b - V_{b0} - V(x) + V_c(x)\right) \tag{1}$$

here Q_{net} is the total mobile charge density, Q_{it} is the interface trap charge density, C_t (C_b) are the top (bottom) oxide capacitances per unit area $C_t = \frac{\epsilon_0\epsilon_t}{t_t}$ ($C_b = \frac{\epsilon_0\epsilon_b}{t_b}$) and $V_g - V_{g0}$ ($V_b - V_{b0}$) are the top (bottom) overdrive voltages, where V_{g0} (V_{b0}) takes into consideration the work function difference and any possible additional charges resulting from impurities or doping. In MoS_2 FET devices, the interface trap charge density Q_{it} has a significant role in the transistor behavior. However, as an initial approximation in developing our compact model, we disregard the dependence of Q_{it} on the gate voltage. Instead, we treat Q_{it} as a constant value that impacts both the threshold voltage V_{TH} and the subthreshold slope SS. $V(x)$ is the quasi-Fermi level along the channel, where $V(x=0) = V_s$ (source voltage) and $V(x=L) = V_D$ (drain voltage). $V_c(x)$ is the shift of the quasi-Fermi level with respect to the conduction band. The overall charge density can be also expressed as follows,

$$Q_{net} = -qn(x) = -C_{dq}V_{th}\ln\left(1 + e^{\frac{-V_c(x)}{V_{th}}}\right) \tag{2}$$

where $C_{dq} = q^2D_0$ is defined as the degenerated-quantum capacitance and D_0 is the density of states and defined as follows,

$$D_0 = g_K\left(\frac{m^K}{2\pi\hbar^2}\right) + g_Q\left(\frac{m^Q}{2\pi\hbar^2}\right)\exp\left(-\frac{\Delta E_2}{K_B T}\right) \tag{3}$$

here g_K, g_Q are the degeneracy factors, m^K, m^Q are the conduction band effective masses for the K and Q band valley and ΔE_2 is the energy separation between K and Q valleys. By rearranging (2), we get,

$$V_c(x) = -V_{th}\ln\left(exp\left(-\frac{Q_{net}}{C_{dq}V_{th}}\right) - 1\right) \tag{4}$$

Combining (4) and (1), we obtain the uniform charge control model (UCCM) that is expressed as follows,

$$Q_{net} - C_{tb}V_{th}\ln\left(exp\left(-\frac{Q_{net}}{C_{dq}V_{th}}\right) - 1\right) = -C_t\left(V_g - V_{g0} - V(x)\right) - C_b\left(V_b - V_{b0} - V(x)\right) \tag{5}$$

with $C_{tb} = C_t + C_b$.

Although Equation (5) can be used to obtain the overall mobile charge density through numerical methods, such solutions may not be practical in compact modeling, given their high computational cost and unsuitability for efficient circuit simulations. As a result, we approximate the poly-logarithmic term $\ln\left(exp\left(-\frac{Q_{net}}{C_{dq}V_{th}}\right) - 1\right)$ to formulate our core model.

Using a two terms Taylor's expansion, we can rewrite the UCCM as follows,

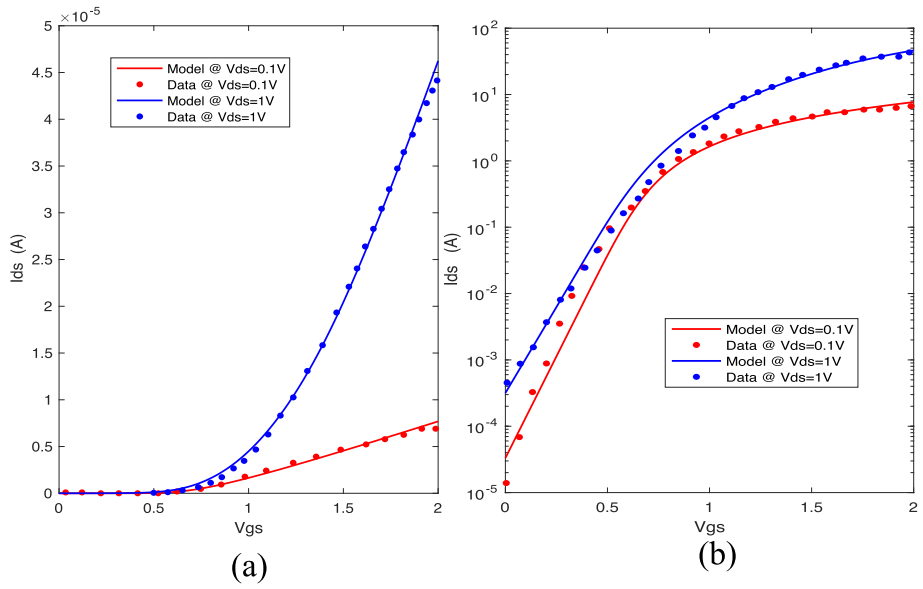

Fig. 2. Validation of the 2D FET model against experimental data for Device 1. (a) Linear transfer characteristics ($I_D - V_{gs}$) at $V_{ds} = 0.1$, 1 V. (b) Transfer characteristics on the logarithmic scale.

$$Q_{net}(x) - C_{tb}V_{th}\ln\left(-\frac{Q_{net}(x)}{C_{dq}V_{th}}\right) = -C_t\left(V_g - V_{g0} - V(x)\right) - C_b(V_b - V_{b0} - V(x)) \tag{6}$$

The mobile charge density throughout the semiconductor can be obtained by solving (6) analytically. To achieve that, we reformulate (6) in the form where the Lambert W function ($\omega\exp(\omega) = z$) can be applied. We do so by dividing both sides by $C_{tb}V_{th}$ then exponentiate both sides. This allows us to rewrite (6) as follows,

$$\left(-\frac{Q_{net}(x)}{C_{tb}V_{th}}\right) \times \exp\left(-\frac{Q_{net}(x)}{C_{tb}V_{th}}\right) = \frac{C_{dq}}{C_{tb}}\exp\left(\frac{C_t\left(V_g - V_{g0} - V(x)\right) + C_b(V_b - V_{b0} - V(x))}{C_{tb}V_{th}}\right) \tag{7}$$

Consequently, we can represent the total mobile charge density inside the semiconductor in terms of Lambert W function after introducing two fitting parameters α and β as,

$$Q_{net}(x) = -\beta C_{tb}V_{th}\mathrm{W}\left[\frac{C_{dq}}{C_{tb}}\exp\left(\frac{C_t\left(V_g - V_{g0} - V(x)\right) + C_b(V_b - V_{b0} - V(x))}{\alpha C_{tb}V_{th}}\right)\right] \tag{8}$$

To calculate the current, we need to calculate the charge densities at the source and drain ends. The current equation can be expressed as,

$$I_{DS} = \frac{W\mu}{L}\int_0^{V_{DS}} Q(V).\mathrm{d}V \tag{9}$$

Using equation (6), we can rewrite $\mathrm{d}V$ in terms of $\mathrm{d}Q$ as follows,

$$\frac{Q_{net}(x)}{C_{tb}V_{th}} - \ln\left(-\frac{Q_{net}(x)}{C_{dq}V_{th}}\right) = \frac{-C_t\left(V_g - V_{g0} - V(x)\right) - C_b(V_b - V_{b0} - V(x))}{C_{tb}V_{th}} \tag{10}$$

$$\frac{\mathrm{d}Q}{C_{tb}V_{th}} - \frac{\mathrm{d}Q}{Q} = \frac{C_t\mathrm{d}V + C_b\mathrm{d}V}{C_{tb}V_{th}} \tag{11}$$

$$\frac{\mathrm{d}Q}{C_{tb}V_{th}} - \frac{\mathrm{d}Q}{Q} = \frac{C_{tb}\mathrm{d}V}{C_{tb}V_{th}} \tag{12}$$

$$\mathrm{d}V = \frac{\mathrm{d}Q}{C_{tb}} - V_{th}\frac{\mathrm{d}Q}{Q} \tag{13}$$

Therefore, (9) can be written as follows,

$$I_{DS} = \frac{W\mu}{L}\int_{Q_S}^{Q_D} Q(V)\left[\frac{\mathrm{d}Q}{C_{tb}} - V_{th}\frac{\mathrm{d}Q}{Q}\right] \tag{14}$$

Integrating (14) results in,

$$I_{DS} = \frac{W\mu}{L}\left[\frac{{Q_D}^2 - {Q_S}^2}{2C_{tb}} - V_{th}(Q_D - Q_S)\right] \tag{15}$$

where Q_D and Q_S can be found by substituting $V_D = V_{DS}$ and $V_S = 0$, respectively, in the charge equation, Equation (8). For the device technology with the super linear current increased observed, we have taken a three terms Taylor's expansion for the exponential term in (5), which is then used to develop the current equation, as derived in [16] after adjusting the model to a single back-gated structure. Hence, in this case the expression for the current is,

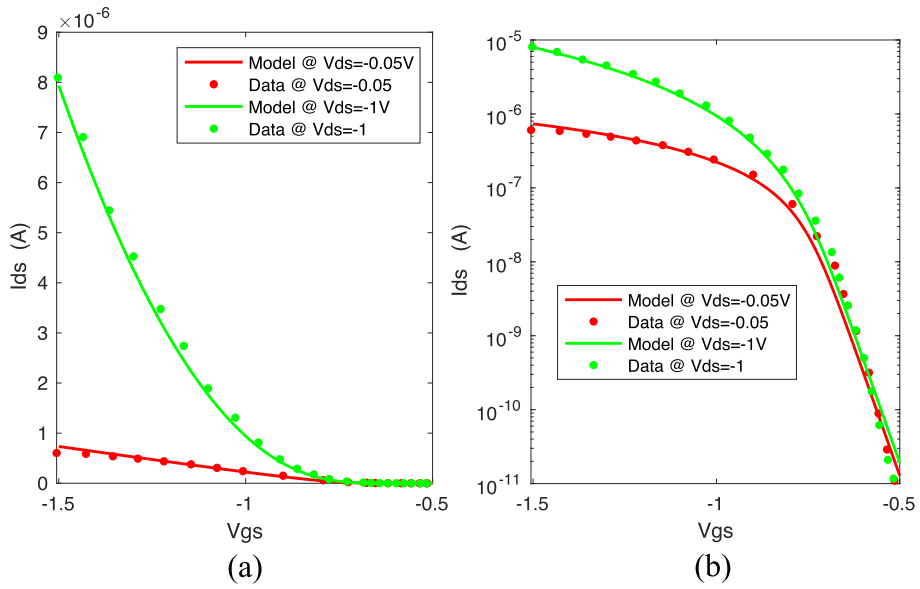

Fig. 3. Validation of the 2D FET model against experimental data for Device 2. (a) Linear transfer characteristics ($I_D - V_{gs}$) at $V_{ds} = -0.05, -1$ V. (b) Transfer characteristics on the logarithmic scale.

$$I_{DS} = \frac{W\mu}{L} M \left(\frac{V_b}{V_A} + 1\right)^{\gamma} \left[\frac{Q_D{}^2 - Q_S{}^2}{2C_b} - 2V_{th}(Q_D - Q_S) - 2C_{dq}V_{th}^2 \ln\left(\frac{Q_D - 2C_{dq}V_{th}}{Q_S - 2C_{dq}V_{th}}\right)\right] \tag{16}$$

3. Results and discussion

We validate our model against measurement data for four different device structures. Device 1 is a double gate structure that is composed of a single layer n-type MoS_2, which was grown using chemical vapor deposition (CVD), and then transferred onto a 285 nm intrinsic Si/SiO_2 wafer [15]. Device 2 is a double gate structure that was reported in [17], which consists of a p-type monoatomic channel of WSe_2. It is placed on top of 270 nm of SiO_2, which serves as an insulator and separates it from a doped-Si back-gate. Additionally, the channel is covered with 17.5 nm of ZrO_2, which acts as a barrier for a top Pd gate. Device 3 is a single back-gate structure with multilayer MoS_2 as a channel grown on 90 nm SiO_2 [18]. Device 4 is a single back-gate structure using a monolayer MoS_2 which was grown on SiO_2 (25 nm)/p++-Si substrates via chemical vapor deposition (CVD) at 850 °C [19]. Fig. 1 shows the cross section for the devices used for validation. Table 1 shows the parameters used for

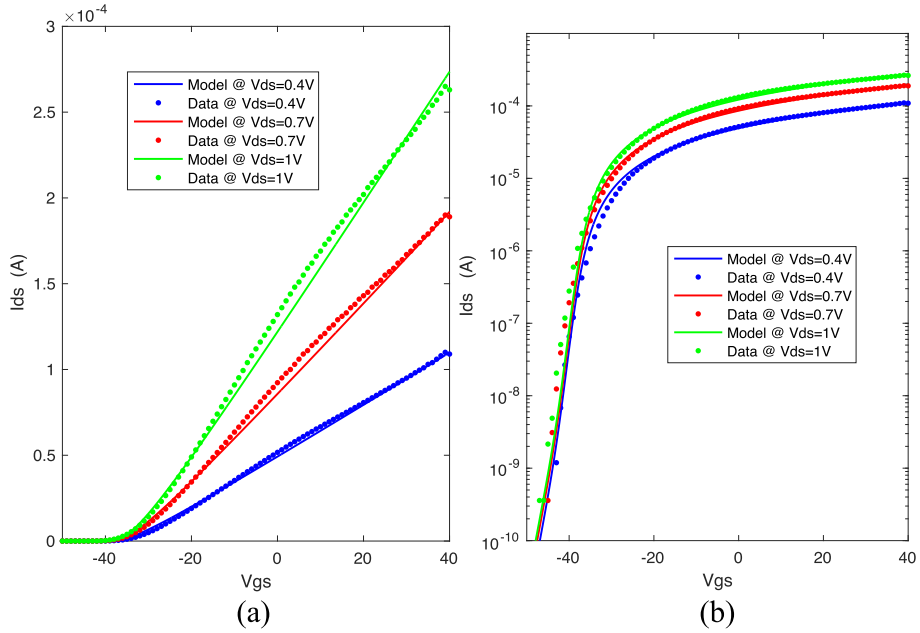

Fig. 4. Validation of the 2D FET model against experimental data for Device 3. a) Linear transfer characteristics ($I_D - V_{gs}$) at $V_{ds} = 0.4, 0.7, 1$ V. b) Transfer characteristics on the logarithmic scale.

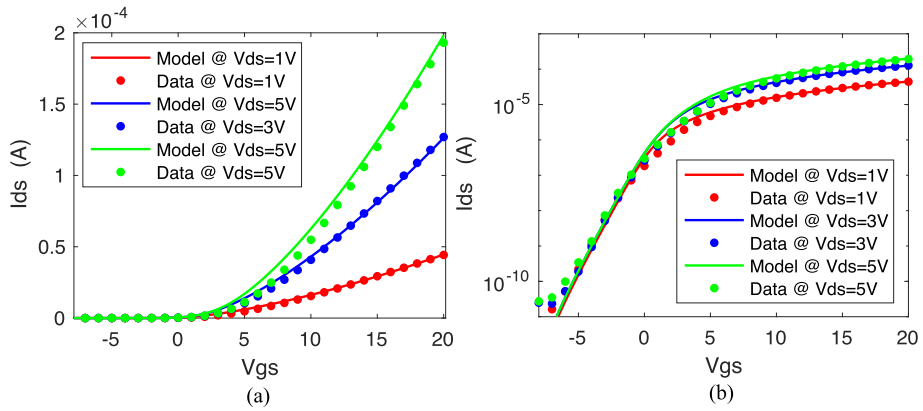

Fig. 5. Validation of the 2D FET model against experimental data for a single back gated structure Device 4. (a) Linear Transfer characteristics ($I_D - Vgs$) for Vds = 1 V, 3 V, 5 V for an encapsulated device at T = 165 °C. (b) Transfer characteristics on the logarithmc scale for an encapsulated device at T = 165 °C.

each device. As mentioned before, Device 1:3 have less gate voltage sweep than Device 4, where the superlinear current increase has been observed.

Figs. 2–5 shows the validation for our model against measurement data for different device structures. The fitting was carried out to the best fit, where α represents the ideality factor of the subthreshold slope which considers the interface trap densities and β is a fitting parameter that corrects the back gate capacitance. In Figs. 2 and 3 where the model fits Device 1 and 2, α has lower values compared to Device 3 and 4 indicating lower values of interface state densities. Regarding Device 4, we needed to modify the mobility parameter to account for the super-linear current increase. As mentioned above this phenomenon might be related to the trap filling, which takes place above certain gate voltage. After the traps are filled, the excess carrier generation is now contributing to the current conduction resulting to a higher current value than expected.

4. Conclusion

We have presented a unified charge control model for double and single back-gated TMD FETs. The charge is expressed in terms of the Lambert W function. Subsequently, we compute the current by using the charge densities located at the source and drain terminals of the channel. One of the measured devices have much higher gate voltage sweep for the transfer characteristics, where we have observed a superlinear current increase in which we modified the mobility parameter to account for this phenomenon. Despite the simplicity of our model, it shows very good agreement with the experimental results and is expressed in an explicit closed form equation which is preferred for the incorporation into circuit simulators.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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