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Abstract

Over the past decades, the continued scaling of transistors has reduced the energy consumption for every switching event and has increased the computational power of integrated circuits. However, nowadays, state-of-the-art silicon technology is reaching its physical limits and two-dimensional (2D) materials hold the promise of continued scaling down to dimensions of a few nanometers. In contrast to silicon, 2D materials maintain sizable mobilities in atomically thin layers. Gate control is enhanced over such thin channels, thereby mitigating short-channel effects in ultrascaled devices. Therefore, the community has devoted considerable efforts to develop performant, competitive and reliable field-effect transistors (FETs) based on 2D semiconductors. While numerous 2D semiconductors have been explored as channel materials and tremendous progress was made regarding the contacts to 2D materials, the equally important challenge of finding suitable gate insulators has yet received little attention. This thesis addresses this challenge of identifying good gate insulators, which is inherently linked to the goal of achieving a stable and reliable operation of 2D transistors.
At the moment, substantial threshold voltage drifts render 2D FETs electrically unstable. These drifts are caused mainly by charge trapping at border traps in the gate insulator. Here, this issue is investigated using comprehensive measurements of the hysteresis in the transfer characteristics and the bias temperature instability, combined with physical modeling of these phenomena based on the charge transfer to border traps. Further insights on charge trapping are gained in single defect studies on nanoscaled 2D FETs at cryogenic temperatures. Based on these observations, we suggest a stability-aware design strategy for 2D FETs which can improve their electrical stability and reliability. By choosing a suitable alignment of the conduction and valence band edges of the 2D semiconductor in relation to the defect bands in the gate insulator, the number of charge trapping events can be considerably reduced.
Another essential requirement for suitable gate insulators is their scalability down to equivalent oxide thicknesses of below one nanometer. At the same time, these thin layers need to sufficiently block tunneling currents to ensure low standby power consumption. Here, a theoretical lower limit of the projected leakage currents is established by modeling the tunnel currents in the defect-free case. In this way, it is shown that the layered crystalline insulator hBN is unsuitable as a gate insulator for ultrascaled CMOS circuits.
Based on our insights, we conclude that the most promising candidates for gate insulators for 2D FETs are crystalline gate insulators which form van der Waals interfaces with semiconducting monolayers while providing medium-sized dielectric constants and large band gaps. Besides, the understanding of charge trapping processes in 2D FETs developed within this thesis can be used to design novel 2D nanoelectronic devices for promising applications.

Kurzfassung

In den letzten Jahrzehnten hat die kontinuierliche Skalierung von Transistoren den Energieverbrauch für jeden Schaltvorgang reduziert und die Rechenleistung integrierter Schaltungen erhöht. Allerdings stößt die moderne Siliziumtechnologie heute an ihre physikalischen Grenzen und zweidimensionale (2D) Materialien versprechen eine weitere Verkleinerung bis hin zu Dimensionen von wenigen Nanometern. Im Gegensatz zu Silizium behalten 2D Materialien hohe Beweglichkeiten in atomar dünnen Schichten bei und die Gatekontrolle wird durch die Verwendung solch dünner Kanäle verbessert. Daher wurden erhebliche Anstrengungen unternommen um leistungsfähige und zuverlässige Feldeffekttransistoren (FETs) auf Basis von 2D Halbleitern zu entwickeln. Obwohl zahlreiche 2D Halbleiter erforscht wurden und große Fortschritte auf dem Gebiet der Kontakte zu 2D Materialien erzielt werden konnten, wurde bis jetzt der ebenso wichtigen Herausforderung, geeignete Gateisolatoren zu finden, noch wenig Aufmerksamkeit geschenkt. In dieser Arbeit widmen wir uns dieser Herausforderung, welche inhärent mit dem Ziel verbunden ist, 2D FETs stabil und zuverlässig zu betreiben.
Derzeit sind 2D FETs aufgrund erheblicher Schwellspannungsverschiebungen elektrisch instabil. Diese Spannungsverschiebungen werden hauptsächlich durch Ladungseinfang an Grenzdefekten im Gateisolator verursacht. Dieses Problem untersuchen wir anhand umfassender Messungen der Hysterese in den Transferkennlinien und der Spannungs-Temperatur-Instabilität, unterstützt durch die physikalische Modellierung dieser Phänomene. Basierend auf diesen Beobachtungen schlagen wir eine stabilitätsbasierte Designstrategie vor, die die elektrische Stabilität und Zuverlässigkeit von 2D FETs verbessern kann. Indem eine geeignete Ausrichtung der Leitungs- und Valenzbandkanten des 2D Halbleiters zu den Defektbändern im Gateisolator gewählt wird, kann die Anzahl der Ladungseinfänge stark reduziert werden.
Eine weitere wesentliche Voraussetzung für geeignete Gateisolatoren ist ihre Skalierbarkeit bis hin zu äquivalenten Oxiddicken von unter einem Nanometer. Gleichzeitig müssen diese dünnen Schichten Tunnelströme ausreichend blockieren, um so einen geringen Stromverbrauch im Standbymodus zu gewährleisten. Hier wird durch die Modellierung der Tunnelströme für den idealen, defektfreien Fall eine theoretische Untergrenze für die zu erwartenden Leckströme ermittelt. Auf diese Weise wird gezeigt, dass der geschichtete kristalline Isolator hBN als Gateisolator für ultraskalierte CMOS-Schaltungen ungeeignet ist.
Basierend auf unseren Erkenntnissen kommen wir zu dem Schluss, dass die vielversprechendsten Kandidaten für Gateisolatoren von 2D FETs kristalline Materialien sind, die Van-der-Waals-Grenzflächen mit halbleitenden Monolagen bilden und gleichzeitig mittlere Dielektrizitätskonstanten und große Bandlücken bieten. Außerdem kann das im Rahmen dieser Arbeit entwickelte Verständnis der Ladungseinfangprozesse in 2D FETs genutzt werden, um neuartige nanoelektronische Bauelemente zu entwickeln.

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Contents

Abstract i

Kurzfassung iii

Acknowledgements v

Acronyms xi

1 Introduction 1
- 1.1 Field-Effect Transistor . . . 2
- 1.2 CMOS Logic Scaling . . . 4
- 1.3 2D Materials Promise Ultimate Thinness . . . 6
- 1.4 Motivation and Scope . . . 8
- 1.5 Outline . . . 9

I State-of-the-Art 11

2 Transistors based on 2D Materials 13
- 2.1 Material Synthesis and Transfer Methods . . . 14
  - 2.1.1 Chemical Vapor Deposition . . . 15
  - 2.1.2 Metal Organic Chemical Vapor Deposition . . . 17
  - 2.1.3 Molecular Beam Epitaxy . . . 19
  - 2.1.4 Atomic Layer Deposition . . . 20
  - 2.1.5 Transfer Methods for Layered Materials . . . 20
- 2.2 Device Fabrication . . . 23
  - 2.2.1 Etching 2D Materials . . . 25
  - 2.2.2 Scaling the Channel Area in 2D Transistors . . . 28
- 2.3 Contacts to 2D Transistors . . . 30
  - 2.3.1 Impact of Schottky Barriers . . . 32
  - 2.3.2 Contact Gating and Scaling . . . 37

3 Characterization and Modeling of Performance and Reliability 39
- 3.1 Performance Analysis . . . 39
  - 3.1.1 Transfer Characteristics . . . 40
  - 3.1.2 Threshold Voltage . . . 42
  - 3.1.3 Mobility Evaluation . . . 44
- 3.2 Device Stability and Reliability . . . 46

3.2.1 Low Frequency Noise . . . 46
3.2.2 Random Telegraph Noise . . . 48
3.2.3 Bias Temperature Instability . . . 49
3.2.4 Time-Dependent Defect Spectroscopy . . . 52
3.2.5 Hot Carrier Degradation . . . 52
3.2.6 Time-Dependent Dielectric Breakdown . . . 53
3.3 Modeling Transistors Based on 2D Materials . . . 54
3.3.1 Non-Equilibrium Green's Functions . . . 55
3.3.2 Drift Diffusion Models . . . 57
3.3.3 Compact Models . . . 59
3.4 Charge Transfer Models . . . 62
3.4.1 Shockley-Read-Hall Model . . . 62
3.4.2 Non-Radiative Multi-Phonon Model . . . 65

II Improving Transistors Based on 2D Materials 71

4 Suitable Gate Insulators for 2D Transistors 73
4.1 Scaling Requirements . . . 73
4.2 Reducing Charge Trap Densities and Their Impact . . . 78
4.2.1 Interface Traps . . . 78
4.2.2 Border Traps . . . 82
4.3 Deposition Technology for Gate Insulators . . . 85
4.4 Insulating Materials for Nanoscaled 2D Transistors . . . 87

5 Experimental Characterization of the Electrical Stability of 2D Transistors 91
5.1 Stability of the Threshold Voltage in 2D Transistors . . . 92
5.1.1 Hysteresis in MoS_2 and Graphene Transistors . . . 93
5.1.2 BTI in MoS_2 and Graphene Transistors . . . 101
5.1.3 Tuning the Fermi Level . . . 106
5.2 Single Defect Analysis in Nanoscaled 2D Transistors . . . 113
5.2.1 RTN in MoS_2 Transistors . . . 114
5.2.2 Charge Transfer at Cryogenic Temperatures . . . 116
5.2.3 TDDS in MoS_2 Transistors . . . 121

6 Modeling the Operation and Stability of 2D Transistors 123
6.1 Modeling Molybdenum Disulfide Transistors . . . 124
6.1.1 Contact Models . . . 129
6.1.2 Impact of Interface Traps . . . 130
6.1.3 Modeling the Hysteresis . . . 131
6.2 Modeling Leakage Currents through Gate Insulators . . . 134
6.2.1 Adaptations of the Tsu-Esaki Model for hBN . . . 135
6.2.2 Coupled DFT and NEGF Model . . . 138
6.2.3 Performance Projection of the Tunnel Current through hBN . . . 140

7 Conclusions and Outlook **145**
7.1 Conclusions 146
7.2 Outlook 148

A Estimation of the Doping Level in MOCVD grown MoS_2 **151**

Bibliography **155**

List of Publications **203**

Curriculum Vitae **207**

Acronyms

AFM	atomic force microscopy
ALD	atomic layer deposition
ALE	atomic layer etching
BEOL	back end of line
BP	black phosphorus
BTE	Boltzmann transport equation
BTI	bias temperature instability
CAFM	conductive atomic force microscopy
CC	configuration coordinate
CMOS	complementary metal oxide semiconductor
CNT	carbon nanotube
CV	capacitance voltage
CVD	chemical vapor deposition
DD	drift diffusion
DFT	density functional theory
DIBL	drain induced barrier lowering
DOS	density of states
EOT	equivalent oxide thickness
FE	field emission
FEOL	front end of line
FET	field-effect transistor
GAA	gate all around
GFET	graphene field-effect transistor
GGA	generalized gradient approximation
hBN	hexagonal boron nitride
HCD	hot carrier degradation
HOPG	highly oriented pyrolytic graphite
LDA	local density approximation

MBE	molecular beam epitaxy
MIS	metal insulator semiconductor
MLWF	maximally localized Wannier function
MOCVD	metal organic chemical vapor deposition
MOS	metal oxide semiconductor
MSM	measure-stress-measure
NEGF	non-equilibrium Green's function
NBTI	negative bias temperature instability
NMP	non-radiative multi-phonon
PA	photoabsorption
PBTI	positive bias temperature instability
PBE	Perdew Burke Ernzerhof
PDF	probability density function
PEC	potential energy curve
PES	potential energy surface
PL	photoluminescence
PS	photocurrent spectroscopy
PSD	power spectral density
RF	radio frequency
RIE	reactive ion etching
RTN	random telegraph noise
SB	Schottky barrier
SCE	short channel effect
SCTD	surface charge transfer doping
SEM	scanning electron microscopy
SILC	stress induced leakage currents
SOI	silicon on insulator
SRH	Shockley-Read-Hall
SS	subthreshold swing
STS	scanning tunneling spectroscopy
TAT	trap-assisted tunneling
TCAD	technology computer aided design
TDDB	time-dependent dielectric breakdown
TDDS	time-dependent defect spectroscopy
TE	thermionic emission
TEM	transmission electron microscopy
TFE	thermionic field emission
TLM	transfer length method
TMD	transition metal dichalcogenide
TSCIS	trap spectroscopy by charge injection and sensing
vdW	van der Waals
WKB	Wentzel-Kramers-Brillouin

List of Figures

1.1 Schematic of an n-type silicon MOSFET including its transfer characteristics. . 2
1.2 Market opportunities of 2D material-based devices and schematic structure of a top gated MoS_2 based MOSFET. 7

2.1 Chemical vapor deposition (CVD) of TMDs, including a schematic drawing of the CVD furnace, optical microscope images of large area MoS_2 monolayers and the dependence of the growth shape on growth temperature and the ratio of partial precursor pressures. 16
2.2 Metal organic chemical vapor deposition (MOCVD) of TMDs, including a schematic drawing of the MOCVD furnace, SEM and TEM images of grown MoS_2 monolayers and fabricated large area MOSFETs based on Nb-doped MoS_2 for evaluating the dopant distribution. 18
2.3 Cross sections through the five most common 2D semiconductor based FET device layouts. 24
2.4 Fabricated, back gated MoS_2 MOSFETs with a bare channel and SiO_2 as a gate oxide shown in a cross section, optical microscopy and atomic force microscopy images. 25
2.5 Comparison of different plasma etch chemistries for etching multilayer MoS_2, showing the AFM images for a layer etched with SF_6/Ar and for a layer etched with Cl_2/O_2. 27
2.6 Fabrication of back gated devices with nanoscaled device dimensions including an SEM of the final device, an SEM image of the dose test pattern and the cross section and top view shown schematically. 29
2.7 Transfer length method measurements of the contact resistance to 2D semiconductors as reported in literature. 31
2.8 Schottky barriers form due to strong Fermi level pinning at the metal to semiconductor contacts. Here the transfer characteristics of Schottky barrier FETs are discussed with respect to the band bending in different regimes. 34
2.9 Cross section of the 2D MOSFET layout with double gating and doped contact regions alongside a figure showing the dependence of the contact resistance on the contact length including available literature values. 38

3.1 Standard FET characteristics as measured on an MoS_2 FET. 40
3.2 Extraction of performance parameters from characteristics measured on an MoS_2 FET. 42
3.3 Low frequency noise on an MoS_2 FET and its origin in charge trapping. 47

3.4 BTI data for the recovery and stress phases on Si/SiO_2 and on MoS_2/SiO_2 FETs. 50
3.5 Overview of modeling approaches for the simulation of 2D material-based transistors. . . . 54
3.6 Non-equilibrium Green's function modeling of a FET based on a 2D semiconducting channel. . . . 56
3.7 Tsu-Esaki model for the tunneling current through an insulating barrier between two reservoirs formed by a metal and a semiconductor. . . . 60
3.8 Schematic showing the potential energy curves involved for charge transitions and for thermal transitions within NMP theory. . . . 66
3.9 States of the 4-state NMP model together with a configuration diagram including all model parameters. . . . 69

4.1 Requirements for gate insulators. . . . 74
4.2 Comparison of measured gate leakage current densities as reported in literature. 75
4.3 Calculated gate leakage current densities through various gate insulators in the ideal, defect-free case. . . . 76
4.4 Subthreshold swing as a function of EOT as reported in literature. . . . 79
4.5 Impact of interface traps and remote phonon scattering on the mobility including a schematic to illustrate the effects of hBN interlayers and a comparison of mobility values with and without an hBN substrate as reported in literature. . . . 81
4.6 Time constants and energetic band alignment of border traps. . . . 83
4.7 Schematic showing the 2D channel/insulator interfaces for various insulators. 87

5.1 Hysteresis measurements in top gated MoS_2 FETs with an Al_2O_3 gate oxide. . . . 94
5.2 Hysteresis widths of MoS_2 FETs in comparison with commercial Si FETs. . . . 95
5.3 Top-gated GFETs based on two types of graphene with Al_2O_3 as gate oxide. . . . 97
5.4 Defect band alignment in Al_2O_3. . . . 99
5.5 Hysteresis in two GFET types at varying sweep times and sweep ranges. . . . 100
5.6 BTI in back gated, encapsulated MoS_2 FETs with SiO_2 as a gate oxide. . . . 102
5.7 BTI in top gated GFETs with an Al_2O_3 gate oxide for high gate fields of 5.8 MV/cm. 104
5.8 BTI in GFETs with an Al_2O_3 top gate for moderate gate oxide fields of 2.9 MV/cm. 105
5.9 Fermi level tuning to maximize the energetic distance to the oxide defect bands. 107
5.10 Estimation of the electrical stability improvement based on TCAD simulations. 109
5.11 Hysteresis in the transfer characteristics of double gated GFETs and the impact of a dynamically tuned Fermi level via electrostatic doping. . . . 111
5.12 Experimental verification of the hysteresis reduction by Fermi tuning. . . . 112
5.13 Single defect limit for the analysis of discrete steps in nanoscaled FETs. . . . 114
5.14 Random telegraph noise measured on nanoscale MoS_2 on SiO_2 FETs. . . . 115
5.15 RTN on MoS_2/SiO_2 FETs at 25 K. . . . 117
5.16 Temperature dependence of capture and emission time constants at cryogenic temperatures. . . . 118
5.17 Estimated depth of the observed single charge trap based on its time constants. 120
5.18 TDDS on MoS_2/SiO_2 FETs at cryogenic temperatures. . . . 122

6.1 Impact of the dielectric environment on the band gap of MoS_2. . . . 126

6.2 Drift-diffusion TCAD simulations of MoS_2 FETs. 128
6.3 Schottky contact models as implemented in drift diffusion TCAD simulations. . 129
6.4 Impact of interface traps on MoS_2 FETs. 130
6.5 Band diagram of the MoS_2/SiO_2 FET showing the alignment of interface traps and oxide defect bands. 132
6.6 TCAD simulation of the measured hysteresis using an NMP model. 133
6.7 hBN band structure and adaptations of the Tsu-Esaki model. 136
6.8 Ab initio quantum transport calculations. 139
6.9 Performance projection of the tunneling current through hBN in the defect-free case. 141
6.10 Impact of the metal work function on the projected current density. 142

A.1 Impact of the Nb doping level on the transfer characteristics of MOCVD grown MoS_2 FETs. 151

List of Tables

4.1 Alignment of the known oxide defect bands. 84
4.2 Comparison of the material parameters of potential gate insulators for 2D CMOS. 88

5.1 Parameters of the Al_2O_3 defect band. 98

6.1 Band gap of monolayer MoS_2. 125
6.2 Material parameters of MoS_2 monolayers used for drift diffusion based TCAD simulations. 127
6.3 Material parameters of bulk hBN. 138

A.1 Extracted doping levels on different locations of Nb-doped MOCVD grown MoS_2 film. 153

1 Introduction

In the ongoing era of the digital transformation, microelectronic chips play an increasingly important role in our society. In fact, microelectronic chips are the backbone of this transformation. Nowadays, economic growth is driven by digital storage of ever increasing amounts of data and converting this data into actionable knowledge [1]. Therefore, making microelectronic chips faster and more versatile is key to economic growth and, more importantly, it is key to exploiting the full potential offered by information technology to solve many problems we face as a society. In addition, as microelectronic chips become cheaper, more people all around the world gain access to the vast amount of data available and to the possibilities and opportunities provided by this technology.

One effective way to work towards faster, cheaper, less energy consuming, and more versatile microelectronic chips is to focus on the transistor, the basic building block of a microelectronic chip. As one microprocessor currently contains up to 40 billion single transistors, powerful scaling laws apply. If transistors themselves are made faster and less energy consuming, while at the same time becoming cheaper, and more easily integrable with memory elements and sensors through monolithic integration, this would be a substantial step towards the goal of more performant, versatile, and accessible microelectronics. Over the last several decades, progress in fabricating faster, more energy-efficient, and cheaper transistors has been made by scaling down the dimensions of silicon-based transistors. In this way, the semiconductor industry has recently started to fabricate microprocessors at the 5 nm node which is a manufacturing generation, associated with a certain transistor size, e.g. 18 nm gate length and 7 nm gate width. At these ultimately small dimensions, the integration of two-dimensional (2D) materials could add considerable value to microprocessors by offering both a promising route towards further downscaling as well as the possibility of diversification of the microelectronic chip [2, 3].

In the introduction of this work, the basic operating principle of FETs is briefly discussed and a historical perspective is provided on the motivation and driving forces behind the continuous downscaling of complementary metal oxide semiconductor (CMOS) logic circuits. This leads to the prospects and ambitions associated with the introduction of 2D materials as building blocks for future transistors. These considerations form the basis for the motivation of this work and the central research question studied. The introduction is finalized by defining the scope of the work and giving a brief outline over the subsequent chapters.

1.1 Field-Effect Transistor

The operating principle of a field-effect transistor is as follows. The voltage applied to a controlling electrode, the gate, creates an electric field which controls the current flow through the semiconducting channel, connecting the source to the drain electrode. Here, the operating principle of the most common variant, the enhancement-mode metal oxide semiconductor field-effect transistor (MOSFET) which is based on a silicon channel is explained. In a MOSFET, a metal gate determines the electrical potential in the semiconducting channel, which is separated from the gate by the gate oxide. Inside the channel, the current is dominated by carriers of one polarity (only electrons or only holes), thus the MOSFET is a unipolar device. Here, the operation of an n-type MOSFET is described, where an abundance of electrons forms the conducting channel. However, to describe a p-type device only the dopant types would have to be exchanged and the voltage polarities reversed.

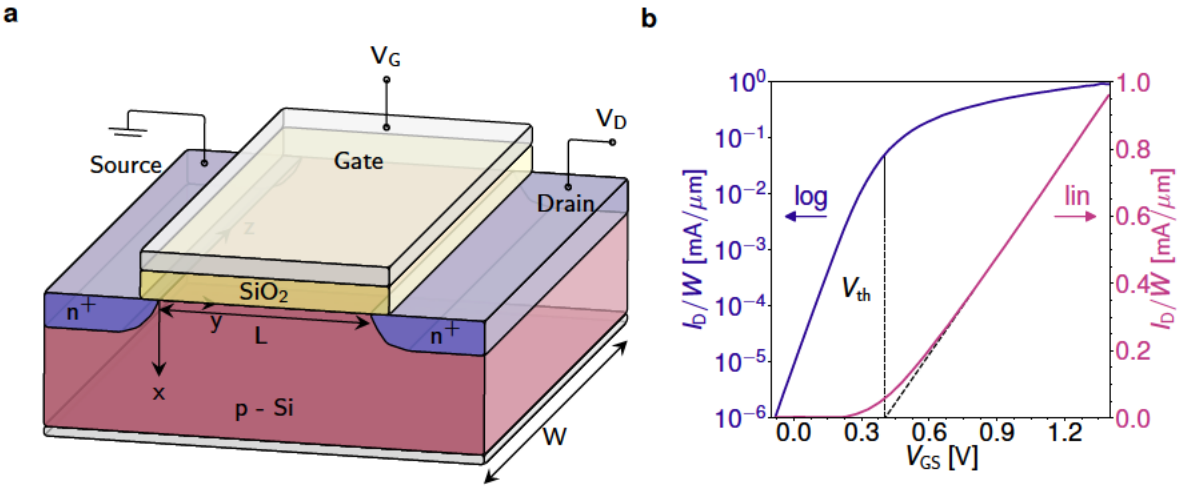

Figure 1.1. **(a)** Schematic drawing of an n-type silicon MOSFET. If a positive bias above the threshold voltage is applied to the gate ($V_{GS} > V_{th}$) an inversion channel forms and the MOSFET turns on. **(b)** Transfer characteristics of an n-type MOSFET both on a logarithmic (log) and on a linear (lin) scale, indicating the threshold voltage (V_{th}). The drain current I_D is normalized by the transistor width W.

In Figure 1.1(a) an n-type MOSFET is shown in a schematic drawing. It consists of a p-type silicon substrate, where two heavily n-doped (n^+) regions are formed, the source and drain regions. On top of the channel area, between these regions, a thin silicon dioxide (SiO_2) film is formed via thermal oxidation, the gate oxide. A metal contact on top of the gate oxide serves as the gate electrode. The central element of the MOSFET is formed by the MOS stack, the metal gate, the gate oxide, and the semiconducting silicon channel. In particular, the interface of the channel to the gate oxide is critical for current conduction and for device stability. As long as a negative gate voltage (V_{GS}) is applied or V_{GS} is zero, majority carriers are accumulated in the Si/SiO_2 interface region or the region is depleted. In this accumulation mode, the two back-to-back pn junctions which form the channel block the current flow. Only when a sufficiently large positive voltage V_{GS} is applied to the channel, the Si/SiO_2 interface is inverted to n-type and thus a conductive inversion channel between the two n^+ regions is formed. If then a voltage is applied to the drain (V_{DS}), electrons will flow from source to drain. In a nutshell, a MOSFET operates as a switch, as the gate electrode is insulated from

the channel and turns the channel current on and off via pure capacitive coupling only, which is commonly referred to as the field effect [4]. This behavior of a MOSFET is reflected in its transfer characteristics, where the drain current I_D (the switched quantity) is given as a function of V_{GS} (the switching quantity), see Figure 1.1(b). Below the threshold voltage V_{th}, there is an exponential current increase and once the MOSFET is turned on there is typically a linear dependence of I_D on V_{GS}.

A historical perspective on the development of the silicon MOSFET holds insights on the relevant breakthroughs which allow for stable operation of these devices when fabricated in large numbers on an industrial scale. These insights contain some parallels between the important achievements in the early days of silicon MOSFET development and today's development of stable FETs based on 2D materials. Nearly 100 years ago the idea of exploiting the field effect to control the current flow was first described by Lilienfeld in his 1928 patent application [5]. Despite detailed descriptions of amplifier circuits, later attempts to build an amplifying transistor based on Lilienfeld's plans failed and it is unknown whether any of his early prototypes ever provided current amplification [6]. Two decades later, in 1948 at Bell Laboratories a team of engineers consisting of Shockley, Bardeen, and Brattain used a different design to build the first working junction-gate field-effect transistor in the form of a point-contact transistor. This prototype consisted of n-type germanium, connected with two point contacts, which contact the p-type surface inversion layer through a thin oxide [7, 8].

In fact, the engineers at Bell labs had also established a first theory of detrimental surface states, which are called interface traps according to today's nomenclature [9]. They showed that the charge trapping at interface traps was responsible for the weak modulation of the surface potential in thin silicon and germanium semiconductor films, which was orders of magnitude smaller than expected. In their work, they extrapolated the density of interface traps to be as high as $5 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$ [10], more than 10000 times higher than the standard in today's silicon MOSFETs at $10^{9}\,\mathrm{cm^{-2}eV^{-1}}$. Soon thereafter in 1952, the reaction kinetics of charge trapping at interface traps were described by Shockley, Read, and Hall in a model formulation which is still used today due to its simplicity [11], see Sections 3.4.1 and 6.1.2. The early MOSFETs showed highly unstable operation for two main reasons. Firstly, they suffered from large interface trap densities which degraded the surface where the current flows in the inversion layer. Secondly, early MOSFETs relied on the introduction of n-type surface inversion in p-type Si and p-type surface inversion in n-type Ge, introduced by weak charging from the air. At that time, the stabilization of MOSFETs was the primary concern for researchers in the field. In 1959, Atalla, Tannenbaum, and Scheibner showed that the surface of silicon pn junctions can be stabilized by thermally grown SiO_2 [12]. This passivation of a silicon pn diode by dry oxidation resulted in a significant reduction in the diode's low frequency noise. More importantly, their discovery of the stabilization of the MOSFET through thermal SiO_2 paved the way towards the first successful operation of an enhancement mode silicon FET [13, 14]. The discovery of the stabilization of MOSFETs using thermal oxidation and the subsequent development of the silicon MOSFET were presumably the most important technological advances which lead to silicon integrated circuits and mass production [6]. It should also be noted that this discovery was made on silicon, whereas most previous discoveries had used germanium due to its higher inherent carrier mobilities. However, since

silicon possesses a stable oxide and the oxide of germanium is water soluble, silicon was used as a basis for the fabrication of integrated circuits, as the operation of silicon MOSFETS was comparatively stable. Hence, the Si/SiO_2 system was central to the success of integrated circuits.

Thus, 30 years after the first mention of the MOSFET concept, the MOSFET in its current form had been designed and built. Already in the same year, Kilby built an integrated circuit to realize a flip-flop out of germanium mesa transistors and gold interconnects [15]. Soon afterwards, the complementary metal oxide semiconductor (CMOS) inverter circuit consisting of an n-type and a p-type MOSFET was invented, which acted as a basic building block for all microprocessor architectures which followed [16]. At that time it also became clear that for the economic success of the novel technology it would be important to significantly reduce the size of electronic circuits. In 1960 Englebart presented the first considerations for scaling laws of electronic circuits [17] and five years later Moore published an article including the projection that the number of transistors on an integrated circuit would double every year [18]. This projection, albeit later adapted, became known as Moore's law and steered the progress in the semiconductor industry over the subsequent five decades. The parallels between the development of the MOSFET described above and today's development of the 2D FET will be detailed when describing the motivation behind this work in Section 1.4.

1.2 CMOS Logic Scaling

Over the last fifty years, the number of transistors per chip has doubled every one-and-a-half to two years. Moore first hypothesized in 1965 that an exponential growth would drive progress in microelectronics over the next several years [18] and recalibrated the growth rate to a doubling every second year in 1975 [19]. This doubling of the transistor count was realized by reducing the transistor size by a factor of two every two years. A reduction of the transistor size holds many benefits. First, it translates to a reduction of the energy consumed during switching, second, it increases the switching speed, thus the maximum clock frequency of the integrated circuit, and third, it reduces the production costs per single transistor. These benefits, and the pressure to remain economical in a highly competitive market, motivated the semiconductor industry to uphold the mentioned scaling trends. Related efforts for upholding the scaling trends were high and in order to make investments more predictable, in 2000, an industry consortium came together to align their research goals in the form of the International Technology Roadmap for Semiconductors (ITRS) [20]. In the ITRS, roadmap development standards were set and the timelines for future developments were outlined. When further scaling became even more competitive and challenging to uphold, the ITRS was disbanded, with the last report being issued in 2015. In its wake, new efforts were undertaken to address the broader field of progress in electronic devices and systems. These new reports are called the International Roadmap for Devices and Systems (IRDS) and appear annually [21]. IRDS focuses on providing an outline to facilitate the coordination of research and development efforts in the field and sets reference values which will be used throughout this work.

At the core of downscaling lies the idea that the dimensions of transistors can be reduced without degrading key performance characteristics. By reducing the horizontal dimensions of the MOSFET, in particular the channel length, L, the MOSFET becomes easier to switch and requires less chip area. However, if only the horizontal dimensions are reduced, the gate increasingly looses control over the channel, which gives rise to a number of phenomena summarized under short-channel effects (SCEs). Most importantly, the threshold voltage, V_{th}, becomes dependent on the channel length, being reduced for short L, and the drain bias, V_{DS}, starts to have an impact on the drain current as it increasingly modifies the electric field below the gate. These SCEs degrade device performance and consequently the advantages gained by downscaling, unless they are controlled by a suitable device design. In 1974, Dennard *et al.* suggested that SCEs could be held at bay by maintaining a constant electric field throughout the device while reducing device dimensions [22]. This is realized by scaling down the vertical dimensions along with the horizontal dimensions, by increasing the substrate doping concentration to decrease the depletion width, and by simultaneously decreasing the applied voltages. If all dimensions and applied voltages are scaled down by a factor κ, the circuits are sped up by the same factor and in addition, power dissipation per circuit is reduced by κ^2. However, the requirement of scaling the supply voltage together with the dimensions proved to be too restrictive as it was desirable to maintain the same supply voltage over several technology generations [4]. Instead, the voltage was kept constant, leading to constant-voltage scaling where the electric field increases while the shape of the electric field pattern in the device is preserved to avoid SCEs [23]. Thus, both scaling regimes, constant-field and constant-voltage scaling, can control short channel effects to a certain extent and have been combined in the rules of generalized scaling, where the dimensions scale by a factor κ and the electric field increases by a factor α [24].

As the circuits were increasingly scaled down, more and more severe physical limitations were observed. There are some quantities central to the operation of MOSFETs which do not scale and set natural limits. First, the thermal voltage $k_{\mathrm{B}}T/q$ is a fundamental property which does not scale and which determines the slope in the subthreshold region [4]. As the slope of the MOSFET's transfer characteristics stays constant instead of increasing beyond the thermal voltage, the on currents decrease as the supply voltage is scaled down. Second, as the silicon bandgap does not scale, the built-in potential and surface potential do not change, which translates to a reduced scaling of the depletion widths and in consequence more severe SCEs. Third, the increase of the electric field has detrimental effects on a number of properties. A higher electric field degrades the mobility, which becomes even more pronounced in thin silicon layers due to surface roughness scattering. Furthermore, higher electric fields in the oxide increase leakage currents and bring the oxide closer to breakdown conditions. In order to maintain small leakage currents while reducing the equivalent oxide thickness (EOT), gate oxides with a higher permittivity (ε_{R}) such as HfO_2 have been introduced. In addition, the oxide thickness has been reduced less than required by scaling laws.

As a whole, all these fundamental limitations have slowed down scaling over recent years and have called for more radical changes to the transistor geometry and the involved materials. A first step to reduce short channel effects was the introduction of the silicon-on-insulator (SOI) substrate. In SOI technology, a conventional MOSFET is built on a thin layer of crystalline

silicon which is separated from the substrate by a several hundred nanometer thick buried SiO_2 film. In this configuration the devices are isolated from the underlying silicon substrate, which results in enhanced gate control [25]. Soon after the first CMOS SOI microprocessor was fabricated in 1997 [26], high gate leakage currents motivated the transition from SiO_2 as a gate oxide with $\varepsilon_R = 3.9$ to SiON ($\varepsilon_R \sim 4.5$) [27] and to HfO_2 ($\varepsilon_R \sim 20$) [28, 29] in the production lines. However, even if gate oxides with high permittivity (high-k oxides) allow for further reduction of the EOT at acceptable levels of the leakage currents, further downscaling of dimensions soon exacerbates SCEs. A direct approach to improve SCEs is to change the transistor geometry with the aim of maximizing gate control over the channel. Towards this aim, the gate encloses increasingly more regions of the channel. In a first step a second gate is added below the silicon channel to form a double-gated transistor [30], in the second step the gate encloses the channel from three sides in a finFET geometry [31] and in the third step the gate is wrapped around a silicon nanowire or nanosheet in a gate-all-around (GAA) geometry [32]. Today, the finFET geometry is the state of the art, being used in production since the 22 nm-node in 2012 [33] and dominating the current mass production at the 7 nm node. Over the next five years the GAA geometry might be introduced into fabrication lines at the 3 nm node [34, 35]. Nowadays, the industry has come close to the end of the silicon roadmap, towards ultimately scaled devices, where further scaling requires more significant changes to the device geometry and to the materials used to build MOSFETs. In order to allow for continued shrinking of the gate length a thinner channel is required. In this context, 2D materials are a promising candidate, as they offer atomically thin channels while maintaining sizable electron and hole mobilities [36]. In contrast, in silicon, the channel mobility degrades substantially if the thickness is reduced below 3 nm [37].

1.3 2D Materials Promise Ultimate Thinness

The key benefit of 2D materials is their 2D nature, meaning the fact that they are thermodynamically stable as single atomic layers [38]. Most 2D materials can be fabricated by isolating them from their closely related 3D variants which are characterized by a layered structure. In this structure, the layers are loosely bonded to each other by weak van der Waals forces and show strong covalent bonds only within the single layers. Thus, a single 2D layer does not have any dangling bonds and forms ideally defect-free van der Waals interfaces with other layered materials. Therefore, the charge carrier mobility in 2D materials is comparatively high, as scattering at surface traps is minimized [39, 40]. These high mobilities in addition to the excellent scalability of atomically thin semiconductors as FET channels are the main selling points of 2D materials as channels for FETs in logic applications [3]. A channel with a thickness below 1 nm suppresses short channel effects, thus allowing to scale the channel length below 15 nm [41], required for the beyond 3 nm technology nodes [42].

Besides the advantages of 2D materials used as a channel in a classical MOSFET device design, the van der Waals interface between adjacent layers creates the possibility to combine different 2D materials in van der Waals heterostructures [43]. These heterostructures offer a wide variety of options to create novel device designs [44], among them designs which exploit quantum mechanics to overcome the limitation of the subthreshold slope of FETs

which do not exceed the thermal voltage $k_B T/q$. This non-scalability of the subthreshold slope has led to the gradual decrease of on-state currents of devices for increasingly scaled technology nodes. Promising device concepts which could help to overcome this problem are tunnel FETs [45] and Dirac source FETs [46]. In addition to the numerous options provided by van der Waals heterostructures, the research efforts so far have focused on a small selection of 2D materials, like graphene [47], transition metal dichalcogenides (TMDs) [48] or black phosphorus [49]. However, computational studies have predicted a plethora of more than 1800 layered candidates with a stable 2D variant which is exptected to be reasonably easy to be separated from the 3D layer stack [50]. Thus, the options provided by 2D materials as building blocks for FETs are far from being fully exploited yet.

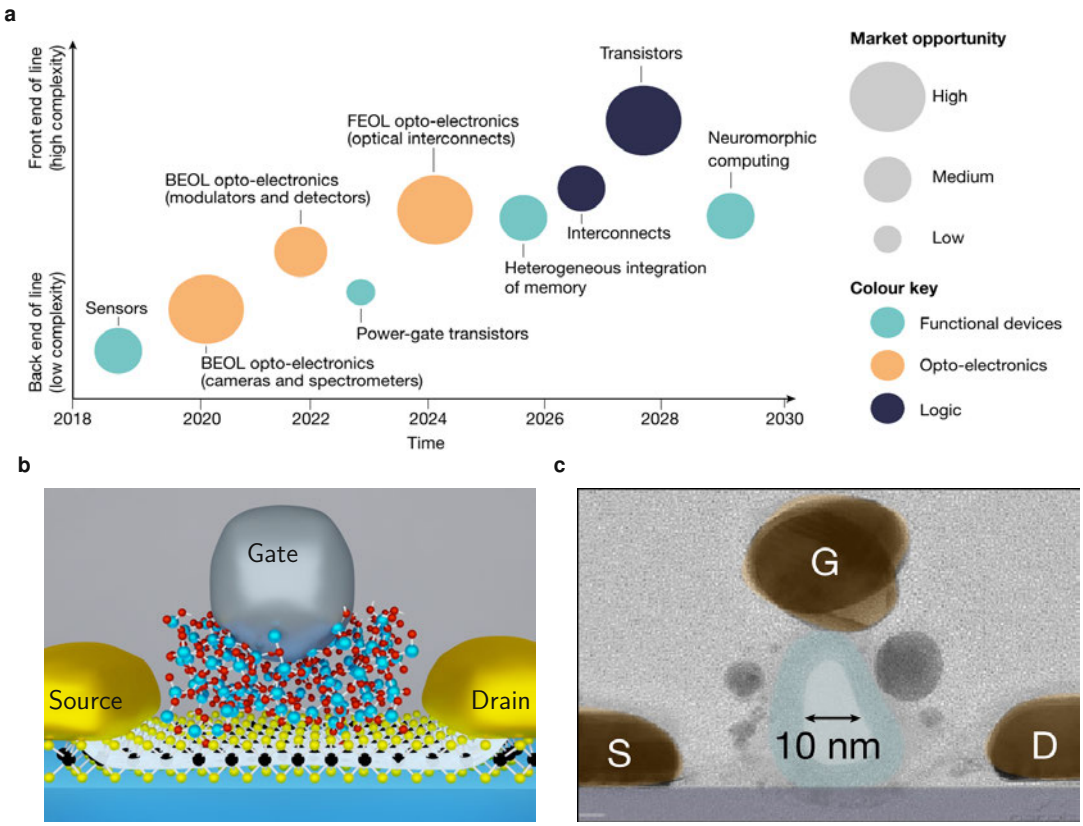

Figure 1.2. **(a)** Illustration of the market opportunities of 2D based devices as a function of the foreseen time when the products will be introduced to the market, giving an optimistic projection for the market readiness of the respective application scenarios. However, we argue that the proposed schedule is out of reach unless the electrical stability of 2D material-based FETs is considerably improved. Image reproduced from [3], reprinted with permission of Springer Nature. **(b)** Schematic illustration of a top gated MOSFET based on the 2D TMD MoS_2 (Mo - black atoms, S - yellow atoms) using amorphous Al_2O_3 (Al - blue atoms, O - red atoms) as a gate oxide. Also a shining, transparent layer is shown in the MoS_2 to illustrate the current flow. **(c)** Transmission electron microscopy (TEM) image of a cross section through a nanoscaled MoS_2 FET using Al_2O_3 as a gate oxide. Image reproduced from [51] [3], reprinted with permission of Springer Nature.

Beyond the prospect of advancing nanoelectronics in itself, 2D materials could be used to enhance the functionality of nanoelectronic devices through monolithic integration of 2D material-based devices at the back end of the line (BEOL) of nanoelectronic chips. Appli-

cation scenarios for 2D material-based devices are manifold, ranging from neuromorphic devices [52], over photonics [53] and optoelectronics [54] to sensors [55]. Most intriguingly, many of these devices can be fabricated on top of a silicon CMOS chip which provides the driver, read-out, and peripheral circuitry [56, 57]. This compatibility paves the way for a faster integration and adaptation of these device systems by the semiconductor industry with the promise to reach market readiness within this decade [3]. In Figure 1.2(a) the market opportunities of 2D material-based devices are shown over the time axis of this decade, differentiating between applications in functional devices, optoelectronics, and digital logic. In addition, the basic structure of a top gated MoS_2 based FET with an Al_2O_3 gate oxide is shown in a schematic in Figure 1.2(b) and a transmission electron microscopy (TEM) image of the cross section through a nanoscaled MoS_2 FET is presented in Figure 1.2(c). However, market readiness of 2D material-based systems remains elusive unless stable device operation of the prototypes can be demonstrated throughout their entire lifetimes. This notion sets the stage for the motivation of this work.

1.4 Motivation and Scope

This thesis aims to analyze the stability of field-effect transistors based on 2D materials. Despite the requirement of stable operation being essential to the success of a novel technology, this research area has been explored by relatively few scientists up to now. Historically, it has been the discovery of Atalla, Tannenbaum, and Scheibner [12] related to the stabilization of silicon devices by thermal oxidation of the silicon surface which paved the way for the breakthrough of silicon technology. Inspired by this historical perspective, it seems plausible that the question of whether or not 2D material-based transistors might make the leap towards market readiness in the future will be linked to the question if stable device operation for extended lifetimes can be achieved. Therefore, in this work the state-of-the-art of 2D material-based transistors is examined, describing measurement methods, theories, and models which are dedicated to the assessment of the stability of FETs. FETs based on 2D materials are a comparatively young research field with the first work being published in 2004 [38] and most of the science related to FETs being performed within the last decade [41, 58]. This gives rise to a central problem for the objective assessment of device stability, as all FETs which are currently available are prototype devices with large variations in sample quality, depending on the chosen fabrication process. Thus, we have chosen a combination of a comprehensive experimental analysis and physics-based modeling in this work. The aim is to understand the mechanisms which determine device stability and to be able to differentiate between fabrication-related instabilities and instabilities arising from the inherent material properties. Nevertheless, all of our evaluations rely on a number of chosen model descriptions including required simplifications. Therefore, despite all applied scientific rigor, the conclusions drawn within this thesis depend on the chosen methods and can only give a limited perspective on this complex topic. In addition, the research field evolves quickly and thus the presented work can only attempt to present the current level of knowledge without claiming to cover all of the latest developments. Also, there is no claim to the completeness of the presented picture, on the contrary, this thesis only aims to give a balanced overview over the subject, while highlighting the author's contributions to this research field.

1.5 Outline

In Chapters 2 and 3 the state-of-the-art regarding fabrication, performance and electrical stability and reliability of 2D material-based transistors is outlined. In the second part, consisting of Chapters 4, 5, and 6, the advancements made within this work to the state-of-the-art are described. In particular, the impact of gate insulators on the operation and properties of 2D material-based FETs is highlighted and possible routes for improving the performance, electrical stability, and reliability of 2D FETs are discussed.

Chapter 2 gives an overview of the state-of-the-art in the fabrication of FETs based on 2D materials. Starting from the synthesis of the materials themselves, the fabrication process is described. As it is difficult to create good metal contacts to 2D material devices, special emphasis is placed on contact formation.

Chapter 3 describes the state-of-the-art for the characterization of FET performance and reliability with a special focus on the particulars of FETs based on 2D materials. In addition, an overview is given over modeling approaches for 2D material-based FETs, starting from the computationally most expensive, fully quantum mechanical models, going over to semi-classical descriptions within a technology computer-aided design (TCAD) framework, and finally discussing compact models. At the end of the chapter, two models are reviewed for describing charge transfer processes to interface and border traps in the vicinity of the 2D channel.

Chapter 4 discusses the question of good insulators for 2D FETs that is at the center of this thesis. Three challenges for suitable insulators are identified. Firstly, scaling requirements, secondly, a reduction of the charge trap densities and their impact, and finally requirements for the deposition technology of gate insulators. At the end of the chapter an overview over potential gate insulators for 2D FETs is provided. This chapter is based predominantly on references [TKJ5, TKJ2, TKJ3, TKJ7].

Chapter 5 describes the experimental characterization of the electrical stability of 2D FETs. In the first part, the stability of the threshold voltage in large area 2D FETs is investigated using both hysteresis and bias temperature instability (BTI) measurements. Additionally, based on the insights obtained, a stability-based design method is proposed where the Fermi level is tuned to avoid defect bands in the gate insulators. In the second part, single charge trapping events in nanoscaled 2D FETs are studied with random telegraph noise (RTN) and time-dependent defect spectroscopy (TDDS) measurements at cryogenic temperatures. This chapter is based primarily on references [TKJ3, TKC6, TKJ15, TKJ14, TKJ16].

Chapter 6 discusses the modeling of 2D material-based FETs. In the first section, the modeling of MoS_2 FETs with a drift-diffusion based TCAD framework is described with a special focus on the modelling of the hysteresis. In the second section, the tunnel currents through scaled gate insulators for 2D FETs are evaluated with a special focus on hexagonal boron nitride. This chapter is based mainly on references [TKJ2, TKJ12, TKJ18].

State-of-the-Art Part I

2 Transistors based on 2D Materials

In 2004, Novoselov *et al.* [38] reported the observation of a field effect in the first successfully isolated 2D material. They had successfully isolated the 2D allotrope of graphite, graphene, with thicknesses ranging from a few layers down to single layers and demonstrated a sizable field effect as well as high room-temperature mobilities of about 10 000 $cm^2V^{-1}s^{-1}$. However, graphene's high mobility is linked to its lack of a band gap [41]. In general, materials with smaller band gaps tend to have higher mobilities and as graphene is a semi-metal without a band gap, its mobilities are especially high. At the same time, the band gap is essential for logic applications, since the energy gap between the valence and conduction band is what allows to switch the transistor off, giving rise to high on/off current ratios. Such a high on/off current ratio is essential for the operation of digital logic circuits, thus the lack of a band gap renders graphene FETs unsuitable for logic applications [41, 59].

Therefore, subsequent research focused on 2D semiconductors which offer a sizable band gap, among them the material group of transition metal dichalcogenides (TMDs) [60, 61]. TMDs offer large band gaps and moderate mobilities and thus in 2007-2013, the first transistor prototypes based on various TMDs were demonstrated, among them molybdenum disulfide (MoS_2) [58, 62], molybdenum diselenide ($MoSe_2$) [63], tungsten disulfide (WS_2) [64], and tungsten diselenide (WSe_2) [65]. Another 2D semiconductor with a promising outlook for nanoelectronic applications is black phosphorus (BP) [66]. In addition to the 2D semiconductors which could potentially serve as a channel material in FETs, layered insulators with an even larger band gap are particularly interesting as a substrate for 2D materials or gate insulator in a FET. Currently, hexaognal boron nitride (hBN) is considered by most to be the most promising layered insulator [67, 68].

These 2D materials are selected representatives of a large variety of several thousand compounds which possess a stable 2D variant according to theoretical calculations [50, 69]. In this chapter, methods for synthesizing 2D materials will be discussed with a particular emphasis on growth methods which are compatible with batch processing. Following the material synthesis, the process of fabricating prototypes of 2D FETs in the cleanroom will be described. These first two sections of this chapter are based on experience gained from visits of the author to the Birck Nanotechnology Center at Purdue University in 2018 and 2019. After providing an overview over the fabrication process, the formation of good contacts to 2D FETs will be discussed as this is a key challenge.

2.1 Material Synthesis and Transfer Methods

The use of 2D materials for electronic applications was discovered just over 15 years ago by using the process of mechanical exfoliation to isolate few layers and single layers of the layered compounds from they layered bulk crystals [38]. Even though this process is not scalable, it is still being widely used today for lab-based research on 2D materials due to its simplicity and the comparatively high quality of the 2D layers obtained [40]. In essence, during mechanical exfoliation a thick flake of a layered crystal is thinned down by placing it on adhesive tape and repeatedly folding and unfolding the tape several times until the flakes are placed on a SiO_2/Si wafer which serves as a substrate. Based on the interference pattern of light being reflected at the Si, the SiO_2, and the top surface, monolayer and few layer flakes can be identified under an optical microscope [61]. For a good optical contrast the SiO_2 layer is typically 270 nm or 90 nm thick, with 20 nm being the lower limit in order to be able to identify flakes under an optical microscope. This initial assessment of the layer thickness via optical contrast is required to select a few suitable flakes among thousands of unsuitable ones and can afterwards be confirmed using atomic force microscopy or Raman spectroscopy [70, 71].

Inherently, the quality of the single crystalline bulk materials, from which the layers are exfoliated, directly determines the purity and crystal quality of the 2D layers after exfoliation. For all 2D materials investigated here, several commercial vendors offer bulk single-crystals of highly-oriented pyrolytic graphite for the exfoliation of graphene or MoS_2, WSe_2, and other TMDs. Naturally, the available samples vary in purity and especially critically so in the case of hBN where the quality of available samples varies strongly. Currently, the most successful growth of high-quality hBN relies on high pressures of around 5 GPa and temperatures of up to 1650 °C [72]. Just as important as pure bulk crystals, from which to initiate growth, is the careful execution of the mechanical exfoliation process itself. Since the early demonstrations of the exfoliation of graphene [38], MoS_2 [61], WSe_2 [71], or hBN [73], the process has been further developed. Studies have shown that the number of cleavage steps when the tape is folded and opened up multiple times is critical [74], as few cleavages correspond to a small percentage of obtained monolayer flakes and too many cleavages result in too small flake areas, as the flakes also cleave along in-plane directions [75]. In order to obtain pure flakes of high-quality, organic residues from the tape should be reduced and removed with annealing steps [76]. In addition, the time-consuming process of selecting the most promising exfoliated flakes from thousands of candidates based on optical microscopy images of the sample's surface can be automated using a machine learning approach [77]. Despite all progress, mechanical exfoliation is an inherently random process where single suitable flakes have to be identified out of thousands of unsuitable flakes which do not meet the requirements regarding thickness homogeneity, size, and shape. Thus, scalable batch processes for the growth of 2D materials are required. All growth processes discussed in the next paragraphs aim for controllable and reproducible growth of high-quality 2D crystals on an industrial scale.

2.1.1 Chemical Vapor Deposition

Among the scalable growth methods for 2D materials, chemical vapor deposition (CVD) is the most widely explored. CVD is a bottom-up growth approach which offers flexibility regarding the material precursors, a fast growth rate, and a comparatively simple process. In a CVD process, 2D materials are deposited in a furnace under low pressures at temperatures which typically lie in the range of 600 °C to 1200 °C [78, 79]. In general, during CVD, growth precursor materials are evaporated, the reactants are transported with gaseous species to the substrate, where the 2D films grow in a heterogeneous surface-mediated reaction. As the CVD growth mechanism depends on the chemical structure of the grown film, the discussion focuses first on graphene and hBN, two layered materials with similar crystal structure, then reviewing CVD growth of TMDs and in the end briefly touching upon BP growth.

For the CVD growth of graphene, methane typically serves as the precursor gas in a mixture with hydrogen [80]. However, the pyrolysis of methane requires temperatures exceeding 1000 °C, thus for low temperature growth processes at about 500 °C, other carbon sources like benzene or toluene must be used, even though they typically result in more defective layers [81]. For growing hBN, the most commonly used precursors are solid ammonia borane [82] or liquid borazine [83] as they offer the required one-to-one stoichiometry of boron to nitrogen. In both cases of graphene and hBN, the growth mechanism and the resulting layer thickness depend on the solubility of the precursor atoms on the growth substrates. Copper (Cu) has been the preferred growth substrate for monolayer growth due to its small solubility for carbon, nitrogen, and boron [80, 82]. In general, the crystalline orientation of the growth substrate can be used to grow monocrystalline layers in an epitaxial growth process. In this way, larger area single crystalline graphene monolayers were grown on Cu (111) [84] or the epitaxial growth of 100 cm^2 sized monolayer single crystals of hBN was demonstrated on Cu (110) [85]. Moreover, single crystalline large area hBN monolayers have been grown on sputter-deposited crystalline Cu (111) surfaces on c-plane sapphire wafers, where hBN orients itself during growth along the Cu (111) steps [86].

However, in particular for using hBN as a substrate or gate insulator, multilayer hBN is required. For growing multilayers of graphene or hBN, metal substrates with high solubility like Ni or Fe can be used to mediate a precipitation growth mechanism [87]. In this process, boron and nitrogen dissolve in the iron substrate and precipitate to the surface to form a hBN film during the cooling of the sample. Thus, the thickness of the film critically depends on the cooling rate, resulting in thin layers for fast cooling rates and thick layers for slow rates [88]. Shi *et al.* [89] developed this approach further by using a liquid Fe-B alloy as a catalyst for epitaxial precipitation of hBN on (0001) sapphire substrates. In their vapor-liquid-solid growth approach, the liquid Fe-B catalyst promotes the dissociation of N_2 and assists the lateral growth of hBN, resulting in crystalline multilayer hBN samples with large areas.

Strategies for CVD growth of TMDs differ from the principles governing the growth of hBN and graphene. To synthesize TMDs, a vapor phase reaction of two separate precursors has been widely adopted, where in separate locations of the furnace metal oxide powders (e.g. MoO_3 or WO_3) and solid chalcogen elements (e.g. S or Se) are evaporated and then transported using a carrier gas (e.g. Ar) to the heated substrate where a TMD film grows [90, 91]. In Figure 2.1(a)

a CVD furnace in the configuration for TMD growth is shown schematically, indicating the controlled variables of the growth process, for example, temperature and pressure. Contrary to the CVD growth process of graphene or hBN, when growing TMDs the substrate typically does not serve as a catalyst, but instead, chemically inert substrates with smooth surfaces are used, i.e. SiO_2 [92, 93], mica [94], or hBN [95]. In general, the observed growth mechanism depends on the ratio of the adhesive force exerted by the substrate relative to the adatom cohesive force of the gaseous precursors. As the growth of atomic monolayers is preferred over island growth, the poor adhesion of the precursors on the chemically inert substrates is an obstacle.

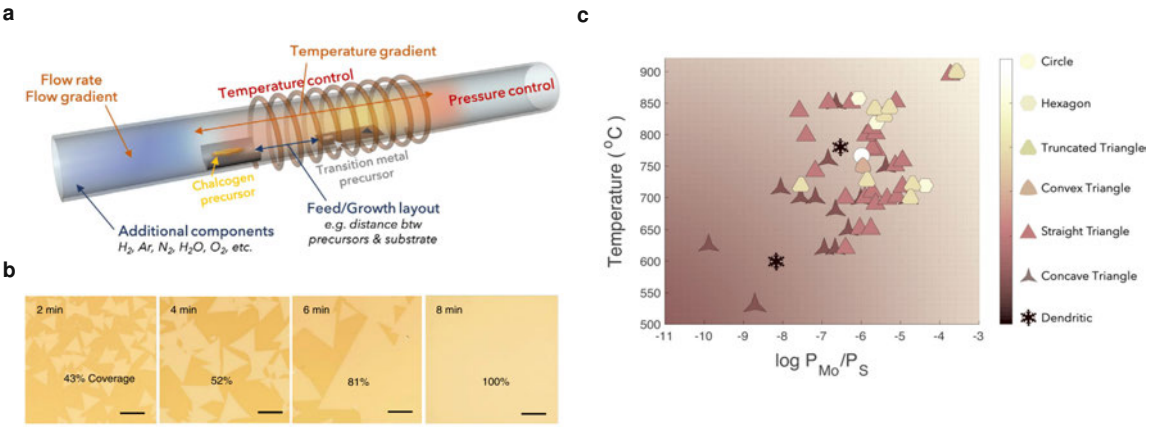

Figure 2.1. **(a)** Schematic drawing of a chemical vapor deposition (CVD) furnace for the growth of TMDs. Typically, the chalcogen precursor (e.g. S,Se) is placed upstream of the transition metal precursor (e.g. MoO_3, WO_3), close to the growth substrate. Image reproduced from [79], reprinted with permission of Elsevier. **(b)** Optical microscopy image of grown large area MoS_2 monolayers. As the growth time increases from left to right, the triangles cover larger areas of the soda-lime glass substrate with Na acting as a seeding promoter [96]. The inset scale bars measure 100 µm, image reproduced from [96]. **(c)** Overview over the reported shape of the CVD grown MoS_2 crystals for different growth temperatures and partial pressures of the molybdenum and sulfur precursor. The morphology of the MoS_2 crystals is rather point-star shaped at low temperatures in a sulfur rich environment and has the form of truncated triangles or hexagons at high temperatures in a molybdenum rich environment. Image reproduced from [79], reprinted with permission of Elsevier.

To overcome the limitation of poor adhesion, seeding promoters have been used. These seeding promoters are chemicals which bind to the surface and serve both as nucleation sites while simultaneously laterally enlarging the growth area of TMDs [90]. In 2012, Lee *et al.* [90] suggested that graphene-like organic molecules such as perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) and perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA) can promote layer growth of TMDs. While several other organic molecules have been suggested as seeding promoters, PTAS has been demonstrated to be highly effective [97]. It can promote the growth of different TMDs on various substrates [98] and has been used to grow lateral TMD heterostructures [99] and large area films for competitive FETs [TKJ16, 100]. In an alternative approach, soda-lime glass has been demonstrated to be a suitable substrate for TMD growth, as the uniformly distributed soda (Na) within the glass acts as a catalyst for the growth process. With this method, a 6 inch wide MoS_2 monolayer was grown at 730 °C [96], see Figure 2.1(b).

Despite these successful demonstrations of the CVD growth of TMD monolayers on a wafer scale, considerable challenges still remain. On one hand, the understanding of the reaction kinetics and mechanisms governing the growth process is incomplete, as important aspects of the growth are being explored [101], including nucleation, intermediate reactions, and long-range transport via diffusion. On the other hand, the relation between process variables which can be easily controlled in experiments, and the intrinsic thermodynamic processes which govern crystal growth is highly convoluted and complex [79]. For example, the distance between the crucible with the MoO_3 precursor and the substrate controls not only the MoO_x partial pressure at the substrate site, but also changes the partial pressure of sulfur as the carrier gas flow rate is changed [102]. Due to these complex relationships, 2D material growth often suffers from poor reproducibility and inconsistent results under apparently similar conditions, for example resulting in varying grain sizes. One promising route to address these problems could lie in the mapping and analysis of crystal shapes and the growth morphology depending on crystal growth parameters [79]. For instance, under a low-temperature or sulfur-rich growth conditions MoS_2 grows in a more concave point-star shaped triangle whose edges are terminated by S-zigzag edges. In contrast, in an molybdenum-rich or high temperature growth environment, truncated triangles or hexagons are formed with both Mo- and S-terminated edges, see Figure 2.1(c). Under non-equilibrium growth conditions and high gas carrier flow rates, dendritic-like growth is observed [78].

In contrast to the CVD growth of graphene, hBN, and TMDs, which has been widely explored, only few studies have investigated CVD growth of BP. There are two main reasons that render CVD unsuitable for the synthesis of BP. First, black phosphorus quickly oxidizes in the presence of oxygen, requiring an oxygen-free growth and handling environment [103], which is difficult to achieve. Second, and more importantly, CVD growth of BP would require phosphine as a precursor which is highly toxic, thus pulsed laser deposition or the direct phase transformation of red phosphorus is more suitable [104].

2.1.2 Metal Organic Chemical Vapor Deposition

Metal Organic Chemical Vapor Deposition (MOCVD) is based on a similar process as CVD but uses gaseous metal-organic compounds as precursors instead of solids in powder-form. This offers the key advantage of a precise control over the partial pressures of all precursors in the growth chamber, by introducing the precursors using mass flow controllers, see the schematic in Figure 2.2(a). With MOCVD, the growth of 4 inch wafer scale MoS_2 and WS_2 monolayers on a SiO_2/Si substrate at a growth temperature of only about 550 °C was demonstrated [93]. This growth process resulted in a polycrystalline film with a grain size on the order of µm, with the grain sizes critically depending on the H_2 flow rate, see Figure 2.2(b). Overall, this process showed excellent yield, layer uniformity, and good charge carrier mobilities [93]. However, a follow-up spectroscopic study has revealed a high density of trap states within the MoS_2 band gap [105], which needs to be reduced. Other difficulties of the MOCVD process are the comparatively small grain sizes and the long overall growth time for one monolayer of ~26 h.

In fact, the often extremely slow growth rates of MOCVD are both a disadvantage and a strength, as the slow growth allows for heteroepitaxy near thermodynamic equilibrium. In this

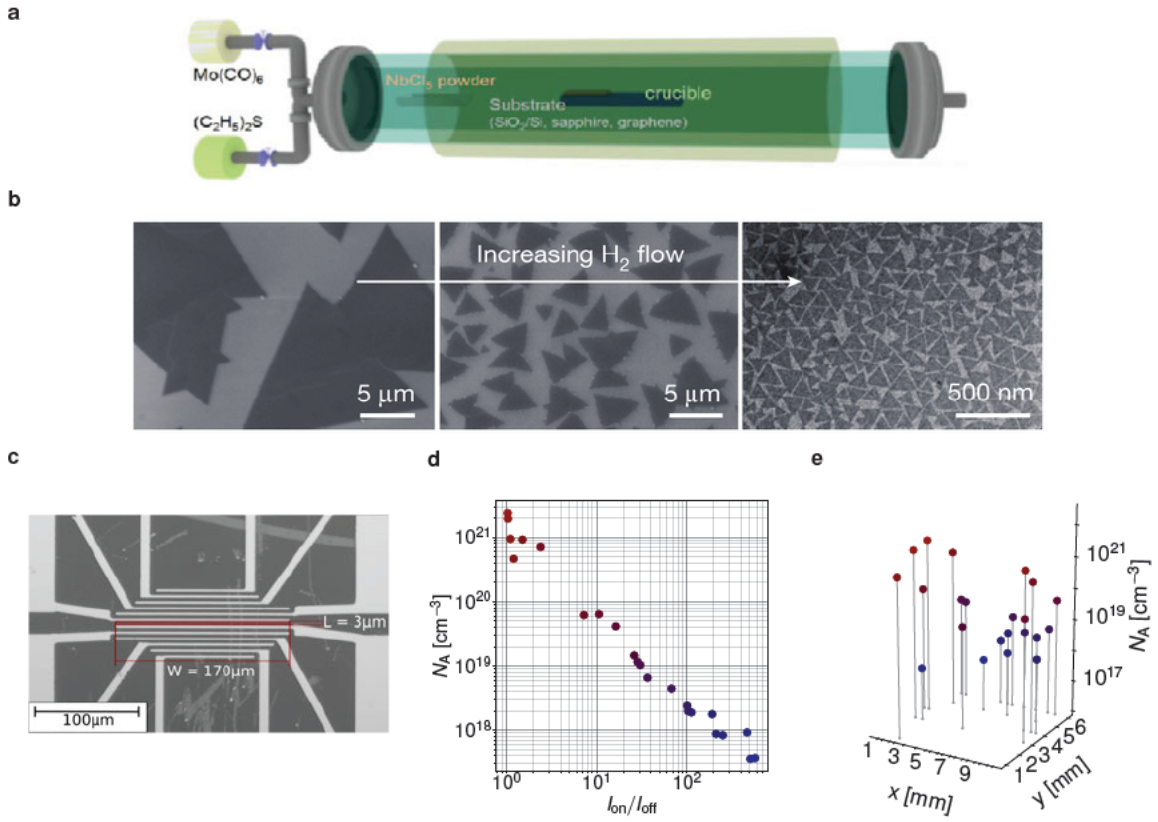

Figure 2.2. **(a)** Schematic drawing of a metal organic chemical vapor deposition (MOCVD) furnace for the growth of MoS_2 showing the mass flow controllers to the left. $NbCl_5$ powder was placed upstream to p-dope the MoS_2 layers. Image reproduced from [TKJ10], reprinted with permission of Wiley. **(b)** Scanning/ tunneling electron microscopy images (SEM for two images to the left, TEM to the right) of MOCVD grown MoS_2 monolayers, showing a grain size variation depending on the hydrogen flow rate [93]. Image reproduced from [93], reprinted with permission of Springer Nature. **(c)** To evaluate the distribution of doping in Nb-doped MoS_2 5-6 layer films, we fabricated larger area back gated FETs, showing an optical microscopy image. Image reproduced from [TKJ10], reprinted with permission of Wiley. **(d)** Based on the measured transfer characteristics of 23 FETs distributed across the 1 cm^2 MoS_2 flake grown at 650 °C, the p-doping level was calculated [TKJ10]. **(e)** Extracted approximate doping levels vary across the entire flake, with the highest doping levels close to the $NbCl_5$ precursor located to the left (at negative x).

way, the growth of coherent superlattices of WS_2 and WSe_2 with straight heterointerfaces has been achieved [106]. In addition, for MOCVD the growth temperature can be further reduced down to 450 °C to become compatible with back-end-of-line processing requirements. At the same time, the conductivity of an MoS_2 film was shown to be enhanced by p-doping the film with Niobium which renders the film suitable for applications as an interconnect liner [TKJ10]. In order to evaluate the homogeneity of the introduced p-doping, FETs were fabricated on a Nb doped 1 cm^2 MoS_2 flake grown at 650 °C. Based on the measured transfer characteristics of 23 FETs, approximate p-doping levels were calculated according to the basic device theory summarized in Appendix A. In this way, doping levels varying between 10^{17} cm^{-3} and 10^{21} cm^{-3} were obtained, see Figure 2.2(d). Considerably higher doping levels were detected to the left of the sample, close to the $NbCl_5$ powder as the dopant source, see Figure 2.2(e).

In a similar process to the MOCVD growth of TMDs, hBN can be deposited with MOCVD too, benefiting from the enhanced controllability of the process based on two gaseous precursors. Thus, MOCVD growth of hBN yields highly stoichiometric and uniform films over large areas and has been demonstrated on (111) Ni and c-axis sapphire as growth substrates [107]. Similarly to the MOCVD growth of TMDs, also these layers are polycrystalline with comparatively small grains. In summary, MOCVD offers a promising perspective of epitaxial growth on a large scale with high homogeneity and uniformity of the films at moderate growth temperatures. At the same time, future studies need to address the issue of the small grain size of the grown films. Towards this goal, several strategies have been suggested including the thermal activation of the surface reconstruction of crystalline substrates [108], the control of the partial pressures of water and H_2 during growth [93], and an elaborate temperature profile including nucleation steps prior to growth and post-growth annealing steps [108]. However, hitherto none of these approaches has succeeded in growing single crystalline layers.

2.1.3 Molecular Beam Epitaxy

In epitaxial growth methods, the crystalline information of the substrate is retained and serves as a template for crystalline growth of the 2D material. Besides CVD and MOCVD, which under ideal conditions can offer epitaxial growth, Molecular Beam Epitaxy (MBE) provides epitaxial growth on a large scale. In an MBE process, gaseous precursors are introduced in an ultrahigh vacuum chamber at a pressure typically below 10^{-10} mbar [48]. There, the precursor molecules form a film on a heated crystalline substrate. This substrate provides crystallographic information for the formation of the film and, as the substrate only needs to be crystalline and has no catalytic effect, MBE allows for direct *in situ* growth of vertically stacked heterostructures [109, 110]. As the thickness and crystallinity are monitored in an MBE process *in situ* using reflection high-energy electron diffraction, highly crystalline layers can be grown with relative ease.

In general, epitaxial growth of 2D materials differs from conventional epitaxy of 3D crystals. As 2D materials do not have dangling bonds between van der Waals layers, their surfaces are inherently passivated and they do not require strict lattice matching. Nevertheless, for growth of single crystalline layers, the substrate needs to provide the information for the alignment of the grown 2D layer. This information can be given through direct lattice matching or if commensuration conditions are satisfied [109, 111]. This process of epitaxially growing 2D materials is called van der Waals epitaxy [112, 113]. Without any alignment information, the growth on different parts of the surface will start at arbitrary crystalline orientations resulting in a polycrystalline sample [110].

MBE is a powerful tool to grow high quality films and recent demonstrations included the growth of highly crystalline $MoSe_2$ layers [110, 111], MoS_2 layers [109, 114], graphene [115, 116], and hBN [117, 118]. Additionally, *in situ* growth of van der Waals heterostructures has been demonstrated both for vertical [109, 110] and lateral heterostructures [116]. While MBE is very well suited for studies of fundamental properties of the material systems [114, 119], the reproducible and reliable growth of large-area single crystalline systems remains challenging. In addition, the high vacuum requirements and high process sensitivity to small variations

are the reasons why MBE is mostly used as a tool for fundamental research and has not yet taken hold in industrial processing.

2.1.4 Atomic Layer Deposition

In atomic layer deposition (ALD) two or more gaseous precursors are introduced in alternating pulses into the growth chamber. On the heated substrate a surface catalytic reaction takes place where subsequent reaction steps run until the surface is fully covered with a reaction product before the chamber is purged and the next precursor is introduced. Thus, an ALD process consists of partial reactions building up the material layer in a sequential, self-limiting way. This self-limiting character of ALD growth allows for the precise control of the thickness of the grown layer by the number of performed growth cycles [120]. ALD growth of various 2D materials was demonstrated, including graphene [121], hBN [122], MoS_2 [123, 124, 125], and WSe_2 [126]. These works have shown that the advantages of growing 2D materials with ALD are the inherently good thickness control [123, 126], high homogeneity of grown layers [124], and the conformal deposition on theoretically arbitrary substrates [122]. In contrast, the central disadvantage of ALD growth are the often amorphous or polycrystalline layers whose crystallinity can be improved with post annealing steps at high temperatures [121, 123]. In addition, for the growth of most 2D materials, suitable precursors have not yet been identified. The precursors used at the moment often show a limited reactivity and decompose on the heated sample surface instead of reacting with it in a surface reaction. Thus, the self-limiting component of the growth process is often missing when growing 2D materials [120, 125]. This problem is also related to the general lack of reactivity of the basal planes between adjacent 2D materials, which detrimentally affects growth and fabrication of van der Waals heterostructures [120].

This difficulty of nucleation on the inert basal planes of 2D materials also affects the nucleation and ALD growth of other compounds, such as amorphous oxides, on top of 2D materials. This is of particular importance, as ALD is used extensively in silicon technology to grow gate oxides with high permittivities such as Al_2O_3 and HfO_2. Thus, in the preferred top gated device architecture amorphous gate oxides would be grown directly on top of the 2D semiconductor serving as a channel. Towards the goal of nucleating ALD growth on top of 2D layers considerable efforts have been undertaken which can be loosely grouped in activating the surface of the 2D layer by plasma exposure [127, 128] or including a buffer/seeding layer on top of the 2D surface [129, 130]. While it seems unlikely that ALD growth will be used for the 2D material itself due to the inferior crystallinity of the obtained layers, ALD growth of gate insulators on top of the 2D layers could be key for fabricating 2D material-based MOSFETs, thus further studies on ALD growth of insulators on 2D layers are required.

2.1.5 Transfer Methods for Layered Materials

In the above discussion on the most important approaches to synthesize 2D material layers, it becomes clear that many approaches rely on a specific substrate, for example mechanical exfoliation requires a substrate of at least 20 nm SiO_2 on Si for identification under an optical

microscope, CVD growth of graphene and hBN relies on the catalytic effect of a Cu, Ni, or Fe substrate. While CVD and MOCVD growth of TMDs can be performed directly on SiO_2, the high temperature processes often introduce defects in the SiO_2, thereby degrading device stability via border traps, ion diffusion, and reduced breakdown fields. In order to avoid these problems, transfer processes suitable for large-area 2D materials are required. Such a transfer step could prove essential for fabrication of high-performance FETs, flexible electronics, or van der Waals heterostructures. Developed transfer approaches can be divided into three categories depending on their respective mechanism, mainly etchant based transfer, water based transfer, and dry transfer.

Etchant based transfer methods rely on wet etching to etch away the initial growth substrate, thereby releasing the grown 2D material. For example, a polymethyl methacrylat (PMMA) layer deposited on top of a CVD grown graphene layer serves as an intermediate carrier for the graphene layer as the copper substrate is etched away. Subsequently, the floating PMMA/graphene stack is picked up with the new SiO_2/Si substrate [131]. In order to be able to also use flexible or hydrophobic substrates which cannot be immersed in a wet etchant, a direct transfer was suggested [132]. In this direct transfer process the graphene/copper stack is laminated together with the new substrate in a polyethylene terephthalate (PET) enclosure. In this way, a tight bond between the substrate and graphene is established before the copper is dissolved in the etching step. While metal etchants are the chemicals used to release graphene and hBN layers grown on metal substrates like Cu, Ni, or Fe, 2D materials grown on insulating substrates such as TMDs require different etchants. For example, hydrofluoric acid was used to release WS_2 from the SiO_2/Si substrate [133]. A major drawback of all etchant based transfer methods is that the contact with the wet etchant contaminates the sample with metal impurities [134] which act as charge impurity scatterers and charge traps in FETs. In addition, hydrofluoric acid used for etching SiO_2 directly degrades the transferred TMD layer. Thus, the used etchant either directly attacks the transferred 2D material or introduces impurities. In order to avoid these problems the second group of developed transfer methods dispenses with the etchants and is based on water alone.

Water based transfer methods are relevant mainly for TMDs and take advantage of the weak van der Waals interaction of the TMD layer and the insulating growth substrate which is often amorphous SiO_2 or sapphire. As an example, the transfer process for CVD grown MoS_2 from a sapphire growth substrate on a new SiO_2 layer is described. In this process, the sample is coated with a polystyrene film (PS) and immersed in water. The edge of the film is slightly scratched to allow for the water to penetrate the interface between the MoS_2 and the sapphire. This penetration of water underneath the MoS_2 is assisted by the surface energy of the involved films as MoS_2 is hydrophobic while sapphire is hydrophilic [135]. This approach was used by the author to transfer MOCVD grown and Nb doped MoS_2 layers for FET fabrication during a research visit to Purdue University [TKJ10]. It has been reported that this process can be improved by pre-etching the PS covered sample with hot NaOH before immersing it in water for delamination [136]. This was adapted for the transfer of wafer-scale films by automating the previously manually performed delamination process. By using a guide rail with a step motor to slowly peel the PS/MoS_2 film from the sapphire substrate, films covering a 2 inch wafer were successfully transferred [137]. However, this process is

limited to the delamination of films from sufficiently hydrophilic substrates, like sapphire. In order to transfer TMDs from arbitrary growth substrates including SiO_2, mica and strontium titanate (STO), ultrasonification can be used [138]. In case of a perfect van der Waals surface, however, this might not be necessary, as it has been reported that high quality TMD layers grown in a low temperature MOCVD process delaminate from the SiO_2 growth substrate when dipped in water [139]. The main disadvantage of a water based transfer is that it does not work if the destination substrate is hydrophobic, flexible, or soft. In order to overcome these limitations, dry transfer needs to be used.

Dry transfer can be used to stack 2D materials on top of each other to form van der Waals heterostructures [140]. In 2011 a dry transfer was first demonstrated by exfoliating graphene onto a polyvinyl alcohol (PVA)/PMMA stack on an oxidized silicon substrate . This entire stack of exfoliated graphene/PVA/PMMA is then mechanically peeled off from the substrate and mounted onto a support frame, where the desired graphene flakes are selected and placed on the target substrate, aligning it under the optical microscope and finalizing the stack by dissolving PMMA [141]. Using this method the transferred layer will often show bubbles or ripples and impurities between the transferred graphene layer and the other 2D materials below. The process was improved by using a thermal release tape to mechanically peel off the PMMA/MoS_2 stack. This stack was introduced into a vacuum chamber where it was brought in contact with another TMD layer, ensuring a perfectly clean van der Waals interface. After the transfer the thermal release tape can be easily removed by annealing at 180 °C and subsequently dissolving the PMMA in acetone [139]. However, also in this process PMMA residues and impurities remain on the MoS_2 surface. This can be avoided in a process where only other 2D materials, usually hBN, are used to pick up and transfer 2D layers.

Wang *et al.* developed a van der Waals pick-up and transfer method where a stamp formed by a polydimethylsiloxane (PDMS) film, covered with a layer of polypropylene carbonate (PPC), first picks up an hBN flake and then other 2D layers [142]. In this process the PDMS/PPC/hBN stamp is mounted in a micromanipulator where it is aligned to the desired flake below. Then the stamp is lowered until the hBN contacts the target flake. Because of the layers' atomically flat surfaces, the contact area and the resulting van der Waals adhesion forces are large resulting in the lifting of the 2D material together with the hBN. The entire stack is then placed on a target substrate where it is gently released from the PPC layer. This process is comparatively complex but results in ultra-clean van der Waals interfaces between the layers, especially if the stacking is performed inside a glove box, minimizing charge impurities which act as scattering centers [40]. In addition, Jung *et al.* have suggested that when creating source and drain contacts directly on top of 2D layers, impurities and scattering centers are introduced, which can be avoided by using a transfer of pre-patterned via contacts [143]. This idea concerns a central part of the device fabrication of 2D material-based FETs, namely the formation of source and drain contacts, which is discussed in detail in the next section.

2.2 Device Fabrication

In the following, the process of fabricating devices will be described, starting from a film composed of a monolayer or few-layer 2D semiconductor on the target substrate. Depending on the FET layout the substrate can act as a gate oxide and gate contact for back gated devices or as a mere support layer which aims to minimize charge carrier scattering. In general, 2D material-based FETs can be classified according to their layout. At the present state-of-the-art Schottky barrier based FETs with undoped contact areas dominate the field of 2D FETs and comprise all devices investigated in this work. The operating principles of Schottky barrier based FETs will be detailed in the next Section 2.3, but the fact that Schottky barriers are the defining component which switches 2D material-based FETs on and off is important for the device layout. Under this premise, five categories of widely used device layouts can be introduced: back gated devices with a bare channel, back gated devices with an encapsulated channel, encapsulated devices with a local back gate, top gated devices without contact gating and top gated devices with contact gating. For a schematic comparing the cross section through these five device layouts, see Figure 2.3.

The first 2D material-based FETs used the back gated device layout, as it involves the fewest fabrication steps [61, 62]. In addition, with this layout it is easiest to reduce device dimensions down to the nanoscale [TKJ14] with device demonstrations reaching a channel length of only ~1 nm when using a carbon nanotube for gating [148]. Encapsulation of the devices with an additional dielectric layer on top of the semiconducting channel is required to render the devices insensitive to the impact of the surrounding atmosphere [40, TKJ16]. This is of particular importance for black phosphorus which oxidizes when exposed to an oxygen-containing environment [TKJ17, 149]. In order to fabricate integrated circuits based on 2D FETs, adjacent prototype devices need to be addressed with separate gates which is impossible in the basic back gated design, where a global back gate simultaneously gates all FETs. Thus, local back gates are required for separate gate control of adjacent FETs. Such devices have been used for demonstrations of microprocessors [144] and analogue amplifiers [145]. A top gated device design also allows to selectively address neighboring devices [58, TKJ15, 146] and while the conventional layout suffers from high Schottky barriers with little tunability of the barrier height resulting in high contact resistances and low on-currents, a design with gated contact areas avoids these problems [147]. Out of the discussed five device layouts, the encapsulated layout with a local back gate (layout c) or the top gated layout with contact gating (layout e) are expected to provide the best performance.

Here, we will describe in detail the device fabrication of MoS_2 FETs with a global back gate of varying dimensions which were used for the studies [TKC6, TKJ14] and fabricated as part of the work leading up to this thesis at the Birck Nanotechnology Center. The steps described here can be adapted and complemented with further fabrication steps such as ALD growth, to fabricate all of the device layouts described in Figure 2.3. In a back gated layout the substrate where the layered semiconductor, e.g. TMD, is placed upon serves as a gate oxide. Thus, either the substrate used for the mechanical exfoliation or 2D layer growth can be used directly as gate oxide or, alternatively, the layered semiconductor can be transferred to the intended target substrate with one of the methods discussed in Section 2.1.5. For flakes originating from

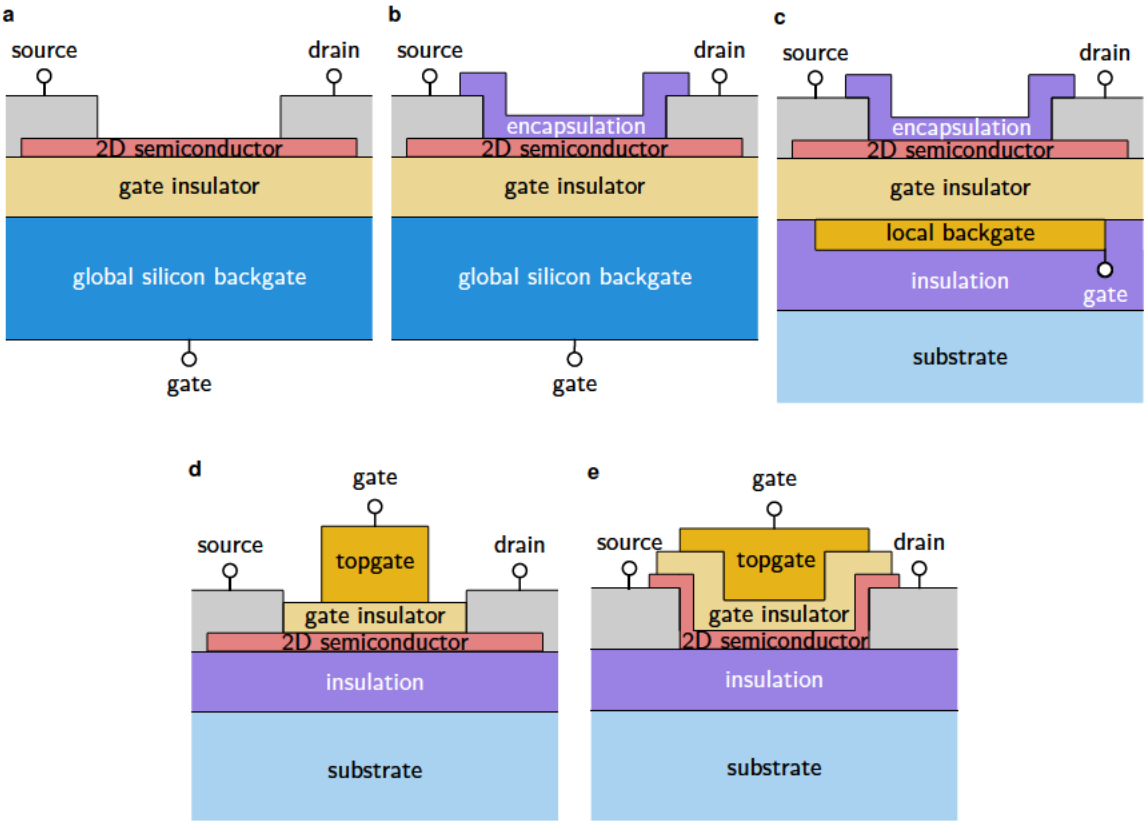

Figure 2.3. **(a)** Schematic drawing of a back gated 2D FET with a bare semiconducting 2D material as a channel. A silicon wafer serves both as a substrate and as a global back gate for all devices on the chip. This layout was used for example in [58, 61, TKJ21]. **(b)** Back gated 2D FET with an encapsulated channel which is protected from the ambient by an encapsulation layer, again all devices share a common global back gate [40, TKJ17]. **(c)** Cross section through an encapsulated 2D FET with local back gate. Every FET is gated by its own buried metal electrode, which allows for the fabrication of integrated circuits, as demonstrated in [144, 145]. **(d)** Top gated FET based on a 2D semiconductor in the more common design without contact gating, resulting in elevated contact resistances. This design was used for example in [58, TKJ15, 146]. **(e)** Cross section through a top gated 2D FET with gated contact regions allowing for full control of the Schottky barriers at the contacts, see [147].

mechanical exfoliation the lateral dimensions are typically limited with areas on the order of $\sim 50\,\mu m^2$. For flakes grown by CVD or other methods as described in Section 2.1, the channel material covers the entire substrate with lateral dimensions of typically $\sim 10\,cm^2$. Thus, for grown 2D layers, contacts can be patterned with optical lithography using predefined masks of a standardized layout. For mechanically exfoliated layers, on the other hand, the flakes are randomly distributed across the surface, This, in addition to their small size requires electron beam lithography to fabricate source and drain contacts. Besides, electron beam lithography can fabricate line widths and pitches as small as 20 nm while traditional optical lithography is limited to around 1 µm, setting in this way lower limits for the dimensions of the manufactured FETs. For a well defined channel area, which is of special importance for realizing small device dimensions, the 2D material needs to be patterned using for example plasma etching as detailed in the following Section 2.2.1. For basic investigations of the FET it is sufficient to directly pattern source and drain leads on top of the 2D layer with a high

W/L ratio, thereby ensuring that even under elevated drain biases the electric response is dominated by a homogeneous electric field between source and drain, avoiding electric stray fields. In this case the channel length is defined by the distance of the parallel source and drain leads, while the width of the device can only be approximated as the length of the parallel leads.

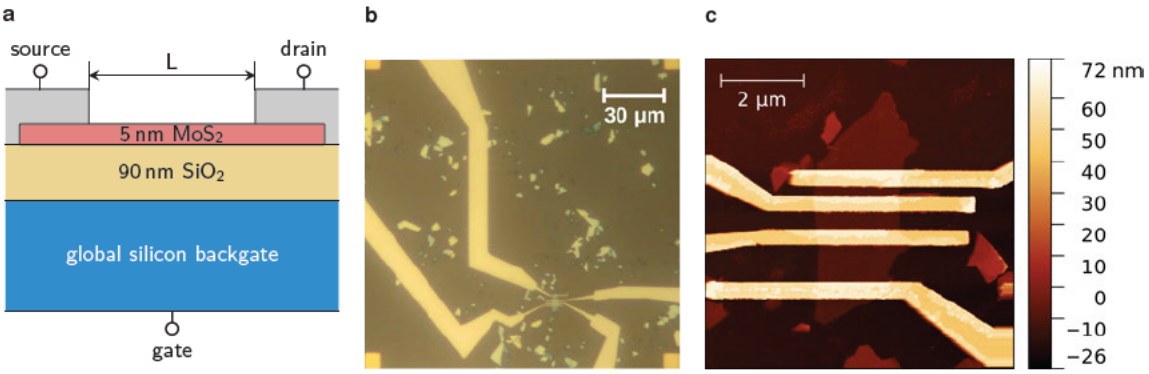

Figure 2.4. **(a)** Schematic drawing of the cross section through a back gated FET with few layers of MoS_2 serving as a bare channel. **(b)** Optical microscopy image of three exemplary device prototypes fabricated on a single few-layer MoS_2 flake with different lengths at 300 nm, 500 nm and 1 µm. **(c)** AFM image of the three MOSFETs on the exfoliated MoS_2 flake, showing the top view of the fabricated FETs.

Metal leads and pads for source and drain contacts are patterned using a lift-off process, explained here for the example of electron-beam lithography. On top of the 2D material an approximately ~ 160 nm thick layer of PMMA resist (e.g. A4-950) is deposited by spin coating at a high rotational speed of 6000 rpm. This layer of resist is patterned by exposing it to a focused electron beam at an electron dose of 200 µC/cm^2 which locally splits up the PMMA chains making them soluble in the developer solution (e.g. a 3:1 mixture of isopropyl alcohol and ultra pure water). The metal is deposited on top of the developed pattern, for example 65 nm Ni in an electron beam evaporation process. Subsequently, the PMMA is dissolved in acetone, lifting off the metal film wherever it is not directly attached to the sample surface. For the exemplary batch described here the schematic cross section is shown in Figure 2.4 (a), an optical microscopy image and an AFM scan of one prototype is shown in Figures 2.4 (b) and (c). For these prototypes the channel widths result from the shape of the exfoliated flakes and are on the order of several µm while the lengths, determined by the distances of the deposited metal leads, are varied from 300 nm, 500 nm to 1 µm. In order to fabricate devices with well defined widths and/or to scale down the device dimensions, the 2D material needs to be etched with one of the methods described in the next subsection.

2.2.1 Etching 2D Materials

In order to pattern 2D materials, processes are required to locally etch areas directly exposed to the etchant while preserving the material underneath an etch mask. The etching process should neither damage the 2D material nor contaminate it with residues. First, an etch mask is deposited on the 2D film and patterned laterally using lithography. For the sake of simplicity, often the lithographic resist is directly used as an etch mask, as a metal hard mask would

require a subsequent mask removal step and is a potential source for impurities. In the next step the sample is exposed to the etchant which etches away the unmasked areas of the 2D material. Then the mask is removed, resulting in a laterally patterned 2D material. When etching 2D materials the efficiency of the etch process is not important as the material to be etched is thin. What is critical, however, is to pattern the 2D film at a high resolution and a high anisotropy, thereby avoiding modifications and under-etching of the 2D material and minimizing impurities originating from the etch mask [150]. For special applications it is required to thin down layered 2D semiconductors in a layer-by-layer manner, thereby tuning for example the band gap of the material. These atomic layer etching (ALE) techniques require well controlled etch processes [151, 152].

In general, three categories of etch processes can be distinguished, wet chemical etching, reactive gas etching, and plasma etching which is also termed reactive ion etching (RIE). Wet chemical etching is carried out by submerging the entire sample into a liquid solution which etches away the exposed material. This method has been used to etch away MoS_2 [153] but shows highly isotropic etch rates and residues from the wet etchant which contaminate the remaining film. Reactive gas etching suffers from similar drawbacks. While exposure to a reactive gas such as XeF_2 [154] or O_2 [155] at elevated temperatures effectively removes unmasked 2D material, it also often degrades the remaining 2D layers.

In comparison, plasma etching or RIE offers many advantages over other etching methods which makes it the most commonly used method. In a RIE system a plasma is generated by capacitively or inductively coupling electromagnetic fields to the precursor gases. This plasma is ignited either directly in contact to the sample in direct plasma systems or at a small distance from the sample in a remote plasma system which offers the advantage of tuning the ion flow to the sample by an additional parameter, namely by the bias voltage between the plasma and the sample. RIE systems provide highly anisotropic etching and allow for good control over the processing conditions. These conditions are governed by the process parameters, in particular the mass flow rates of the etch gases, the overall gas pressure during the process, the source power for creating the plasma and the etch time. For etching TMDs several etch chemistries have been used, among them a pure Argon (Ar) plasma [156], an SF_6 plasma [157, 158], a remote O_2 plasma [TKJ16, 159], and combinations of several atomic species forming for example an SF_6 +N_2 [160], an SF_6+Ar [TKJ14] or a Cl_2 +O_2 plasma [161]. In this work we tested these last two etch chemistries for etching MoS_2 using a structured PMMA layer as a mask and compared these two etch processes with regards to the respective etching rates and the residues on top of the remaining MoS_2 after mask removal.

In the first process we etched multilayers of MoS_2 in a plasma formed by 10 sccm SF_6 and 10 sccm Ar at a pressure of 3 Pa. The plasma was ignited at a radio frequency (RF) source power of 50 W with the ions being accelerated towards the sample at a RF bias power of 50 W for 40 s, adapted from [TKJ14]. While the MoS_2 is successfully etched away, the high energetic impact of Ar ions on the PMMA mask creates a hardened PMMA layer on top of the PMMA which becomes insoluble to the acetone used to remove the PMMA mask after the etching process. In Figure 2.5 (a) an AFM scan of an etched MoS_2 flake is shown from which the MoS_2 etch rate was calculated to amount to 0.77 nm/s, thus approximately one layer per second is

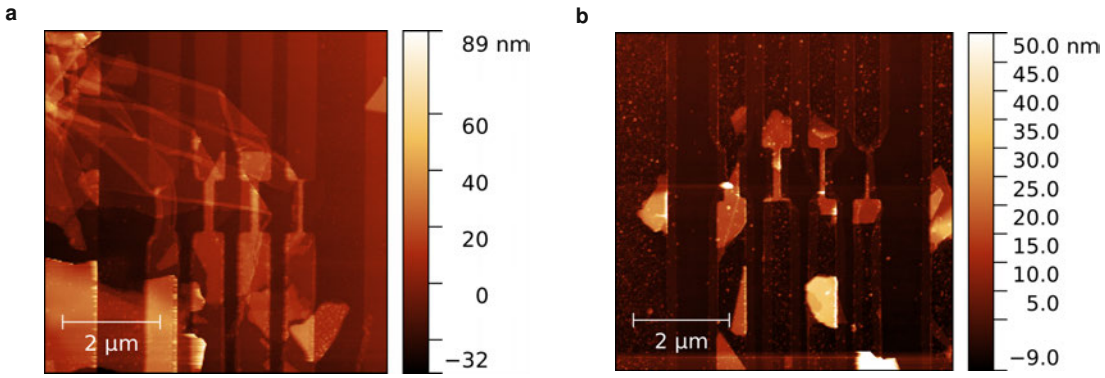

Figure 2.5. **(a)** AFM scan of an exfoliated multilayer MoS_2 flake patterned using remote RIE etching with an SF_6/Ar plasma where residues of the PMMA mask are clearly visible. The process parameters used were 10 sccm SF_6, 10 sccm Ar at a pressure of 3 Pa, an RF source power of 50 W, an RF bias power of 50 W for 40 s. **(b)** AFM image of an exfoliated multilayer MoS_2 flake patterned using remote RIE etching with a Cl_2/O_2 plasma. The process parameters used were 15 sccm Cl_2, 5 sccm O_2 at a pressure of 3 Pa, an RF source power of 40 W, an RF bias power of 40 W for 50 s.

etched away. However, a hardened PMMA residue is visible at a thickness of about 10 nm that could not be removed.

In the second process MoS_2 multilayers were etched in a plasma formed by 15 sccm Cl_2 and 5 sccm O_2 at a pressure of 3 Pa at an RF source power of 40 W and an RF bias power of 40 W for an etch time of 50 s, adapted from [161]. In this process chemistry the presence of oxygen ions prevents the hardening of PMMA, resulting in nearly no remaining PMMA residue at a thickness < 3 nm after mask removal in acetone, see the AFM scan in Figure 2.5 (b). At the same time the process resulted in a similar etch rate of 0.69 nm/s, thus also approximately one monolayer per second is etched away. Due to the smaller residue this process was used for fabricating the nanoscaled MoS_2 FETs used in [TKC6].

Nevertheless, even if the visible PMMA residue is smaller when using a Cl_2/O_2 plasma compared to the SF_6/Ar plasma, other studies have shown that reactive oxygen species in the plasma can result in the partial oxidation of the remaining MoS_2 films [159] or that Cl atoms can be included in the remaining MoS_2 films [162]. Thus, it is expected that small quantities of the plasma compounds might be included in the remaining MoS_2, in particular at the edges of the masked areas, acting as charge scattering centers and reducing the conductivity of the MoS_2 layer. These problems are particularly harmful if the TMD in the unmasked parts should not be completely removed but only selectively thinned down layer-by-layer, using for example alternating etching steps in a Cl_2 and an Ar plasma [152, 162]. Therefore, in these ALE processes, the inflicted damage on the underlying unetched film needs to be carefully monitored and ideally mitigated by reducing the ion energies [158, 160] or performing re-sulfurization or annealing steps after the etching [159]. In this way, one comes closer to the aim of patterning 2D semiconductors into small areas, while simultaneously minimizing the amount of additional impurities created through etching, thereby allowing for 2D based FETs with a scaled down active channel area.

2.2.2 Scaling the Channel Area in 2D Transistors

In general, for the fabrication of nanostructures two approaches can be distinguished, namely top-down and bottom-up processing. Top-down processes start from macroscopic dimensions and use tools which operate at the nanometer scale (for example electron beams) to pattern materials. In contrast, bottom-up approaches use the self-alignment of molecules at the nanometer scale to fabricate nanometer-sized structures, such as for example during the growth of carbon nanotubes (CNTs) [163]. Here, we will focus mostly on the top-down method for fabricating nanoscaled 2D FETs, as it is more straightforward to apply and more compatible with industrial processing. At the end of the subsection, some general tricks and elements from bottom up approaches which have been successfully used to overcome the inherent size limitations of top down processing will be discussed.

In university cleanrooms, electron beam lithography is used to pattern structures at the nanoscale. In the following, we will describe the process flow used by the author [TKC6, TKJ14] for the fabrication of back gated devices at nanosized dimensions. Starting from a 2D material on top of the substrate which serves as a global back gate, an electron beam lithography step is used to define the device width and the source and drain contact areas. In this first electron beam lithography step, the areas around the designed channel are opened where the 2D material is subsequently etched away, as described in the previous Section 2.2.1. In a second electron beam lithography step the metal contacts are patterned using a lift-off process in a FET design which targets nanoscale dimensions, where the distance between the metal fingers defines the device length, see the SEM image of an exemplary device in Figure 2.6(a).

In order to successfully pattern structures at the nanoscale using electron beam lithography, the electron beam needs to be carefully adjusted and calibrated. In particular, a dose test is required to optimize the electron dose for the respective thickness of the PMMA and the designed pattern [164]. In a dose test, several test structures are written next to each other, varying both the pattern's dimensions and geometries as well as the exposure dose. After the resist development a thin metal layer is deposited and lifted off, forming the structures which are subsequently inspected by SEM, see the image in Figure 2.6(b). In addition, any electron beam design aiming at nanometer dimensions needs to take proximity effects into account. This means that during the design process it needs to be taken into account that the local electron dose at every point also depends on the scattering of electrons from neighboring structures, thus it is impossible to pattern thin lines and line pitches in close proximity to large pads. As a consequence, for nanoscaled devices, the electron dose for both lithography steps was carefully adjusted and the lateral design accounted for proximity effects, which motivated for example the additional thin MoS_2 stripes next to the actual channel, shown in Figure 2.6(a).

For good electrostatic control over the channel at a channel length below 100 nm also the gate oxide thickness had to be scaled down. For this purpose either a thermally grown 20 nm SiO_2 on top of the silicon wafer can be used, or alternatively, a locally gated FET design can be employed which relies on a thin layer of the high-k dielectric HfO_2. For our nanoscaled devices based on thin HfO_2 [TKC6], back gate electrodes consisting of 2 nm Cr and 6 nm Au

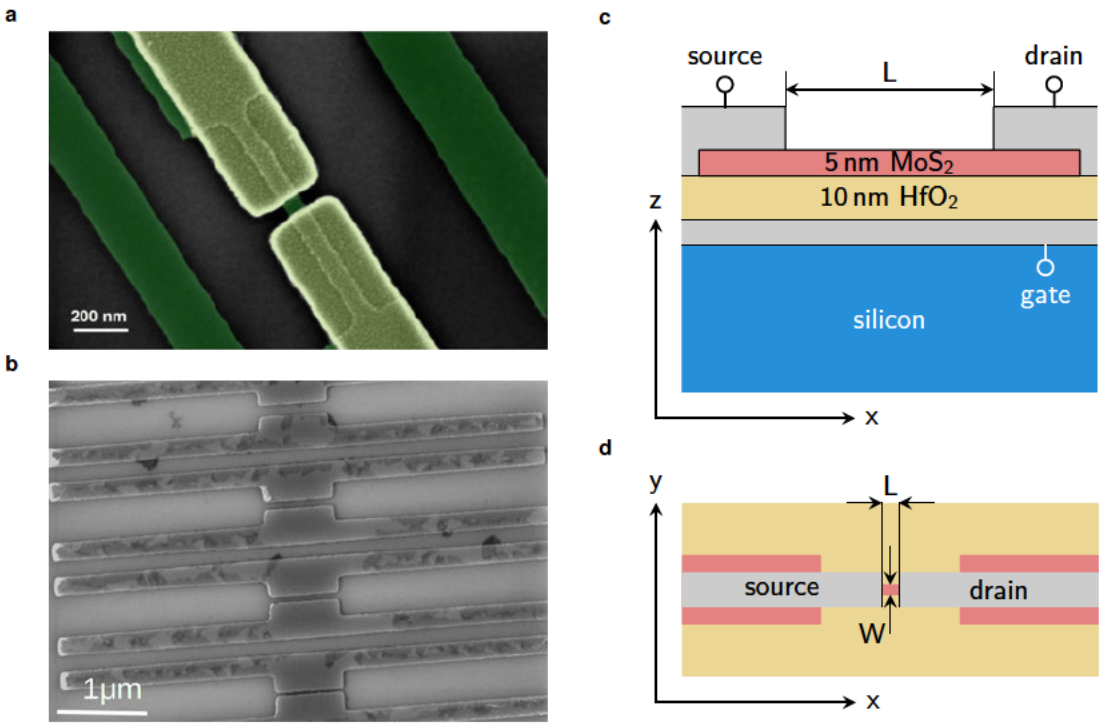

Figure 2.6. **(a)** SEM scan of an MoS_2 device with a 50 nm channel length and 50 nm channel width, regions colored in dark green are covered in few-layer MoS_2 and the light green areas are Ni contacts. [TKJ14] **(b)** SEM scan of a dose test for the etching pattern. In the darker areas a thin metal film indicates where the MoS_2 would be exposed to the plasma for removal. The dark flakes are PMMA residues due to under exposure. **(c)** Schematic of the cross section through nanoscaled devices using a thin ALD HfO_2 as a local back gate. **(d)** Schematic top view of the nanoscaled device design used, this structure can be compared with the SEM image shown in (a).

are evaporated on top of the SiO_2 substrate. Subsequently, 10 nm HfO_2 are grown using ALD at 200 °C, covering the gate electrodes and the entire sample surface. On top of this gate stack the 2D material is deposited via mechanical exfoliation or via layer transfer and then the same steps as described above are repeated to structure the channel and deposit source and drain contacts. Schematics of these locally back gated devices can be seen in Figures 2.6(c) and (d).

For the MOSFETs which were designed and fabricated for the studies presented here, the device widths and lengths reached down to 50 nm [TKC6, TKJ14]. When aiming for smaller dimensions, a number of measures could be taken to further optimize the electron beam lithography process. Besides the critical factors already mentioned, a well adjusted electron dose and a carefully designed writing pattern, a PMMA residue of lower anisole fraction, an adaptive dose pattern, or a decrease in the development temperature of the PMMA could result in smaller structures. However, these changes would be expected to provide only little improvements towards smaller dimensions, while by using a different electron beam lithography system with a higher acceleration voltage of 100 kV instead of the 30 kV used here, the feature size could probably be decreased even further. Nevertheless, the minimal dimensions which can be attained are limited to about 10 nm. This is a fundamental limit set by the optical bending and scattering of the electron beam and by the locality of the bond breaking and the solubility of the PMMA resist. Interestingly, this lower limit of the lateral

feature size attainable under laboratory conditions in academic research is about the same as the minimum feature size of extreme ultraviolet lithography used by industry for ultrascaled devices, as can be seen from the IRDS roadmap where the gate length levels off at a minimal gate length of 12 nm for the technology nodes of 2 nm and beyond [21].

Monolayer MoS_2 transistors of a gate length of only 10 nm have been demonstrated in 2016 by English *et al.* [51]. For achieving these small dimensions they used the self alignment of source and drain contacts with respect to the top gate. Thus, after defining the channel width of 1 µm by etching, a narrow (~20 nm) Al electrode is patterned on top of the MoS_2 band. This electrode serves as a top gate and forms a 5 nm self-passivating surface oxidation layer around the entire electrode which forms the gate dielectric of the FET. In the next step, a 10 nm Au film is evaporated in high vacuum over the entire structure [36] which forms self-aligned source and drain contacts with a small underlap of about 10 nm, separating the contacts from the gate dielectric. Thus, while the gate length of these FETs amounts to only 10 nm, the entire channel length measures about 30 nm and the contact lengths measure about 300 nm. A transmission electron microscopy image of the structure is shown in Figure 1.2(c). In comparison, using a back gated device design based on MOCVD grown MoS_2 and Ni contacts, recently devices with a channel length of 30 nm and a contact length of only 13 nm have been reported, which also demonstrate a small overall device area with a channel width of 135 nm [165].

Up to now the smallest gate length ever reported for 2D material-based FETs amounts to only 1 nm and was realized by using a metallic single-walled CNT as a back gate electrode [148]. Here, the device fabrication involved the manual characterization and alignment of the metallic CNT before the deposition of ZrO_2 serving as a back gate dielectric and the subsequent transfer of the exfoliated MoS_2 flake, thus the fabrication process is clearly not scalable. These FETs achieved an impressive subthreshold swing of only 65 mV/decade, but it should be noted that the overall channel length is considerably larger than the gated length at about 200 nm and the device width amounted to about 2 µm. Thus, despite the larger channel length, the rectangular channel area means that the devices fabricated and studied in [TKC6, TKJ14] are to our knowledge among the 2D MOSFETs with the smallest overall device area, measuring here about 0.0025 μm^2, similar to the areas of 0.004 μm^2 from [165], and orders of magnitude smaller than 0.03 μm^2 [36] and 0.4 μm^2 [148]. For all MOSFETs based on 2D semiconductors and in particular for those with nanoscaled device dimensions, challenges related to the formation of contacts often limit the overall device performance, thus these challenges are briefly discussed in Section 2.3.

2.3 Contacts to 2D Transistors

Contacts are the communication link between 2D semiconductors and the three-dimensional world. However, it is exactly this interface which often considerably reduces or even limits the overall current flow through the 2D channel in the MOSFET. In addition, also for conventional silicon technologies the contact resistances in nanoscaled MOSFETs become increasingly difficult to control. As the current increases in scaled devices, the continuing demand for

lower resistances for simultaneously reduced contact areas poses an enormous challenge. In the IRDS roadmap the total parasitic series resistance (R_{SD}) for the current technology node amounts to 285 Ωμm and a reduction of this value by 15 % in every node cycle, thus every 2-3 years, is targeted [21]. For silicon transistors, this overall parasitic series resistance can be decomposed into $R_{SD} = 2R_C + 2R_A$. In this expression, the factor 2 stems from the contributions of the source and drain, R_C denotes the contact resistance, and R_A is the access resistance which comprises contributions from the accumulation layer, the spreading resistance, and the sheet resistance. Consequently, even for the optimistic assumption of a negligible access resistance, a contact resistance $R_C < 140\,\Omega\mu m$ needs to be achieved. However, for 2D materials of all the contact resistances reported in literature only few come close to this target, most missing it by at least one order of magnitude, see the comparison of different published values in Figure 2.7 (a).

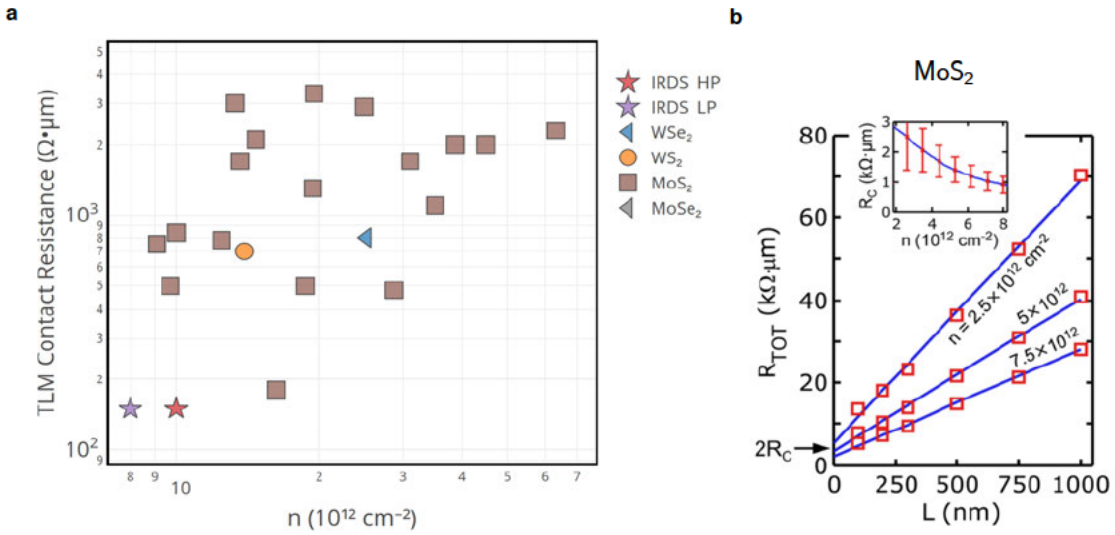

Figure 2.7. **(a)** Comparison of contact resistances reported in literature for different transition metal dichalcogenides, revealing a variation over about two decades with most values being one order of magnitude higher than the IRDS targets. All values summarized here were measured by applying the transfer length method. Figure reproduced from [166]. **(b)** TLM measurement data of the contact resistance as recorded on MoS_2. Here, the overall resistance R_{TOT} is measured for devices of different lengths on the same MoS_2 film for different overdrive voltages and thus charge carrier densities. For every charge carrier density the total resistances measured on six FETs with different L are connected with a straight line where the intercepts with the y-axis at $L = 0$ nm determine $2R_C$ which is shown in the inset. Figure adapted with permission from [36]. Copyright (2016) American Chemical Society.

In general, there are two different approaches for measuring the contact resistance, a four-probe measurement or a transfer length method (TLM) measurement. In a four probe measurement a wide channel is fabricated with two large contacts at the end and two small voltage probes next to each other, to one side of the wide channel probing the voltage at different channel lengths. In the ideal case, these small voltage probes act as sense electrodes and allow for an accurate measurement of the channel resistance by $R_{CH} = (V_1 - V_2)/I_{BIAS}$. This channel resistance is then used to calculate the contact resistance by subtracting it from the total resistance $2R_C = R_{TOT} - R_{CH}$. In a TLM measurement also a wide and long

channel is fabricated but many (ideally more than 8) contacts are fabricated across this same channel at different distances, forming many FETs next to each other with varying channel lengths. For these FETs the total resistances are plotted as a function of the channel length for different applied gate voltages and thus different charge concentrations in the channel, see Figure 2.7 (b). From the intercept of the linear extrapolations of these curves with the y-axis at a channel length $L = 0\,\text{nm}$ the value of $2R_C$ is extracted. In the inset of Figure 2.7 (b) it can be seen how the contact resistance increases for smaller charge densities in the channel, thus for smaller overdrive voltages. In comparison to a TLM measurement, a four probe measurement has been reported to give inaccurate results. In particular, if the assumption that the current flow is not disturbed by the two sense electrodes is violated, a four probe measurement can severely underestimate the contact resistance. Thus, for successful four probe measurements it is of paramount importance that the sense electrodes only touch the channel on the side and show a considerably smaller contact area than the other contacting electrodes. In general, it can be concluded that for these systems, with often highly resistive channels, in particular for wide channels of a large area, the TLM measurement provides more accurate results [36].

To date, the best contact resistance values reported for 2D materials are $180\,\Omega\mu\text{m}$ for n-channel monolayer MoS_2 after the channel was strongly n-doped via surface charge transfer doping (SCTD) [167]. Comparable results yielding a contact resistance at the same order of magnitude of $240\,\Omega\mu\text{m}$ have been demonstrated with phase engineered contacts where the metallic 1T phase of MoS_2 was used to form contacts to the semiconducting 2H MoS_2 used as a channel [168]. Using a similar contacting approach, a 2D material was connected with another 2D material to form low resistive contacts to WSe_2, resulting in a p-type MOSFET with high drive currents. Chuang *et al.* demonstrated that substitutionally p-doped WSe_2 obtained by replacing tungsten with niobium serves as a good contact material to pristine WSe_2 forming the channel, obtaining a contact resistance of $300\,\Omega\mu\text{m}$ [169]. It should be noted that most contacts to 2D semiconductors show considerably higher contact resistances. While a comparatively small contact resistance of $750\,\Omega\mu\text{m}$ was obtained for Au contacts deposited in ultra-high vacuum at 1×10^{-9} Torr [36], most other approaches like an hBN interlayer [170], transferred contacts or Nickel contacts to MoS_2 result in typical contact resistances of $1.8\,\text{k}\Omega\mu\text{m}$ [170], $3.5\,\text{k}\Omega\mu\text{m}$ [143] and $1.7\,\text{k}\Omega\mu\text{m}$ [165] respectively, see Figure 2.7 (a) for a comparison of more than 25 literature values [166].

2.3.1 Impact of Schottky Barriers

One fundamental challenge towards achieving low contact resistances to 2D semiconductors arises from the formation of Schottky barriers (SBs) at the metal to semiconductor interface. Quite generally, at every interface of a metal to a semiconductor a Schottky barrier forms, unless either the semiconductor is degenerately doped or the metal work function of the metal contact ensures that the Fermi level in the metal is aligned within the conduction or valence band of the semiconductor resulting in a negative Schottky barrier. In silicon technology, Schottky contacts are typically avoided by using highly doped n or p contact regions to form Ohmic contacts together with silicides. However, the general lack of well controllable, sustainable, and stable doping schemes for 2D materials result in the omnipresence of SBs

in prototype 2D MOSFETs [171]. For any combination of a metal with a semiconductor the Schottky barrier ($\Phi_{SB,n}$) can be calculated according to the following expression [172]

$$\Phi_{SB,n} = S\left(\Phi_M - \chi_S\right) + (1-S)\,\Phi_{IS}. \tag{2.1}$$

Here, Φ_M denotes the metal work function and χ_S gives the electron affinity of the semiconductor, defined as the difference between the conduction band edge energy of the semiconductor and the vacuum energy level, thus the difference describes the theoretical difference of the Fermi level in the metal and the conduction band edge in the semiconductor. In the second term Φ_{IS} is the semiconductor interface state energy which is located in vicinity to the charge neutrality level if the interface states arise from metal induced gap states and are thus located in the band gap. The respective relevance of both terms is given by the Schottky pinning factor S which can be calculated from measured Schottky barrier heights, according to $S = \partial\Phi_{SB,n}/\partial\Phi_M$. The pinning factor S is a material parameter of the semiconductor and its interface. For $S = 1$ the barrier heights are determined by the Schottky limit and for $S = 0$ they are given by the Bardeen limit.

While in general all metal/semiconductor interfaces fall in between these two limiting cases, metal contacts to 2D semiconductors are typically closer to the Bardeen limit which is described as strong Fermi level pinning. When comparing the extracted SB heights on multilayer MoS_2 for metals of different work functions it can be noted that in MoS_2, the metal Fermi levels pin close to the conduction band edge, thus n-type FET behavior is observed independent of the contacting metal. In Figure 2.8 (a) the band gap of bulk MoS_2 is shown together with the measured alignment of metal Fermi levels and the theoretical alignment of the metal work functions in the Schottky limit [171]. Based on the measured SB heights for Sc, Ti, Ni, and Pt contacts to bulk MoS_2 [173] as well as for Ag [174], W [175], Co [176], Au [177], and Al contacts [178], a Schottky pinning factor of about 0.1 was determined for MoS_2 [171], see Figure 2.8 (b). In contrast, for WSe_2 the metal Fermi levels pin closer to the middle of the band gap leading to ambipolar device behavior where both the electron and hole branch of the current are visible [179]. Consensus on the origin of the Fermi level pinning in 2D semiconductors like MoS_2 has not yet been reached [171] but several physical mechanisms have been identified as contributors to the Fermi level pinning. Metal Fermi levels pin when contacting MoS_2 because elemental impurities and metal-like defects in the MoS_2 form underneath the metal contacts [180]. Also, nanoscale metal grains can cause inhomogeneities and local strain in the 2D layer [181] which can cause Fermi level pinning as well as the observed local charge redistribution and interface dipole formation at the metal semiconductor interface [182]. In addition, the typically used evaporation process for contact formation has been shown to locally damage the 2D semiconductor underneath, thus paving the way for reactions between the contact metal and the semiconductor, which cause Fermi level pinning [143]. In order to find ways to reduce Fermi level pinning, it is important to first understand the mechanisms which govern it. Fermi level pinning makes it highly difficult to effectively eliminate SBs by designing negative SB heights and to create both and n- and p-type FETs based on one 2D material, in particular for 2D semiconductors like MoS_2, where the Fermi level pins close to one of the band edges.

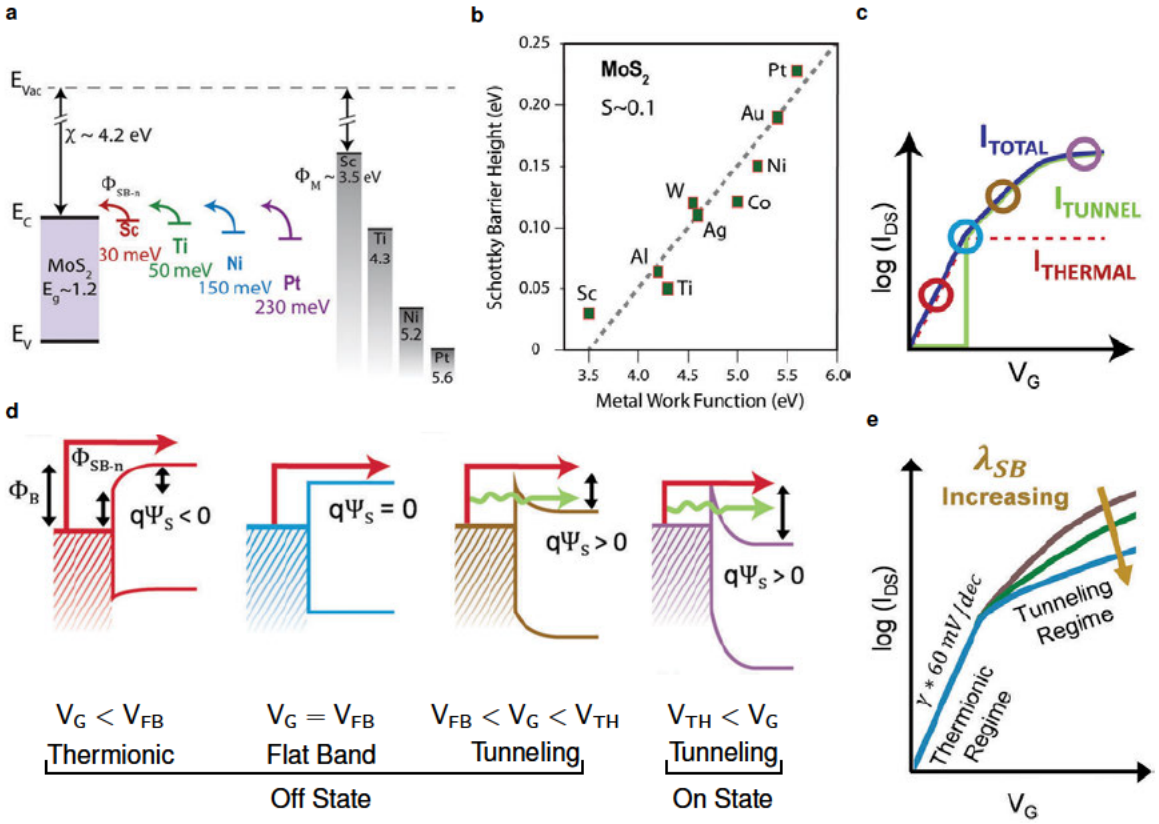

Figure 2.8. **(a)** Fermi level pinning at the MoS_2/metal interface is illustrated schematically, to the left the experimentally determined alignment of the pinned metal Fermi level in comparison to the work function alignment of Sc, Ti, Ni, and Pt in the Schottky limit [171]. **(b)** Determination of the Schottky pinning factor S for MoS_2 based on the experimentally extracted SB heights ($\Phi_{SB,n}$) as a function of the metal work functions (Φ_M) for Sc, Ti, Ni, Pt [173], Ag [174], W [175], Co [176], Au [177], and Al [178] contacts [171]. **(c)** Schematic illustration of the transfer characteristic of a typical SB-FET, indicating the thermal component (red) and the tunnel component (green) to the total current (purple). Colored circles correspond to the thermionic regime (red), the flat band condition (blue), the tunneling dominated regime in the off-state (brown) and in the on-state (purple) with the band diagrams at the source side shown in **(d)** [171]. **(e)** If the tunnel barrier width λ_{SB} increases for thicker oxides and multilayers, see Equation (2.6), the slope and the on-current are reduced. Adapted from [171] with permission from The Royal Society of Chemistry.

Before giving a review over possible approaches to reduce the Schottky barriers at the source and drain contacts of 2D FETs which is needed to achieve small contact resistances, in the following the characteristic features of Schottky barrier FETs (SB-FETs) will be discussed. In general, the drain current through a SB-FET consists of two components, the thermionic field emission current over the top of the energy barrier and the tunneling current through the SB, $I_D = I_{thermal} + I_{tunnel}$. Both contributions depend on the gate voltage, $I_{thermal}$ and I_{tunnel} dominate the behavior below and above flatband voltage (V_{FB}), respectively. In Figures 2.8 (c) and (d) the schematic transfer characteristics of a SB-FET are shown together with the band diagrams at the source side for the different gate voltage regimes [171]. For simplicity it is assumed in the following that a large enough drain bias is applied to move the SB at the drain side out of the electron path, thus it will be assumed that every charge injected over the SB at the source contributes to I_D. In addition, only expressions for electron injection

to the conduction band are discussed as hole injection into the valence band is described analogously. In a first approximation the thermionic field emission current for applied $V_{GS} < V_{FB}$ is given by [171]

$$I_{\text{thermal}} \approx AT^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right); \qquad A = \frac{4\pi m k^2 q}{h^3}; \qquad \Phi_B = \Phi_{SB,n} - q\Psi_S, \tag{2.2}$$

where A is Richardson's constant, and the barrier height Φ_B is the difference of the inherent Schottky barrier height and the surface potential Ψ_S. Below the flatband voltage V_{FB}, Ψ_S depends linearly on the applied gate voltage V_{GS}. The defining characteristic of the thermal current component which dominates for $V_{GS} < V_{FB}$ is the exponential dependence on the temperature T and on V_{GS}. Beyond flatband conditions, I_{thermal} becomes constant and the tunnel current starts to dominate I_D. The tunnel current can be described by the following expression, using a Wentzel-Kramers-Brillouin(WKB) approximation for the tunneling coefficient through a barrier of triangular shape at the source contact and $f(E)$ denoting the Fermi-Dirac distribution of the charge carriers [183, 184]

$$I_{\text{tunnel}} \approx \frac{2q}{h} \int_{q\Psi_S}^{\Phi_{SB,n}} f(E)\, g_{2D}(E)\, T_{WKB}(E)\, \mathrm{d}E, \quad \text{with} \tag{2.3}$$

$$g_{2D} = \frac{2\sqrt{2m^\star (E - q\Psi_S)}}{h^2} \quad \text{and} \tag{2.4}$$

$$T_{WKB} = \exp\left(-\frac{8\pi}{3h}\sqrt{2m^\star (\Phi_{SB,n} - E)^3}\,\frac{\lambda_{SB}}{\Phi_{SB,n}}\right). \tag{2.5}$$

In the tunneling regime for $V_{FB} < V_{GS} < V_{th}$ also the subthreshold swing (SS) becomes tunneling limited which means that the best SS which can be achieved in this regime is larger than 60 mV/decade. Here, the threshold voltage is defined as the gate voltage beyond which band movement within the semiconducting channel ceases and the surface potential becomes constant due to the high charge carrier density in the channel. In the on-state of the MOSFET, above V_{th}, the drain current is dominated by I_{tunnel} which will of course also be subjected to scattering, entirely neglected in the simple picture presented here. For a more comprehensive description see Section 3.1.1 and chapter 6. In Equation 2.5, λ_{SB} denotes the tunneling width of the Schottky barrier, given by the degree of band bending at the metal to semiconductor interface. For ultrathin body devices such as the 2D material-based FETs studied here, where the body thickness is smaller than ~ 20 nm, this SB tunneling width can be approximated as [185, 186]

$$\lambda_{SB} = \sqrt{\frac{\varepsilon_{semi}}{\varepsilon_{ins}}\, t_{semi}\, t_{ins}}, \tag{2.6}$$

with the dielectric constants of the semiconducting channel (ε_{semi}) and the gate insulator (ε_{ins}) as well as the physical thicknesses of the channel (t_{semi}) and the insulator (t_{ins}). Equation (2.5) demonstrates that as the width λ_{SB} approaches zero, the tunneling coefficient T_{WKB} approaches one. From Equation (2.6) it can be observed that for high-k or ultrathin gate dielectrics with a monolayer 2D channel the impact of the SBs becomes negligible. Consequently, for ultrascaled devices the impact of the SB will diminish, helping to achieve smaller

contact resistances. This impact of a variation in λ_{SB} on the transfer characteristics can be seen in Figure 2.8 (e).

Besides the neglect of scattering effects, this simple model for the Schottky barriers at the contacts of SB-FETs has another important drawback, namely that it does not account for the physical length of the gated contact region. In fact, current device designs often use the applied gate voltage on the contacted area to locally lower the SB height, and thus effectively reducing the contact resistance in the on state, see for example the device designs shown in schematic cross sections in Figures 2.3 (a)-(c) and (e). In order to improve the model [183] a third current contribution which describes the tunnel current through the gated part of the contact was introduced and the extended model was successfully applied to describe the transfer characteristics of WSe_2 FETs [187]. However, both of these analytic models greatly simplify charge transport processes in the SB-FET. In order to account for the injection of charge carriers depending on the device geometry across the entire contact length (L_C), a TCAD model of the contacts is required, see Section 6.1.1.

As there is no band gap in the metal source and drain regions of a SB-FET, both electrons and holes can be injected into the channel, causing ambipolar device characteristics, where at both high positive and high negative voltages the FET is in the on state, being turned off for gate voltages close to 0 V. In effect, the degree of ambipolarity depends on the size of the band gap of the 2D semiconductor and materials with a small band gap like BP usually show ambipolar conduction while materials with a large band gap like MoS_2 or WSe_2 typically prefer one polarity determined by the energetic location of the pinned metal Fermi levels. Even for materials with strong Fermi level pinning at the conduction band edge such as MoS_2, extremely high work function contact materials such as MoO_x have been demonstrated to provide p-type conduction [188]. In an alternative approach to uncover the hole branch of MoS_2, the SB tunneling width λ_{SB} was reduced by using ionic liquid gating as an effectively ultrathin gate insulator [189]. For applications in CMOS logic the ambipolarity of BP transistors is a problem as the small band gap of bulk BP means that the device never fully reaches the off-state, thereby limiting the on/off ratio to 10^2 for bulk BP and to 10^4 for monolayer BP [183]. Thus, in order to use BP FETs for logic applications a different device design is required which relies either on doped contact regions or polarity gates [190].

In general, the impact of the Schottky barriers needs to be reduced to fabricate scaled 2D FETs with small contact resistances. Towards this aim, one of the most common methods is to tune the metal work function, using for example low work function metals such as Sc to form small Schottky barriers to n-type FETs based on MoS_2 [173]. However, Fermi level tuning does not have a sufficient impact as long as strong Fermi level pinning dominates. Therefore, in order to achieve negative Schottky barriers by work function tuning, the Fermi level needs to be depinned. This Fermi level depinning can be achieved by spatially separating the metal and the semiconductor by inserting an ultra-thin insulating layer between the metal and the 2D TMD [170, 191]. Such an insulating interlayer prevents the formation of metal induced gap states at the semiconductor interface that contribute to Fermi level pinning. However, this thin insulator also acts as an additional tunnel barrier which limits the current flow. Thus, the ideal thickness of a depinning interlayer is determined by the trade-off. This behavior

was observed for thin Ta_2O_5 interlayers inserted between the MoS_2 channel and Ti metal contacts [192]. Another insulator which can serve as a good depinning interlayer is the layered insulator hBN [170, 193]. In an alternative approach 2D/2D contacts are formed by using for example the Dirac semi-metal graphene to contact 2D semiconductors, thereby providing low contact resistances to MoS_2 [194, 195] and to WSe_2 [196]. In a similar way phase-engineered metallic phases of a TMD can be used to contact the respective semiconducting phases. For example, 2H MoS_2 monolayers can be transformed into 1T MoS_2 by locally immersing the contact regions in n-butyl lithium [168]. Another strategy towards low resistive contacts is to narrow the SB width using surface charge transfer doping. Exposure to an oxygen plasma locally converts the top-most layers of WSe_2 to WO_x which acts as a p-dopant, allowing to form a p-i-p doping pattern [197]. In addition, record-low contact resistances for MoS_2 were achieved using amorphous titanium suboxide on top of MoS_2 to heavily n-dope the entire layer with the drawback of a strongly negative V_{th} [167]. In summary, none of the proposed approaches have as of yet been able to achieve low contact resistances for both n- and p-type MOSFETs while at the same time preserving small $|V_{th}|$ and high on/off current ratios.

2.3.2 Contact Gating and Scaling

Most modern device designs use the applied gate voltage instead of chemical doping to narrow the SB width and consequently increase the drain current flow. In fact, the device designs shown in Figures 2.3 (a)-(c) and (e) use contact gating. While this is a practical and easily adaptable approach to reduce the impact of Schottky barriers and increase the current drive for 2D material-based FETs it also entails an essential disadvantage. In fact, contact gating means that there is a large gate overlap of the gate contact with source and drain electrodes, giving rise to large overlap capacitances. These overlap capacitances act as parasitic capacitances and prevent fast switching. Thus, even if the best performance of 2D FETs is at the moment typically achieved with device designs shown in Figures 2.3 (c) or (e), future device designs should aim for an adaptation derived from Figure 2.3 (d) by introducing additional degenerately doped regions under the contacts [TKJ1]. This ideal 2D FET design is shown in Figure 2.9(a). Here, a doping of the contact regions is used to narrow the SB widths. However, while some attempts to fabricate devices with p-i-p [197] or n-i-n [198] doping profiles have been made, the device performance still remains unsatisfactory.

In addition to the issues discussed above, the nanoscaled devices which are targeted with FETs based on 2D materials require nanoscaled contacts. Thus, scaling down contact dimensions is another important requirement besides the reduction of contact resistances without introducing new parasitic capacitances in the device design. In general, the contact resistance increases as L_C is reduced because of current crowding, which can be described by the following expression derived from a transmission line model which accounts for both the semiconductor sheet resistance and the contact resistance [199]

$$R_C = \sqrt{\rho_C R_{SH}} \coth\left(L_C / L_T\right), \tag{2.7}$$

with the specific contact resistivity ρ_C, the channel sheet resistance under the contact R_{SH}, and the transfer length $L_T = \sqrt{\rho_C / R_{sh}}$. This transfer length is the distance over which most of

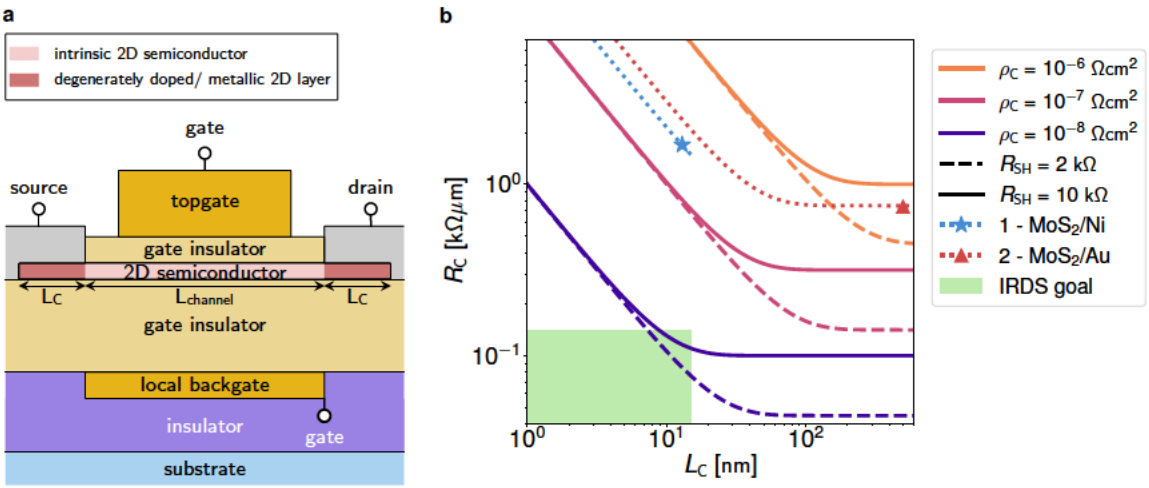

Figure 2.9. **(a)** Cross section of the device layout for a double gated FET to ensure low contact resistances and high on currents while avoiding overlap capacitances. Both n- and p-type doping schemes for the 2D semiconductors need to be developed in order to build CMOS circuitry [TKJ1]. **(b)** Calculated R_C as a function of the contact length L_C for several combinations of the specific resistivity ρ_C and R_{SH}. At the bottom left the green area indicates the targeted regime according to IRDS [21]. In comparison, at the current state-of-the-art, as reported in references 1 ([165]) and 2 ([36]), ρ_C is about two orders of magnitude too high. In this log-log figure R_C bends where $L_C = L_T$.

the current transfers from the metal into the semiconductor or vice-versa. In Figure 2.9(b) the contact resistance is shown as a function of the contact length for typical values of ρ_C and R_{sh}. It is instructive to analyze equation (2.7) in the two limiting cases of long contacts with $L_C \gg L_T$ where $R_C \approx \sqrt{\rho_C R_{sh}}$ on one side and short contacts with $L_C \ll L_T$ on the other side yielding $R_C = \sqrt{\rho_C R_{sh}}\,(L_C/L_T)^{-1} \approx \rho_C/L_C$. Thus, for a reduction of R_C in scaled devices either L_T needs to be scaled down and/or ρ_C needs to be reduced. On scaled devices $L_T < 10\,\text{nm}$ should be targeted which translates for typical sheet resistances on the order of $R_{sh} \sim 10\,\text{k}\Omega/\square$ to a specific resistivity of $\rho_C \sim 10^{-8}\,\Omega\text{cm}^2$ [TKJ1]. However, even for the lowest R_C reported in literature, the resistivity is more than an order of magnitude too high, for example for gold contacts deposited in ultra high vacuum a resistivity of about $10^{-6}\,\Omega\text{cm}^2$ and a transfer length of $L_T \sim 40\,\text{nm}$ [36] have been obtained, see Figure 2.9(b).

Furthermore, there are ongoing considerations of where carriers are injected most efficiently at the 2D/metal interface. Currently available evidence suggests that top-contacted devices with thin flakes and contact gating (thus device layout of Figure 2.3(c)) lead to edge dominated injection and offer better contact scalability [165, 187]. However, without contact gating these observations might not hold, thus pure edge contacts are a promising alternative. Advantages of edge contacts include a higher degree of covalent bonding and smaller tunnel barrier widths, alongside efficient charge injection into all layers of multilayered TMD crystals as well as the fact that there are no overlap capacitances. However, while on Pd/Au edge contacts to hBN encapsulated graphene reached contact resistances as small as 100 Ωμm [142], for Ni edge contacts formed at locally etched holes in MoS_2 [200] or for graphene edge contacts to TMDs [201] the contact resistances are high at about 30 kΩμm. These high contact resistances might originate from the minuscule contact area or from defects at the contacting interface. It remains to be seen whether these values can be improved in the future.

3 Characterization and Modeling of Performance and Reliability

In general, the performance of transistors based on 2D semiconductors is characterized with similar measurement methods and described with the same modeling approaches as nanoscaled transistors in standard silicon technologies. Here, these measurement methods used to evaluate transistor performance and reliability are briefly reviewed and, where applicable, a short literature review is given regarding how these methods have been applied to devices based on 2D materials in the last decade. Thus, the state of the art of performance and reliability of 2D material-based transistors is presented in the following. A special focus will be put on adaptations and critical points which must be considered when analyzing prototype FETs based on 2D materials. Along similar lines, approaches for modeling nanoscaled transistors are introduced and adaptations of these models to 2D FETs are reviewed. In addition, models for charge transfer to traps at the interface between the 2D material and the insulator and border traps inside the insulator in the vicinity of the channel will be discussed. Both charge transfer models introduced here are well-established for silicon devices and will be later applied to describe observations in transistors based on 2D materials.

3.1 Performance Analysis

In this section, the best approach for evaluating the performance of FETs based on 2D materials is outlined. As the electrical characteristics of 2D FETs are often sensitive to the surrounding atmosphere [202] and light exposure [203, 204], especially for devices with a bare channel (see Figure 2.3), electrical characterization should be performed in vacuum ($p < 10^{-5}$ Torr) and in darkness. In addition, the device characteristics of prototype FETs frequently drift, thus the conditions should be stabilized by controlled biasing schemes and repeated measurements before performance parameters are extracted [TKJ1]. Standard measurement procedures to analyze the performance of 2D FETs include measurements of the transfer characteristics, thus measuring I_D while sweeping V_{GS} at constant V_{DS} and showing the results both on a linear and a logarithmic scale in Figure 3.1 (a) and (b). In addition, output characteristics are measured, thus measuring I_D while sweeping V_{DS} at constant V_{GS} in Figure 3.1 (c). To ensure comparability of the measured currents, they are reported as current densities obtained by normalizing the currents by the channel width (W).

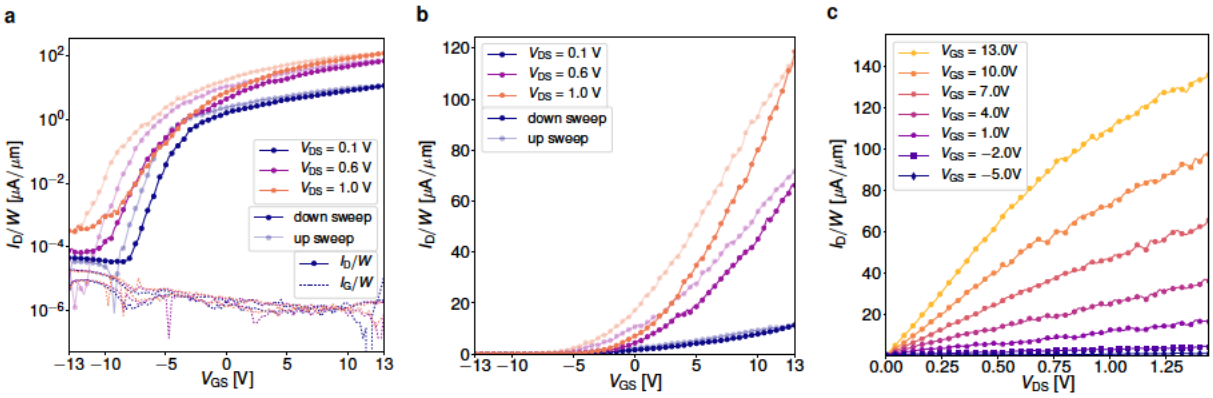

Figure 3.1. Nanoscaled MoS_2 FET characteristics recorded in vacuum using multilayer, exfoliated and patterned MoS_2 as a channel, 20 nm SiO_2 as a gate insulator and 65 nm Ni source and drain contacts, for the device layout see Figure 2.6. **(a)** Transfer characteristics on a logarithmic scale for drain voltages varying between 0.1 V and 1 V. Here, the gate leakage current is shown as a dotted line, however, I_{off} is dominated by short-channel effects as can be seen in the figure. In addition, a sizable hysteresis is observed. **(b)** Transfer characteristics on a linear scale for varying drain voltages. **(c)** Output characteristics for varying gate voltages.

3.1.1 Transfer Characteristics

An exemplary transfer characteristic for a 2D FETs is shown in Figure 3.1 (a) and (b) on a linear and on a logarithmic scale. When measuring the transfer characteristics, the gate leakage current (I_G) should be recorded to make sure that I_D is free from artifacts. Besides, the gate leakage current density (J_G) obtained by normalizing the gate leakage by the device area ($W \times L$) sets a lower limit for the drain current in the off-state (I_{off}). Furthermore, the gate voltage sweeps should be reported in both sweep directions, thus for increasing and decreasing V_{GS}, at a fixed gate voltage sweep rate(S_H) in V/s, to reveal the hysteresis in the transfer characteristics [TKJ21, 202]. However, for most applications the observed hysteresis should be minimized, thus performance indicators should be extracted from transfer characteristics recorded at fast voltage sweeps [205, 206]. Comprehensively assessing the performance of 2D FETs requires the following performance indicators; the off-state current (I_{off}), the on-state current (I_{on}), the on/off current ratio (I_{on}/I_{off}), the threshold voltage (V_{th}), the charge carrier mobility (μ), the subthreshold swing (SS), the contact resistance (R_C), and the hysteresis width (ΔV_H). All of these quantities can be extracted from the transfer characteristics as is described in the following.

From the recorded transfer characteristics the *off-state current* (I_{off}) is extracted as the lowest drain current level reached, see Figure 3.2 (a). The lower limit of I_{off} is given by the gate leakage current, however, short channel effects can lead to an increased, and voltage dependent off-state current. If both contributions are negligible, I_{off} is typically determined by the noise floor of the measurement instrument used. The *on-state current* (I_{on}) is defined as the current density reached above the threshold voltage in the on state of the FET, see Figure 3.2 (a). According to the general drain-current model for a long channel silicon based MOSFET using the charge sheet approximation [4] the drain current in the linear region of transistor operation, $V_{GS} > V_{th}$ and $V_{DS} < V_{DS,sat}$ with the drain saturation voltage $V_{DS,sat}$, can

be described by

$$I_D = \mu_{eff} C_G (V_{GS} - V_{th}) \frac{W}{L} V_{DS} = q \mu_{eff} n_S \frac{W}{L} V_{DS}. \tag{3.1}$$

In this analytic approximation μ_{eff} denotes the effective mobility in the MOSFET channel. The charge carrier concentration per area (n_S) in units of cm^{-2} is given by

$$n_S = \frac{C_G}{q} (V_{GS} - V_{th}) = \frac{C_G}{q} V_{od} \tag{3.2}$$

with the gate overdrive voltage (V_{od}) and the overall gate capacitance per unit area (C_G) given by

$$C_G = \frac{C_{ins} (C_{semi} + C_{it})}{C_{ins} + C_{semi} + C_{it}}. \tag{3.3}$$

Here, C_{ins}, C_{semi}, and C_{it} are the capacitances per unit area of the gate insulator, the semiconducting channel, and the interface traps, respectively. These capacitances can, in principle, be estimated based on the permittivities and layer thicknesses as $\varepsilon_{ins}/t_{ins}$, $\varepsilon_{semi}/t_{semi}$ and from the interface trap density as $q^2 D_{it}$. However, D_{it} can be extracted either from models or measurements of the capacitance-voltage $C_G(V_{GS})$ characteristics, thus for an accurate evaluation of the gate capacitance direct measurements of C_G are required. Based on these considerations, I_{on} should always be reported together with the drain voltage V_{DS} and the gate overdrive voltage $(V_{GS} - V_{th})$ or the charge concentration n_S.

From the on- and off-state currents, the *on/off current ratio* (I_{on}/I_{off}) is calculated as their quotient. To be able to meaningfully compare the on/off current ratio with the IRDS requirements, it needs to be stated for a specified gate voltage range between $V_{GS,max}$, where the on current was measured, and $V_{GS,min}$, where the off-current was evaluated [41]. This range corresponds to the minimum supply voltage V_{DD} which would be required by such a technology. At the current technology node a ratio of 9×10^4 should be reached for high performance applications and of 5×10^6 for low power applications, both at $V_{DD} = 0.7\,V$ [21].

The *subthreshold swing* (SS) is defined as the inverse of the subthreshold slope. Thus, it is obtained as the derivative of the logarithmic I_D for $V_{GS} < V_{th}$ [4, 207]

$$SS \equiv \left(\frac{d(\log_{10}(I_D))}{dV_G} \right)^{-1} = \ln(10) \left(\frac{d(\psi_S/(k_B T))}{dV_G} \right)^{-1} = 2.3 \frac{k_B T}{q} \left(\frac{C_{ins} + C_{semi} + C_{it}}{C_{ins}} \right). \tag{3.4}$$

From an experimentally recorded transfer characteristic, SS is calculated by a fit of the slope in the subthreshold regime that should be evaluated as an average over several orders of magnitude change in I_D, see Figure 3.2 (a). For ultrathin body FETs based on 2D semiconductors it generally holds true that $C_{semi} \gg C_{ins}$. Nevertheless, the ideal value for SS of $2.3 V_{thermal} = 59.5\,mV/dec$ is rarely reached for prototype 2D FETs. In 2D FETs D_{it} and hence the interface trap capacitance $C_{it} = q^2 D_{it}$ is typically high, thereby severely degrading SS. This high interface trap density is presumably caused by the highly defective interface between amorphous gate oxides and layered semiconductors, see Section 4.2.1.

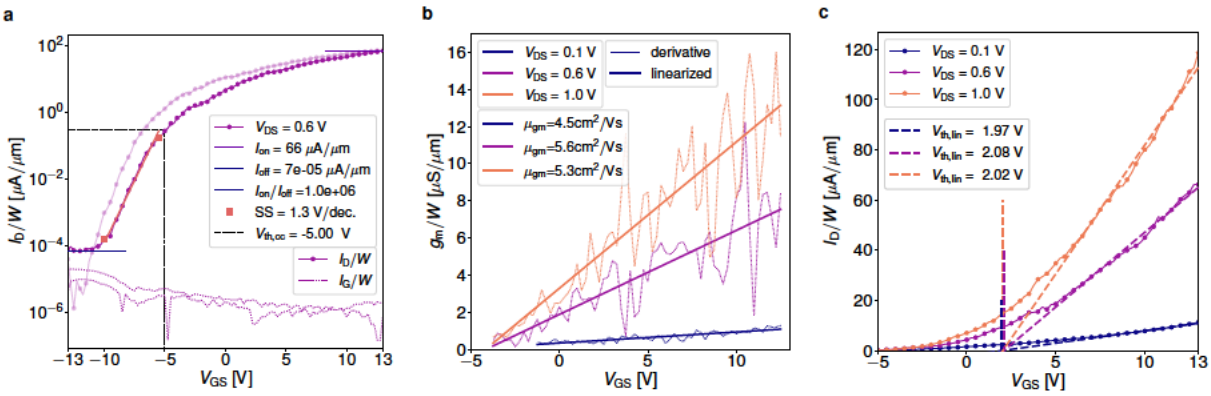

Figure 3.2. **(a)** From the transfer characteristics of a nanoscaled MoS_2 FET on a logarithmic scale, several performance characteristics can be extracted, most importantly I_{on}, I_{off}, I_{on}/I_{off}, SS and the threshold voltage when using a constant current criterion $V_{th,cc}$. **(b)** Transconductance of this device including the calculated mobility using the peak transconductance method. However, as in this device layout (see Figure 2.6) back gated Ni contacts are used these values could both over- and underestimate the actual mobility of the 2D channel. **(c)** Based on the transfer characteristics on a linear scale the threshold voltage is determined using the linear extrapolation method $V_{th,lin}$, arriving at a value for $V_{th,lin}$ which is in this example 7 V higher than $V_{th,cc}$.

As another performance indicator, the *contact resistance* (R_C) is extracted using the transfer length method (TLM) for different charge concentrations n_S, thus varying gate overdrive voltages. In 2D FETs, R_C often depends on n_S as the contact regions are under the electrostatic control of the gate in back gated transistor geometries, see Section 2.3.2. Consequently, the dependence of R_C on the gate overdrive voltage is a peculiarity of 2D material-based FETs and needs to be characterized in a comprehensive device characterization. As detailed in Section 2.3 the contact resistances can be evaluated either by TLM measurements or by four probe measurements, even though TLM measurements give in general more accurate results. In a TLM measurement the total resistance (R_{tot}) of a long and wide patterned channel is evaluated for multiple effective channel lengths. The total resistance is given as

$$R_{tot} = R_{ch} + 2R_C, \qquad R_{ch} = \frac{L}{q n_S \mu_{sheet}}, \tag{3.5}$$

with the contact resistances at source and drain R_C and the sheet resistance of the 2D channel R_{ch}. The channel is contacted at increasing distances, corresponding to increasing lengths L in the sheet resistance R_{ch}. Thus, the values for R_{ch} and $2R_C$ are obtained as the slope and the y-axis intercept of the measured R_{tot} as a function of L, see Figure 2.7 (b).

3.1.2 Threshold Voltage

Naturally, the *threshold voltage* (V_{th}) which identifies the bias at which the FET is turned on is an essential device parameter. In conventional silicon MOSFETs, the threshold voltage is defined as the gate voltage, where an inversion channel forms at the silicon surface and the surface potential equals two times the Fermi potential in the semiconductor bulk [4]. However, this definition does not hold for ultrathin body MOSFETs with an undoped, intrinsic channel

formed by a 2D semiconductor. The energy barrier that is modulated to turn on FETs using 2D channels is given by the Schottky barrier at the metal-semiconductor contacts. Instead, in this context, a more general definition of the threshold voltage should be invoked. In fact, the threshold voltage can be defined as the gate voltage beyond which band bending within the semiconducting channel ceases and the surface potential becomes constant due to the high charge carrier density in the channel [184]. This definition also applies to FETs based on 2D materials, even though the value of the surface potential in the on-state is undefined. Some analytical expressions for the threshold voltage in ultrathin body FETs have been derived [208, 209], however, these expressions depend on the device layout, single or double gating of the devices and in short channel devices also on the gate length L. Hence, no expressions which would be valid for the majority of prototype FETs based on 2D materials can be provided, as common device layouts vary greatly, see Figure 2.3.

Independent of the theoretical definition of V_{th}, several methods can be used to experimentally determine V_{th} [100, 210, 211]. In the following, three of the most important methods to extract V_{th} experimentally will be briefly reviewed. First, in the constant-current method $V_{\mathrm{th,CC}}$ is defined as the gate voltage where

$$I_{\mathrm{D}} \frac{L}{W} = I_{\mathrm{ref}} \tag{3.6}$$

holds. Therefore, as the gate bias where the drain current normalized by the geometric dimensions of the FET equals a reference current level (I_{ref}), see Figure 3.2 (a). This reference current level is a predefined value, typically in the range of 10 µA and 10 nA. The constant-current method is widely used in industry because of its simplicity, despite the major disadvantage that the defined threshold voltage depends on the drain current level chosen to apply the criterion [210].

Second, using the linear extrapolation method $V_{\mathrm{th,lin}}$ is defined as the V_{GS} axis intercept of the transfer characteristics on a linear scale. Typically, the extrapolation of the $I_{\mathrm{D}}(V_{\mathrm{GS}})$ curve is based on its maximum slope, thus where the transconductance

$$g_{\mathrm{m}} = \frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}V_{\mathrm{GS}}} \tag{3.7}$$

has a maximum, see Figures 3.2 (b) and (c). This linear extrapolation is probably the most widely used method [100] while having the drawback that the extracted $V_{\mathrm{th,lin}}$ can be strongly influenced by source and drain contact resistances as the maximum g_{m} value is impacted by parasitic source and drain resistances [210].

Third, in the Y function method $V_{\mathrm{th,Y}}$ is evaluated as the intercept of the Y function with the V_{GS} axis, which is given by

$$Y = \frac{I_{\mathrm{D}}}{\sqrt{g_{\mathrm{m}}}} = \left(V_{\mathrm{GS}} - V_{\mathrm{th,Y}}\right) \sqrt{\mu_{\mathrm{Y}} \frac{W}{L} C_{\mathrm{G}} V_{\mathrm{DS}}} \tag{3.8}$$

as a function of V_{GS}. This approximate expression for Y can be obtained by inserting the expression for I_{D}, see Equation (3.1) in the definition of the Y function. This method, also

termed Current-to-square-root-of-the-Transconductance Ratio (CsrTR) method [210], has the advantage that the resulting $V_{\mathrm{th,Y}}$ values are independent of contact resistances in silicon technologies [210] as well as in Schottky-barrier dominated FETs based on 2D materials [212]. However, it was recently demonstrated that certain 2D materials impose limits on the Y function method. For example, the strong inversion regime with $V_{\mathrm{GS}} \gg V_{\mathrm{th,Y}}$ cannot be accessed in WSe_2 FETs, due to the formation of large Schottky barriers. Therefore, the extracted $V_{\mathrm{th,Y}}$ will depend on the contact resistance in this case [211].

Summarizing the above, it should be noted that the quantification of V_{th} strongly depends on the chosen extraction scheme

$$V_{\mathrm{th,CC}} \neq V_{\mathrm{th,lin}} \neq V_{\mathrm{th,Y}} \tag{3.9}$$

because in all methods E_{F} will be different. Therefore, the extraction method used should be reported together with the obtained V_{th} value. In this work the constant current criterion was used. Besides, the *hysteresis width* (ΔV_{H}) in the transfer characteristics is typically measured as the difference between the threshold voltage for the up sweep $V_{\mathrm{th,up}}$, and the down sweep $V_{\mathrm{th,down}}$ [TKJ21, 202]

$$\Delta V_{\mathrm{H}} \equiv V_{\mathrm{th,up}} - V_{\mathrm{th,down}}. \tag{3.10}$$

Thus, when reporting on the hysteresis of 2D material-based FETs the ΔV_{H} values will depend on the threshold voltage extraction method as well as on the sweep rate S_{H}, and the gate voltage sweep range. In Section 5.1.1 the evaluation, properties, and information obtained from analyzing the hysteresis in 2D material-based FETs will be discussed. Furthermore, an important reliability measure which is well known from silicon technologies, the bias temperature instability (BTI), see Section 3.2.3, is quantified as the shift of the threshold voltage(ΔV_{th}) during combined gate bias and elevated temperature stress and recovery thereof. In a similar way as for the hysteresis also the exact values of ΔV_{H}, see (3.10), will depend on the chosen threshold voltage extraction method.

3.1.3 Mobility Evaluation

In a similar way as the threshold voltage, the resulting *charge carrier mobility* (μ) in the semiconducting channel is a key performance parameter for a 2D FET. Carrier transport and current flow through any semiconductor are driven by two mechanisms; on the one hand by the drift of the carriers in the presence of an electric field and on the other hand by the diffusion caused by concentration gradients. At small electric fields, the drift velocity v_{D} is directly proportional to the electric field $\mathscr{E}$ with the mobility μ being defined as the proportionality constant, $v_{\mathrm{D}} = \mu\mathscr{E}$. This charge carrier mobility is inversely proportional to the average time interval between scattering events. In general, the most important physical scattering mechanisms are impurity scattering and phonon scattering [4]. It should be noted that in ultrathin 2D materials, the dielectric environment surrounding the 2D semiconductor considerably contributes to the scattering of charges, see Section 4.2.1.

In order to extract the mobility of charge carriers from measurements, several methods are routinely applied, among them the peak transconductance method (μ_{gm}), the Y function method (μ_Y), and four-probe or TLM measurements which directly probe the sheet resistance of the channel (μ_{sheet}). In the peak transconductance method, the mobility is calculated from the maximum of the transconductance. Combining Equations (3.7) and (3.1) yields the following expression for the mobility μ_{gm}

$$\mu_{gm} = \frac{g_{m,max} L}{W C_G V_{DS}}, \tag{3.11}$$

see also Figure 3.2 (b). However, the estimate of μ with this method is prone to errors, especially for transistor layouts with contact gating where R_C strongly depends on V_{GS}. While it is commonly believed that μ_{gm} underestimates the real mobility as contact resistances are neglected, it has recently been shown that μ_{gm} is equally likely to overestimate the actual channel mobility due to an overshooting of $g_{m,max}$ caused by contact gating [42, 211].

In comparison, the Y-function method is more robust, yielding more accurate results in the presence of Schottky contacts with large R_C [212]. When using the Y-function method, the mobility μ_Y is extracted from the slope of the Y-function according to Equation (3.8). Nevertheless, also the value of μ_Y is subjected to errors for contact-gated devices. At the same time, the Y-function method together with a thorough inspection of the shape of g_m as a function of the gate voltage V_{GS} can be used to diagnose if the device performance is severely limited by the contacts [211]. In the case of a strong contact limitation and contact gating the mobility needs to be extracted from the sheet resistance R_{ch}.

This sheet resistance of the channel (R_{ch}) is either obtained from four-probe or TLM measurements and is defined as

$$R_{ch} = \frac{W}{I_D} V_{DS}. \tag{3.12}$$

By inserting Equation (3.1) in the above expression, the connection between R_{ch} and μ_{sheet} is obtained, as given in Equation (3.5) and rearranged to

$$\mu_{sheet} = \frac{L}{q n_S R_{ch}}. \tag{3.13}$$

From this expression it can be seen that errors in μ_{sheet} can be easily introduced when approximating the charge carrier concentration n_S using Equation (3.2). According to this estimate n_S depends on the overdrive voltage ($V_{GS} - V_{th}$) and thus on the threshold voltage which is subjected to inaccuracies depending on the extraction method used , see the previous Section 3.1.2. Alternatively, a Hall measurement can be used to determine n_S accurately [40, 213]. Even though the obtained mobility values differ based on the extraction method, for a careful extraction of μ_{sheet}, its value corresponds to the effective mobility μ_{eff}. This effective mobility is defined as the average of the local mobility $\mu(x, y, z)$ weighted with the carrier concentration $n(x, y, z)$ and is used as a material parameter in the drift diffusion models, see Section 3.3.2.

3.2 Device Stability and Reliability

In this section, a brief overview will be given about the state of the art in evaluating degradation mechanisms in FETs and important terms for describing the reliability of nanoelectronic devices will be introduced. The terminology used to characterize the reliability of conventional silicon technologies typically becomes relevant for the stability of 2D material-based FETs already at much shorter timescales, thereby affecting normal device operation [TKJ15, 214, 215]. In addition, the IRDS lists device reliability as an important requirement for any applications in VLSI logic [21]. At the same time, these reliability goals become increasingly difficult to meet due to scaling which drives materials towards their physical limits and increases applied electric fields. Independently, these reliability targets are particularly challenging for transistors based on 2D materials, see Section 4.2.

In the following, the most important terms as defined for silicon technologies will be introduced, and, where applicable, available literature on these phenomena in 2D material-based FETs will be reviewed. This discussion then serves as the foundation for the detailed investigation of these phenomena in 2D material-based FETs in Chapter 5.

3.2.1 Low Frequency Noise

Low frequency noise is commonly also called flicker noise or 1/f noise and comprises random fluctuations in the measured drain current levels or equivalently in V_{th} over a wide range of frequencies from mHz to MHz. Its characterizing feature is that noise components of many different periodicities overlap which then results in a $1/f^{\alpha}$ dependence of the power spectral density (PSD). This PSD is obtained experimentally by applying a fast Fourier transformation to the current trace recorded in the time domain ($I_{\mathrm{D}}(t)$) and is defined as the Fourier transform of the autocorrelation function which quantifies a signal's periodicity in the time domain. Thus, the frequency dependence of the power spectral density is central to identifying and analyzing $1/f$ noise. As the equipment to record a power spectrum is often readily available, $1/f$ noise is among the most frequently studied reliability issues in 2D material-based FETs [216, 217, 218].

In general, there are two possible sources of noise current fluctuations in a FET. Both stem from physical processes in the material system formed by the 2D semiconductor and the gate insulator. One noise source comes from the fluctuations in the number of charge carriers contributing to the current as charges are constantly exchanged between the channel and defects in its direct vicinity. Another potential noise source comes from fluctuations in the charge carrier velocity and thus in the mobility due to local variations in the phonon scattering rate and scattering at charged impurities. Note that, for noise arising from mobility fluctuations, no physics-based theoretical model has been established as of yet [219]. Instead, Hooge's empirical relation is often used, relating the noise spectrum of I_{D} to the total number of charge carriers in the channel $N = WLn_{\mathrm{S}}$ with the Hooge parameter α_{H} as the proportionality factor [220]. In bilayer MoS_2 FETs the determined Hooge parameter is orders of magnitude higher than expected with an additional dependence on the applied V_{GS} and temperature [217].

Consequently, in FETs with an ultrathin channel the large surface to volume ratio of the 2D material together with the overall high defect density suggest that carrier number fluctuations, caused by charge trapping, are the dominant noise source [217, 221]. A single charge trap which randomly captures and emits charge carriers at an average time constant τ and an average number of full and empty traps N_T causes noise with a PSD of [219]

$$\frac{S_{I_D}}{I_{D\,\text{single}}^2}(f) = \frac{N_T}{(WLn_S)^2}\frac{\tau}{1+(2\pi f)^2\tau^2} = \frac{B\tau}{1+(2\pi f)^2\tau^2}. \tag{3.14}$$

This equation describes a Lorentzian power spectrum which shows a plateau for frequencies smaller than a certain corner frequency and a decline proportional to f^{-2} above that, see Figure 3.3 (a). On nanoscaled FETs, with a sufficiently small device area $W \times L$, single charge trapping events can be observed directly as discrete steps in the current traces in the time domain. This case is called Random Telegraph Noise (RTN), see Section 3.2.2. If instead a large area device is characterized many charge trapping events are superimposed. Assuming that these traps are isolated and do not interact with each other, the overall PSD is given by the sum over the contributions from every single trap

$$\frac{S_{I_D}}{I_{D\,\text{multiple}}^2}(f) = B\sum_i^{N_T}\frac{\tau_i}{1+(2\pi f)^2\tau_i^2} \approx BN_T\frac{1}{2\pi f}. \tag{3.15}$$

This process of linear superposition of the PSDs of many traps is illustrated in Figure 3.3 (a). It is assumed that the defects' time constants are in a first order approximation uniformly distributed on a logarithmic time scale, for a sufficiently large number of defects [222]. In addition, the inner term of the sum is maximized for $\tau_{max} = 1/(2\pi f)$ and thus the sum can be approximated by a sum over its maximum components. This shows how $1/f$ noise can be interpreted as the superposition of many independent charge trapping processes.

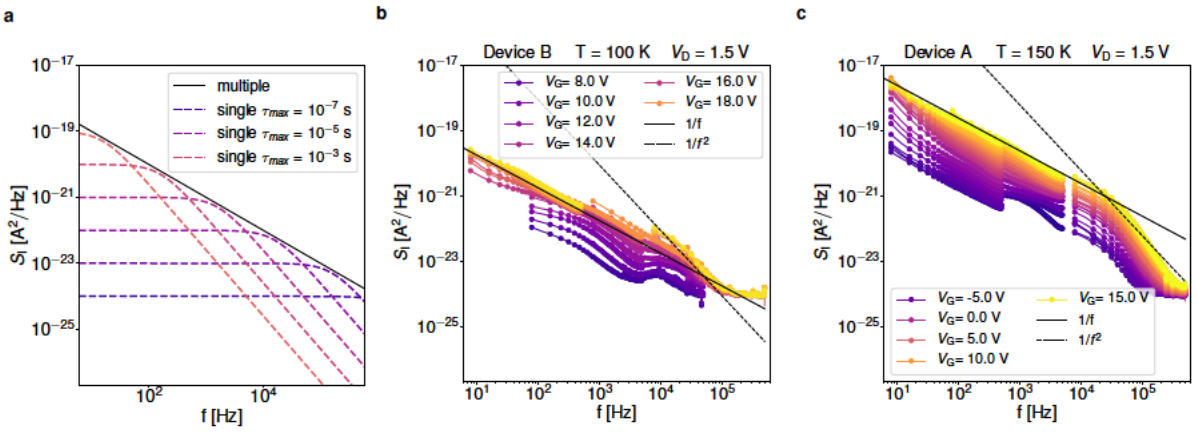

Figure 3.3. **(a)** Here, the superposition of six single charge trapping events with corner frequencies between 1×10^{-7} s and 1×10^{-2} s is shown. The sum over these Lorentzian PSDs results in a PSD with a $1/f$ frequency dependence. **(b)** This PSD was measured on an MoS_2 FET fabricated during the research stay at Purdue, with the device layout shown in Figure 2.6 and dimensions of $W = 70$ nm and $L = 70$ nm for the device B shown here. **(c)** On device A the device dimensions are larger with $W = 100$ nm and $L = 70$ nm. This FET was fabricated from the same flake as device B but on device A the overall noise power is higher, being highest for the highest drain current levels in the on-state.

In Figures 3.3 (b) and (c) the measured $1/f$ noise on multilayered back gated MoS_2 FETs with small device areas is shown at different temperatures. Here, it can be seen that the PSD transitions from a $1/f$ behavior for low frequencies, where many defects contribute, to a $1/f^2$ dependency for high frequencies where only few defects are active. In addition, the analysis of $1/f$ noise can serve as a diagnostic tool to identify operation regimes at smaller gate overdrive voltages where the contacts dominate I_D and at higher V_{od} where the channel dominates I_D [221]. Overall noise levels can be considerably reduced by reducing the electrically active trap densities at the interface and in the gate insulator. For example, an hBN layer can be included in the gate stack or the channel can be encapsulated to avoid noise from adsorbates [218].

McWhorter was the first one to formulate a physics-based model for $1/f$ noise based on the charge transfer of electrons to defects within the gate insulator [223]. For this purpose, he extended the SRH model, see Section 3.4.1, to account for the tunneling of electrons through the insulator. While the McWhorter model is still used to describe $1/f$ noise, it cannot account for the fact that capture and emission time constants of border traps typically differ and that τ_C has a temperature dependence [224]. These shortcomings are addressed by the non-radiative multi-phonon (NMP) model, see Section 3.4.2.

3.2.2 Random Telegraph Noise

On small area MOSFETs at certain bias and temperature conditions individual point defects in the insulator are electrically active and exchange electrons with the semiconducting channel. These single charge transfer processes are characterized by a PSD with a Lorentzian shape with amplitude S_{I_D}/I_D^2, see Equation (3.14). In the time domain every charge capture or emission process is seen as a step in the drain current ΔI_D and thus ΔV_{th}. Therefore, if the current is observed as a function of time, a trace of many subsequent charging and emission events is seen which is termed Random Telegraph Noise (RTN) [224, 225]. RTN is found in MOSFETs when the active channel area is small enough to exhibit only a handful of active defects. For more details on this single-defect limit for various technologies see Section 5.2 and Figure 5.13.

First reports of RTN trace measurements come from Ralls *et al.* in 1984 [226], as the fabrication capabilities for silicon based MOSFET first allowed devices in the nanoscale regime, measuring $L = 1\,\mu m$ and $W = 100\,nm$. These measurements paved the way for the first systematic investigation and formulation of a comprehensive theory for charge transfer at border traps by Kirton and Uren in the late 1980s [222, 227]. At that time, RTN investigations were mainly of interest for the device physics community [228, 229], as RTN measurements allow one to study the location and nature of defects in the MOS structure. In fact, due to the amorphous nature of the oxide, every point defect is uniquely characterized by its step height $\overline{\Delta V_{th}}$ and the respective capture and emission time constants, τ_c and τ_e. Based on these quantities the defects' distance from the channel-oxide interface can be determined. Furthermore, in conjunction with an adequate physical description, see the NMP model in Section 3.4.2, its atomistic properties and nature can be compared to *ab-initio* calculations [230]. Hence, often the terminology "fingerprints of defects" is associated with RTN measurements [224]. As the

dimensions of silicon FETs were scaled down, the importance of RTN gradually increased. In recent years RTN has become an important phenomenon for nanoscaled silicon FETs also from the perspective of industry and commercial devices [231, 232]. In highly scaled MOSFETs, the step height of single defects increases [233] which ultimately leads to the failure of MOSFETs and logic circuits caused by individual charge traps.

Up to now, technological difficulties related to the fabrication of high quality 2D FETs, which exhibit a small active area $W \times L$ and a simultaneously sufficiently low border trap density, have strongly limited the number of studies on RTN in 2D FETs [TKC6, TKJ14, 234, 235]. It was shown that RTN in monolayer MoS_2 FETs features higher step heights than their few-layer counterparts [234], rendering RTN a severe reliability concern for scaled monolayer 2D FETs. In addition, lateral voltage probes were used to localize single electrically active defects along the channel [235], while their vertical position has been determined based on the voltage dependence of the time constants [TKJ14]. In a recent analysis of RTN in nanoscaled MoS_2 FETs employing SiO_2 as the gate oxide, the temperature dependence of the time constants at cryogenic temperatures is discussed [TKC6], see Sections 5.2.1 and 5.2.2.

3.2.3 Bias Temperature Instability

Charge transfer to pre-existing defects in the gate insulator is a central degradation mechanism in MOSFETs. Since the first observations of charge trapping in the insulator at high gate biases and temperatures in the mid-1960s [236, 237], this degradation mechanism has become one of the most serious reliability concerns for CMOS technologies [21] and is nowadays referred to as bias temperature instability (BTI). As charge trapping is a thermally activated process, where barrier heights depend on the applied gate bias, BTI can provide an estimate for the lifetime of FETs using a power law approximation or physics-based modeling, see Section 3.4.2. In a BTI measurement, the electric field across the gate insulator reaches values of up to 10 MV/cm and the temperatures typically range between room temperature and 300 °C. These conditions are usually referred to as stress conditions. In contrast to hot carrier degradation, see Section 3.2.5, no drain bias is applied during stress, $V_{DS,stress} = 0\,V$. Throughout a stress period the degradation of the FET is quantified by the threshold voltage shift (ΔV_{th}) as charge trapping at border traps leads to a shift of the FET's transfer characteristics. After the stress time t_{stress}, the stress conditions (stress voltage $V_{GS,stress}$ and temperature T_{stress}) are switched to recovery conditions, which typically refers to a small gate bias below threshold close to 0 V ($V_{GS,rec}$). For a comprehensive BTI measurement several stress and recovery cycles are repeated at regular time intervals on a logarithmic scale [238, 239], see Figure 3.4 (a).

Depending on the sign of the applied stress bias, positive bias temperature instability (PBTI) at positive gate biases and negative bias temperature instability (NBTI) at negative gate biases are distinguished. Typically, pre-existing insulator defects become positively charged during NBTI stress and thereby shift V_{th} towards more negative voltages. Equivalently, negatively charged defects during PBTI stress impose a V_{th} shift towards more positive gate voltages. However, shifts of the opposite polarity are observed in rare cases and are thus termed anomalous BTI. In scaled silicon technologies, this observation has been explained by charge trapping at insulator defects of charges originating from the gate, for example for NBTI

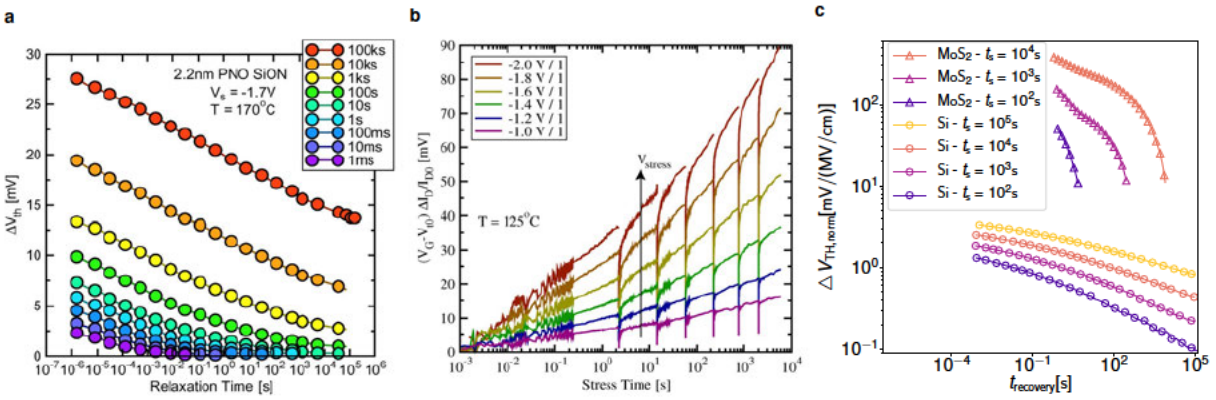

Figure 3.4. **(a)** NBTI recovery traces on commercial silicon/silicon oxynitride p-type FETs. Here, the FETs are stressed at 170 °C and a bias of −1.7 V and ΔV_{th} shifts are shown for recovery and stress times spanning more than 10 orders of magnitude, reproduced from [239]. **(b)** NBTI stress traces as measured on plasma nitridated silicon/silicon oxynitride p-type FETs using an extended measure stress measure scheme and on-the fly characterization. I_D is recorded for stress times increasing on a logarithmic time axis and converted to ΔV_{th} shifts. In these measurements, the stress cycles are interrupted by extended recovery cycles without an effect on the subsequent degradation, reproduced from [240]. **(c)** Comparison of NBTI recovery traces as recorded on silicon/silicon oxynitride [215] and MoS_2/silicon dioxide [TKJ16] devices. To allow for a fair comparison ΔV_{th} is normalized by the applied gate oxide stress field, adapted from [TKJ1].

causing positive ΔV_{th} [241] and PBTI causing negative ΔV_{th} [242]. Another well-known property of BTI in silicon technologies is its recoverable and its permanent component, meaning that parts, but not all, of the ΔV_{th} shifts observed during stress are reversed during long recovery periods [243]. However, usually, only the combination of both recoverable and permanent components can be experimentally detected, thereby complicating the analysis and theoretical description of the underlying physical mechanisms. In general, it is accepted that the recoverable component is caused by charge transfer to insulator defects as described by the non-radiative multi-phonon model [224, 244], see Section 3.4.2. For the permanent component of BTI either an empirical double-well model can be used or recently a model was proposed, which explains the permanent degradation via a thermally activated redistribution of hydrogen within the oxide [245]. Recently, this model was extended to account for the depassivation of Si-H bonds at the interface which leads to the creation of P_b-centers at the interface [246].

For evaluating the threshold voltage shifts which are used to quantify BTI, the most straightforward and well established method is the measure-stress-measure (MSM) scheme. Here, at first the initial threshold voltage $V_{th,0}$ is extracted from an $I_D\,(V_{GS})$ sweep. Then, stress conditions in the form of elevated V_{GS} and temperature are applied for a certain time, after which the threshold voltage shift is evaluated by measuring again an $I_D\,(V_{GS})$ curve and calculating $\Delta V_{th} = \left(V_{th} - V_{th,0}\right)$. This method is easy to use but suffers from an unavoidable measurement delay. In fact, a non-negligible part of the device degradation already recovers during the delay t_D between the end of the stress phase and the subsequent measurement [247]. Thus, over the last decades, considerable progress was made to reduce this measurement delay, starting from 1 ms in 2003 [248], reaching 1 µs in 2006 [205], down to only 1 ns in 2018 [249].

At the same time, the fast recovery after stress contains valuable information about the kinetics of the underlying charge transfer processes. To access this information, the extended measure-stress-measure (eMSM) scheme was devised [238, 240]. Here, the recovery period is extended after the evaluation of V_{th} which is instead monitored during a prolonged recovery period. After that period, the same stress conditions are applied for times at regular intervals on a logarithmic time scale and typically the observed degradation is not affected by extended recovery phases between the stress phases [240], see Figure 3.4 (b).

When this BTI characterization methodology, known from silicon technologies, is applied to prototype 2D material-based FETs, the observed phenomena and trends are mostly similar [TKJ21, 214, 250]. Numerous studies demonstrate how BTI saturates slowly and also after a long recovery often shows a small permanent component [251, 252]. Furthermore, the observed BTI degradation on 2D FETs is strongly temperature activated, similar to conventional silicon technology. Consequently, BTI substantially increases at elevated temperatures, e.g. between 40 °C and 160 °C [TKJ21, 214, 250]. While mostly normal BTI is reported [TKJ16, 253], also anomalous BTI has been observed on FETs based on MoS_2 using a thick SiO_2 back gate [254]. However, in all these studies the measured threshold voltage shifts are typically a few orders of magnitude larger than what is observed in commercial silicon FETs [TKJ16, 215], see Figure 3.4 (c). The reasons for this increased instability will be addressed in Sections 4.2.2 and 5.1.2.

For the characterization of BTI on transistors with semiconducting 2D channels, several peculiarities need to be considered. First, if the devices have a bare channel, their transfer characteristics and also the threshold voltage drifts will depend on the ambient environment. Accessing the intrinsic BTI characteristics of the device, hence, requires the measurements to be performed in vacuum. To improve the device quality and to overcome this issue, numerous materials have been tested as encapsulation layers including hBN [TKJ21], Al_2O_3 [255], and polymers like copolymers [256] or PMMA [257]. Only few studies achieved an encapsulation quality good enough to ensure that the BTI degradation becomes independent from the ambient environment with Al_2O_3 being the most successful candidate [TKJ16, 257].

An additional source of BTI measurement uncertainties is associated with the experimental method to determine V_{th} itself, see Section 3.1.2. As the obtained values for V_{th} and consequently also the values for ΔV_{th} depend on the selected method, this method always needs to be specified. This issue is more severe for prototype 2D material FETs, where under stress conditions the overall transfer characteristics start to deteriorate [TKJ21]. In addition, graphene transistors (GFETs) do not have a threshold voltage and only modulate the current level in the on state. Thus, for BTI studies on GFETs ΔV_{th} cannot serve as a measure for the drifts of the characteristics, instead the closest analogon of the threshold voltage in a GFET, the Dirac voltage, is used. It is defined as the voltage where the current is minimal and p- and n-branch of the transfer characteristics meet [258]. Finally, it should be noted that in a comprehensive characterization of BTI both stress and recovery traces need to be recorded, as especially the recovery traces contain important information required to identify the recoverable and permanent components.

3.2.4 Time-Dependent Defect Spectroscopy

On nanoscaled FETs, a countable number of defects contributes to the observed BTI degradation. Therefore, instead of a continuous ΔV_{th} recovery trace, on nanoscaled FETs the ΔV_{th} trace exhibits multiple steps which originate from single charge trapping events at border traps. In a time-dependent defect spectroscopy (TDDS) measurement these steps are analyzed, thereby collecting information on single point defects in the insulator close to the semiconductor interface [259, 260]. Similarly to RTN being the discrete analogon of $1/f$ noise in transistors with small active areas, TDDS traces represent the discrete analogon of continuous BTI drifts. At the same time, TDDS can also be interpreted as an advancement to the analysis of RTN traces. There are two central advantages of TDDS compared to RTN measurements. First, TDDS allows to access a much wider regime of gate biases. Second, it is much easier to analyze a TDDS signal with several defects, whereas an RTN trace which contains more than three defects is almost impossible to evaluate [260]. Also, while RTN is performed in quasi-thermal equilibrium at a constant gate bias, during a TDDS measurement the MOSFET's space charge layer is switched between inversion and depletion or accumulation. During a TDDS measurement, either positive or negative stress bias is applied, thus triggering charge capture or emission events at several border traps. Subsequently, a TDDS trace is recorded at the recovery bias and the gradual (dis-)charging of single border traps is observed.

In general, it should be noted that, besides RTN, see Section 3.2.2, TDDS is among the few measurement methods that can reveal direct information about the time constants of the charge trapping processes. This renders TDDS a powerful tool to develop a better understanding of MOSFET degradation inflicted by border traps. TDDS has gained importance since the introduction of high-k gate stacks [261] and its significance will increase even more for nanoscaled FETs based on 2D materials. Thus, since the term TDDS was coined in 2010 [259, 262] numerous large-scale TDDS measurements have been performed, where on repeated measurements a large total number (>1000) of capture/emission events of single defects have been reported for state-of-the art silicon MOSFETs [263, 264, 265]. To the best of our knowledge, the first preliminary TDDS measurements on 2D FETs have only recently been performed [TKC6] and are described in detail in Section 5.2.3.

3.2.5 Hot Carrier Degradation

In contrast to BTI, which is concerned with the degradation of MOSFETs at elevated gate insulator fields and equilibrium carrier distributions in the channel, hot carrier degradation (HCD) describes the deterioration of MOSFETs' characteristics due to elevated drain bias conditions. At high drain fields, charge carriers in the channel reach high energies and are thus termed "hot carriers". As these hot carriers interact with the MOSFET channel and its surrounding, they are able to create new defects which degrade the device performance. In the 1980s it was established that hot carriers break silicon-hydrogen bonds at the Si/SiO_2 interface, thereby creating P_b centers [266, 267]. However, the detailed mechanism of bond breaking and defect creation is still being debated in the research community [268, 269]. These newly created P_b

centers at the interface act as scattering centers and as such they degrade the mobility, the sub-threshold slope and cause V_{th} shifts. As a consequence, in silicon technologies the change of the drain current in the linear region is usually used to quantify HCD. Furthermore, HCD typically barely recovers, which is in stark contrast to BTI. HCD has become an increasingly important degradation mechanism over recent years as in advanced technology nodes the drain fields have reached critical levels [270]. Thus, it is expected that HCD will also play an important role in ultra-scaled FETs based on 2D materials. However, up to date little is known about HCD in 2D material-based devices [TKJ15, 271, 272].

3.2.6 Time-Dependent Dielectric Breakdown

Time-dependent dielectric breakdown (TDDB) is becoming an increasingly important reliability concern for strongly scaled FETs, as the electric gate fields increase. At elevated gate fields the insulator will break down after a certain time, and as the distribution of this time to failure is an important characteristic, it is termed TDDB [273, 274, 275]. It is well established, that the underlying physical mechanism of TDDB consists of the creation of traps which then act as tunneling centers and further increase the leakage current [274]. More and more defects are created in the insulator until at one location a small conductive filament is formed in the dielectric. This formation is typically observed as a strong increase of I_G which leads to device failure. In the standard measurement process a high constant gate voltage is applied and the time is recorded until the gate insulator breaks down. As the trap formation and local accumulation are stochastic processes, many devices must undergo the same stress tests to determine the statistical distribution of the time to failure [275]. Besides stressing real FETs, spatial information about the dielectric breakdown and filament formation can be obtained by Conductive Atomic Force Microscopy (CAFM) measurements, where a nanoscale tip is used to locally probe the stability of the dielectric [276].

In general, TDDB depends primarily on the insulator used, even though metal contacts play an important role in the formation of the filament. Up to now most TDDB studies were performed on silicon CMOS technologies using conventional amorphous gate insulators, among them SiO_2 [277], Al_2O_3 [278], and HfO_2 [279]. While it is expected that the TDDB stability of 2D FETs based on these insulators will be similar to silicon FETs, this yet needs to be confirmed. At the same time, the TDDB mechanisms observed on novel crystalline insulators, see Section 4.4, are different from the mechanisms in amorphous oxides. In FETs using layered, crystalline hBN as a gate insulator, a layer-by-layer breakdown mechanism was observed where the single layers break consecutively [280]. In more defective CVD grown hBN layers, the pre-existing defects play an important role in the breakdown and it was shown that boron vacancies can act as precursor sites [281]. In hBN, typically a large dispersion of onset voltages is observed due to the strongly varying local concentrations of pre-existing defects introduced during CVD growth. In contrast to this behavior, MBE grown CaF_2 layers feature a high homogeneity, even at the nanoscale, with a uniform onset voltage at high electric fields, showing the promise of this material as a gate insulator [TKJ6].

3.3 Modeling Transistors Based on 2D Materials

To model the current in a transistor, the charge carrier distribution is evaluated for a simulation domain, where external voltages are applied to the terminals and electrons can flow in and out of the contact leads. This setup forms an open boundary problem outside of the thermodynamic equilibrium. To solve this problem either a quantum mechanical or a semiclassical modeling approach can be chosen, depending on the transport regime which is governed by the ratio of the device dimensions W, L to the approximate mean free path l of charge carriers in the device. Typically, l is on the order of a few nm in 2D semiconductors, for example about 2 nm for a monolayer of MoS_2 on SiO_2 [51]. If the device dimensions are smaller than l, the transport is ballistic and quantum mechanical effects such as tunneling dominate. In this regime quantum mechanical models are used, for example based on the Non-Equilibrium Green's Function (NEGF) formalism [282]. However, a full quantum mechanical description is typically computationally too expensive to describe transport through prototype FETs. Thus, if device dimensions are larger than l, a semiclassical description is used based on solving the Boltzmann Transport Equation (BTE). The BTE can be solved either directly based on the Spherical Harmonics Expansion or numerically using a stochastic Monte Carlo approach. Solving the BTE gives the full carrier distribution function, however, one can also solve for the moments of this distribution, arriving at the drift-diffusion (DD) equations or the hydrodynamic model when taking higher moments into account. The NEGF formalism is the most computationally expensive but highly accurate, inherently including quantum mechanical effects. In the transport model hierarchy, it is followed by Monte Carlo solutions of the BTE and solutions to the DD equations which offer reduced complexity at the cost of limited accuracy. At the bottom of the hierarchy are simplified compact models which provide analytic solutions for the main device quantities. Compact models can be based both on a quantum mechanical description like the Landauer formula [283, 284] or on the classical drift diffusion equations, and are the basis for circuit models. Figure 3.5 gives an overview of available models and approaches for the simulation of 2D transistors and their ranking regarding accessible device dimensions, their accuracy and computational costs.

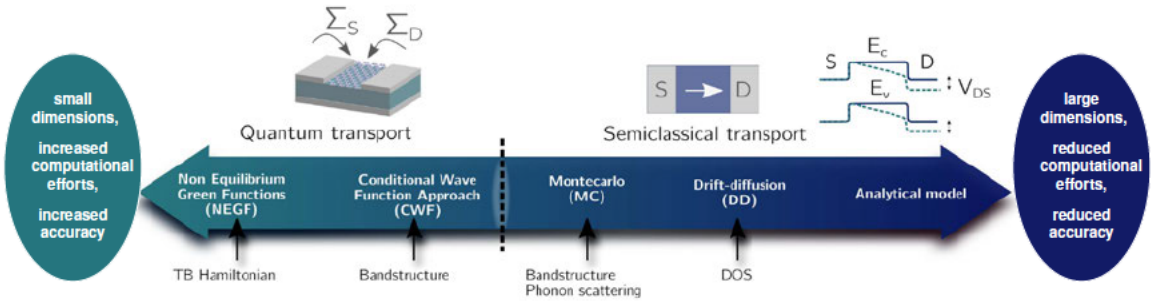

Figure 3.5. An overview of different approaches for simulating nanoscaled transistors based on 2D materials is presented. In this schematic, the approaches are ranked hierarchically according to their related computational demands and accuracies. As a consequence of the computational demand, the methods to the left are only applicable for nanoscaled devices whereas the models to the right can also be used to describe the operation of larger prototypes. Adapted from [285].

For a self-consistent solution of the charge carrier distributions and electrostatic field inside a transistor, the charge carrier concentrations must be coupled to the external potentials by

solving the Poisson equation. In addition, depending on the modeling approach used, the information about the material properties of the layered materials forming the semiconducting channel and the insulators used enter in different ways. While NEGF is usually based upon a tight binding Hamiltonian describing the system, a Monte Carlo approach requires the band structure and the respective scattering rates. The DD method needs several macroscopic material parameters, such as the density of states (DOS), the band gaps and offsets, the effective masses and the mobilities of the involved materials [285]. In the following some of the aforementioned methods will be discussed in more detail, the NEGF approach as an example for a quantum mechanical description, drift diffusion models as a commonly used classical approach, and finally an overview of available compact models for 2D material-based FETs will be provided.

3.3.1 Non-Equilibrium Green's Functions

Since transistors exchange charge carriers and energy with the contacts, this system needs to be described using an open boundary Schrödinger equation [282]. A commonly used formulation of the open boundary Schrödinger equation is based on the NEGF formalism

$$\boldsymbol{G}E = \boldsymbol{G}\boldsymbol{H} + \boldsymbol{G}\boldsymbol{\Sigma} + \mathbf{1}. \tag{3.16}$$

Here, $\boldsymbol{\psi}$ is the wave function of one electron with energy E flowing through the device, H the Hamiltonian containing all of the information about charge transport in the semiconducting 2D material, $\boldsymbol{G}$ the Green's function, and $\boldsymbol{\Sigma}$ is the self-energy that accounts for all particle and energy exchange with the surrounding. In this context, $\boldsymbol{\Sigma}$ also describes the effect of the electrode states on the electronic structure in the device region. This self-energy can be decomposed into the self-energies of the source and drain contacts $\boldsymbol{\Sigma}_\mathrm{S}$, $\boldsymbol{\Sigma}_\mathrm{D}$ and, if inelastic scattering is taken into account, it is introduced via another contribution to the self-energy, $\boldsymbol{\Sigma}_\mathrm{ph}$, resulting in $\boldsymbol{\Sigma} = \boldsymbol{\Sigma}_\mathrm{S} + \boldsymbol{\Sigma}_\mathrm{D} + \boldsymbol{\Sigma}_\mathrm{ph}$. Within the NEGF formalism the open boundary Schrödinger equation solved by finding the retarded Green's function which can be expressed as [284]

$$\boldsymbol{G}(E) = [E\boldsymbol{I} - \boldsymbol{H} - \boldsymbol{\Sigma}]^{-1} = \left[E\boldsymbol{I} - \boldsymbol{H} - \boldsymbol{\Sigma}_\mathrm{S} - \boldsymbol{\Sigma}_\mathrm{D} - \boldsymbol{\Sigma}_\mathrm{ph}\right]^{-1}. \tag{3.17}$$

Thus, for modeling transport through a device by means of the NEGF formalism, first the Hamiltonian $\boldsymbol{H}$ describing the system needs to be calculated, then a self-energy matrix $\boldsymbol{\Sigma}$ is determined, and finally Equation (3.17) is inverted. In Figure 3.6 (a) the quantities for describing a 2D material-based FET within the NEGF formalism are illustrated.

In the first step, the Hamiltonian of the system under investigation needs to be defined on an atomistic basis set [286]. This Hamiltonian can be formulated using several approaches, among them are the Extended Hueckel theory [293, 294], which uses a sparse tight binding Hamiltonian via a semi-empirical fit [295, 296] or with an *ab initio* multi-scale tight binding method, where the Hamiltonian, obtained with DFT in a Bloch base of eigenstates is transformed into a basis of maximally localized Wanner functions (MLWFs) [290, 297]. Rather

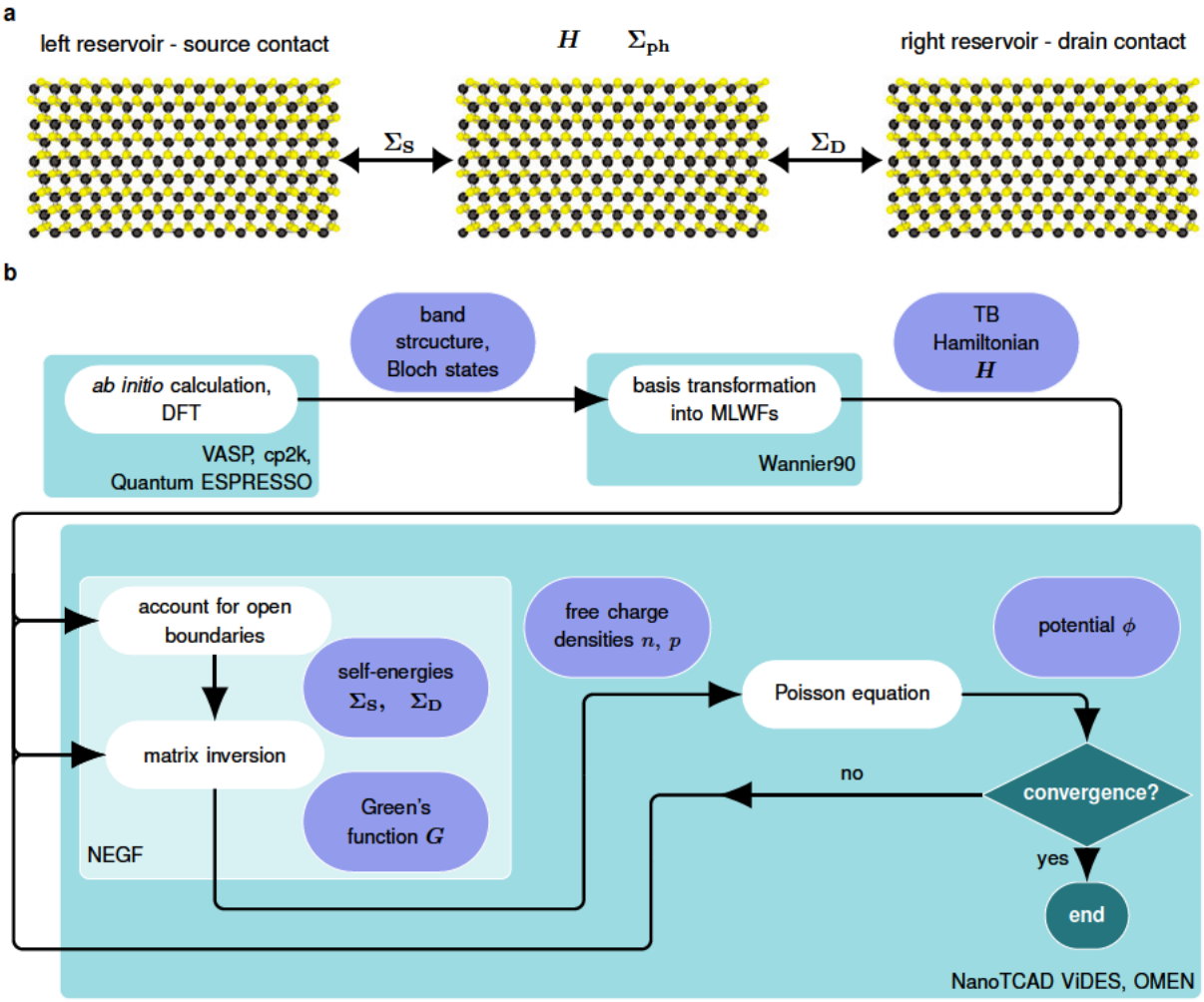

Figure 3.6. **(a)** Within the NEGF approach, the transport through a semiconducting 2D channel, here consisting of a monolayer of MoS_2 (Mo - black, S - yellow), is described by the Hamiltonian **H**. This simulation area is coupled to the semi-infinite leads to the left and right using the self-energies Σ_S and Σ_D. Optionally, electron-phonon scattering can be considered as a contribution to the self-energy Σ_{ph} [284, 286]. **(b)** In this flowchart a schematic simulation process based on NEGF is shown. In the multi-scale modeling approach shown here, *ab-initio* DFT calculations, which can be performed for example using VASP [287], cp2k [288] or Quantum ESPRESSO [289], are the starting point of the transport simulation. The resulting band structure and Bloch eigenstates are transformed into a MLWF basis to obtain the TB Hamiltonian [290]. This TB Hamiltonian is the starting point for the self-consistent solution of the NEGF equations together with Poisson's equation, for example using NanoTCAD ViDES [291] or OMEN [292].

than the delocalized Bloch states, these MLWFs are centered on the actual positions of atoms and bonds in the semiconductor [298]. A basis transformation into Wannier functions is performed with unitary matrices which are not uniquely defined and as different choices lead to different degrees of localizations of the Wannier functions, it is key to finding the set of transformation matrices leading to the MLWFs. For performing this basis transformation of the band structure into MLWFs, usually open source codes such as Wannier90 are used [290].

As soon as a sparse Hamiltonian in a suitable basis representation is obtained, it is used in the next step to calculate the self-energy matrices which account for the open boundary

conditions, coupling the device region to the contacts. In the most general case one can use the transfer Hamiltonian formalism at a higher computational cost [299] or if the structure is periodic in the transport direction, the fastest method known so far is based on closed form algebraic expressions derived by Luisier *et al.* [300]. Finally, the right hand side of Equation 3.17 is inverted most efficiently using the recursive Green's function method [301]. Based on the Green's function $\boldsymbol{G}(E)$, all relevant quantities can be computed, such as the free electron and hole concentrations $n(\boldsymbol{r})$, $p(\boldsymbol{r})$, the transmission coefficients, and thus the current through the device. These calculated free charge carrier concentrations can then be included in a self-consistent scheme with the Poisson equation. In such a self-consistent loop a new potential is obtained as the solution to the Poisson equation. Subsequently, the potential is used as an input to update the Green's function and this loop is repeated until the solutions of both equations converge. This self-consistent solution of the NEGF formalism is required for the quantum mechanical description of nanoscaled FETs and is available in several open-source solvers including NanoTCAD ViDES [291] and OMEN [292]. A flowchart of the simulation chain for describing a 2D FET using NEGF is shown in Figure 3.6 (b).

The NEGF formalism, as presented here, is based upon two assumptions, namely the single particle approach and the near-field approximation, thus it is not valid for strongly correlated transport, such as for example in the case of the Coulomb blockade regime in single electron transistors [285]. Moreover, accounting for scattering events within the NEGF formalism is possible via contributions to the self-energy. However, as such calculations are computationally costly, NEGF is typically used to describe devices in the ballistic regime. NEGF has been widely used to model nanoscaled electronic devices, in particular for establishing their performance and scaling limits [TKJ2, 302, 303]. For example, NEGF was used to simulate transport in transistors based on graphene [286, 304], TMDs [302, 305, 306], monoelemental 2D materials called Xenes, such as BP [307, 308], and semiconducting heterostructures built from layered materials [309, 310]. In this work, the NEGF formalism has been applied to calculate the current density flowing through three atomic layers of hBN, contacted by gold and silicon, see Section 6.2.2.

3.3.2 Drift Diffusion Models

In the semiclassical picture, electronic devices are modeled by solving the Boltzmann transport equation (BTE). However, the BTE is a highly complex equation in the phase space spanned by seven variables (position, momentum, and time) and thus cannot be solved analytically for realistic geometries of electronic devices. Instead, by applying the moments expansion of the BTE a hierarchically ordered set of models with increasing complexity is obtained, ranging from most computationally efficient to the most physically accurate. First, an integration of the BTE over the entire momentum space results in the moment of order zero, yielding the continuity equations. Next, the first order moment gives the drift diffusion relations, which, combined with the continuity equations and Poisson's equation, form the drift diffusion model. If the second order moment is added as an additional equation to the system, the hydrodynamic model is obtained [311].

The drift diffusion model is the simplest and computationally most efficient approximation of the BTE and is nowadays the most frequently used set of equations to describe transport in semiconductors [312]. As the drift diffusion equations are covered extensively in literature [313, 314, 315], the model derivation is only briefly sketched here. The BTE is in essence a balance equation of the charge carrier flow within phase space and is formulated in a partial differential equation for the carrier distribution function $f(\mathbf{r}, \mathbf{k}, t)$,

$$\partial_t f + \mathbf{u} \cdot \nabla_{\mathbf{r}} f + \frac{\mathbf{F}}{\hbar} \cdot \nabla_{\mathbf{k}} f = \hat{C} f. \tag{3.18}$$

Here, the left hand side of the equation is the microscopic formulation of Newton's laws of motion, with the second term describing diffusion and the third term the impact of external forces. On the right hand side, the collision operator $\hat{C}$ captures the impact of scattering processes on f. By forming the first moment of Equation (3.18), thus, by multiplying both sides with $\mathbf{v}(\mathbf{k})$ and integrating over $\mathrm{d}^3\mathbf{v}$, the drift diffusion relations are obtained

$$\mathbf{J}_n(\mathbf{r}, t) = -q\left(n(\mathbf{r}, t)\,\mu_{\mathrm{eff},n} \nabla\phi(\mathbf{r}, t) - D_n \nabla n(\mathbf{r}, t)\right), \tag{3.19a}$$

$$\mathbf{J}_p(\mathbf{r}, t) = -q\left(p(\mathbf{r}, t)\,\mu_{\mathrm{eff},p} \nabla\phi(\mathbf{r}, t) - D_p \nabla p(\mathbf{r}, t)\right). \tag{3.19b}$$

Here, parabolic bands in the semiconductor are assumed and the effective charge carrier mobility $\mu_{\mathrm{eff}} = (q\tau)/m^*$, as introduced in Section 3.1.3, is used. The diffusion coefficient D is linked to μ_{eff} via the Einstein relations $D = \mu_{\mathrm{eff}}(k_{\mathrm{B}}T)/q$. In the continuity equations

$$\frac{\partial n(\mathbf{r}, t)}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J}_n(\mathbf{r}, t) + R\left(n(\mathbf{r}, t), p(\mathbf{r}, t)\right), \tag{3.20a}$$

$$\frac{\partial p(\mathbf{r}, t)}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J}_p(\mathbf{r}, t) + R\left(n(\mathbf{r}, t), p(\mathbf{r}, t)\right), \tag{3.20b}$$

the recombination rates of electrons and holes are given by $R\left(n(\mathbf{r}, t), p(\mathbf{r}, t)\right)$ and in the Poisson equation the impact of defect charges and changes in the charge concentrations on the potential distribution is captured

$$\nabla \cdot \left(\varepsilon \nabla \cdot \phi(\mathbf{r}, t)\right) = q\left(n(\mathbf{r}, t) - p(\mathbf{r}, t) - C(\mathbf{r})\right). \tag{3.21}$$

In summary, by inserting the relations (3.19a) and (3.19b) into the continuity equations (3.20a) and (3.20b), in combination with the Poisson equation (3.21), a set of coupled differential equations for the potential and the electron and hole concentrations are obtained. For modeling semiconductor devices these equations are discretized and solved numerically on a grid spanning the entire semiconductor and insulator regions in the device which form the simulation domain. Solving these equations is computationally highly efficient even on large and complex device geometries due to the discretization scheme developed by Scharfetter and Gummel [316]. Discretized in such a way, the equation set is implemented for example in Minimos-NT [317], the simulation framework used for the simulations performed here and presented in Sections 5.1.3 and 6.1. As the solution of the drift diffusion equations requires a geometric model of the device, including a grid representation of the simulation domain, Minimos-NT is part of a tool chain for creating the model before performing drift diffusion simulations. This tool chain can be used for technology computer aided design (TCAD).

In general, the DD model is well suited for the description of transport in prototype FETs based on 2D semiconductors with dimensions on the scale of micrometers. For these devices, charge transport is in the diffusive regime, thus, the DD equations have been used for example to model transport in graphene [318] and in MoS_2 [TKJ12, 319, 320, 321] FETs, see also Section 6.1.

3.3.3 Compact Models

In contrast to the models discussed in the previous two subsections, compact models do not aim for a comprehensive and versatile description of charge transport through nanoscaled semiconductor structures, but are instead highly specialized and simplified analytical expressions which capture selected aspects of FET operation. In general, these models are either used to provide theoretical support for experiments [285, 322], or they serve as the basic building blocks for circuit simulations, for example in SPICE models, which are required for performance estimates at the circuit level [323].

To model FETs in the thermionic regime, where the gate electrode controls the thermionic emission of charge carriers over the energy barrier at the source, the following models are frequently used. A model which takes a particularly simple form in the ballistic limit is the "top of the barrier model", where the drain source current is described by the Landauer-Büttiker equation [324, 325]

$$I_\mathrm{D} = \frac{2q}{h} \int \theta(E)\, g(E) \left(f_\mathrm{S}(E) - f_\mathrm{D}(E) \right) \mathrm{d}E. \tag{3.22}$$

This equation captures a number of fundamental properties of a nanoscaled FET, for example there is no current for equal Fermi levels on both sides, $\left(f_\mathrm{S}(E) - f_\mathrm{D}(E) \right)$. Additionally, the overall current is proportional to the potential number of conducting channels between source and drain, given by the DOS in the device $g(E)$, and to the transmission probability of the system $\theta(E)$ which amounts to 1 for transport over the barrier in the classical limit. In contrast to the previous sections, Equation (3.22) does not provide any spatial information, thus it is applied at a single location of the semiconducting channel, typically the top of the energy barrier between source and drain. This model was used to provide a performance estimate for FETs based on graphene, silicene, and germanene [326] and forms the basis for the analytical models for Schottky barrier 2D FETs in the off-state developed by Penumatcha, Salazar, and Appenzeller [183, 187], see Section 2.3.1. In addition, the top of the barrier model was used to obtain a performance estimate for MoS_2 FETs in the ballistic limit [TKJ18].

Another approximation that is used by most compact models for thermionic FETs is the gradual channel approximation which assumes that the variation of the electric field along the channel is much smaller than the corresponding variation in the direction of the gate, perpendicular to the channel [4]. This assumption allows one to determine the potential and electric field due to the gate voltage in a first step. This field is subsequently used to calculate the drain current, usually assuming diffusive transport and thus a classical drift relation for the current [322, 323]. In order to find closed form expressions for the current, Boltzmann

statistics are often assumed instead of Fermi-Dirac statistics [322, 327]. In addition, solving the Poisson equation can be avoided by modeling the gate stack with a capacitor network. [323, 328].

When describing only the charge carrier emission over an energy barrier at a heterojunction or across a diode formed by two different 2D materials, Richardson's approach was adapted to 2D materials, deriving different expressions for electron emission over the 2D surface or edge [329, 330]. If tunneling is the dominant phenomenon to be investigated, for example in tunnel transistors, the Wentzel-Kramers-Brillouin (WKB) approximation is often used [331, 332]. Within the WKB approximation the transmission coefficient for electron tunneling through a barrier with the shape $W(x)$ and effective mass m_{diel} is given by

$$\theta(E) = \exp\left(-\frac{2}{\hbar}\int_{x_1}^{x_2}\sqrt{2m_{\text{diel}}\left(W(x)-E\right)}\mathrm{d}x\right). \tag{3.23}$$

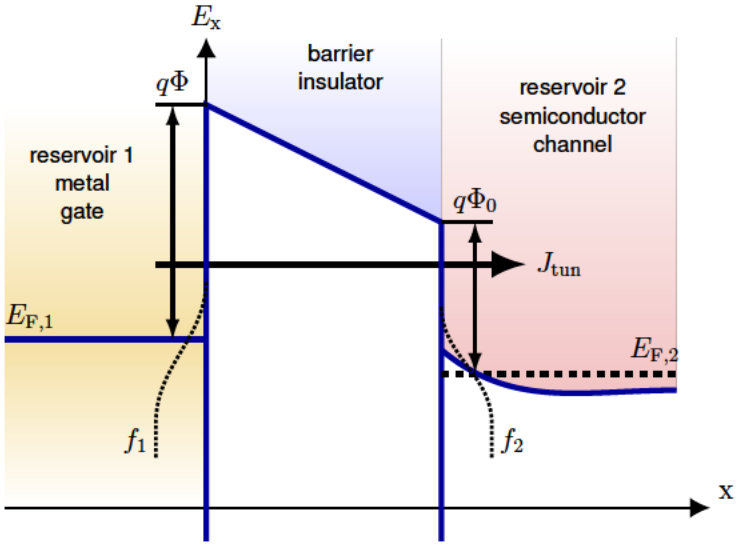

Figure 3.7. Within the Tsu-Esaki model the tunneling current through an energy barrier formed by an insulator between two reservoirs is modelled. In this example it was assumed that the two reservoirs are formed by the gate metal contact (reservoir 1) and the semiconducting channel (reservoir 2). For the transmission coefficient the WKB approximation is typically used and the barrier heights for electrons from both sides are given by Φ and Φ_0 which depend on the respective band alignment and the applied gate voltage V_G.

A schematic barrier of trapezoidal shape, which is typical for direct tunneling through an insulator between two semiconducting or metallic contacts, is shown in Figure 3.7. The integration is only performed for the classically forbidden region, thus for $E < W(x)$ where the integrand is real. For direct tunneling through a trapezoidal barrier Equation (3.23) can be written as [333]

$$\theta(E) = \exp\left(-\frac{2}{\hbar}\int_{0}^{t_{\text{diel}}}\sqrt{2m_{\text{diel}}\left(q\Phi - q\frac{V_G}{t_{\text{diel}}}x - E\right)}\mathrm{d}x\right), \tag{3.24}$$

which, when solving the integral, evaluates to

$$\theta(E) = \exp\left(-\frac{4t_{\text{diel}}\sqrt{2m_{n,\text{diel}}}}{3\hbar q V_{\text{G}}}\left(\left(q\Phi - E\right)^{3/2} - \left(q\Phi_0 - E\right)^{3/2}\right)\right), \tag{3.25}$$

given the thickness of the dielectric barrier t_{diel}, the effective tunneling mass for electrons through the dielectric $m_{\text{n,diel}}$, the applied gate voltage V_{G}, and the respective barrier heights Φ and Φ_0 at the left and right reservoirs, see Figure 3.7. Equation (3.25) is the central element of the Tsu-Esaki model which describes the tunneling current between two semiconducting or metallic regions. It was developed by Tsu and Esaki to compute the current through a finite semiconducting superlattice [334] and was used in [TKJ2] to provide a performance estimate of the current blocking potential of scaled hBN layers and other insulators in nanoscaled transistors, see the discussion in Sections 4.1 and 6.2.

The Tsu-Esaki model assumes that the momentum orthogonal to the transport direction is conserved. Furthermore, the barrier's band structures close to the band edges, need to be sufficiently parabolic to define an effective tunneling mass. In this context, the current density through the barrier in the x direction, see Figure 3.7, is given by [333, 335]

$$J_{\text{tun}} = q\iiint \theta(k_x)\, v_x M(\mathbf{k})\left(f_1(E) - f_2(E)\right)\mathrm{d}^3\mathbf{k}. \tag{3.26}$$

Here, the density of states is given by

$$M(\mathbf{k}) = \frac{2}{L^3\Delta k_x \Delta k_y \Delta k_z} = \frac{1}{4\pi^3}, \qquad \Delta k_x = \Delta k_y = \Delta k_z = \frac{2\pi}{L}, \tag{3.27}$$

with the factor 2 accounting for spin degeneracy. Inserting the relation for the group velocity in the x direction

$$v_x = \frac{1}{\hbar}\frac{\partial E_x}{\partial k_x}, \quad v_x \mathrm{d}k_x = \frac{1}{\hbar}\mathrm{d}E_x, \tag{3.28}$$

and replacing the remaining in-plane coordinates (y, z) with polar coordinates, using $E_\rho = \frac{\hbar^2 k_\rho^2}{2m_n}$, one arrives at

$$\begin{aligned} J_{\text{tun}} &= \frac{q}{4\pi^3\hbar}\int_{E_{\min}}^{E_{\max}} \theta(E_x)\int_0^\infty\int_0^{2\pi}\left(f_1(E) - f_2(E)\right)k_\rho \mathrm{d}k_\rho \mathrm{d}\phi \mathrm{d}E_x = \\ &= \frac{q}{4\pi^3\hbar}\int_{E_{\min}}^{E_{\max}} \theta(E_x)\frac{2\pi m_n}{\hbar^2}\int_0^\infty\left(f_1(E) - f_2(E)\right)\mathrm{d}E_\rho \mathrm{d}E_x = \\ &= \frac{4\pi m_n q}{h^3}\int_{E_{\min}}^{E_{\max}} \theta(E_x)\, N(E_x)\,\mathrm{d}E_x. \end{aligned} \tag{3.29}$$

The final expression in Equation (3.29) is called Tsu-Esaki equation and describes the tunneling current through an energy barrier between two reservoirs with the transmission coefficient

given by the WKB-coefficient in Equation (3.25) and the supply function defined as

$$N(E_x) = \int_0^\infty \left(f_1(E) - f_2(E)\right) \mathrm{d}E_\rho = k_\mathrm{B} T \left(\frac{1 + \exp\left(-\frac{E_x - E_{\mathrm{F},1}}{k_\mathrm{B} T}\right)}{1 + \exp\left(-\frac{E_x - E_{\mathrm{F},2}}{k_\mathrm{B} T}\right)} \right). \tag{3.30}$$

In Equation (3.29) the integration boundaries are given by the considered barrier, for example in the case of direct electron tunneling, as depicted in Figure 3.7, $E_\mathrm{min} = E_\mathrm{CB}$ is given by the conduction band edge of the semiconductor reservoirs and $E_\mathrm{max} = q\Phi_0$ by the conduction band edge of the insulator. This equation was implemented in the compact modeling framework Comphy [TKJ13] to perform the calculations reported in [TKJ2], see Section 6.2.

3.4 Charge Transfer Models

Charge traps directly at the interface and in the surrounding insulators of the semiconducting channel critically influence the operation, stability and reliability of FETs based on 2D materials, see Section 4.2. Interface traps impact the subthreshold swing of the FET, see Section 3.1.1, and therefore need to be included in modeling approaches describing the operation of 2D FETs. At the same time, charge trapping at border traps is the main mechanism responsible for noise, hysteresis, and BTI, see Sections 3.2.1 and 3.2.3. Thus, they affect the stability and reliability of 2D FETs. Accurate models to describe charge transfer mechanisms are, therefore, of utmost importance for the prediction of the stability of 2D FETs.

Here, initially the most basic model for charge transfer, the Shockley-Read-Hall (SRH) model, is introduced. The SRH model is widely used to model charge trapping at interface traps. However, the SRH model is unsuitable for describing charge transfer to border and insulator traps, as it can neither reproduce the bias nor the temperature dependence observed in experiments [224]. This led to the development of the more realistic non-radiative multi-phonon (NMP) model, discussed at the end of this section, which accurately captures both the temperature and bias dependence of charge transfer to border traps in the gate insulator. Recently, it was reported that the NMP model should also be used when modeling interface states [336]. Both models described here, are implemented in the drift diffusion TCAD solver Minimos-NT [317] and were used to model interface traps and oxide traps in MoS_2/SiO_2 transistors, see Section 6.1. At the same time, these models are critical for understanding the mechanisms of charge trapping in general. In particular, defect modeling is central to the idea to improve the stability of 2D material-based FETs by Fermi level tuning, see Section 5.1.3 and the NMP model is needed to interpret the experimental data of Section 5.2.2.

3.4.1 Shockley-Read-Hall Model

The Shockley-Read-Hall (SRH) model was first proposed by Hall [337], Shockley and Read [11] in 1952. It provides a statistical description of the recombination of electrons and holes in a semiconductor through a recombination center, thus a trap level, in the band gap. Originally it was derived for trap levels in bulk semiconductors but can also be applied to

defects at the semiconductor interface. Furthermore, it was used to model defects in the surrounding insulators by introducing a WKB tunneling factor for the charge exchange [223, 338]. However, it has been comprehensively demonstrated that as the extended SRH model lacks a description of structural relaxation effects, it is incapable of capturing the physics of charge exchange with insulator traps [224, 339]. For the same reasons, the SRH model gives rise to errors when used to describe interface traps [336]. Irrespective of their spatial location within the bulk semiconductor, at the interface or in the insulator, charge traps have a charged and a neutral state. In general, electron traps or acceptor-like traps have a negatively charged and a neutral charge state and hole traps or donor-like traps have a neutral and a positively charged state. However, the charge trapping mechanisms are exactly the same for both trap types, only the accessible charge states (-/0) or (0/+) differ. In addition to the distinction of the trap type, the SRH model distinguishes four different charge transfer processes, depending on the reservoir involved. If the charge is transferred between the trap level and the valence band, hole capture and hole emission processes are observed. If instead the charge is transferred to the conduction band, electron capture and electron emission are investigated.

Here, the charge transfer rates are presented for hole capture and emission at a single hole trap or donor-like trap, but these expressions could be extended in a straightforward way to all other processes listed above. This hole trap can be in two states, either neutral, state i, or positive, state j, and for both expectation values f_i and f_j, their sum must equal 1, $f_i + f_j = 1$. A hole can move between the valence band and the trap, at the energy level E_T, according to the following differential rates [224]

$$\mathrm{d}k_{i,j}(E) = c_p(E)\, f_p(E)\, g_p(E)\, \mathrm{d}E \tag{3.31a}$$

$$\mathrm{d}k_{j,i}(E) = e_p(E)\left(1 - f_p(E)\right) g_p(E)\, \mathrm{d}E \tag{3.31b}$$

with the capture and emission probabilities for holes $c_p(E)$, $e_p(E)$, respectively, the Fermi-Dirac distributions of electrons and holes $f_n(E)$, $f_p(E)$, and the density of states in the valence band, $g_p(E)$. All involved physics of the charge transfer process are modeled within the capture and emission probabilities $c_p(E)$, $e_p(E)$. Here, the basic assumption of the SRH model is that hole capture from the valence band, that is the transfer of an electron from the defect state into the valence band, occurs without a barrier [11]. Thus, the hole capture probability is directly proportional to a capture cross section, σ, times the thermal velocity of the electrons, $v_\mathrm{th} = \sqrt{8 k_\mathrm{B} T / (\pi m_n)}$, [222]

$$c_p(E) = v_\mathrm{th}\sigma. \tag{3.32}$$

Inserting Equation (3.32) into Equation (3.31a) and integrating over the entire valence band gives

$$k_{i,j} = v_\mathrm{th}\sigma p = v_\mathrm{th}\sigma N_\mathrm{V} \exp\left(\frac{E_\mathrm{V} - E_\mathrm{F}}{k_\mathrm{B} T}\right), \tag{3.33}$$

an analytical expression for the rate of hole capture with the effective density of states in the valence band N_V. Based on this assumption, also the rate for hole emission can be derived using the relations $f_p(E) = 1 - f_n(E)$ and $f_n(E) / \left(1 - f_n(E)\right) = \exp\left(-(E - E_\mathrm{F}) / (k_\mathrm{B} T)\right)$ for Fermi-

Dirac distributions. In addition, the principle of detailed balance holds, as both transitions form a closed system. Hence, the emission process can be related to the capture process, which is given by

$$e_p(E) = c_p(E) \exp\left(\frac{E - E_T}{k_B T}\right). \tag{3.34}$$

By using these relations, the rate of hole emission can be calculated as

$$\begin{aligned} \mathrm{d}k_{j,i}(E) &= e_p(E) f_n(E) g_p(E) \mathrm{d}E \\ &= \upsilon_{th}\sigma \exp\left(-\frac{E_T - E_F}{k_B T}\right) f_p(E) g_p(E) \mathrm{d}E. \end{aligned} \tag{3.35}$$

Therefore, an integration over the entire valence band gives

$$k_{j,i} = \upsilon_{th}\sigma p \exp\left(-\frac{E_T - E_F}{k_B T}\right) = \upsilon_{th}\sigma N_V \exp\left(\frac{E_V - E_T}{k_B T}\right). \tag{3.36}$$

Equations (3.33) and (3.36) are the SRH expressions for the charge transfer rates of holes between the valence band and the defect level. Intuitively, they give a constant rate for electrons falling from the defect level to the valence band, see Equation (3.33), and a thermally activated transition from the valence band to the defect level, see Equation (3.36).

The phenomenon of charge trapping at defect states within the band gap of the semiconductor, does not only describe an important non-ideality in FETs, but is also vital for the generation and recombination of charge carriers. By calculating the charge transfer rates and balance equations for all four charge exchange processes, namely hole and electron capture and emission, the SRH recombination rate is obtained as [11]

$$R^{SRH} = \frac{np - n_{int}^2}{\tau_p (n + n_{aux}) + \tau_n (p + p_{aux})}. \tag{3.37}$$

Here, τ_n denotes the electron lifetime given by $1/\tau_n = \sigma_n \upsilon_{th}^{n} N_t$ and τ_p the hole lifetime, $1/\tau_p = \sigma_p \upsilon_{th}^{p} N_t$. These lifetimes are indirectly proportional to the charge transfer rates for electrons and holes to the defect states, as given in Equations (3.33) and (3.36). However, in Equation (3.37) not a single charge trap level with the defect level E_T is considered but many defects with a defect density of N_t. In addition, Equation (3.37) uses the intrinsic charge density n_{int} and the auxiliary charge concentrations $n_{aux} = n_{int} \exp(-(E_T - E_{int})/(k_B T))$ and $p_{aux} = p_{int} \exp(-(E_{int} - E_T)/(k_B T))$ with E_{int} denoting the middle of the band gap. In a DD model the SRH recombination rate, see Equation 3.37, is part of the term $R(n(\mathbf{r}, t), p(\mathbf{r}, t))$ on the right hand side of Equations (3.20a) and (3.20b). In the Minimos-NT implementation [317], interface traps are modeled according to the theory. The defect levels are often assumed to obey a Gaussian distribution with certain cutoff limits to be considered.

For the simulations performed in this work, see Section 6.1, the SRH model was used to model interface traps. However, soon after its development it was extended to insulator defects [223]. Thereby, tunneling of carriers from the reservoir to the defect site in the insulator is typically accounted for using a WKB coefficient to modify the capture cross sections, $\sigma = \sigma_0 \theta(E)$ with

θ given by Equation (3.25). However, within the SRH framework, capture and emission coefficients are directly correlated, see Equation (3.34), which strongly contradicts experimental observations [215]. Measurements show that capture and emission time constants can be substantially different, ranging from ns to ks and beyond [224]. Additionally, the strong gate bias and temperature dependence of charge transfer mechanisms cannot be explained by the SRH theory, ultimately raising questions about its validity and physical correctness. This led to the development of the NMP model, as presented in the next section, which provides a more accurate understanding of the involved mechanisms.

3.4.2 Non-Radiative Multi-Phonon Model

The non-radiative multi-phonon (NMP) theory takes into account that charge trapping at defects in the insulator affects the surrounding electrons and nuclei [222, 224]. Therefore, the exchange of an electron between a defect in the insulator and a carrier reservoir like the conduction band of the semiconducting channel is also accompanied by local deformations and relaxations of the defect site. The coupling of electrons and phonons plays a fundamental role in the characteristics of charge transfer reactions. Hence, a thorough physical description needs to include all electrons and nuclei involved in such a mechanism. As electrons move much faster than the nuclei, the Born Oppenheimer approximation can be applied, allowing to treat both systems separately. Within this approximation, atomic nuclei move within an adiabatic potential energy surface (PES) which is a complex $3N$ dimensional surface for a system consisting of N atoms. However, this system needs to be further simplified to allow for the formulation of a computationally feasible model. Towards this aim, the multi-dimensional system is mapped onto an effective one-dimensional (1D) reaction path [340]. By considering the adiabatic potential along such a 1D path, the so-called configuration coordinate (CC), a 1D potential energy curve (PECs) can be obtained, which then defines the dynamics of charge trapping [341].

The current state-of-the art description, the 4-state NMP model, accurately captures the physics of the charge capture and emission processes at pre-existing defects in the oxide [239, 341]. This model was developed based on the first formulation of NMP theory for the description of $1/f$ noise and RTN by Kirton and Uren [222] and was later used to model threshold voltage drifts by Tewksbury, Lee, and Member [342]. Recently, it has been debated whether the 4-state NMP model in its full complexity is necessary to describe charging kinetics related to BTI or whether a simplified 2-state variant is sufficient [TKJ13]. In general, within the 4-state model two types of transitions are considered. On the one side, charge transfer reactions across different PECs, representing different charge states of the defect. On the other side, thermally activated structural reconfigurations within a single PEC, see Figure 3.8. As the name implies, the charge transfer or non-radiative multi-phonon transitions across different PECs are central to the NMP model and are hence the only transition included in the 2-state variant of the model. Additional to these transitions, the full 4-state model also comprises two metastable states that are connected with the stable states via thermal relaxations of the defect structure. It is worth noting that the 2-state model is sufficiently accurate for standard BTI characterizations of a large ensemble of defects [TKJ13]. However, certain observations

such as switching defects, anomalous BTI behavior and anomalous RTN typically require additional metastable configurations, hence a description within the 4-state NMP model [239]. In the following, the physics of a non-radiative multi-phonon transition are described and the expressions for the 2-state model introduced. Then, the experimental evidence for the 4-state model is presented and the 4-state model is explained in detail, as this model was used for the modeling of charge transfer to insulator defects in Sections 5.1.3 and 6.1.

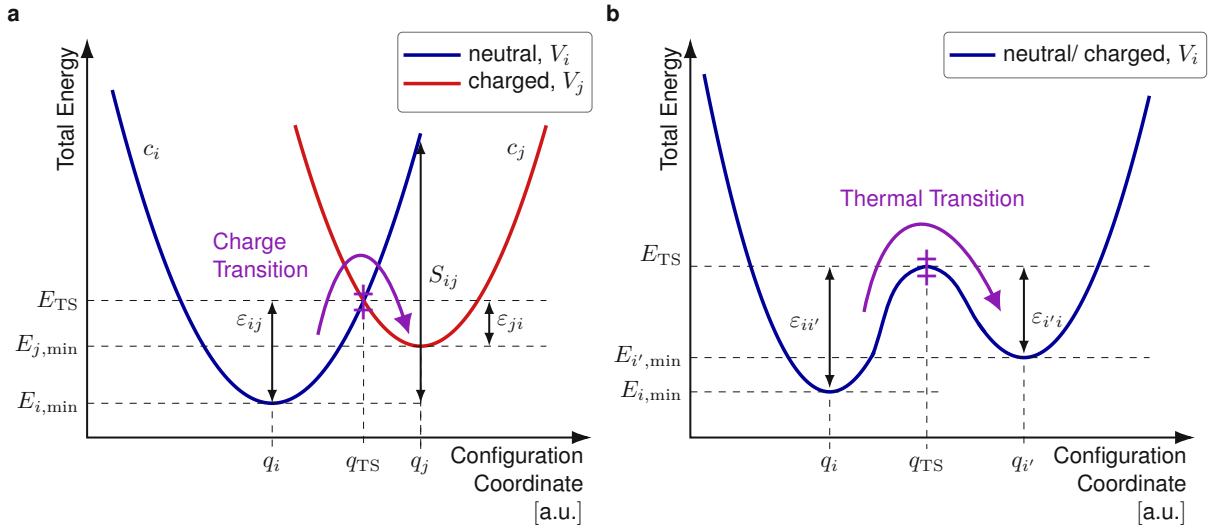

Figure 3.8. **(a)** Two potential energy curves (PECs) are involved in charge transitions. Here, the PECs are approximated as harmonic oscillators and which serve as basis for the NMP transitions of the insulator defect during a hole capture process. For the two parabolas, the minima are located at the energies $E_{i,\text{min}}$, $E_{j,\text{min}}$ at the respective coordinates. Within the classical limit, the transition takes place at the intersection point with the transition state energy E_{TS} and q_{TS}. Using the harmonic approximation, the two PECs and their respective transition barriers ε_{ij}, ε_{ji} are defined by the relaxation energy S_{ij}, the curvatures c_i, c_j and the energy minima of the parabolas. **(b)** Thermal transitions are structural relaxations within a single PEC. Energy barriers for the thermal transition at the transition state with E_{TS} and q_{TS} are given by $\varepsilon_{ii'}$, $\varepsilon_{i'i}$.

In a NMP transition, charges are captured or emitted, thus the system changes from one adiabatic potential energy curve to another one [341, 343]. Such charge exchange processes are assumed to be instantaneous and preferably occur close to the intersection point of the involved PECs [341, 344]. Within a first order perturbation approach, Fermi's golden rule can be applied to calculate the transition rate $k_{i\alpha,j\beta}$ for the system consisting of both electrons, described by the wave functions $|\Phi_i\rangle, |\Phi_j\rangle$, and nuclei represented by $|\eta_{i,\alpha}\rangle, |\eta_{j,\beta}\rangle$

$$\begin{aligned} k_{i\alpha,j\beta} &= \frac{2\pi}{\hbar}|M_{i\alpha,j\beta}|^2 \delta\left(E_{i,\alpha} - E_{j,\beta}\right), \\ |M_{i\alpha,j\beta}|^2 &= \langle\eta_{i,\alpha}|\langle\Phi_i|\hat{H}|\Phi_j\rangle|\eta_{j,\beta}\rangle. \end{aligned} \tag{3.38}$$

Here, the Hamiltonian $\hat{H}$ describes the perturbation which couples the electronic states denoted by i and j with the vibrational states α and β. The delta function ensures that the energy is conserved throughout the transition, where $E_{i,\alpha}$ and $E_{j,\beta}$ include the phonon as well as the electronic contribution to the total energy. Due to the different time scales of the movement of electrons and nuclei, the Born-Oppenheimer approximation can be applied,

allowing to split the wave function into the product of an electronic and a nuclear wave function. As the electronic states can be assumed to vary weakly with the nuclei coordinates, the Franck-Condon principle is applicable, and the matrix element $M_{i\alpha,j\beta}$ in the charge transfer rates can be split into a product of an electronic and a vibrational transition

$$M_{i\alpha,j\beta} = \langle \Phi_i | \hat{H}_{\mathrm{el}} | \Phi_j \rangle \langle \eta_{i,\alpha} | \eta_{j,\beta} \rangle. \tag{3.39}$$

As a consequence, Equation (3.38) can be reformulated as the product $k_{i\alpha,j\beta} = A_{ij} f^{LSF}_{i\alpha,j\beta}$ of the electronic matrix element A_{ij}, which describes the instantaneous electronic excitation, and the lineshape function $f^{LSF}_{i\alpha,j\beta}$, which contains all vibrational interactions caused by the lattice reconfigurations. For describing charge trapping rates all vibrational modes of a potential representing one electronic state need to be taken into account [341, 345], thus summing over all modes β weighted with a Boltzmann factor. Thus, the NMP rate is given by

$$k_{ij} = A_{ij} f^{LSF}_{ij}, \tag{3.40a}$$

$$f^{LSF}_{ij} \mathrel{\hat{=}} \underset{\alpha}{\mathrm{ave}} \left(\sum_{\beta} |\langle \eta_{i,\alpha} | \eta_{j,\beta} \rangle|^2 \delta \left(E_{i,\alpha} - E_{j,\beta} \right) \right), \tag{3.40b}$$

$$A_{ij} \mathrel{\hat{=}} \frac{2\pi}{\hbar} |\langle \Phi_i | \hat{H}_{\mathrm{el}} | \Phi_j \rangle|^2. \tag{3.40c}$$

In a FET, the matrix element A_{ij} defines the coupling strength between a band state in the conduction or valence band of the semiconductor and the electronic wavefunction of the electron at the defect site at the energy E_{T}. As the wave function of the insulator defect is highly localized and the distance between the defect and the delocalized states in the band is large on an atomic length scale [341, 344], this expression can be calculated using the WKB approximation $A_{ij} \approx A_0 \theta_{ij}(E, E_{\mathrm{T}})$.

In comparison, the calculation of the line shape function is more complex, as it requires the evaluation of the quantum mechanical eigenstates of the PECs, $|\eta_{i,\alpha}\rangle$. Analytic solutions to this problem only exist for simple approximations of the PEC, for example for a harmonic PEC. Thus, for TCAD applications the PECs are approximated as parabolas at the respective minima. In the classical limit, the line shape function degenerates into a thermally broadened peak at the intersections of the two parabolas. However, this neglects the fact that the vibrational wave functions can already overlap below the intersection point. In the quantum-mechanical formulation, the line shape function is evaluated as the overlap integral of the nuclear wave functions with the largest contribution coming from the wave functions at energy levels close to the classical intersection point. These overlaps allow for a transition of the system at an effectively lower energy barrier, a phenomenon that is termed “nuclear tunneling” [229, 341]. It will be demonstrated experimentally that this phenomenon dominates at low temperatures below 100 K, see Section 5.2.2. For calculations at room temperature and above, the Dirac peak is a good approximation for f^{LSF}_{ij}, thus this is implemented in the TCAD framework [317] and was used for the simulations in Sections 5.1.3 and 6.1.

In a transistor, not only two isolated states are involved in charge transfer, but rather charges are captured from or emitted to a whole band of electronic states, namely the conduction and valence band of the semiconductor or the bands of the metal gate. In this context, the

NMP rates depend on the energy of the charge carriers in the reservoir E and on the effective trap level E_T, $k_{ij} = A_{ij}(E, E_\mathrm{T})\, f_{ij}^{LSF}(E, E_\mathrm{T})$. Thus, the total charge transfer rates are obtained by integrating over all electronic states in the semiconductor bands

$$k_{ij}^{\mathrm{VB}} \approx \int_{-\infty}^{E_\mathrm{V}} g_p(E) f_p(E) A_0\, \theta_{ij}(E, E_\mathrm{T})\, \mathrm{e}^{\frac{-\varepsilon_{ij}(E,E_\mathrm{T})}{k_\mathrm{B}T}}\, \mathrm{d}E, \tag{3.41a}$$

$$k_{ji}^{\mathrm{VB}} \approx \int_{-\infty}^{E_\mathrm{V}} g_p(E) \big(1 - f_p(E)\big) A_0\, \theta_{ji}(E, E_\mathrm{T})\, \mathrm{e}^{\frac{-\varepsilon_{ji}(E,E_\mathrm{T})}{k_\mathrm{B}T}}\, \mathrm{d}E, \tag{3.41b}$$

$$k_{ij}^{\mathrm{CB}} \approx \int_{E_\mathrm{C}}^{\infty} g_n(E) \big(1 - f_n(E)\big) A_0\, \theta_{ij}(E, E_\mathrm{T})\, \mathrm{e}^{\frac{-\varepsilon_{ij}(E,E_\mathrm{T})}{k_\mathrm{B}T}}\, \mathrm{d}E, \tag{3.41c}$$

$$k_{ji}^{\mathrm{CB}} \approx \int_{E_\mathrm{C}}^{\infty} g_n(E) f_n(E) A_0\, \theta_{ji}(E, E_\mathrm{T})\, \mathrm{e}^{\frac{-\varepsilon_{ji}(E,E_\mathrm{T})}{k_\mathrm{B}T}}\, \mathrm{d}E, \tag{3.41d}$$

with the density of states in the valence/conduction band g_p / g_n and the distribution functions of holes/electrons f_p / f_n. Here, simplified rates are shown, invoking the classical limit and thus the line shape function is approximated with the energy barrier ε_{ij} from state i to state j in the Boltzmann factor, in addition to using the WKB approximation for the matrix element.

When approximating the two PECs of the states i and j with two harmonic oscillators, the barrier height at the intersection point of the two parabolas can be formulated analytically. Two quantum harmonic oscillators, as depicted in Figure 3.8 (a), are uniquely defined by the following quantities

$$\begin{aligned} S_{ij} &= \mathscr{S}_{ij}\hbar\omega = c_i \left(q_j - q_i\right)^2, \qquad & R_{ij}^2 &= \frac{c_i}{c_j}, \\ \Delta E_{ji} &= E_{j,\min} - E_{i,\min}. \end{aligned} \tag{3.42}$$

Here, S_{ij} is the relaxation energy with the Huang-Rhys factor $\mathscr{S}_{ij}$, R_{ij} is the curvature ratio and ΔE_{ij} is their energy difference. With these definitions the energy barrier is obtained as

$$\varepsilon_{ij} = \frac{\left(S_{ij} + \Delta E_{ji}\right)^2}{4 S_{ij}} \qquad \text{for} \qquad R_{ij} = 1, \tag{3.43}$$

with $R_{ij} = 1$ being a good approximation for most insulator defects [346]. In addition, the reverse barrier is obtained from ε_{ij} as $\varepsilon_{ji} = \varepsilon_{ij} - \Delta E_{ji}$. It should be noted that the barrier ε_{ij} also depends on the applied electric field $\mathscr{E}$ which changes the defect's trap level in the insulator. In a first approximation the relative energy difference changes linearly with the applied electric field and the defect's depth x, $\Delta E_{ji}(\mathscr{E}) = \Delta E_{ji}(\mathscr{E} = 0) - q x \mathscr{E}$.

As the numerical integration over the entire conduction or valence band is computationally costly, a further simplification of Equations (3.41a) - (3.41d) is required. These integrands are dominated by the product $f_{\mathrm{p/n}}(E) A_{ij} f_{ij}^{LSF}(E, E_\mathrm{T})$ which has the largest contribution close to the band edges. In a first order approximation, the so-called band edge approximation, the rates $A_{ij}(E, E_\mathrm{T})\, f_{ij}^{LSF}(E, E_\mathrm{T})$ are assumed to depend in the classical limit only on their respective values at the band edges and can thus be factored out of the integrals. These integrals then evaluate to the carrier concentrations p, n and the charge transfer rates become

analytic expressions. With the energy barriers $\varepsilon_{ij}^{\mathrm{VB}}$ and $\varepsilon_{ij}^{\mathrm{CB}}$ for transitions to and from the valence and conduction band, the transition rates are obtained as

$$k_{ij}^{\mathrm{VB}} = p\, v_{\mathrm{th,p}} \sigma_{0,p} \theta_p \exp\left(-\frac{\varepsilon_{ij}^{\mathrm{VB}}}{k_{\mathrm{B}} T}\right), \tag{3.44a}$$

$$k_{ji}^{\mathrm{VB}} = p\, v_{\mathrm{th,p}} \sigma_{0,p} \theta_p \exp\left(-\frac{\varepsilon_{ji}^{\mathrm{VB}} + E_{\mathrm{F}} - E_{\mathrm{VB}}}{k_{\mathrm{B}} T}\right), \tag{3.44b}$$

$$k_{ij}^{\mathrm{CB}} = n\, v_{\mathrm{th,n}} \sigma_{0,n} \theta_n \exp\left(-\frac{\varepsilon_{ij}^{\mathrm{CB}} - E_{\mathrm{F}} + E_{\mathrm{CB}}}{k_{\mathrm{B}} T}\right), \tag{3.44c}$$

$$k_{ji}^{\mathrm{CB}} = n\, v_{\mathrm{th,n}} \sigma_{0,n} \theta_n \exp\left(-\frac{\varepsilon_{ji}^{\mathrm{CB}}}{k_{\mathrm{B}} T}\right). \tag{3.44d}$$

Here, the NMP transition rates between states i and j are given by $k_{ij}^{\mathrm{NMP}} = k_{ij}^{\mathrm{VB}} + k_{ij}^{\mathrm{CB}}$, $k_{ji}^{\mathrm{NMP}} = k_{ji}^{\mathrm{VB}} + k_{ji}^{\mathrm{CB}}$.

A particular feature of the full 4-state NMP model is the integration of two additional metastable configurations $1'$ and $2'$. These two states are connected to their respective stable states, 1 and 2 via thermally activated structural relaxations within their respective PECs. These purely thermal transitions correspond to reconfigurations of the nuclei at the defect site and the transition rate between the states i and i' is given by

$$k_{\mathrm{ii'}}^{\mathrm{therm}} = \nu_0 \mathrm{e}^{-\varepsilon_{ii'}(k_{\mathrm{B}} T)} \tag{3.45}$$

with the attempt frequency ν_0 and the energy barrier ε_{ij}. For the structural relaxations the energy barrier is assumed to be independent of the applied electric field.

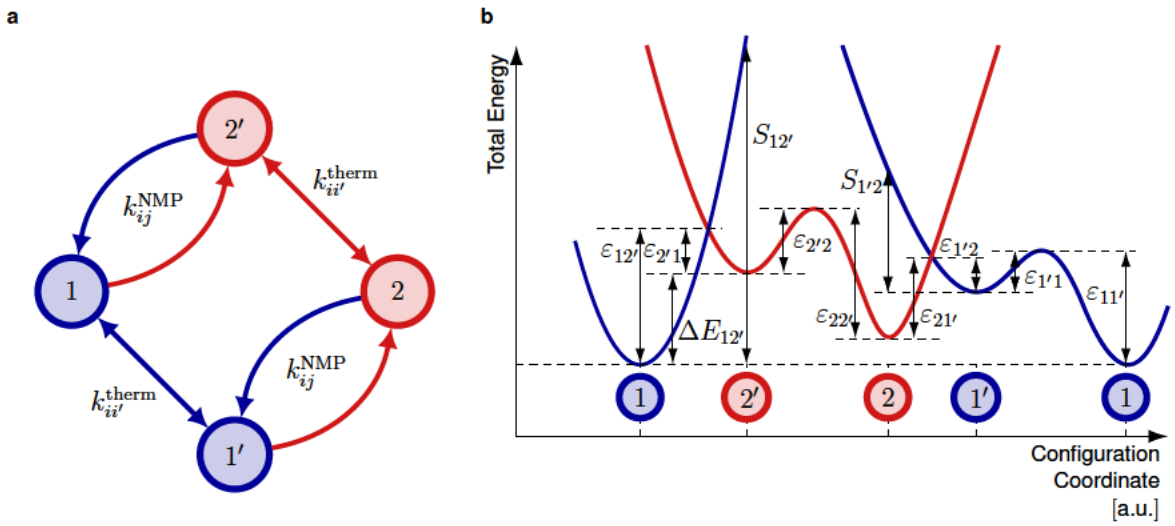

Figure 3.9. **(a)** State diagram showing the NMP transitions between states $2 \rightarrow 1$ via the two possible routes $2 \rightarrow 2' \rightarrow 1$ and $2 \rightarrow 1' \rightarrow 1$ with the two NMP transitions $1 \Leftrightarrow 2'$ and $1' \Leftrightarrow 2$ and the structural relaxations $1 \Leftrightarrow 1'$ and $2 \Leftrightarrow 2'$. **(b)** Configuration Coordinate diagram of a 4-state NMP defect, including all parameters required to unambiguously define the transition rates, including the energy barriers ε_{ij}, the energy difference $\Delta E_{12'}$ and the relaxation energies S_{ij}.

Based on microscopic considerations, it is expected that the atomic defect sites in the insulators will frequently undergo structural relaxations depending on their respective local surroundings and the available (meta-)stable configurations [230, 347]. Especially single defect studies on nanoscaled transistors where many isolated charge transfer reactions are observed, such as RTN [227, 231] and TDDS [259], have provided comprehensive evidence for the involvement of metastable states in charge trapping processes in the oxides. Further compelling evidence for the involvement of metastable states was provided by the observation of two different types of hole traps in pMOS transistors, fixed positive charge traps and switching traps [224, 259]. Fixed positive charge traps are characterized by a comparatively constant emission time τ_e over V_G, whereas switching traps show a rapid decrease of τ_e towards small gate voltages [239]. Both trap types can be explained within the 4-state NMP model, see the diagram in Figure 3.9 (a). In Figure 3.9 (b) a schematic configuration coordinate diagram of a 4-state NMP defect is shown together with all of the relevant parameters which uniquely determine the transition rates for this defect. All parameters highlighted in Figure 3.9 (b), together with Equations (3.42), (3.43), the non-radiative multi-phonon rates given in Equations (3.41a) - (3.41d), and the thermal rates in Equation (3.45) define the 4-state NMP model. Assuming that the system is initially in state 1, the time to reach the stable configuration 2, is called first passage time. In the 4-state NMP model these transitions $1 \Leftrightarrow 2$ always proceed via the metastable states $1'$ or $2'$ and under the assumption that only one transition path is active, the first passage times are given by

$$\tau^i_{\mathrm{c,FPT}} = \frac{k_{1,i} + k_{i,1} + k_{i,2}}{k_{1,i} + k_{i,2}}, \qquad \tau^i_{\mathrm{e,FPT}} = \frac{k_{2,i} + k_{i,2} + k_{i,1}}{k_{2,i} + k_{i,1}} \tag{3.46}$$

with i denoting the metastable state of the active path $1'$ or $2'$. Using these definitions the capture and emission times of the 4-state model are given by

$$\tau_c = \left(\sum_i \frac{1}{\tau^i_{\mathrm{c,FPT}}} \right)^{-1}, \qquad \tau_e = \left(\sum_i \frac{1}{\tau^i_{\mathrm{e,FPT}}} \right)^{-1}. \tag{3.47}$$

These capture and emission times can then be compared with experimental data obtained from single defect studies and can accurately describe RTN, TDDS, 1/f noise, and BTI data. In a simplified two-state model, the capture and emission time constants are given directly as $\tau_C = \tau_{12} = 1/k_{12}$ and $\tau_E = \tau_{21} = 1/k_{21}$ with the NMP rates k_{12}, k_{21} between states 1 and 2.

The extracted parameter sets for the PECs and the energy barriers of the involved stable and metastable configurations within the 4-state model place stringent requirements on defect candidates identified and characterized with *ab-initio* methods. Previous studies have mainly focused on atomic defects responsible for the observed charging dynamics in conventional Si/SiO_2 systems, identifying hydrogen-related defects such as the hydroxyl E' center as one of the most probable defect candidates in amorphous SiO_2 [347, 348]. However, apart from SiO_2 and HfO_2, other insulators are largely unexplored with respect to possible defect structures. At the same time, the problem becomes more complex for 2D FETs, as depending on the alignment of the conduction and valence band edges of various 2D layers, different insulator defects will contribute to device degradation.

Part II
Improving Transistors Based on 2D Materials

4 Suitable Gate Insulators for 2D Transistors

In the early days of semiconductor technology the first transistor prototypes were fabricated based on germanium [7], as germanium provides higher mobilities than silicon. However, germanium's native oxide GeO_2 is water soluble [349] and early studies revealed high interface trap densities on the order of $5 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$ [10]. Thus, it was the passivation of the silicon surface and the formation of a high quality Si/SiO_2 interface [12] which paved the way for the success of integrated circuits, see Section 1.1. In fact, even as the gate oxide transitioned from SiO_2 to high-k gate dielectrics such as HfO_2 the immediate interface to the silicon channel is, to the present day, formed by a silicon oxide compound such as SiON [29]. This shows that the interface of the gate insulator to the semiconductor plays a critical role for the performance of FETs in general and FETs based on 2D semiconductors are no exception [350]. However, up to now, no gate insulator has been identified which would complement 2D semiconductors as well as SiO_2 fits to silicon. For any insulator to serve as a suitable gate insulator to scaled FETs with 2D semiconducting channels, numerous requirements must be met. In Figure 4.1, an overview over the main requirements for competitive gate insulators is provided.

In the following three subsections the requirements for a good gate insulator are discussed based on the three categories, illustrated in Figure 4.1, scaling requirements, minimization of insulator-related charge traps, and requirements for the deposition technology. In the last subsection, potential candidates that can be used as gate insulators in 2D material-based FETs are compared and evaluated with respect to the aforementioned criteria. The discussions in this chapter are based predominantly on the author's work in [TKJ5, TKJ2, TKJ3].

4.1 Scaling Requirements

In order to benefit from a further reduction in the dimensions of a FET in terms of power savings and switching speeds it is essential to preserve the electrostatics of the FET during scaling. Thus, even for scaled dimensions the gate insulator needs to provide excellent gate control, listed as requirement (a) in Figure 4.1. This gate control is quantified by the insulator capacitance which needs to exceed $3\,\mu\mathrm{Fcm^{-2}}$ for the current technology node [21]. As a consequence, a small gate voltage of $V_G < 0.7\,\mathrm{V}$ suffices to provide a charge carrier density in the channel of more than $10^{13}\,\mathrm{cm^{-2}}$. Due to the high insulator capacitance, high charge densities in the channel are preserved and a high on current drive is maintained, targeting

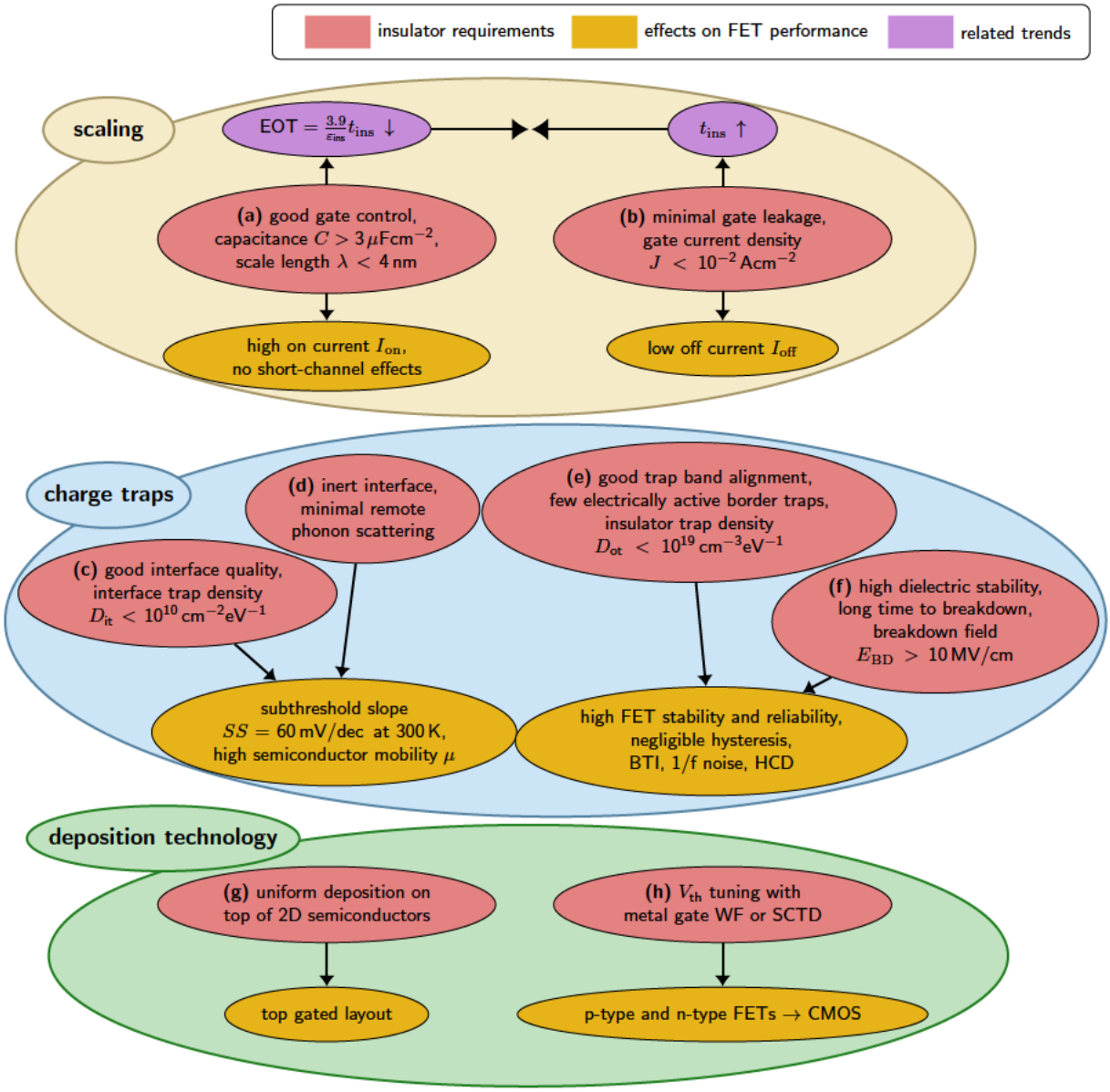

Figure 4.1. Schematic overview over the requirements for competitive gate insulators for 2D nanoelectronics. We identify eight requirements, enumerated with (a) to (h), shown in red. These requirements can be divided into three categories, the insulator requirements caused by the downscaling of the FETs (in light yellow), the requirements of minimizing insulator-related defects and charge traps both at the interface and within the insulator (in blue), and the constraints set by the deposition technology for insulators (in green).

$I_D > 1.2\,$mA/μm. This high capacitance helps to sustain high drain current levels, even as the supply voltage (V_{DD}) is scaled down.

In addition, a certain level of gate control is required to maintain the functionality of the FET, as the gate electrode needs to control the surface potential in the channel region and must not allow the applied drain bias to impact charge injection at the source side. This effect, describing the energy barrier lowering at the source side by V_{DS}, is called drain induced barrier lowering (DIBL) and is one of the most detrimental short-channel effects. DIBL leads to an increased off-current for applied elevated drain biases, thereby deteriorating the switching

performance, and can be quantified using the scale length λ. It describes the channel length where V_{DS} starts to control the surface potential, thus to avoid short channel effects an overall device length three to four times longer than λ, $L > 3$ to 4λ, should be targeted. A common approximation of the scale length for SOI transistors is [185, 351]

$$\lambda = \sqrt{\frac{\varepsilon_{semi}}{\varepsilon_{ins}} t_{semi}\, t_{ins}}. \tag{4.1}$$

It should be noted that this expression for the scale length λ is the same as the approximation for the tunneling width through the Schottky barrier, given in equation (2.6), with $\varepsilon_{semi/ins}$ being the dielectric constants and $t_{semi/ins}$ the thicknesses of the semiconducting channel and the gate insulator respectively. This equality arises because both the scale length and the Schottky barrier width describe the same quantity, namely the portion of the overall barrier which is impacted by the potential applied at the contacts.

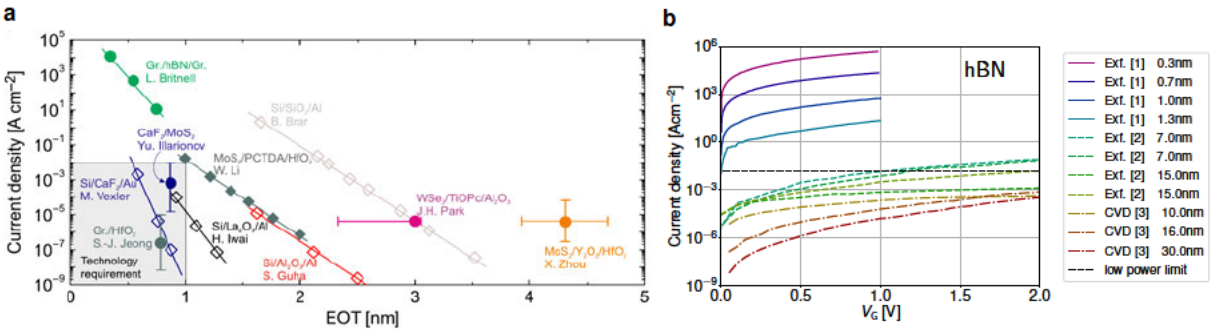

Figure 4.2. **(a)** Comparison of experimental gate current densities through different gate insulators as reported in literature, shown for gate voltages in the range 1 V to 3 V. Data points represented by open symbols were measured on silicon FETs [352, 353, 354, 355] and data given by full symbols on 2D material-based FETs [TKJ7, 129, 356, 357, 358, 359]. Reproduced from [TKJ5]. **(b)** Comparison of the experimental gate current densities through hBN as reported in literature, [1]-[356], [2]-[TKJ2], [3]-[83]. Dashed [TKJ2] and solid lines [356] show currents through exfoliated hBN, while dash-dotted lines show samples fabricated using CVD [83]. Adapted from [TKJ2].

In general, equation (4.1) is an approximation and depends on the exact FET geometry (see Figure 2.3), on whether the FET is single or double-gated, on the use of gated contacts or doped contacts, among many other dependencies. In addition, it also assumes isotropic permittivities, whereas for layered semiconductors or insulators the permittivities are typically highly anisotropic with a higher in-plane than out-of-plane dielectric constant [360]. Depending on the exact device geometry different approximations for λ were derived, for example for an entirely symmetric double gated FET the following expression was obtained [361, 362]

$$\tan\left(\frac{t_{semi}}{2\lambda}\right)\tan\left(\frac{t_{ins}}{\lambda}\right) = \frac{\varepsilon_{ins}}{\varepsilon_{semi}} \tag{4.2}$$

which simplifies to $\lambda = \sqrt{\frac{\varepsilon_{semi}}{2\varepsilon_{ins}} t_{semi}\, t_{ins}}$ for thin layers with $t_{semi} \ll \lambda$ and $t_{ins} \ll \lambda$ where $\tan(x)$ can be expanded into a Taylor series around $x = 0$. For FETs based on 2D semiconductors, the first expansion for $t_{semi} \ll \lambda$ is fully justified as for any 2D semiconductor the layer thickness is at the atomic limit of one monolayer with a thickness of about 0.5 nm [TKJ1]. In addition,

the permittivity of 2D semiconductors is about $10\,\varepsilon_0$ [360], thus the remaining parameters which can be tuned to reduce λ are the insulator properties ε_{ins} and t_{ins}.

Both the reduction of the scale length and the increase in the gate capacitance can only be achieved by reducing the equivalent oxide thickness (EOT), as illustrated in purple in Figure 4.1. The EOT measures the effective thickness of an arbitrary insulator in comparison to SiO_2, with EOT = $\varepsilon_{SiO_2}/\varepsilon_{\text{ins}}\,t_{\text{ins}}$. As the reduction of EOT is an important requirement for efficient scaling, the IRDS roadmap specifies EOT target values for every technology generation. In the IRDS the EOT targets are given indirectly, following from the reported inversion layer thickness which amounts to 1.1 nm for the latest technology node and should decrease to 1.0 nm in 2022 and to 0.9 nm in 2028 [21]. This inversion layer thickness comprises the sum of the EOT and the physical extension of the inversion layer, which amounts to about 0.4 nm, corresponding to the size of an electron orbit [363]. Thus, an EOT of 0.7 nm is targeted in 2020 and should be scaled down to 0.6 nm in 2022 and to 0.5 nm in 2028. Depending on the dielectric constant of the insulator, this corresponds to only few atomic layers of the insulator t_{ins}.

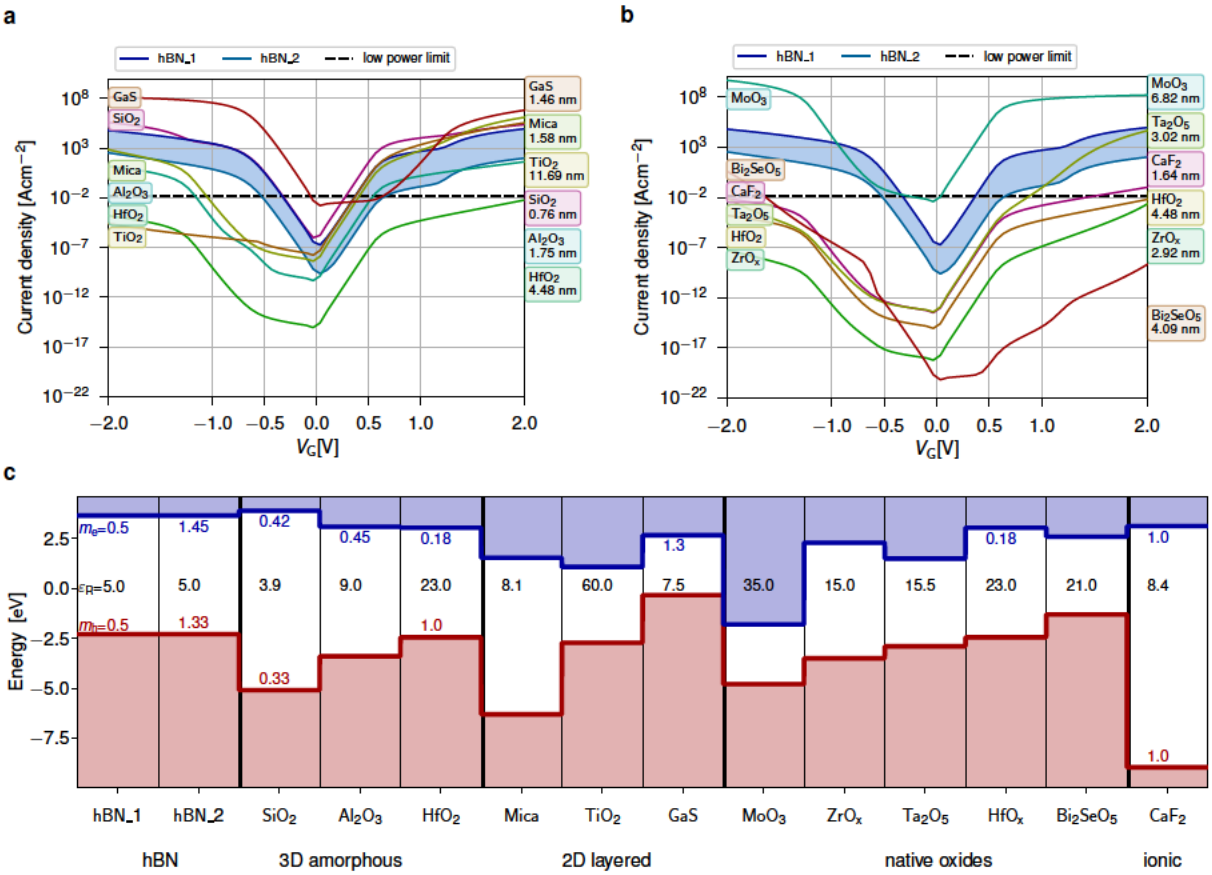

Figure 4.3. **(a)** Calculated gate current densities through different amorphous oxides and layered insulators for an EOT of 0.76 nm. The blue range indicates the interval of tunnel currents for hBN spanned by two different sets of effective tunnel masses. **(b)** Calculated gate current densities through different native oxides and ionic insulators for an EOT of 0.76 nm. If no effective masses were known, the free electron mass was used. **(c)** Band diagram comparing the band alignments, effective masses and dielectric constants for insulators which have been identified as potential candidates for being used as gate insulators in scaled 2D FETs. Adapted from [TKJ2].

As a consequence, this reduction of EOT makes it increasingly difficult to maintain minimal gate leakage currents through the gate insulator, listed as requirement (b) in Figure 4.1. For low-power applications the gate leakage current should be below $10^{-2}\,\mathrm{Acm}^{-2}$ for $V_G < 0.7\,\mathrm{V}$ which relaxes to a limit of $1\,\mathrm{Acm}^{-2}$ for high-power applications [21, 364]. Higher gate leakage currents directly contribute to the off-state drain current I_{off} which determines the standby power consumption of the circuit via $P_D = I_{off} V_{DD}$, thus higher gate leakage increases P_D. In general, the leakage current through the gate insulator consists of tunneling through the energy barrier and thermionic emission over the barrier. However, in real insulators charge traps within the insulator can contribute to the tunneling process, giving rise to trap assisted tunneling (TAT) which often dominates the leakage current [365, 366]. In Figure 4.2 (a) the measured gate current densities, as reported in literature for different gate stacks, are compared as a function of EOT [TKJ5]. Gate leakage currents measured on silicon FETs are shown as open symbols and leakage currents measured on 2D material-based FETs as full symbols [TKJ5]. In Figure 4.2 (b) measured gate current densities through hBN are compared for exfoliated layers and CVD samples. It can be observed that, for the CVD samples, the gate leakage for comparatively thicker layers [83] is comparable to thinner exfoliated samples [TKJ2], presumably due to the better material quality of exfoliated hBN. Depending on the growth method used, the same insulator can show orders of magnitude different gate leakage currents at the same thickness depending on the defect properties, i.e. defect density, thermodynamic trap levels and relaxation energies [367].

However, this strong dependence of the tunnel current density on the insulator defect properties, and thus on the sample quality, makes it difficult to compare the current blocking potential of different insulators. Therefore, in Figures 4.3 (a) and (b) the minimum tunnel currents through different insulators are compared for the ideal case without any defects at an EOT of 0.76 nm. These simulated currents, calculated based on the Tsu-Esaki model as discussed in Section 6.2.1, provide a lower boundary stating how small the tunnel currents can in principle become for the respective insulators under ideal processing conditions. These calculations are based on the band alignment for the different insulators, as shown in Figure 4.3 (c) and on their dielectric constants and effective tunnel masses. It should be noted that calculated tunnel current densities strongly depend on the effective tunnel masses for electrons and holes which are barely known for most insulators compared here. For example, for hBN two limiting sets of tunnel masses are compared, resulting in an interval of around three orders of magnitude for the projected current through scaled hBN layers [TKJ2]. For all materials whose tunnel masses are unknown, effective masses of $1 \times m_0$ were assumed with the free electron mass m_0. Based on these estimates, hBN seems unlikely to be a good choice for scaled insulators [TKJ2] as it allows for excessive leakage currents due to its small dielectric constant of about 5 [368] and small band offsets to most semiconductors, for more details see Section 6.2.

4.2 Reducing Charge Trap Densities and Their Impact

In addition to the criteria for gate insulators related to the scaling of the FETs, good gate insulators minimize the number of electrically active charge traps, both at the interface of the insulator to the layered channel as well as within the insulator itself.

4.2.1 Interface Traps

A suitable gate insulator should form a high quality interface with the van der Waals surface of layered materials, resulting in an interface trap density (D_{it}) of $D_{\mathrm{it}} < 10^{10}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$, listed as requirement (c) in Figure 4.1. On the atomic scale, interface traps are often identified as dangling bonds and P_b centers at the interface with amorphous oxides like SiO_2. Charge traps at the interface typically have short time constants faster than milliseconds. Thus, when performing an $I_{\mathrm{DS}}(V_{\mathrm{G}})$ sweep to evaluate a FET's transfer characteristic, traps charge quasi instantaneously as the Fermi level sweeps through the semiconductor's band gap, thereby slowing down the drain current response to the applied gate voltage. This effect is captured in the subthreshold swing (SS), see Section 3.1.1, with the link between SS and D_{it} being described by [4]

$$SS = 2.3\frac{k_{\mathrm{B}}T}{q}\left(1+\frac{C_{\mathrm{ch}}+q^2D_{\mathrm{it}}}{C_{\mathrm{ins}}}\right), \tag{4.3}$$

with the capacitances of the insulator C_{ins} and the channel C_{ch} per unit area. From Equation (4.3) it can be observed that, in the ideal case for $C_{\mathrm{it}} \ll C_{\mathrm{ch}} \ll C_{\mathrm{ins}}$, the subthreshold swing approaches its lower limit, given by $2.3V_{\mathrm{thermal}} = 59.5\,\mathrm{mV/dec}$ at room temperature. This sets a lower limit to the reachable $I_{\mathrm{on}}/I_{\mathrm{off}}$ current ratio with a given supply voltage V_{DD}. In order to overcome this limit the operating principles of the FET must be modified. Approaches that could reach this goal take advantage of a constrained energy injection window for charge carriers such as tunnel FETs [369, 370], a nonmonotonic variation in the density of states around the Fermi level acting as an energy filter [46, 310], or an insulator which creates a negative capacitance of the gate stack using for example a ferroelectric, thereby amplifying the surface potential in the channel [371, 372, 373]. All these steep-slope device concepts potentially allow for a SS below 59 mV/dec but can only attain their goal if the interface trap density can be minimized.

At the same time, it becomes easier to achieve the minimum SS for ultra-scaled FETs with a small EOT, as can be seen from the following reformulation of Equation (4.3),

$$SS = 2.3\frac{k_{\mathrm{B}}T}{q}\left(1+\mathrm{EOT}\left(\frac{\varepsilon_{\mathrm{semi}}}{\varepsilon_{\mathrm{SiO_2}}\,t_{\mathrm{semi}}}+\frac{q^2D_{\mathrm{it}}}{\varepsilon_0\varepsilon_{\mathrm{SiO_2}}}\right)\right) = 2.3\frac{k_{\mathrm{B}}T}{q}\left(1+a\cdot\mathrm{EOT}\right). \tag{4.4}$$

Thus, for monolayers of a 2D semiconductor, such as for example MoS_2, SS as a function of EOT depends only on the density of interface traps D_{it} as the remaining factors in a are either physical constants or material constants of the MoS_2 monolayer, respectively. In Figure 4.4 SS is shown as a function of EOT for literature reports of FETs using monolayer MoS_2 as a channel and different gate insulators. Under the assumption that D_{it} is primarily a material

constant determined by the quality of the interface formed between a specific insulator and an MoS_2 monolayer, for all literature reports using the same insulator, the D_{it} should be similar. Consequently, *SS* depends linearly on EOT, as shown in Equation (4.4) with a slope a proportional to D_{it} in the respective material system. Thus, from a linear regression through all data points for one insulator combination with MoS_2, D_{it} can be extracted, see the colored, solid lines in Figure 4.4. The assumption that D_{it} is the same for devices with the same channel/gate insulator combination is a simplification, as the processing is expected to also have an impact on D_{it}. However, these processing variations are superimposed on the underlying material trends which are analyzed here.

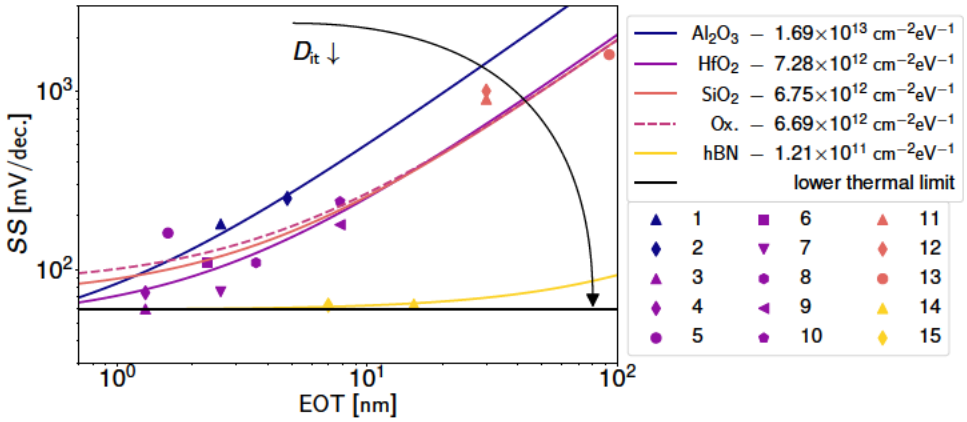

Figure 4.4. Subthreshold swing as a function of EOT for various FETs based on monolayer MoS_2 as reported in literature: 1-[374], 2-[51], 3-[359], 4-[375], 5-[376], 6-[377], 7-[378], 8-[379], 9-[380], 10-[381], 11-[382], 12-[383], 13-[167], 14-[384], 15-[385]. Solid, colored lines represent fits of Equation (4.4) to the data points from literature, assuming that for a combination of monolayer MoS_2 with one insulator a similar density of interface traps is obtained. For the solid dashed line it is assumed that all amorphous oxide insulators form an interface of similar quality and thus similar D_{it} with the MoS_2. The solid black line at the bottom indicates the lower thermal limit of 59.5 mV/dec and the arrow shows the trend for a decreasing interface trap density.

As a result, the highest trap density is observed for the Al_2O_3/MoS_2 material system at about 1.7×10^{13} cm^{-2}eV^{-1} with similar interface trap densities reported for HfO_2/MoS_2 at 7.3×10^{12} cm^{-2}eV^{-1} and SiO_2/MoS_2 at 6.8×10^{12} cm^{-2}eV^{-1}. These similar interface trap densities observed for all amorphous oxides suggest that independent of the exact material the chemical bonding nature and structure of amorphous oxides are the origin of the high D_{it}. This surface of the amorphous oxide onto which the 2D layer is grown or transferred becomes the critical insulator/semiconductor interface which is inherently defective. Thus, a linear regression through all measurement points on amorphous oxide results in a D_{it} of 6.7×10^{12} cm^{-2}eV^{-1}, see the dashed line in Figure 4.4. In contrast, the layered insulator hBN exhibits a substantially smaller D_{it} of about 1.2×10^{11} cm^{-2}eV^{-1} as it forms a high-quality van der Waals (vdW) interface with MoS_2.

These interface trap densities are comparable to D_{it} values reported in literature based on other measurement methods. For example, Takenaka *et al.* [386] used the Terman method, thus the evaluation of high-frequency capacitance voltage (CV) characteristics or more precisely of the observed stretch-out of those characteristics [387]. They applied the Terman

method to thick-body MoS_2 capacitors, with a thickness $t_{semi} > 200\,nm \sim W_{DM}$, because a thickness higher than the depletion width is required to see capacitance changes as the MoS_2 gradually depletes. The authors obtained for HfO_2, Al_2O_3 and SiO_2 comparable D_{it} values of about $10^{13}\,cm^{-2}eV^{-1}$ [386]. However, due to their ultra-thin body, the analysis of CV characteristics of 2D material-based FETs is in general more difficult and less frequently used in comparison to conventional silicon FETs. An alternative approach to extract D_{it} from measurement data is the analysis of the $1/f$ low-frequency noise, see Section 3.2.1. Based on a correlated carrier and mobility fluctuation model Vu *et al.* [385] extracted a D_{it} of $5 \times 10^9\,cm^{-2}eV^{-1}$ for monolayer MoS_2 transistors encapsulated in thick hBN, which is below the target value of $10^{10}\,cm^{-2}eV^{-1}$. Thus, in principle, the insulator requirement of reducing the interface trap density for 2D material-based FETs can be met, even though it has up to now only been fulfilled for hBN, which does not satisfy the scaling requirements, see Section 4.1.

Besides reducing the subthreshold swing, interface traps also impact the mobility of charge carriers in the 2D semiconductor, as charged impurity scattering is one of the main scattering sources. When performing mobility measurements for a wide temperature range, two main scattering sources can be identified, phonon scattering which dominates at temperatures exceeding 150 K and impurity scattering which determines the resistivity at low temperatures. It has been observed that the impurity dominated mobility is layer dependent [40], thus demonstrating that scattering events at the interface play a critical role for the mobility in the 2D channel. This dependence of the low temperature mobility on the interface trap density can also be used to determine D_{it}. In this way, the low temperature mobility in few-layer MoS_2 encapsulated in about 20 nm thick hBN was modeled with a charged impurity concentration of $6 \times 10^9\,cm^{-2}$ [40]. This value is about two orders of magnitude lower than the concentration of interfacial traps for MoS_2 on SiO_2 which causes a two order of magnitude smaller low temperature mobility [213][403]. As the impurity dominated mobility increases by one order of magnitude for an increase in t_{semi} by 2 nm, it is expected that an hBN interlayer would also have to be at least 2.5 nm thick, corresponding to about 10 layers, in order to effectively screen fixed charges at the underlying SiO_2 surface [TKJ2], see the schematic in Figure 4.5 (a).

In addition to the impact of interface traps on the mobility via impurity scattering, the interface quality and dielectric environment also play a key role in determining the room temperature mobility in 2D semiconductors via so-called remote phonon or surface optical phonon scattering mechanisms. Electrons in semiconductors can excite phonons in the surrounding insulators via long-range Coulomb interactions, if the insulator supports polar vibrational modes. These modes in turn reduce the mobility in the semiconductor, thus the supported mode density and mode scattering strength in the insulator should be minimized, see requirement (d) in Figure 4.1. This effect was first described for the silicon/ insulator interface [410] and surface optical phonon scattering was identified as the dominant phonon scattering mechanism in graphene devices [399, 411]. In general, for devices based on 2D materials surface optical phonon scattering becomes more important as the channel is atomically thin, thus polar vibrational modes are excited in the insulators on both sides of the 2D material. In insulators with high dielectric constants ε_{ins} (high-k dielectrics), for example HfO_2, low-energy polar vibrational modes are allowed, thus surface optical phonon scattering

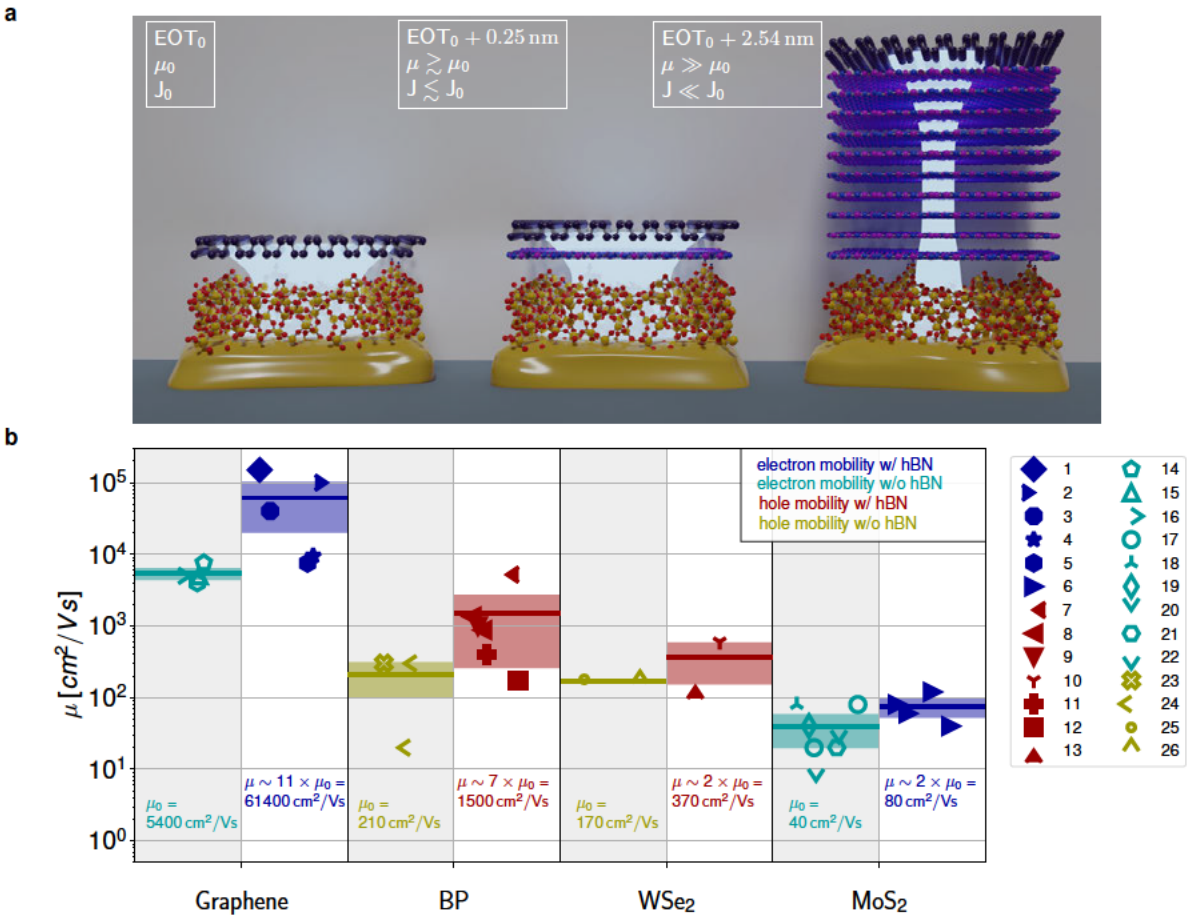

Figure 4.5. **(a)** Schematic drawing illustrating the impact of hBN interlayers on the mobility in a 2D material, like for example black phosphorus (P-purple) shown here. At least 2.5 nm of an hBN interlayer (B-magenta, N-blue) are required to shield interface defects at the SiO_2 surface (Si-yellow, O-red) and considerably reduce leakage currents through the gate stack, reproduced from [TKJ2]. **(b)** Comparison of mobility values as reported in literature based on four-probe measurements for the 2D materials graphene, BP, WSe_2, and MoS_2: 1-[39],2-[388],3-[67], 4-[389], 5-[390], 6-[40], 7-[391], 8-[392], 9-[393], 10-[394], 11-[395], 12-[396], 13-[397], 14-[398], 15-[399], 16-[400], 17-[213], 18-[401], 19-[402], 20-[403], 21-[404], 22-[405], 23-[406], 24-[407], 25-[408], 26-[409]. Solid lines indicate mean values inside this category and shaded areas correspond to one standard deviation, μ is the mobility with hBN substrate and μ_0 without hBN, adapted from [TKJ2].

degrades the mobility the most in comparison to materials with a lower permittivity such as SiO_2 or hBN. This effect is so strong that, in the ideal case, the theoretically predicted mobility in monolayer MoS_2 is two orders of magnitude higher, if the layer is surrounded by hBN than when it is surrounded by HfO_2 [412]. In combination, the small permittivity of hBN and the few interface defects at the vdW interface with the 2D material can minimize both remote phonon scattering and Coulomb scattering at interfacial impurities. Thus, an hBN encapsulation with thick, crystalline hBN leads to an enhanced mobility for 2D material-based devices. In this configuration, the mobility is a factor of 2 or up to 10 higher than for a 2D material in direct contact with an amorphous oxide [TKJ2], see the comparison of literature values in Figure 4.5 (b).

4.2.2 Border Traps

Besides minimizing the density of charge traps directly at the interface, also the density of electrically active border traps in the insulator should be as small as possible. Border traps are defined as charge traps within the insulator at a distance of a few nm away from the interface [413]. These border traps determine the electrical device stability and reliability, thus the trap density of electrically active traps (D_{ot}) should not exceed about $10^{19}\,\mathrm{cm}^{-3}\mathrm{eV}^{-1}$ [TKJ13], given as requirement (e) in Figure 4.1. In the most frequently used gate insulators, amorphous oxides, the trap level of every single insulator defect varies, as the surrounding of the defect differs depending on the local environment. In a linear superposition of many border traps, this results in defect bands [TKJ5, 341], which is often approximated by a normal distribution of trap levels around an average defect level $\overline{E_{\mathrm{T}}}$ [414]. In optimized and electrically stable silicon FETs these border traps in the gate insulator determine the reliability [215, 415], such as the Bias Temperature Instability (BTI) and $1/f$ or low frequency noise, see Section 3.2. In 2D material-based FETs however, due to their higher trap density, border traps are responsible for limited device stability on shorter time scales, giving for example rise to a pronounced hysteresis in the transfer characteristics [TKJ21]. In addition, the increased border trap densities in 2D FETs amplify all stability and reliability issues known from silicon technologies, see Section 5. It is characteristic for these border traps that their average time constants span an extremely wide range, starting from nanoseconds (and likely faster) to many years [TKJ1, 224]. Thus, border traps can only be comprehensively characterized using a combination of several measurement methods, for example a noise analysis in combination with BTI measurements, see Figure 4.6 (a).

In general, the energetic position of defect bands in gate insulators is an intrinsic material property [230, TKJ13, 417]. For every material there are characteristic defective atomic configurations corresponding to specific trap levels, subject to a certain variation depending on the local surroundings of every defect instance. While the defect bands have up to now been only investigated for amorphous gate oxides, the underlying physics of atomic defect configurations and their energy levels are universal and thus defect bands will presumably be found in any insulator. What is more, it is expected that for crystalline insulators such as hBN or calcium fluoride (CaF_2) the defect bands are narrower, as due to the crystalline nature the surroundings of the defect instances are more similar [TKJ5]. Defect bands are characterized by their average trap level $\overline{E_{\mathrm{T}}}$ and the standard deviation of the trap level distribution $\sigma_{\mathrm{E_T}}$. These parameters can be determined both experimentally or through theoretical calculations. With experimental approaches, defect states can be probed by electrically measuring conductance variations in MOS systems [418, 419] or by measuring the electron paramagnetic resonance of insulator samples, detecting the magnetic moment of unpaired electronics [420]. Using *ab-initio* calculations potential defect candidates and their prevalence can be analyzed, in this way identifying electrically active defect configurations such as oxygen vacancies [421] or hydrogen-related defects [422]. At the moment, the energetic position of the defect bands are known for SiO_2 [419], HfO_2 [TKJ13, 421], and Al_2O_3 [TKJ15, 418], see Table 4.1 for a summary of the known defect band parameters [TKJ5].

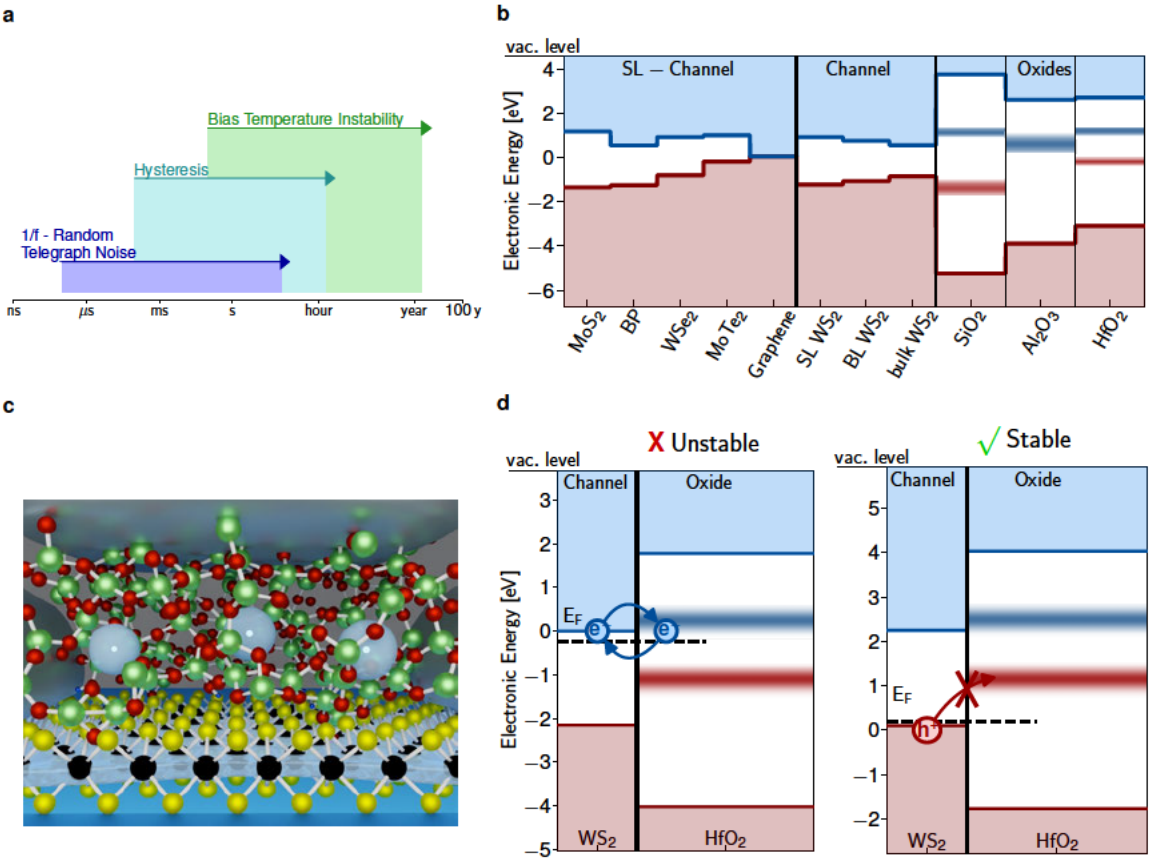

Figure 4.6. **(a)** Charge trapping time constant ranges of border traps which are accessible for different measurement schemes. For example, 1/f noise spectra cover the µHz to MHz regime but in order to capture the entire span of time constants, several measurement methods need to be combined. Adapted from [TKJ1]. **(b)** Band diagram of the insulators with known defect bands in relation to the band edges of a variety of 2D semiconductors. To the left the band gaps are given for various single layers of 2D materials, in the center the impact of the layer variation on the band gap is shown for the example of WS_2 [416] and to the right the oxide defect bands are shown in SiO_2, Al_2O_3, and HfO_2, according to the values given in Table 4.1. **(c)** Schematic drawing of a top gated MOSFET using HfO_2 as a gate insulator (green - Hf, red - O) and WS_2 as a channel (black - W, yellow - S) including a visualization of the electron flow and charge traps in the oxide. Adapted from [TKJ3]. **(d)** For an n-type WS_2 FET using a HfO_2 gate insulator the Fermi level is close to the electron trapping band, rendering the device electrically unstable. For a p-type WS_2 FET, shown to the right, the Fermi level is far away from the hole trapping band, rendering the device stable. Adapted from [TKJ3].

Defect bands are classified in electron trapping (acceptor-type) and hole trapping (donor-type) bands depending on their possible charge states and the overall charge balance in the device. In an acceptor-type defect the charge state changes from neutral to negative upon electron capture and in a donor-type defect from positive to neutral. Thus, these trap types can only be distinguished based on the overall amount of fixed charges in the insulator. In general, it is assumed that in the initial state the majority of defects in the insulator are neutral, thus rendering all defect bands in the upper part of the band gap electron trapping bands and all deep defect bands in the lower part of the band gap hole trapping bands [TKJ3, TKJ13].

Insulator	Band gap [eV]	EA, χ [eV]	Type	$\overline{E_T}$ ref. E_C [eV]	$\overline{E_T}$ ref. vac. [eV]	σ_{E_T} [eV]
SiO_2	9 [207, 423]	0.85 [28]	e^- h^+	2.65 5.1	3.5 [TKJ13] 5.95 [TKJ13]	0.15 [TKJ13] 0.25 [TKJ13]
HfO_2	5.8 [28, 423]	2 [423, 424]	e^- h^+	1.45 2.8	3.45 [TKJ13] 4.8 [TKJ13]	0.15 [TKJ13] 0.15 [TKJ13]
Al_2O_3	6.5 [423]	1.9 [423, 425]	e^-	2.1	4.0 [426]	0.3 [TKJ15]

Table 4.1. Parameters of known oxide defect bands. The average energetic trap level is given with reference to the respective conduction band edge of the oxide ($\overline{E_T}$ ref. E_C) and with respect to the vacuum level ($\overline{E_T}$ ref. vac.). These two quantities are related by the electron affinity (EA), χ, defined as the energetic distance between the conduction band level and the vacuum level.

For amorphous oxides, the defect band alignments are shown together with a selection of the band edge locations of various 2D materials in Figure 4.6 (b). This knowledge about the alignment of the Fermi level in the semiconducting channel to the defect bands in the gate insulator was used to design more stable transistors based on a stability aware design approach [TKJ3]. In principle, this approach aims to maximize the distance between the Fermi level and the oxide defect bands, thereby minimizing the amount of electrically active border traps without actually modifying the total number of traps present in the insulator. In Schottky barrier FETs without doped contact regions, the alignment of the Fermi level within the band gap of the semiconductor depends on the doping of the entire layer and the choice of contact metals which pin the Fermi level, see Section 2.3. As the contact materials are typically chosen to minimize the Schottky barrier heights, the Fermi level is aligned close to the conduction band edge in n-type FETs and close to the valence band edge in p-type FETs.

For designing an electrically stable n-type FET one needs to choose a combination of a semiconductor to a gate insulator where the conduction band edge is far away from any defect bands in the insulator and equivalently for a p-type FET the valence band edge of the semiconductor needs to be far away from the insulator's defect bands. For example, charge trapping processes in a n-type WS_2 FET with a HfO_2 gate insulator render these devices electrically unstable, as illustrated in Figure 4.6 (c). If instead a p-type FET was fabricated using a WS_2 monolayer in combination with a HfO_2 gate insulator, this would, according to the known defect band alignments, result in a more stable FET [TKJ2], see Figure 4.6 (d). A band diagram serves as a basis for the selection process of suitable semiconductor to insulator combinations, such as the one shown in Figure 4.6 (b). For layered semiconductors, the band gap depends on the sample thickness which provides another degree of freedom for the selection process. For example, bulk WS_2 with a thickness of over 10 layers would result in more stable devices in combination with a SiO_2 gate insulator than a monolayer of WS_2, see Figure 4.6 (b). In comparison to 2D semiconductors, the 2D Dirac semi-metal graphene offers even more freedom for the design of stable FETs as its work function and thus its Fermi level can be quasi-continuously tuned over a wide range from 3.4 eV to 5.1 eV via doping [427, 428]. Therefore, within the scope of this work, the applicability of the stability-based design approach in graphene FETs using Al_2O_3 as a gate insulator was experimentally demonstrated,

see Section 5.1. It should be noted that while the defect bands are currently only known for amorphous oxides it is expected that in crystalline insulators it will be easier to avoid defect bands, as the defect bands there are expected to be narrower [TKJ5, TKJ2].

Another requirement that a good gate insulator has to meet is that it has a high dielectric stability, see requirement (f) in Figure 4.1. A gate insulator needs to withstand high electric fields before it breaks down and loses its insulating properties as conductive filaments are formed. This electric breakdown field (E_{BD}), where the insulator fails completely, typically depends on the material and the bulk defect density in the insulator and should exceed 10 MV/cm. In addition, the time it takes for the insulator to reach this breakdown when subjected to constant voltage stress should be as long as possible and is characterized in a Time Dependent Dielectric Breakdown (TDDB) measurement [275, 429], see Section 3.2.6. Dielectric breakdown typically occurs at the electrically weakest location of the insulator which is given by the location with the highest density of pre-existing defects. In addition, the accumulation of charges in the insulator during previous stressing, such as charge trapping at border traps as described previously, can increase the leakage currents, leading to a phenomenon known as stress induced leakage currents (SILC) [430]. These leakage currents in turn trigger dielectric breakdown. In amorphous oxides the observed breakdown mechanism is typically progressive [431], in layered materials with van der Waals bonding it takes place layer by layer [218, 280], even though layer by layer breakdown has until now only been observed using CAFM. For another crystalline gate insulator, CaF_2, a high dielectric strength and a high spatial localization of the formed conductive filaments was reported [TKJ6].

Overall, the high interface trap and border trap densities in amorphous oxides require a careful stability-aware design, where the location of the Fermi level needs to be moved away as far as possible from the defect bands in the oxides. However, the improvement which can be attained with this method might not exceed one order of magnitude, see Section 5.1.3. Thus, in order to reach the levels of electrical stability and reliability required for industrial applications, crystalline gate insulators are likely needed, as they have the potential to tremendously increase device stability because of their reduced density of interface and border traps.

4.3 Deposition Technology for Gate Insulators

Top-gate or gate-all-around device designs are the most relevant for future technology nodes [34, 432] and thus it is necessary that insulators can be deposited uniformly on top of 2D semiconductors, see requirement (g) in Figure 4.1. The most promising deposition technology for top-gate integration is atomic layer deposition (ALD). In general, ALD growth of layers on top of 2D materials is challenging, as the inert basal planes of 2D semiconductors inhibit the nucleation required for the growth of ALD layers [TKJ1]. To overcome this problem numerous efforts have been undertaken which can be loosely grouped into four categories. First, the surface can be activated with surface treatments [433] or additional steps and modifications of the ALD process such as plasma enhanced ALD [434]. For example, plasma exposure of the layered semiconductor, e.g. to O_2 [433] plasma, has been suggested

but partially damages the semiconductor and results in growth of low uniformity. In a plasma enhanced ALD process the plasma precursor step is part of the ALD process. In this way, some of the thinnest high-k dielectrics on top of 2D materials have been demonstrated [435]. However, the plasma exposure severely damages the topmost 2D layer which is unacceptable for monolayer channels [128].

Second, a buffer or seeding layer can be used to support the nucleation of insulators on top of 2D materials [130, 436]. However, these buffer layers are rarely high-k, thus in order to meet the scaling targets, see Section 4.1, they need to be as thin as possible. A buffer layer can be formed by depositing a thin metal seed on top of the layered semiconductor via evaporation, which is subsequently oxidized in air or in a dry furnace, for example Al turning into Al_2O_3 [130, 383]. As an alternative to evaporated metals, organic films like perylene-3,4,9,10-tetracarboxylic dianhydride (PTCDA) can form self-assembled monolayers on graphene [436] or on TMDs [359]. This organic compound forms a monolayer in self-limited epitaxy when deposited in vacuum, leading to highly uniform films. Recently, a PTCDA seed was used to deposit ultrathin HfO_2 on top of hBN and MoS_2 with an EOT of about 1 nm [359]. Third, an insulator can be transferred on top of the layered semiconductor instead of growing a film with ALD, using one of the transfer methods discussed in Section 2.1.5. The most common material which is often transferred is hBN [68, 83], but recently other layered 2D insulators which could be transferred have been considered, for example mica [437], GaS [438] or MoO_3 [439]. Despite a promising first demonstration of a dry layer transfer for 2D materials based only on scalable methods [440], the adaptation of a transfer approach by industry poses many challenges in terms of yield and uniformity.

In the fourth and last approach for top gate integration of insulators with 2D semiconductors, the layered semiconductor is partially transformed into its native oxide [441, 442]. Typically the oxidation of the semiconductor progresses layer-by-layer through the layered semiconductor resulting in a clean, sharp interface between semiconductor and insulator [443, 444]. This method has shown promising results for Bi_2O_2Se being converted to the insulator Bi_2SeO_5 [443], for HfS_2 being converted to HfO_2 [442] or for $HfSe_2$ being converted to HfO_2 [441]. In addition, other growth methods for insulators besides ALD have been suggested. For example, CaF_2 can be grown at a high quality and uniformity as ultrathin layers using MBE. However, this is still limited to Si (111) as a growth substrate and thus to back gated configurations in combination with 2D semiconductors [TKJ7].

Finally, insulators deposited on top of 2D semiconductors also have to allow for threshold voltage tuning either by means of the metal gate work function or through surface charge transfer doping (SCTD), see requirement (h) in Figure 4.1. It requires both, doping methods and the tunability of the threshold voltage to provide for symmetric n- and p-type FETs next to each other in order to obtain symmetric inverter characteristics as the basic building block for CMOS. Up to now, CMOS inverters made from 2D materials have frequently combined different TMDs such as MoS_2 for the n-type FET and WSe_2 for the p-type FET, even though this approach makes both the integration of n- and p-type in close vicinity as well as the tuning of the respective V_{th} values difficult [445, 446]. Alternatively, one single 2D material can be doped chemically [447], electrostatically [448, 449], or by selecting different contact

materials for n- and p-type devices [450]. In this way inverters based on WSe_2 [446, 447, 449, 450], $MoTe_2$ [451], and BP [448] have been fabricated, achieving gains of up to 80 for supply voltages of $V_{DD} = 2\,V$ [446] and up to 20 for a supply voltage of only 0.4 V [448]. After giving an overview of the requirements for a good gate insulator for 2D scaled CMOS logic, in the following a brief overview of the potential of various insulators with respect to those requirements will be provided.

4.4 Insulating Materials for Nanoscaled 2D Transistors

Potential insulators for transistors based on 2D semiconductors can be divided into four categories: amorphous oxides (e.g. SiO_2 [382], Al_2O_3 [384], and HfO_2 [359]), crystalline, layered insulators (e.g. hBN [68], muscovite mica [437], TiO_2 [452], and GaS [438]), native oxides to layered semiconductors (e.g. MoO_3 [439], ZrO_x [441], HfO_x [442], Ta_2O_5 [453], and Bi_2SeO_5 [443]) and crystalline ionic fluorides (e.g. CaF_2 [TKJ7]). As the interface of the insulator to the semiconductor is critical for the performance of 2D material-based FETs, see Section 4.2, the interfaces of the semiconducting 2D channel to insulators of the four categories introduced above are compared in the schematic in Figure 4.7. In the following, the properties of every group will be briefly discussed and an overview over the most important characteristics and material parameters for potential gate insulators are compared in Table 4.2.

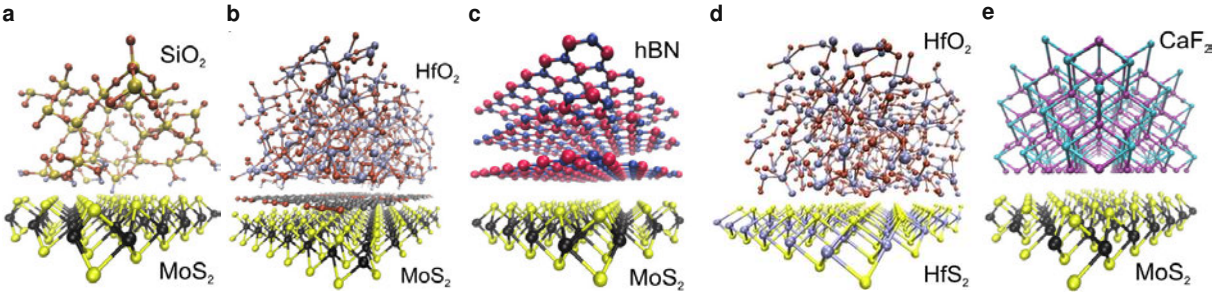

Figure 4.7. **(a)** Interface formed between an amorphous oxide and a layered semiconducting channel, for example SiO_2 (Si-yellow, O-red) and MoS_2 (Mo-black, S-yellow). **(b)** If a self assembled monolayer is used to seed the ALD growth of the amorphous oxide a clean interface can be formed, for example HfO_2 (Hf-blue, O-red) grown using PTCDA (C-black, O-red) as a seed layer on MoS_2. **(c)** Van der Waals interface formed between a layered, crystalline insulator and a layered channel, for example hBN (B-magenta, N-blue) and MoS_2, reproduced from [TKJ5]. **(d)** Native oxide formed by oxidizing several layers of a layered semiconductor, for example HfO_2 grown from HfS_2. **(e)** Ionic fluorides have an inert fluor-terminated surface which forms a high quality interface with layered semiconductors, for example CaF_2 (Ca-purple, F-cyan) and MoS_2. All graphics in this figure are reproduced from [TKJ5].

Most prototype 2D material-based FETs have relied on amorphous oxides [51, 165]. These materials have the advantage of the possibility to use well-established ALD growth of Al_2O_3 [434] or HfO_2 [435] to grow the insulators on top of 2D semiconductors. In this context, the problem of nucleation on the van der Waals surface has been successfully addressed either by using evaporated metals [383] or organic compounds such as PTCDA [359]. The use of self-assembled PTCDA monolayers as a seed for ALD growth offers the additional advantage that

Cat.	Mat.	Layered	VdW int.	Band gap [eV]	Elect. aff. [eV]	Diel. con. [ε_0]
amorph.	SiO_2	no	no	9[423]	0.85[28]	3.9[364]
	Al_2O_3	no	no	6.5[423]	1.9[423, 425]	9[364]
	HfO_2	no	no	5.8[28, 423]	2[423, 424]	23[454]
layered	hBN	yes	yes	5.95[455]	1.14[456]	5.06[457]
	Mica	yes	yes	7.85[458]	3.26[459]	8.1[460]
	TiO_2	yes	yes	3.8[461]	3.72[461]	60[462]
	GaS	yes	yes	3[438]	2.13[438]	7.5[463]
native	MoO_3	yes	yes	3[439]	6.6[464]	35[439]
	ZrO_x	no	yes	5.8[364]	2.5[465]	15[466]
	Ta_2O_5	no	yes	4.4[364]	3.3[465]	15.5[453]
	HfO_x	no	yes	5.5[467]	1.75[424]	23[454]
	Bi_2SeO_5	yes	yes	3.9[443]	2.2[443]	21[443]
fluorides	CaF_2	no	quasi	12.1 [468]	1.67[469]	8.4[470]

Table 4.2. Material parameters and properties of potential gate insulators for MOSFETs based on 2D materials, adapted from [TKJ2].

these layers form a clean van der Waals interface with the 2D semiconductors and thus can reduce the density of interface traps, leading to a steep *SS* of 60 mV/dec [359]. However, such self-assembled monolayers are used only rarely [359, 436], thus the quality of the interface formed between the amorphous oxide and the layered semiconductor is in general poor [380, 386]. Furthermore, amorphous oxides typically exhibit wide oxide defect bands which are intrinsic material properties of the oxides [230, TKJ13]. In Figure 4.6 (b) the alignment of the defect bands in amorphous oxides to various 2D semiconductors is shown. Based on this alignment of the defect bands to the Fermi level in the channel, more stable 2D material-based transistors can be designed, since, by moving the Fermi level away from the defect bands, the number of electrically active traps can be reduced [TKJ2]. However, the thinner the defect bands are, the easier it becomes to avoid them, providing a key advantage for crystalline insulators. As a consequence, while in particular high-k amorphous oxides such as HfO_2 show good scaling potential and can be deposited with ALD on top of 2D semiconductors, the reduction of electrically active charge trap densities is a major challenge for amorphous oxides.

In the second category of layered insulators, hBN is the most well known [471]. hBN is an excellent substrate for 2D layers, as it forms a perfect vdW interface with layered 2D semiconductors and shows small densities of intrinsic defects [472]. Theses small charge trap densities lead to highly stable 2D material-based FETs [385]. In addition, hBN allows for high mobilities in the semiconductors due to minimal remote phonon scattering [40, 412]. In order to fabricate top gated transistors with hBN, multilayers must be transferred on top of the channel material [140] and, despite the associated difficulties, transfer processes could in theory be adapted for large scale industry processing. However, hBN's small dielectric constant translates into limited scaling potential and high leakage currents through scaled

hBN layers [TKJ2], see Section 4.1. Even though hBN is likely unsuitable for scaled CMOS, it is a promising candidate as a substrate for 2D material-based devices or as an insulator for devices which operate at small electric fields like photodetectors [473, 474] or sensors [475].

Another layered insulator besides hBN is muscovite mica. Mica is a complex layered compound with the chemical formula $KAl_3Si_3O_{10}(OH)_2$, where single layers consist of AlO_6 octahedra surrounded on both sides by SiO_4 tetrahedra with intercalated potassium K^+ ions between the layers [458]. In general, mica is a promising insulator with a larger band gap and a higher permittivity compared to hBN [459, 476] and thus a better scaling potential and smaller leakage currents, see Figure 4.3. However, the band gap decreases as the layer thickness is reduced in a mechanism related to the potassium ion density. Therefore, mica might lose its good insulating properties at atomically thin layers [458, 477]. Up to now several studies have used mica as a growth substrate [477, 478] for growing graphene, but only few studies have yet transferred mica layers on top of 2D semiconductors to study the performance of FETs with mica as an insulator [437, 479]. While these initial studies show promise, they require verification on a broader scale by multiple groups. Other layered insulators which have been suggested include GaS [438], TiO_2 [452, 461], layered perovskites like $Ca_2Nb_3O_{10}$ [480], or crystalline silica bilayers [481]. However, for most of these materials FET demonstrations are missing. Additionally, while the enormous permittivites of some materials promise excellent scaling properties, many of them suffer from small band gaps. In summary, the lack of comprehensive data about these rather exotic materials up to date makes a profound and exhaustive assessment of their potential impossible at the present stage.

Native oxides form the third category of potential insulators. For example, TaS_2 can be oxidized to form Ta_2O_5 [453] or $HfSe_2$ or Hf_2 can be oxidized to HfO_2 [441, 442, 482] or more precisely HfO_x, as the resulting insulating layers are often non-stoichiometric. This non-stoichiometry can be taken advantage of to dope the underlying 2D layer using surface charge transfer doping (SCTD) [197, 483]. Often, the oxidation of layered semiconductors proceeds in a controlled manner, oxidizing the semiconductor layer-by-layer, which leads to a sharp and smooth interface [443, 444]. However, especially for non-stoichiometric and amorphous native oxides, the corresponding defect bands in the oxides are expected to be wide, at least as wide as those known for HfO_2 [TKJ13] and potentially wider. Thus, the long-term electrical stability of 2D FETs based on these native oxides will likely be mediocre. Recently, Li *et al.* have demonstrated that Bi_2O_2Se oxidizes layer-by-layer to form crystalline Bi_2SeO_5 [443]. This novel native layered oxide is scalable down to an EOT of below 1 nm due to its high permittivity of about 20 while, in addition, Bi_2SeO_5 can be etched selectively over Bi_2O_2Se in diluted HF [443]. Consequently, Bi_2SeO_5 is a promising candidate, even though the hysteresis and long-term stability of FETs based on the Bi_2O_2Se/Bi_2SeO_5 has not yet been studied.

Ionic fluorides are the fourth category of potential insulators. Fluorides consist of three dimensionally coordinated crystals with ionic bonding and possess high band gaps and moderate dielectric constants. Within the scope of this work, CaF_2 has been used as a gate insulator for MoS_2 based FETs at a physical thickness of only 2 nm, corresponding to an EOT smaller than 1 nm [TKJ7]. A key advantage in using fluorides as gate insulators for 2D material FETs is that they have a chemically inert, F-terminated surface without dangling

bonds which then becomes a high quality van der Waals interface when combined with 2D semiconductors [112, 484]. In addition, it was demonstrated that CaF_2 has a high dielectric stability at the microscopic level [TKJ6] and shows a small amount of charge trapping at border traps, making 2D FETs with CaF_2 exceptionally stable [TKJ8]. However, up to now there have been no demonstrations of top gated MOSFETs using CaF_2. While in theory epitaxial growth of CaF_2 on top of MoS_2 in an MBE process should be feasible [112], all device demonstrations up to now have used transferred 2D layers on top of CaF_2 [TKJ7]. In addition, the direct growth of $MoSe_2$ and $MoTe_2$ on inert CaF_2 surfaces has been reported but without any device prototypes thus far [111, 485]. Therefore, an MBE growth process of CaF_2 on top of common 2D semiconductors like TMDs needs to be developed in the future for top gate integration. Besides CaF_2, many other fluorides exist which are closely related to CaF_2 in their bonding nature and structure such as MgF_2 and NaF [TKJ5]. These compounds could be promising candidates as they both have large band gaps with medium-sized dielectric constants [486]. In addition, the ferroelectric $BaMgF_4$ was used in negative-capacitance FETs which offer a steep slope for low power switching [487]. It should be noted, however, that negative capacitance FETs have recently been critically discussed in literature, reporting that the advantages for scaled devices would likely be minimal [373].

In summary, the requirements for a good gate insulator to 2D material-based FETs are numerous and up to now no material meets all of these requirements satisfactorily. Moreover, this current lack of good gate insulators for 2D FETs manifests itself in a reduced scalability of the devices, a reduced mobility in the 2D semiconductors, an increased subthreshold swing and unstable device behavior due to charge trapping in the insulator. Thus, finding a good gate insulator is necessary for 2D FETs to become competitive to standard silicon technologies and to eventually outperform the state-of-the-art of ultrascaled silicon based CMOS.

5 Experimental Characterization of the Electrical Stability of 2D Transistors

After presenting an overview over the numerous requirements for suitable gate insulators for nanoscaled 2D transistors in Chapter 4, this chapter focuses on the electrical stability and reliability of 2D FETs. In contrast to well-established silicon technologies, most prototype 2D FETs suffer from an unstable threshold voltage [TKJ21, 488] and a hysteresis in the transfer characteristics, during standard device operation [TKJ15, 202]. These phenomena are causally linked to the high concentrations of border traps and the often unfavorable alignment of the defect bands in amorphous oxides to the band edges of 2D semiconductors such as MoS_2 [TKJ3, TKJ21]. As described in Section 4.2.2, border traps are charge traps within the insulator at a few nm distance from the semiconductor interface [413]. While border traps are an intrinsic material property of all gate insulators, their concentration and, in particular, their impact on device operation depends critically on the interface to the semiconducting channel and the conduction and valence band alignments in the semiconductor. In silicon FETs which have seen decades of optimization and which benefit from the high quality interface between Si and its native oxide, SiO_2, border traps in SiO_2 and HfO_2 determine the reliability of MOSFETs [239, TKJ13, 415]. In contrast, at the current state-of-the-art border traps have a much more pronounced impact on the operation of 2D material-based FETs, often preventing stable device operation [TKJ5, TKJ1, 250, 489].

This chapter describes how well established measurement methodologies to characterize the performance, electrical stability, and reliability of 2D FETs based on 2D semiconductors were applied, adapted, and extended within the scope of this thesis. The studies focus on comprehensively characterizing the impact of border traps on the device operation of 2D FETs. In Section 5.1 the role of border traps is analyzed for large-area MoS_2 and graphene based FETs with an active area larger than $0.1 \times 0.1\,\mu m^2$ using hysteresis and BTI measurements. In these devices, charge trapping and detrapping events at many border traps superimpose and thereby form the total threshold voltage shifts observed. In addition, the knowledge about the physics of charge trapping at border traps can be taken advantage of in a stability-based design approach which could be used to reduce the impact of border traps on device characteristics. The discussion of experimental results in this section is based mostly on the author's work in [TKJ3, TKJ15, TKJ16].

In Section 5.2 border traps in small-area MoS_2 based FETs with an active area smaller than $0.1 \times 0.1\,\mu m^2$ are analyzed. In those small-area devices, discrete charge trapping events can

be observed, thereby revealing detailed information about the charge trapping dynamics and consequently about the locations of atomic traps. Here, RTN and TDDS on these devices is studied, mostly at cryogenic temperatures below 100 K. The experiments demonstrate that charge trapping events do not freeze out because of the onset of strong nuclear tunneling which dominates the atomic rearrangements at the defect site at these low temperatures [341]. Predominantly, the experimental results and insights discussed here have been reported by the author in [TKC6, TKJ14].

5.1 Stability of the Threshold Voltage in 2D Transistors

Parts of this section (marked by a vertical sidebar) are currently under review in

[TKJ3] Nature Electronics, (2021).

In FETs based on 2D materials drifts of the threshold voltage are frequently observed during device operation [202, 214, 489]. These drifts are caused by charge capture and emission events at border traps in the gate insulator [TKJ21, 206, 253]. Thus, all experimental methods focusing on a comprehensive evaluation of ΔV_{th} drifts at the same time provide information about the ensemble of electrically active border traps. In the following continuous ΔV_{th} drifts as observed on large area 2D FETs with active areas above $W \times L = 0.1 \times 0.1\,\mu\mathrm{m}^2$ are investigated. For FETs with dimensions in the µm regime, always an ensemble of border traps actively emits or captures charges, as opposed to nanoscaled devices where discrete V_{th} steps are associated with single capture or emission events, see Section 5.2.

For these large-area FETs the most common measurement methods to systematically analyze V_{th} drifts are measurements of the hysteresis in the transfer characteristics that is evaluated at V_{th}, see Section 3.1.2 and BTI measurements, see Section 3.2.3. As the hysteresis in Si based FETs is generally so small that it is of no concern for standard operating conditions, it is usually not analyzed [TKJ7, 490] and is only a phenomenon of interest in less mature device technologies, such as SiC power FETs [491, 492] or 2D material-based FET prototypes [202, 489]. In contrast, BTI is one of the most important reliability concerns in Si devices [236, 239, 244] and also orders of magnitude larger in most 2D prototypes [214, 253]. Nevertheless, both phenomena are caused by border traps and the different measurement processes only give two different views on the same charge trapping events. To be precise, in a hysteresis measurement the gate voltage is swept from a minimum gate voltage level to a maximum gate voltage at a certain constant sweep rate. Thus, to a hysteresis measurement all border traps which are triggered by the applied electric field contribute to change their charge state during the up sweep and retain this changed charged state until after the down sweep. Thus, a specific subset of border traps is activated during a hysteresis measurement, depending on the sweep range and the sweep rate of the gate voltage. During a BTI measurement, border traps are charged during an initial stress phase and their recovery during the recovery phase is observed, thereby activating another subset of border traps. Under standard measurement conditions, these subsets typically overlap to a considerable extent, thus a hysteresis and BTI analysis reveal two complementary perspectives on the border traps which are active within a

certain device design and technology. In the following, the hysteresis and BTI are analyzed in two different batches of MoS_2 based FETs using SiO_2 and Al_2O_3 as gate oxides [TKJ15, TKJ16] and three batches of graphene FETs with an Al_2O_3 gate oxide [TKJ3].

5.1.1 Hysteresis in MoS_2 and Graphene Transistors

As described in Section 3.1.2, the hysteresis in the transfer characteristics is quantified by the hysteresis width (ΔV_H) which is evaluated at the threshold voltage measured during up and down sweep ($\Delta V_H = V_{th,up} - V_{th,down}$). A comprehensive hysteresis measurement records ΔV_H for different voltage sweep ranges and voltage sweep times (t_{sw}), where typically the largest hysteresis is observed for large voltage ranges and long sweep times.

For example, the hysteresis in the I_D-V_{GS} characteristics measured at the top gate of double gated monolayer MoS_2 FETs is shown in Figure 5.1 (a). For these devices, as reported in [TKJ15], the layout is similar to Figure 2.3 (d) and uses exfoliated MoS_2 monolayers in combination with 23.5 nm of Al_2O_3 as a top gate oxide and 280 nm SiO_2 as a back gate oxide. When sweeping the top gate from −10 V to 12 V and back at a voltage sweep rate of $S = 50\,V/s$, the resulting transfer characteristics are shown in Figure 5.1 (a) on the left. For describing a hysteresis in the I_D-V_{GS} characteristics, the sweep rate S is defined as the quotient of the gate step voltage V_{step} and the sampling time t_{step}, $S = V_{step}/t_{step}$. If the entire voltage sweep range for one up and down sweep cycle is known, the total swept voltage per cycle V_{tot} is twice the sweep range, given by $V_{tot} = 2 \times |V_{GS,max} - V_{GS,min}|$. The sweep rate can be converted into the sweep time, t_{sw}, via $t_{sw} = V_{tot}/S$, which in turn corresponds to a sweep frequency of $f = 1/t_{sw}$. Consequently, in this case with $V_{tot} = 44\,V$ a sweep frequency of $f = 1.1\,Hz$ is obtained. In Figure 5.1 (a) on the right, the sweep frequency is varied between 0.9 mHz and 22 Hz, showing that indeed the largest hysteresis is observed for the smallest sweep frequency of 0.9 mHz, thus for the longest sweep time. In both Figures 5.1 (a) and (b) the points show measured values and the solid lines simulation results, as obtained with TCAD simulations using Minimos-NT [317], for details see Section 6.1.3.

When evaluating the hysteresis widths at the threshold voltage as defined by a constant-current criterion, see Section 3.1.2 for both varying gate sweep ranges V_{tot} and sweep rates S, a wide variation of the hysteresis widths between 0.1 V and 12 V is observed that spans more than two orders of magnitude, see Figure 5.1 (b). The largest ΔV_H is observed for the largest sweep range of $[-10\,V, 14\,V]$ and the smallest sweep frequency of 0.9 mHz. These hysteresis results were modeled using charge transfer of electrons from the MoS_2 conduction band to border traps in the Al_2O_3, which are shown in the band diagrams in Figure 5.1 (c). It can be observed that as V_{tg} becomes increasingly more positive, more and more electron traps of the defect band in the Al_2O_3 become charged. Based on the TCAD simulations an electron trapping band at 2.15 eV below the conduction band edge of the Al_2O_3 was extracted, which is in good agreement with literature data, see Table 5.1 and the discussion in the section about the hysteresis in graphene FETs below. In Figure 5.1 (d) the corresponding distribution of border traps in Al_2O_3 and SiO_2 as applied in simulations is shown. Due to the bending of the bands in the Al_2O_3 for different applied top gate voltages, the distribution of the Al_2O_3 border traps is shifted from above the Fermi level, where it is completely inactive, and discharged to

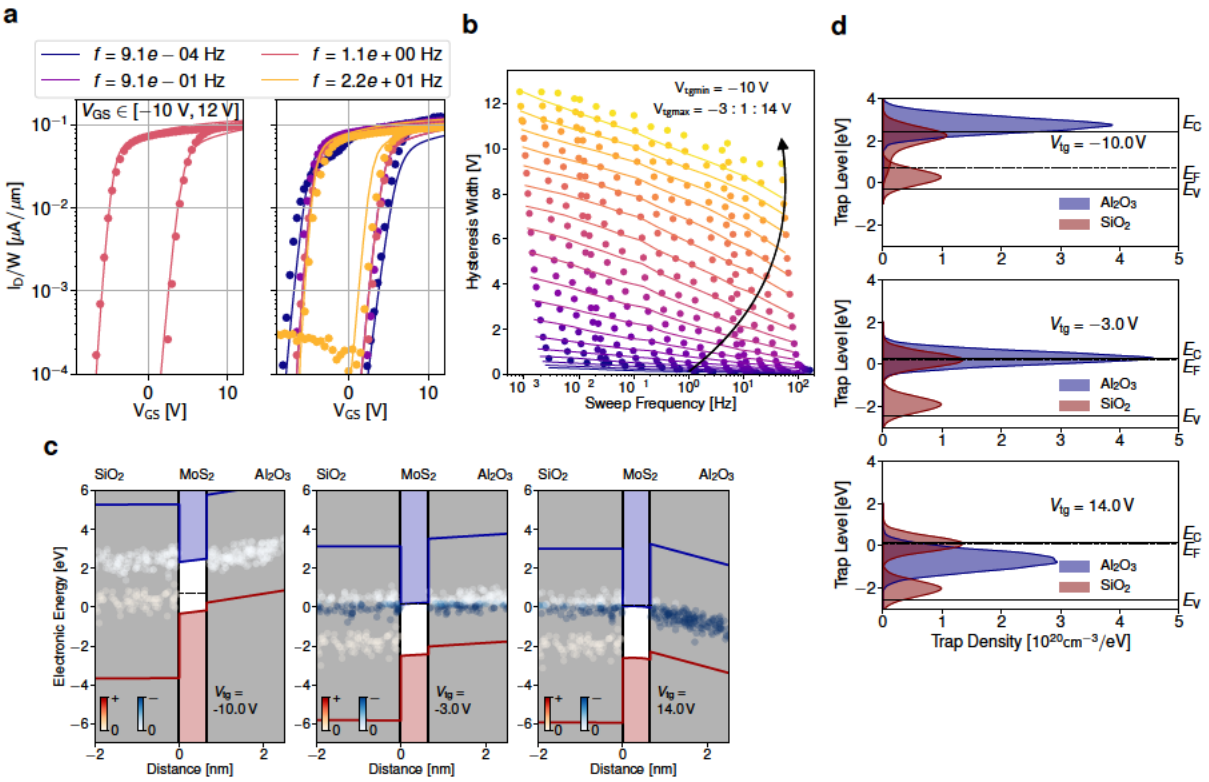

Figure 5.1. **(a)** Hysteresis measurements at the Al_2O_3 top gate for double-gated MoS_2 FETs while keeping the back gate grounded at 0 V. The layout of the FETs is similar to the one shown in Figure 2.3(d) using 23.5 nm of Al_2O_3 as a top gate oxide and 280 nm SiO_2 as a back gate oxide. The hysteresis at the top gate is shown for $V_{tg} \in [-10\,V, 12\,V]$ with different gate sweep frequencies $f = 1/t_{sw}$ on the right. The points correspond to measured values and the solid lines to simulation results, see Section 6.1.3. **(b)** The hysteresis width is shown as a function of the sweep frequency f for varying top gate sweep ranges, with the smallest sweep range of $V_{tg} \in [-10\,V, -3\,V]$ in dark blue and the largest sweep range of $V_{tg} \in [-10\,V, 14\,V]$ in yellow. Once again, the points are measurement values and the lines TCAD simulation results using Minimos-NT [317]. **(c)** Band diagrams showing the charge state of the border traps in SiO_2 and Al_2O_3 at −10 V on the left, at V_{th} =−3 V in the middle and 14 V on the right. As many electron traps in Al_2O_3 change their charge state, this electron trapping is the primary cause for the hysteresis. **(d)** Here, the border trap density is shown as projected on its location with respect to the MoS_2 band gap. Due to band bending the maximum of the border trap distribution in Al_2O_3 crosses the conduction band edge as the top gate voltage sweeps from −10 V to 14 V. All graphics in this figure are adapted from [TKJ15].

below the Fermi level. During this process a considerable number of traps can be charged, even though it should be noted that charge trapping is a stochastic process and only traps with charging time constants below the sweep time will likely be charged. All of these traps, which in addition retain their changed charge state until the end of the down sweep as their emission time constants are large enough, contribute to the hysteresis observed in Figure 5.1 (b).

Other factors besides border traps which are able to contribute to the observed hysteresis are adsorbed molecules from the ambient environment [202, 489], an effect that is particularly strong for bare 2D FETs with a layout comparable to 2.3 (a). Therefore, the hysteresis characteristics shown in Figure 5.1 was measured in vacuum at a pressure below 1×10^{-3} Pa.

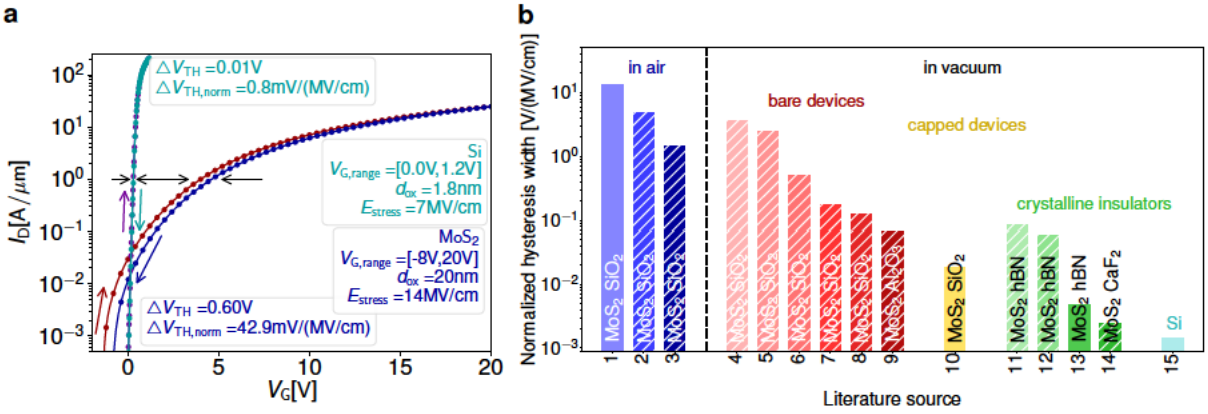

Figure 5.2. **(a)** Comparison of the hysteresis width in MoS_2 FETs [TKJ16] with the hysteresis width in commercial Si FETs [490]. In order to be able to compare the hysteresis for different technologies, the hysteresis width is normalized by the applied electric gate stress field $\Delta V_{H,norm} = \Delta V_H / E_{stress}$. This comparison reveals that $\Delta V_{H,norm}$ is about 50 times larger in MoS_2 as compared to Si FETs. **(b)** When comparing the literature values of the normalized hysteresis width for different MoS_2 based FETs, it can be seen that the hysteresis width is reduced for measurements in vacuum and capped FETs, with the smallest $\Delta V_{H,norm}$ being observed for crystalline insulators. Measurements were performed at a sweep rate (S) of about 1 V/s in references 1-[493], 2-[202], 3-[494], 4-[495], 5-[202], 6-[TKJ21], 7-[TKJ16], 8-[206], 9-[495], 10-[TKJ16], 11-[TKJ21], 12,13-[385], 14-[TKJ7], 15-[490]. Both graphics in this figure are adapted from [TKJ1].

The knowledge that the hysteresis is usually smaller for faster gate voltage sweeps, is taken advantage of in a pulsed measurement scheme, where the hysteresis is reduced if the gate voltage is applied only in short measurement pulses with sampling times below 1 ms [206]. Consequently, this means that the hysteresis will likely be of less concern if FETs are used in logic or RF applications, where switching speeds are typically within the GHz regime [21]. However, the time constant distribution of border traps is extremely broad, stretching even down to the ns range, see Section 4.2.2, thus it cannot be excluded that a considerably smaller but not fully negligible hysteresis might be observed also at fast switching speeds. In addition, it should be noted that the slower border traps, probed with the hysteresis measurements in Figure 5.1 and in reference [TKJ15], cause V_{th} drifts for longer operation times of several weeks, months and years. These same border traps which are responsible for the slow switching hysteresis also cause BTI degradation both under DC and AC operating conditions, for details see Section 5.1.2.

Hence, it is important to considerably reduce the number of electrically active border traps in 2D material-based FETs. For example, a comparatively small hysteresis of $\Delta V_H = 0.6$ V was measured on encapsulated CVD MoS_2 devices using 20 nm of SiO_2 as a back gate oxide [TKJ16]. However, to compare the hysteresis widths as measured on different technologies, they need to be normalized by the effective electric gate field as applied during the sweep,

$$\Delta V_{H,norm} = \frac{\Delta V_H}{K}, \qquad K = \frac{|V_{GS,max} - V_{GS,min}|}{EOT}. \tag{5.1}$$

In this case, for a gate voltage range of [−8 V, 20 V], an electric field factor of $K = 14\,\mathrm{MV/cm}$ was effectively applied, corresponding to $\Delta V_{\mathrm{H,norm}} = 42.9\,\mathrm{mV/(MV/cm)}$. In comparison to the hysteresis measured in commercial Si MOSFETs [490], see Figure 5.2 (a), the hysteresis in MoS_2/SiO_2 devices is about a factor of 50 higher [TKJ1]. Thus, the number of electrically active border traps needs to be reduced. One possible approach is to use insulators which form a high quality van der Waals interface and contain fewer border traps, conditions which are met by crystalline insulators such as hBN or CaF_2. This claim is supported by the comparison of different experimental studies of the hysteresis in MoS_2 FETs at a sweep rate of 1 V/s presented in Figure 5.2 (b), as the smallest hysteresis observed to date was reported when using hBN [385] or CaF_2 [TKJ7] as a gate insulator, see also Section 4.4.

Next, the hysteresis in the transfer characteristics of two types of graphene FETs (GFETs) is analyzed. In GFETs the threshold voltage corresponds to the charge neutrality or the Dirac voltage (V_{Dirac}), the gate voltage where the current is at its minimum [258]. Thus, ΔV_{H} is determined as the shift of the characteristics evaluated at V_{Dirac} [251, 496]. Both batches of GFETs investigated here use graphene monolayers grown with CVD as a channel, see Section 2.1.1. Channel dimensions span $W \times L = 100\,\mu\mathrm{m} \times 160\,\mu\mathrm{m}$, thus the GFETs have a comparatively large active region and were fabricated on top of mechanically flexible polyimide (PI) substrates [497]. In the top gated device layout a 40 nm thick, amorphous Al_2O_3 grown by ALD serves as gate oxide, see Section 2.1.4.

The two fabricated GFET batches use two different graphene layers which mainly differ in their respective doping and layer quality and are referred to in the following as Type 1 and Type 2 graphene. These graphene layers were purchased from different vendors who most likely used different parameters for the CVD process and the layer transfer. These differences in processing result in vastly differing material qualities, with Type 2 graphene revealing a much higher concentration of defects. To assess the functionality and performance of the GFETs, the transfer characteristics are shown in Figures 5.3 (a) for a representative Type 1 GFET. When comparing these characteristics to those of Type 2 GFETs in Figure 5.3 (b), it is evident that the higher quality of Type 1 graphene leads to higher current densities. Based on two-probe measurements of the I_{D}-V_{G} characteristics the field-effect mobilities are estimated to reach up to $5000\,\mathrm{cm^2V^{-1}s^{-1}}$ in Type 1 GFETs, four times higher than the average mobility of about $600\,\mathrm{cm^2V^{-1}s^{-1}}$ in Type 2 GFETs.

Negatively charged dopants in Type 2 graphene lead to a higher variability and shift V_{Dirac} towards more positive voltages, as can be seen from the comparison of V_{Dirac} measured on 50 GFETs for each graphene type in Figure 5.3 (c). A more positive V_{Dirac} corresponds to a higher p-doping of the sample and correlates with a higher work function (E_{W}) [498, 499]. Pristine graphene has a work function of 4.56 eV [500], which is shifted towards higher values by p doping [498, 501] and towards smaller values by n doping [499, 502]. In order to calculate the Fermi level location in the two graphene types, the charge carrier concentration per area (n_{S}) is obtained based on the analytic expression for n_{S} in a MOS capacitor [428, 503, 504], see also Equation (3.2) in Section 3.1.1. Here, n_{S} is evaluated at 0 V top gate bias to extract the charge carrier concentration caused by the intrinsic doping of the graphene samples without

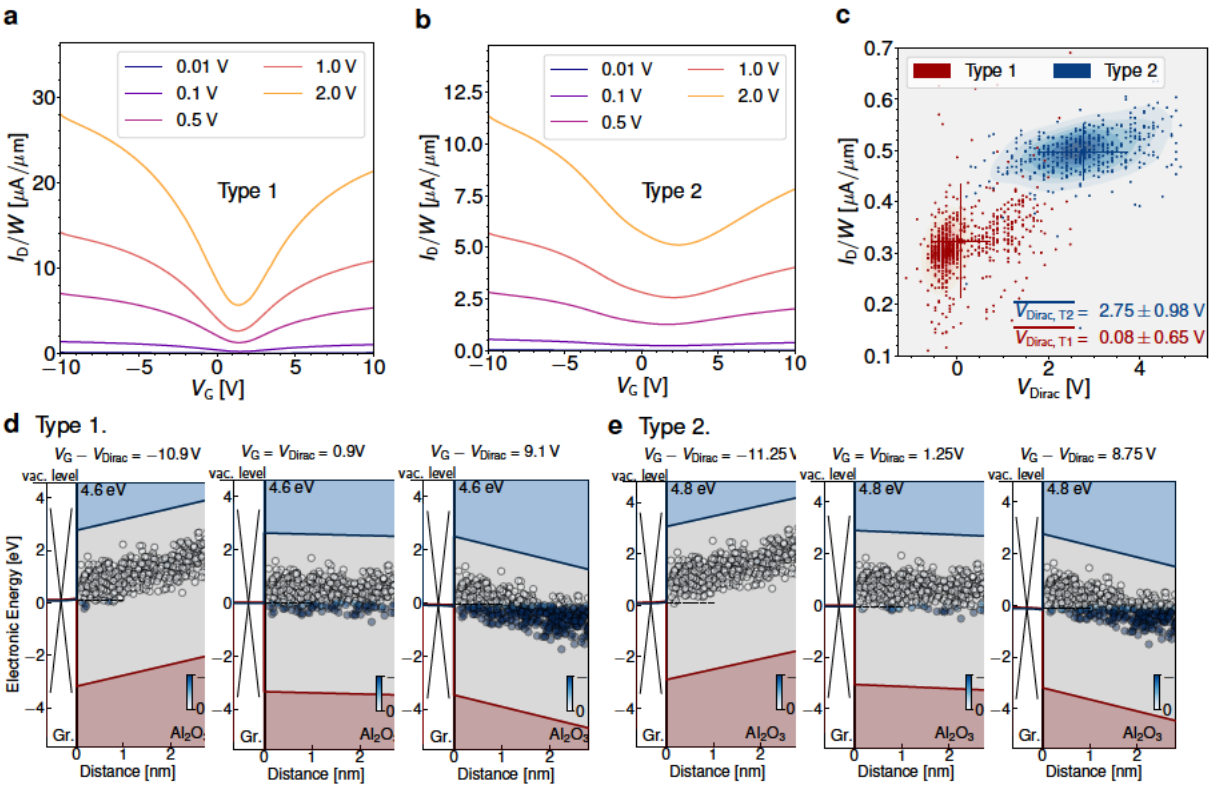

Figure 5.3. **(a)** Transfer (I_D-V_{GS}) characteristics of a top gated graphene FET (GFET). The GFETs' layout is similar to the one shown in Figure 2.3(d) but uses flexible polyimide as a substrate, and 40 nm of Al_2O_3 as top gate oxide. **(b)** I_D-V_{GS} characteristics of a representative Type 2 GFET are shown, including only the forward sweeps, as the backward sweeps are reported in Figure 5.5. Type 2 GFETs use the same layout as Type 1 GFETs but are based on a different CVD graphene from another vendor. **(c)** Comparison of the mean current and voltage at the Dirac point for the two graphene types. These values were extracted from the I_D-V_{GS} characteristics measured on 50 different GFETs per type using $V_{DS} = 0.1$ V. Every single measurement value is given as a small dot and the large dots show the mean value and bars denote error bars, giving the error of 1σ. **(d)** Based on the location of V_{Dirac} a work function of $E_W = 4.6$ eV for Type 1 GFETs was extracted, showing here the schematic band diagram of the alignment of the graphene Fermi level with respect to the Al_2O_3 defect bands. **(e)** Band diagrams for Type 2 GFETs with $E_W = 4.8$ eV are shown at different V_{tg} voltages. All graphics in this figure are adapted from [TKJ3].

gate impact

$$n_S(V_{GS}) = \frac{C_{tot}}{q} |V_{GS} - V_{Dirac}| . \tag{5.2}$$

For these GFETs, the total gate capacitance of the structure (C_{tot}) is given by the capacitance of the Al_2O_3 (C_{ox}) in series with the capacitance of an estimated 0.5 nm van der Waals gap (C_{vdW}) and the quantum capacitance of graphene [505] (C_q), amounting to $C_{tot} = 0.16\,\mu F/cm^2$. This expression gives a p-doping density for Type 1 graphene of $n_1 = 5.5 \times 10^{10}\,cm^{-2}$ and for Type 2 graphene of $n_2 = 2.8 \times 10^{12}\,cm^{-2}$, thus Type 2 graphene is more p-doped by an additional doping density of approximately $2.75 \times 10^{12}\,cm^{-2}$. These hole densities in the graphene layers

at 0 V gate voltage determine the work function via [502, 506]

$$E_W = \hbar v_F \sqrt{\pi n} \tag{5.3}$$

with the Fermi velocity of graphene $v_F = 1.1 \times 10^6\,\mathrm{ms}^{-1}$ [258]. Consequently, the work functions E_{W1} of Type 1 and Type 2 graphene are found to be 4.6 eV and 4.8 eV, respectively. This work function location determines the location of the Fermi level with respect to the border traps in the Al_2O_3 gate oxide. In turn, as will be demonstrated, this alignment governs the electrical stability and reliability of the two types of graphene FETs.

Ref./Defect	Method	Channel	Insulator	χ	E_T (E_C) in [eV]	E_T (vac)	σ_{E_T}
[418]	TSCIS	Si	SiO_2+Al_2O_3	1.3	2.0	3.3	0.5
[426]	TSCIS	Si	SiO_2+Al_2O_3	1.4	2.2	3.6	0.5
[507]	PBTI	InGaAs	Al_2O_3	1.5	1.8	3.3	0.85
[508]	PBTI	InGaAs	Al_2O_3	1.5	1.9	3.4	0.6
[TKJ15]	Hysteresis	MoS_2	Al_2O_3	1.55	2.55	4.1	0.3
[TKJ3]	Hysteresis	Graphene	Al_2O_3	1.95	2.15	4.1	0.3
O vacancy [509]	DFT	-	-	1.5	1.9	3.4	-
O vacancy [510]	DFT	-	-	1.95	2.0	3.95	1.1
Al interstitial [510]	DFT	-	-	1.95	2.1	4.05	1.1

Table 5.1. Parameters of the Al_2O_3 defect band. At the top, the location of defect bands as extracted from experiments is shown and at the bottom possible microscopic defect candidates calculated with DFT, reproduced from [TKJ3].

To accurately determine the alignment of E_F in graphene to the electron trapping band of the amorphous Al_2O_3 gate oxide at $\overline{E_T}$, the precise location of the oxide defect band must be known. Several studies have investigated the alignment of this defect band using trap spectroscopy by charge injection and sensing (TSCIS) [418, 426], BTI [507, 508], and hysteresis measurements [TKJ15]. The defect band parameters of Al_2O_3 as obtained from literature are listed in Table 5.1 and shown in Figure 5.4. Based on density functional theory (DFT) calculations, this defect band can be associated with either oxygen vacancies [509, 510] or aluminum interstitials [510]. To estimate the behavior of these traps, a normally distributed defect band was used, with the mean defect level at $E_C - E_T = 2.15 \pm 0.3$ eV below the conduction band edge of Al_2O_3 [TKJ3]. The electron affinity (χ) of Al_2O_3, which determines the location of the conduction band edge, varies in literature. Here, the value of 1.96 eV, as obtained from internal photoemission measurements, is used [425]. For Type 1 graphene E_F is aligned within the defect band (small $\overline{E_T} - E_F$, electrically unstable), see Figure 5.3 (d), whereas it is aligned below the defect band for Type 2 graphene (high $\overline{E_T} - E_F$, electrically more stable), see Figure 5.3 (e). This predicted electrical stability is tested in the following using hysteresis and BTI measurements.

It is worth noting that the coloring of the defect band in Figures 5.3 (d) and (e) as an electron trapping band is a simplification. The distinction between electron trapping (acceptor-type) bands and hole trapping (donor-type) bands depends only on the overall amount of charges

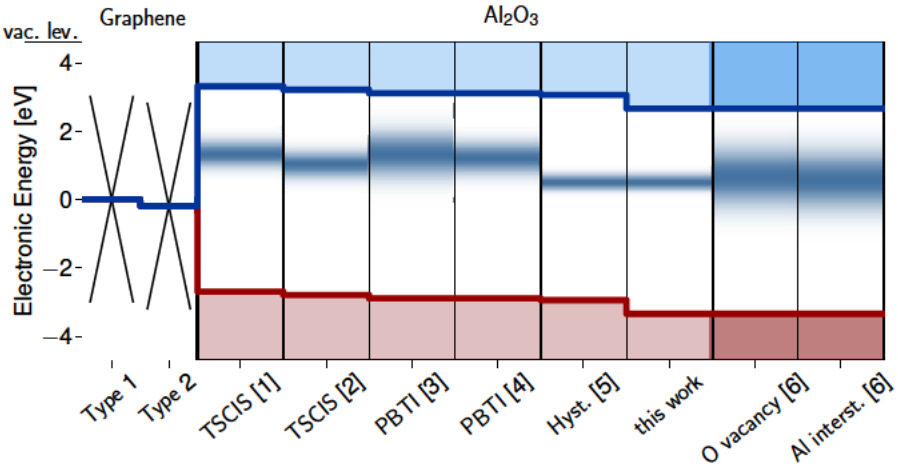

Figure 5.4. The band diagram illustrates the alignment of the Al_2O_3 defect band to the Fermi level in graphene of Type 1 and Type 2. To the left, the defect band location as determined from experiments is shown, 1-[418], 2-[426], 3-[507], 4-[508], 5-[TKJ15]. To the right, the alignment of the defect band is shown according to the DFT calculations, as caused by oxygen vacancies and Al interstitials, 6-[510]. Reproduced from [TKJ3].

in the device. An acceptor-type defect changes its charge state from neutral to negative upon electron capture and a donor-type defect from positive to neutral. The only measurable difference between acceptor- and donor-type bands is the overall amount of fixed charges, which is inaccessible to hysteresis and BTI measurements. Here, the coloring is based on the assumption that in the as-grown Al_2O_3 the majority of defects are neutral. Therefore, all defect bands in the upper part of the band gap are considered to be electron trapping bands and all defect bands in the lower part are denoted as hole trapping bands.

Information about the charge state of the oxide defects can be obtained from DFT calculations. According to Dicks *et al.* the thermodynamically stable states of the oxygen vacancy in amorphous Al_2O_3 are the +2 charge state and the neutral state [510]. The aluminum interstitial is stable at a charge of +3 and +1. The Al_2O_3 defect band corresponds to the transition of these two defects from their more positive to their less positive state. To explain the overall neutrality of the as-grown Al_2O_3 a balance is invoked of negatively charged Al vacancies and O interstitials and positively charged O vacancies and Al interstitials [510]. When the device is subjected to a large gate bias, the O vacancies and Al interstitials become less positively charged and consequently the overall charge within the system changes. The change of the net charge is the same as in the simplified image depicted in Figures 5.3 (d) and (e).

Since the observed hysteresis depends critically on the voltage ranges used for the gate voltage sweeps, we compare the bias ranges used for the hysteresis measurements with the ranges for various applications in Figure 5.5 (a). State-of-the-art silicon transistors operate at an electric gate field of 10 MV/cm, estimated based on the equivalent oxide thickness (EOT) [21], up to which logical switches should show stable operation. As the GFETs studied here employ an Al_2O_3 layer with 40 nm physical thickness as a gate oxide, their EOT amounts to ~17 nm. When used in radio-frequency (RF) circuits the electric gate fields span from 3.5 MV/cm to 8.1 MV/cm [511, 512, 513, 514] and thus the gate oxide fields investigated in the following are

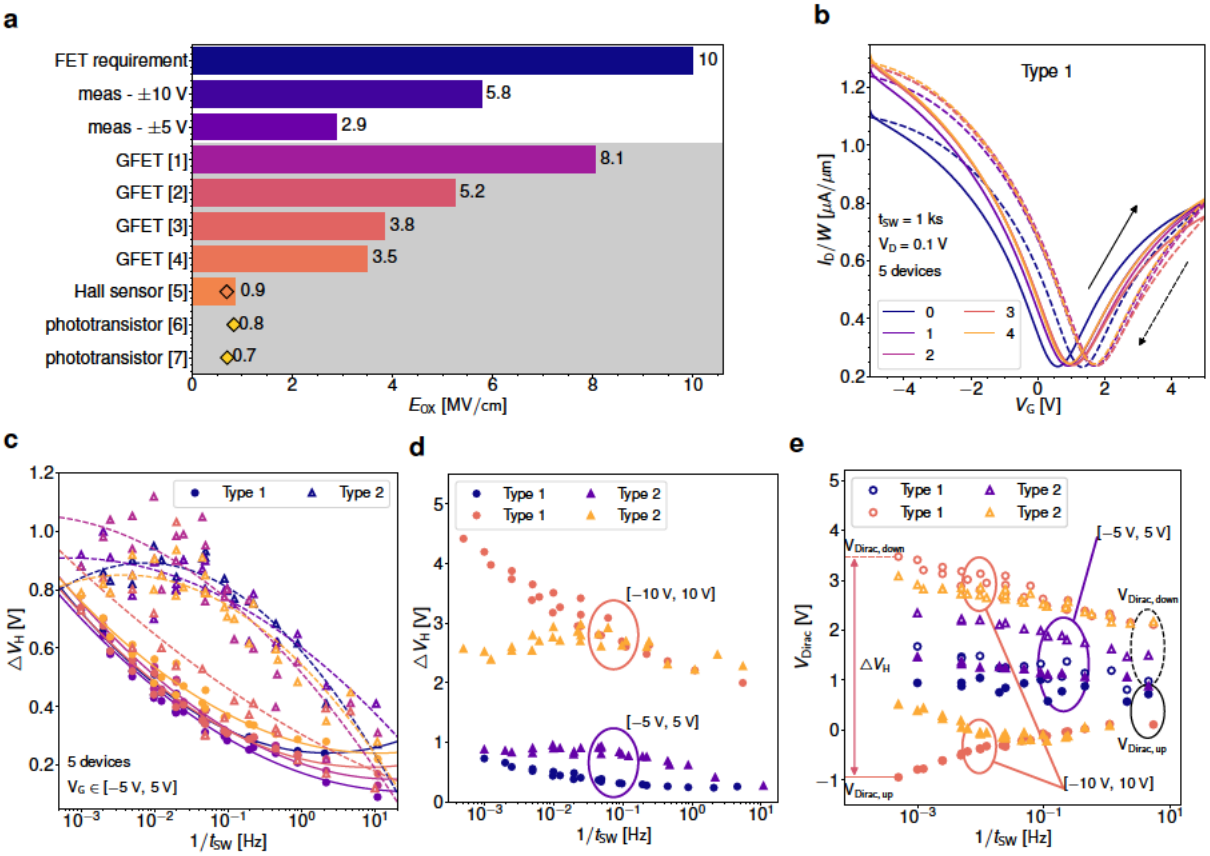

Figure 5.5. **(a)** Comparison of the electric fields for the two measurement voltage ranges used in the GFET study presented here, together with the typical voltage ranges for various applications. The field up to which GFETs should show stable operation is shown at the top in dark blue [21] and the ranges used in this work are shown in purple below. Application scenarios are from 1-[511], 2-[512], 3-[513], 4-[514], 5-[515], 6-[516], 7-[517]. **(b)** Hysteresis in the transfer characteristic as measured on 5 different Type 1 GFETs, where a small variability is observed. **(c)** The hysteresis width is shown as a function of the inverse sweep time $f = 1/t_{SW}$ for 5 devices for each graphene type. Circles and triangles represent Type 1 and Type 2 GFETs and the solid and dashed lines are guides to the eye for Types 1 and 2. **(d)** Comparison of the hysteresis width for Type 1 and Type 2 GFETs. These measurements were performed on one representative GFET per graphene type. **(e)** Comparison of the Dirac point shifts for the up and down sweeps. $V_{Dirac,down}$ / $V_{Dirac,up}$ are shown as empty/full symbols respectively. All graphics in this figure are adapted from [TKJ3].

standard operating conditions for RF applications. If, on the other hand, GFETs are used as sensors in the form of phototransistors [516, 517] or Hall elements [515], moderate gate fields of up to 1 MV/cm are sufficient to maximize responsivity.

To evaluate the hysteresis in the two batches of GFET prototypes, the double sweep transfer characteristics for a small voltage range of [−5 V, 5 V] on five GFETs based on Type 1 graphene are compared in Figure 5.5 (b). Little variability is observed, which is confirmed when studying the hysteresis width ΔV_H as a function of the sweep frequency f. In Figure 5.5 (c) the hysteresis width as a function of the sweep frequency is shown for five GFETs based on Type 1 and five GFETs based on Type 2. Type 2 devices exhibit a considerably higher variability of ΔV_H than Type 1 devices, which is linked to the increased variability of V_{Dirac} on Type 2,

see Figure 5.3 (c). An increased bias range of [−10 V, 10 V] increases the hysteresis, because more oxide defects become accessible for charge transfer, as can be seen in Figure 5.5 (d) for representative Type 1 and Type 2 GFETs. To shed more light on this behavior, the dynamics of the Dirac voltage shifts are analyzed as a function of the sweep frequency in Figure 5.5 (e). For the [−5 V, 5 V] sweep, $V_{\text{Dirac,up}}$ and $V_{\text{Dirac,down}}$ as a function of the sweep frequency show similar slopes for both types. However, for the 10 V sweep range and Type 1, $V_{\text{Dirac,up}}$ is shifted to more negative voltages in slow sweeps, while $V_{\text{Dirac,down}}$ is shifted to more positive voltages. This indicates that for large sweep ranges on Type 1 GFETs, a significant amount of electrons are emitted from oxide traps between −10 V and $V_{\text{Dirac,up}}$, whereas for Type 2, charge trapping in this interval can be neglected. This reversed drift of $V_{\text{Dirac,up}}$ to more negative voltages for slow sweeps results in an increase in the hysteresis width in Type 1 GFETs, shown in Figure 5.5 (d). This observation confirms the expectation that, as the E_{F} of the Type 1 GFET gets closer to the Al_2O_3 defect band, the GFETs become electrically less stable.

The band alignments shown in Figures 5.3 (d) and (e) explain the larger hysteresis in Type 1 GFETs in comparison to Type 2 qualitatively: In Type 1 GFETs biased at V_{Dirac}, a considerable number of defects is negatively charged. If a negative voltage is applied, these defects discharge due to the band bending and thus V_{Dirac} is shifted to more negative voltages during a slow up-sweep (Figure 5.5 (d)). In Type 2 GFETs, in contrast, the Fermi level is located below the defect band at V_{Dirac}, as its Fermi level has been shifted down by 200 meV. Thus, most defects are neutral at the Dirac voltage. If a long time is spent with the GFET biased at negative voltages, the charge states do not change and the location of V_{Dirac} during the up sweep is stable independent of the sweep time. In short, the higher $\overline{E_{\text{T}}} - E_{\text{F}}$ of Type 2 graphene with respect to the Al_2O_3 defect band leads to a smaller hysteresis width for large sweep ranges. At small gate bias ranges and fast hysteresis sweeps, Type 2 devices suffer from more charge trapping at the unclean interface with the Al_2O_3 insulator, and the hysteresis is similar in Type 2 GFETs compared to Type 1. For fast sweeps, fast traps at the unclean interface in Type 2 GFETs increase the hysteresis, giving the impression of a frequency independent hysteresis width (Figure 5.5 (d)). Type 1 GFETs exhibit a cleaner interface but a smaller $\overline{E_{\text{T}}} - E_{\text{F}}$ with respect to the Al_2O_3 defects, strongly degrading the GFETs during slow sweeps. For high gate bias ranges and slow sweeps, the border traps of the Al_2O_3 dominate device stability, thus more stable operation of Type 2 GFETs is observed. In Section 5.1.2, the trapping behavior of the border traps are investigated using BTI measurements, revealing the same trends.

5.1.2 BTI in MoS_2 and Graphene Transistors

As described in detail in Section 3.2.3, BTI measurements are a standardized measurement process to characterize charge trapping in the gate insulator at elevated gate biases and temperatures. Since BTI measurements probe a similar subset of the border traps in the gate insulators as hysteresis measurements, trends similar to those described in Section 5.1.1 are expected to be observed in the following. In a comprehensive BTI measurement, the threshold voltage shifts ΔV_{th} are evaluated both for positive and negative gate biases, PBTI and NBTI, during both stress and recovery periods.

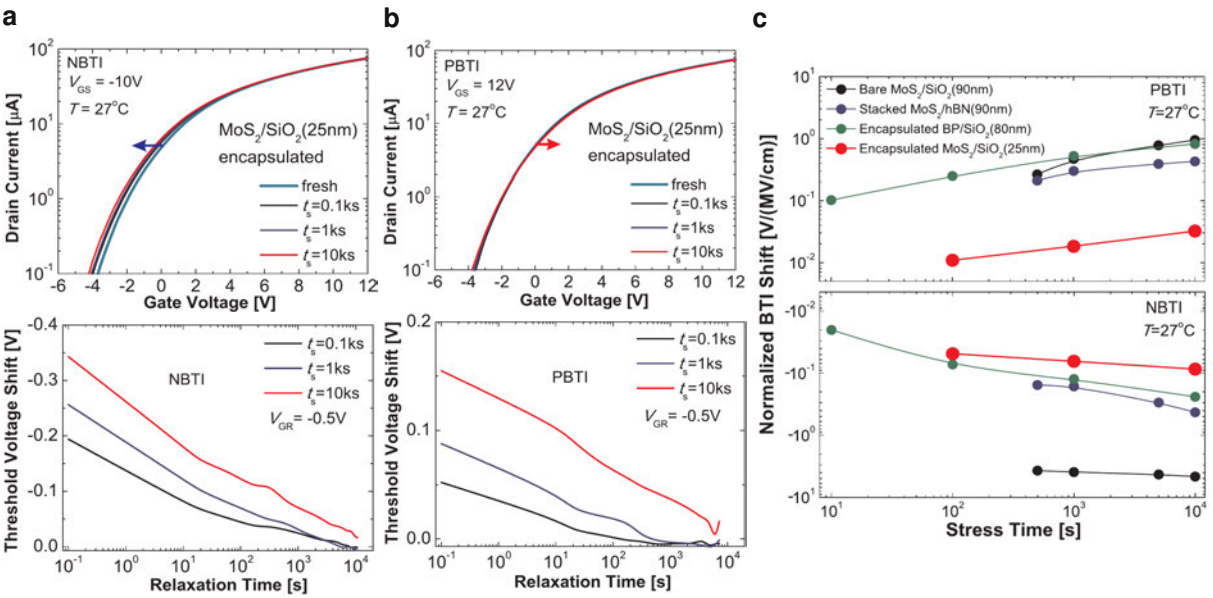

Figure 5.6. **(a)** NBTI measurements on back gated, encapsulated MoS_2 FETs using 20 nm of SiO_2 as a gate oxide. These FETs use a layout similar to Figure 2.3 (b) with 15 nm of ALD Al_2O_3 serving as an encapsulation layer for CVD grown MoS_2 monolayers with an active area of $W \times L = 20\,\mu m \times 8\,\mu m$. At the top the increasing shifts of the I_D-V_{GS} characteristics towards more negative V_{th} is shown for increasingly long stress times t_S. At the bottom, ΔV_{th} drifts are shown for these stress times, revealing complete recovery of the MoS_2 FETs. **(b)** PBTI measurements, showing the increasing shifts of the I_D-V_{GS} characteristics towards more positive V_{th} at the top. At the bottom, the ΔV_{th} drifts are presented, again showing a complete recovery. **(c)** Comparison of the normalized PBTI (top) and NBTI (bottom) shifts with values from literature for different MoS_2 device layouts [TKJ21, 518]. The drifts are smallest for the Al_2O_3 encapsulated FETs based on CVD MoS_2 monolayers. All graphics in this figure are reproduced from [TKJ16].

In Figure 5.6, BTI results on monolayer MoS_2 FETs with a 20 nm SiO_2 back gate oxide and 15 nm of Al_2O_3 as encapsulation are shown. These devices are based on high-quality CVD grown MoS_2 monolayers [TKJ16, 100], see Section 2.1.1, and employ a layout comparable to Figure 2.3 (b). BTI degradation was evaluated at room temperature using sequential stress and recovery cycles. For logarithmically increasing stress times (t_s), a bias of −10 V (NBTI) or 12 V (PBTI) was applied and the V_{th} degradation was evaluated using fast I_D-V_{GS} sweeps both directly after stress and for logarithmically increasing relaxation times. In Figure 5.6 (a) at the top, the increasing shifts of the fast sweep I_D-V_{GS} characteristics towards more negative V_{th} for increasing stress times are shown. It can be seen that the overall drifts are small and that the transfer characteristics are not degraded by the bias stress except for the V_{th} shifts. These ΔV_{th} shifts are presented as a function of the relaxation time (= recovery time), revealing complete recovery of the shifts after 10 ks. For PBTI stress the same trends as for NBTI stress are observed in Figure 5.6 (b), with the exception that the overall PBTI degradation is smaller by a factor of about two.

When comparing these BTI drifts to previously reported BTI degradation [TKJ21, 518] in Figure 5.6 (c), these FETs show considerably reduced BTI levels. Again, in order to be able to compare BTI drifts measured on different technologies, they need to be normalized by the

gate oxide field which is applied during the stress period $\Delta V_{\text{th,norm}} = \Delta V_{\text{th}} / E_{\text{stress}}$, see also Equation (5.1) for the hysteresis. In Figure 5.6 (c) the black lines represent bare exfoliated MoS_2 on 90 nm SiO_2 devices [TKJ21] with a device layout as shown in Figure 2.3 (a). By introducing an hBN stack around the MoS_2, NBTI is substantially reduced (dark blue line) [TKJ21] down to a BTI degradation level comparable to encapsulated BP FETs using 80 nm SiO_2 as a gate insulator and 25 nm Al_2O_3 as an encapsulation [518]. The BTI drifts shown in Figure 5.6 and in [TKJ16] demonstrate very small PBTI degradation levels for 2D material-based FETs.

However, the direct comparison of BTI drifts for different technologies poses numerous challenges. In fact, the observed drifts depend both on the border trap densities in the respective gate insulators, and thus on the processing, as well as on the exact band alignment of the conduction and valence band of the 2D semiconductor to the defect bands in the gate insulator. Therefore, direct comparison studies where selected single components of the FET layout are modified provide excellent opportunities for increasing the understanding of BTI degradation in 2D material-based FETs. Within the scope of this thesis, such a study was performed on the GFETs introduced in the previous Section 5.1.1, where by different CVD and transfer processes the graphene material quality and more importantly the graphene doping were varied. In this way the BTI stability of GFETs using Type 1 graphene with a work function of 4.6 eV was investigated as well as the stability of Type 2 GFETs with $E_W = 4.8$ eV [TKJ3].

Also for the GFETs, the magnitude of the initial ΔV_{Dirac} shift is recorded and the recovery after gate bias stress is monitored using fast I_D-V_{GS} sweeps at logarithmically spaced recovery times. In Figure 5.7 (a) the fast I_D-V_G sweeps recorded during the recovery from negative gate biasing (NBTI) at −10 V are shown. These BTI measurements specifically probe the impact of border traps on long-term stability and drifts, which is why any influence of the hysteresis in the transfer characteristics on the measurement results needs to be minimized. In order to minimize measurement artifacts due to the hysteresis in the probing I_D-V_{GS} curves, the down sweep I_D-V_G curves are used to evaluate the V_{Dirac} shifts for all NBTI measurements and the up sweep I_D-V_G curves for positive gate biasing (PBTI) [251].

NBTI, measured by subjecting the devices to a gate bias of −10 V for increasingly long charging times (=stress times), is shown in Figure 5.7 (b) for Type 1 GFETs and in Figure 5.7 (c) for Type 2 GFETs. As expected, based on the defect band alignment shown in Figures 5.3 (d) and (e), the V_{Dirac} shifts are smaller on Type 2 devices than on Type 1 devices. GFETs based on Type 2 graphene are more stable with respect to long-term degradation because the Fermi level of Type 2 graphene is further away form the Al_2O_3 defect band. Therefore, on Type 2 GFETs fewer oxide traps change their charge state during negative gate biasing, resulting in smaller shifts of V_{Dirac}, which also recover faster since the traps which emit electrons are located closer to the interface and thus have smaller time constants. For Type 2 GFETs, slight over-recovery [271] is observed for the shortest charging time of 1 s. Over-recovery is the phenomenon when, during a BTI measurement, the observed ΔV_{Dirac} shifts do not converge towards the initial state at ΔV_{Dirac} =0 V. Instead, an overshooting behavior is observed where V_{Dirac} continues to drift from negative to positive shifts. This phenomenon has been observed multiple times on FETs based on graphene [271] and TMDs [TKC7, TKC2]. In the GFETs studied here this is only observed for the shortest NBTI charging of 1 s and thus it is probable that the over-recovery

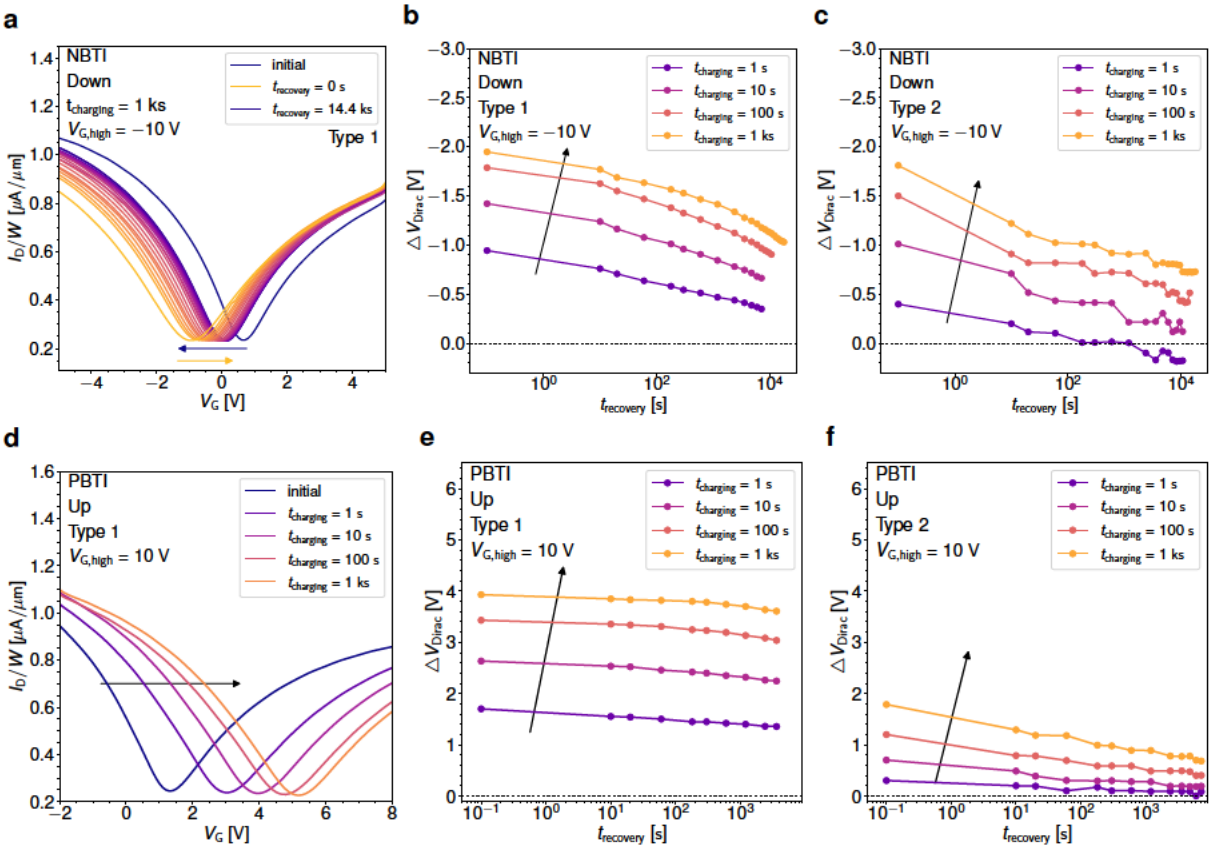

Figure 5.7. **(a)** Shifts of the transfer characteristics as observed for BTI measurements on a Type 1 GFET subjected to −10 V for 1 ks. The device layout of Type 1 GFETs is the same as for Figures 5.3 and 5.5. During the charging of the border traps V_{th} drifts towards increasingly negative biases until it recovers back close to the initial curve after 14.4 ks. **(b)** ΔV_{Dirac} drifts as observed on a Type 1 GFET for increasing long charging or stress times $t_{charging} = t_s$ and an NBTI stress bias of −10 V. **(c)** NBTI recovery traces for a Type 2 GFET when subjected to an NBTI stress of −10 V for increasingly long stress times. As expected, the observed ΔV_{Dirac} drifts are smaller for Type 2 GFETs. **(d)** During PBTI stress at 10 V, the I_D-V_{GS} characteristics of a Type 1 GFET are shown to drift towards more positive gate voltages. **(e)** The PBTI ΔV_{Dirac} drifts on a Type 1 GFET are large and barely recover even for long recovery times of 10 ks. **(f)** On Type 2 GFETs, the drifts during PBTI stress at 10 V are considerably smaller and also recover more than their Type 1 counterparts. In order to avoid an impact of the measurement history, the measurements shown were performed on different devices. All graphics in this figure are reproduced from [TKJ3].

stems from the recovery voltage of 1 V, applied to the gate during the recovery period. These recovery conditions correspond to minor PBTI and, as these PBTI drifts are stronger and less recoverable than NBTI drifts, they dominate for this trace after a recovery time of 1 ks.

In Figure 5.7 (d) the fast I_D-V_{GS} sweeps, measured after a positive bias at 10 V, are shown. In addition, the corresponding recovery traces for Type 1 GFETs are given in Figure 5.7 (e) and for Type 2 GFETs in Figure 5.7 (f). For both device types the degradation, when applying positive biases (PBTI), are higher than NBTI shifts, as the Fermi level in graphene is at the lower edge of the Al_2O_3 defect band, see Figure 5.3 (d). Thus, the number of defects which become more negatively charged during positive bias is larger than the number of defects which emit one of

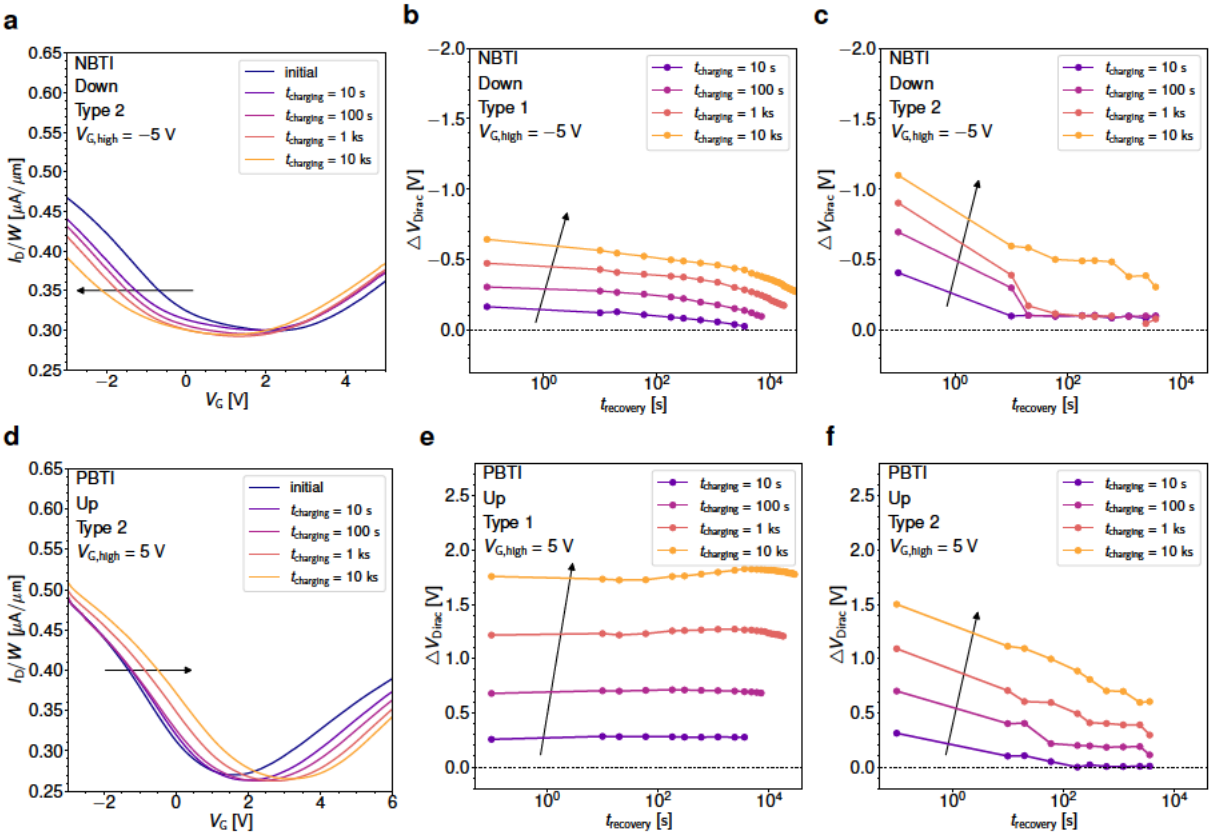

Figure 5.8. **(a)** Shifts of the transfer characteristics as observed for BTI measurements on a Type 2 GFET for a reduced stress bias of −5 V. For increasingly long charging times ($t_{charging} = t_s$) the I_D-V_{GS} characteristics drift towards increasingly more negative gate voltages from 10 s (violet) to 10 ks (yellow). **(b)** NBTI recovery traces show the ΔV_{Dirac} drifts as observed on a Type 1 GFET for a stress bias of −5 V. **(c)** The corresponding NBTI recovery traces at −5 V stress for a Type 2 GFET, showing almost complete and fast recovery already at $t_{recovery}$ = 10 s for most charging times. **(d)** Fast sweep transfer characteristics used to evaluate the PBTI drifts on Type 2 GFETs for a moderate stress bias of 5 V. **(e)** PBTI ΔV_{Dirac} drifts on a Type 1 GFET are large and do not recover also for the moderate stress bias of 5 V. **(f)** On a Type 2 GFET, the PBTI recovery traces show that the PBTI drifts for a stress of 5 V are mostly recoverable. All graphics in this figure are reproduced from [TKJ3].

their electrons during negative bias. Therefore, the picture of charge transfer to oxide defects in Al_2O_3 explains these BTI observations to full satisfaction.

Completing the picture of BTI degradation in the two GFET Types, the degradation for increasing charging times and a constant stress bias of −5 V is shown in Figure 5.8 (a) for a Type 2 GFET. These fast sweep I_D-V_{GS} curves are used to evaluate the BTI drifts on Type 2 devices and complement the fast sweep curves for Type 1 GFETs shown in Figures 5.7 (a) and (d). In Figure 5.8 (b) the ΔV_{th} shifts of Type 1 GFETs after NBTI at −5 V are shown. The recovery of NBTI degradation at −5 V on Type 1 GFETs in Figure 5.8 (b) is smaller than the recovery of NBTI degradation of Type 2 GFETs in Figure 5.8 (c). However, Type 2 GFETs recover much faster than Type 1 GFETs from the reduced voltage level at −5 V. In fact, for Type 2 GFETs the recovery is nearly complete at 10 s. This indicates that the fast-recovering component of the degradation could be related to an increased defect density at the interface of Type 2

graphene to the Al_2O_3 gate oxide. These fast defects have been observed in the hysteresis measurements in Figure 5.5 and are related to the lower quality of Type 2 graphene.

In Figure 5.8 (d) the transfer characteristics directly after PBTI at 5 V on Type 2 GFETs are shown. In Figures 5.8 (e) and (f) the recovery traces of ΔV_{Dirac} are shown for Type 1 and Type 2, respectively. Interestingly, throughout all charging times the PBTI shifts on Type 1 devices do not recover whereas the shifts on Type 2 devices show complete recovery, surprisingly even for a short charging time of 1 s. This observation holds true both for the high stress voltage of 10 V in Figures 5.7 (e) and (f) and for the moderate PBTI stress of 5 V in Figures 5.8 (e) and (f). To explain the permanent component of BTI degradation in Type 1 GFETs, the active creation of defects in Al_2O_3 is hypothesized. In silicon FETs, using SiO_2 as a gate dielectric, the permanent component of BTI has been associated with gate-sided hydrogen release[245]. Here, it is speculated that a similar mechanism of bias facilitated oxide defect creation in the Al_2O_3 is responsible for the permanent PBTI observed on the tested GFETs, which will need to be investigated in future studies.

5.1.3 Tuning the Fermi Level

Based on the comprehensive understanding of the physical mechanism of charge trapping at border traps which is responsible for both the hysteresis as well as for the long-term BTI drifts, a novel stability-based design approach is introduced which can be applied to considerably increase the electrical stability and reliability of 2D material-based FETs. This concept has already been briefly introduced in Section 4.2.2 and is explained here in detail. First, the ideas and concepts behind the stability-based design are explained and then their validity is demonstrated using both theoretical simulations as well as experimental results.

The stability-based design approach is centered on the analysis and the design of the band diagram of the MOS system including the defect bands in the insulator, see for example the schematic of a top gated GFET in Figure 5.9 (a). This GFET is based on a MOS system out of aluminum (metal), Al_2O_3 (oxide) and graphene (semiconductor). By cutting through the MOS stack, as indicated by the arrow in the left of Figure 5.9 (a), the corresponding band diagrams are obtained in Figure 5.9 (b). In this view, every material is characterized by its electron affinity, thus the energetic distance from the conduction band edge to the vacuum level, and its band gap. In the case of metals and semi-metals, the work function, the energetic distance of E_F to the vacuum level, determines the energetic location of charge carriers. In this respect, the Schottky-Mott rule [172] is used to determine the band alignments shown as a zero-order approximation, thereby neglecting interface-specific reactions and charge imbalances which would lead to additional shifts on the order of a few hundred meV [519]. At the core of the proposed stability-based design approach lies the knowledge about the energetic position of the oxide's defect bands and their alignment to E_F.

The energetic position of defect bands in amorphous oxides is an intrinsic material property [230, TKJ13], see also Section 4.2.2. Currently, the energetic locations of oxide defect bands are known for amorphous SiO_2 [419], HfO_2 [TKJ13, 421], and Al_2O_3 [418] insulators, see Table 4.1. Based on the band alignment of the graphene work function to the defect bands

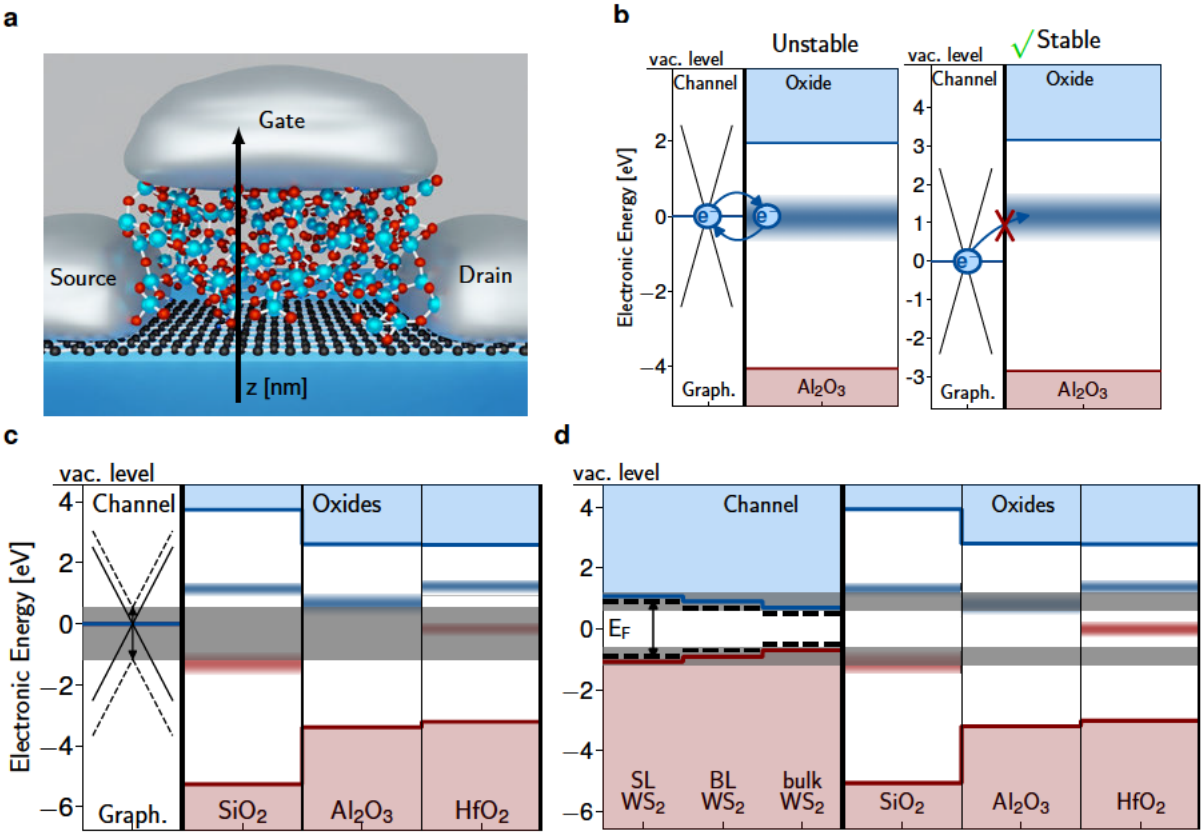

Figure 5.9. **(a)** Schematic image of a top gated GFET with an Al_2O_3 gate oxide including an arrow indicating the direction of the one-dimensional cut where energetic band diagrams are typically drawn. **(b)** In the band diagram to the left, the GFET is electrically unstable with respect to variations in V_{th} as the Fermi level (E_F) is aligned within the defect band. In the band diagram to the right, E_F has been shifted downwards, making the GFET more stable. **(c)** Band diagram indicating the possible range of graphene Fermi levels which is currently achievable by doping as a gray shaded region [427, 428]. The Fermi level can be continuously tuned within this region to avoid the defect bands in the chosen gate oxide. **(d)** Band diagram illustrating the injection of electrons and holes from the band edges of WS_2. In this case the energetic alignment of the semiconductor band edges defines the energy of charges interacting with the defect bands. In a layered semiconductor, the number of layers modifies the band gap and doping determines whether electrons or holes will govern the electrical stability. All graphics in this figure are adapted from [TKJ3].

in Al_2O_3, we can predict the electrical stability of the threshold voltage in these FETs. On the left-hand side band diagram of Figure 5.9 (b), the work function of graphene is shown to be at 3.9 eV which corresponds to n-doped graphene [502]. E_F of this graphene layer lies in the middle of the Al_2O_3 defect band. Due to this alignment within the defect band, charge traps in the oxide will frequently capture and emit charges. As the applied gate voltage modifies the charging probabilities of the defects according to the electric field [224], V_{th} will depend on the biasing history and a pronounced hysteresis will be visible. In addition, V_{th} will drift considerably during prolonged periods of applied gate biases. However, the theoretical considerations of Figure 5.9 (b) to the right suggest that the FET stability can be increased by moving E_F down by p-doping the graphene layer. In this illustration, E_F of graphene amounts to 5.1 eV, as achieved through p-doping [498]. As the Fermi level of graphene is

located below the Al_2O_3 defect band, charge transfer is rare. Therefore, the oxide defects are electrically inactive, resulting in stable V_{th} throughout device operation. In graphene, doping with different adsorbates and substrates yields a quasi-continuous variation of the Fermi level between 3.4 eV and 5.1 eV [427, 428]. This property can be used to tune the Fermi level during device design to maximize the distance of E_F to the defect bands and thus minimize the impact of border traps.

Physical possibilities for tuning the stability with stability-aware device designs are illustrated in Figures 5.9 (c) for graphene and in 5.9 (d) for 2D semiconductors like WS_2. By doping the graphene layer, E_F can be tuned within the entire gray shaded area in Figure 5.9 (c). Thus, the design freedom for stability based device design is large in graphene FETs and the role of SiO_2 defect bands can be reduced with an E_F alignment in the middle of the two defect bands, while the impact of the Al_2O_3 defect band can be minimized when using p-doped graphene layers. For 2D semiconductors like WS_2, the freedom for stability-aware design is smaller. In Figure 5.9 (d) it is shown that either the conduction or the valence band edge can be chosen via doping. However, n-type WS_2 will presumably be electrically unstable for the amorphous oxides investigated here while stable p-type FETs could be designed using Al_2O_3 or HfO_2.

It is worth noting that several studies have reported high densities of fixed charges at the interfaces of 2D materials with amorphous oxides, e.g. for MoS_2/SiO_2 [386, 520, 521], for WS_2/SiO_2 [520, 522] or for graphene/SiO_2 [523]. This evidence suggests that there might be a loss of charge neutrality at the ill-defined interfaces between van der Waals bonded 2D layers and amorphous oxides, causing deviations from the Schottky-Mott rule [519]. These deviations result in offsets to the band alignments which can be determined for example with internal photoemission measurements [524] or scanning probe techniques [506]. While these offsets would need to be taken into account for optimum matching of the Fermi level at a maximum distance to the oxide defect bands, they are neglected for the proof-of-concept study presented here. At the same time an intentional placement of charges at the interface could be used to shift the band edges away from the oxide defect bands using for example SCTD [383, 483]. However, fixed charges at the interfaces would also degrade the mobility in the semiconducting 2D channel [472, 520], which could be avoided by using more complex gate stacks with electric dipoles at the interfaces between different oxides. Such a dipole engineering approach has been successfully applied to improve the reliability of silicon FETs with an HfO_2/SiO_2 gate stack [414, 525].

In order to estimate the electrical stability improvement which is easily accessible by Fermi level tuning in FETs with amorphous oxides, the hysteresis widths in FETs based on 2D semiconductors was simulated. In this regard the key quantifier is ΔV_H in relation to the location of the conduction band edge E_{CB} which is investigated in the following. For simulations, the drift diffusion based TCAD methodology [TKJ12] coupled to a non-radiative multi-phonon (NMP) model [341] was used, see Section 3.3.2. In particular, in Section 6.1 more details on the TCAD modeling methodology as applied to 2D material-based FETs are given and in Section 3.4.2 further details about the NMP model. In Figure 5.10 (a) the hysteresis width is calculated in a model system of monolayer MoS_2 FETs with SiO_2 serving as a back gate oxide, thus a layout comparable to the one shown in Figure 2.3 (a) which is exactly the layout of the FETs

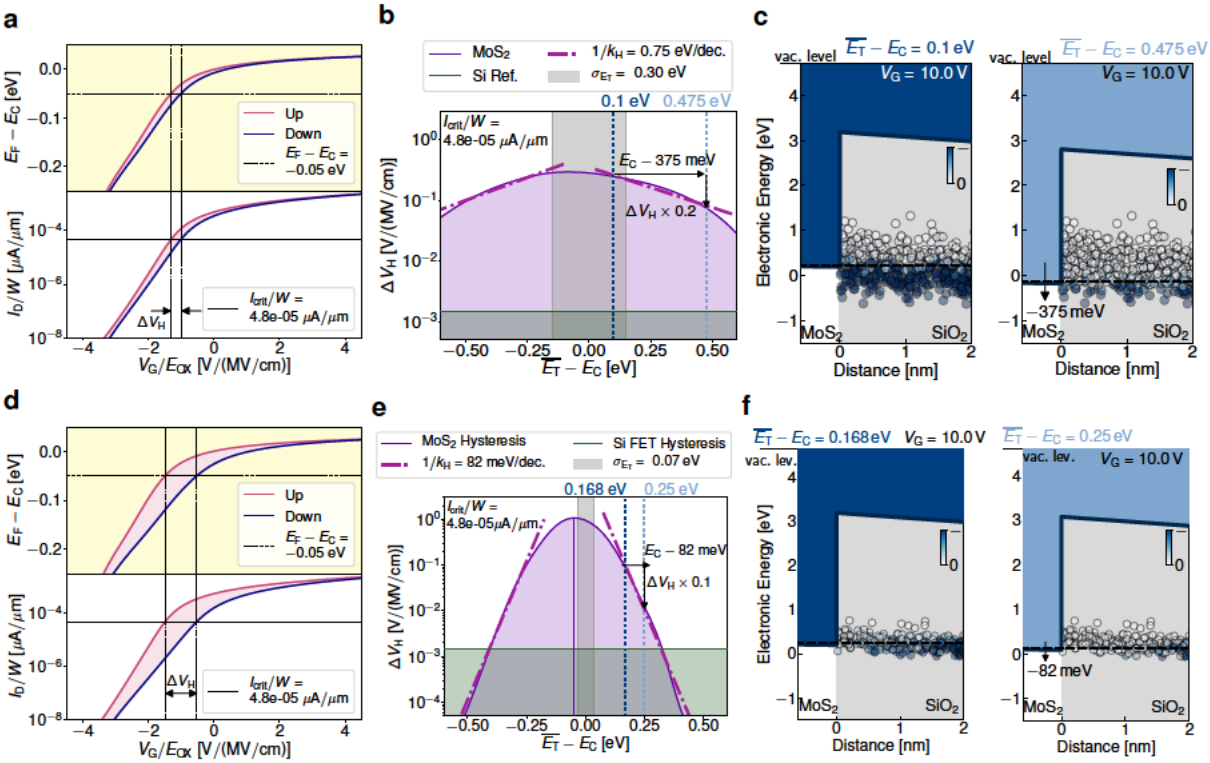

Figure 5.10. **(a)** At the top the calculated distance of the MoS_2 Fermi level to its conduction band edge is shown. The hysteresis width ΔV_H is extracted at the threshold voltage, defined as E_F being located at 50 meV below the conduction band edge E_C. From simulated transfer characteristics of the MoS_2 FETs based on SiO_2, shown below, the constant current criterion of $I_{crit} = 4.8 \times 10^{-5}$ μA/μm was used to evaluate ΔV_H. **(b)** The hysteresis width ΔV_H is shown on a logarithmic scale as a function of the distance of the oxide trap level $\overline{E_T}$ to the MoS_2 conduction band edge E_C. For a defect band with a width of 0.3 eV, the hysteresis will improve by about a factor of 5, if E_{CB} is moved 375 meV down, away from the trap band. **(c)** At two different locations of E_C, namely at $\overline{E_T} - E_C = 0.1$ eV in dark blue and 0.475 eV in light blue, corresponding to the colors of the dotted lines in (b), the band diagrams of the MoS_2/SiO_2 are shown, demonstrating how fewer oxide traps change their charge state if the conduction band edge is shifted down. **(d)** If the defect band width can be reduced to only 0.07 eV, as expected for crystalline insulators, the hysteresis is considerably smaller already for small E_C shifts. For a hysteresis extraction at E_F being located 50 meV below E_C, the constant current criterion amounts again to $I_{crit} = 4.8 \times 10^{-5}$ μA/μm. **(e)** ΔV_H as a function of the distance of $\overline{E_T}$ to E_C in MoS_2. If E_C is moved 82 meV down, the hysteresis width will be reduced by one order of magnitude. **(f)** Band diagrams of the MoS_2/SiO_2 model system at two locations of E_C, at $\overline{E_T} - E_C = 0.168$ eV in dark blue and 0.25 eV in light blue, see the dotted lines in (e). All graphics in this figure are reproduced from [TKJ3].

modeled in Section 6.1. The hysteresis width is evaluated at the V_{th} which is defined here as the voltage where E_F is located −0.05 eV below the conduction band edge, see Figure 5.10 (a). Based on the criterion for $E_F - E_{CB}$ a constant current criterion was defined and the hysteresis width was evaluated as a function of varying distances of the average trap level $\overline{E_T}$ to E_{CB}, see Figure 5.10 (b). For negative values of $\overline{E_T} - E_{CB}$ the oxide defect band is located within the MoS_2 band gap, for positive values it is above the band gap.

For an oxide defect band width of $\sigma_{E_T} = 0.3\,eV$ the hysteresis width can be reduced by half an order of magnitude if the conduction band edge is shifted 350 meV downwards, as illustrated in the band diagrams in Figure 5.10 (c). These shifts of the conduction or valence band edges can be realized for example by transitioning from monolayers to bulk material as illustrated in Figure 5.9 (d). For example in WS_2, conduction and valence band edges shift by approximately 160 meV when using bilayers instead of monolayers or by about 370 meV when using bulk WS_2 [416]. Thus, it would be expected that n-type WS_2 FETs with an HfO_2 gate oxide are more stable when using bulk WS_2 as a channel compared to thinner WS_2 layers. In case an ultimately thin monolayer channel is required, electrically stable FETs could be designed by choosing a different 2D semiconductor to insulator combination. For example, a high electrical stability for BP/ HfO_2 FETs or for $ZrSe_2/Al_2O_3$ FETs is predicted as their band edges are far away from the respective defect bands.

It should be noted that for narrower defect bands, the improvement accessible by tuning the semiconductor's band edges is much larger. For instance, the calculations are repeated in Figure 5.10 (d) to (f) for an insulator defect band with a width of only σ_{E_T} =0.07 eV. In this theoretical scenario, the hysteresis width is reduced by a full order of magnitude if the conduction band edge is shifted by a mere 82 meV, see Figure 5.10 (e). Such a reduction of the defect band width σ_{E_T} is expected for crystalline gate insulators such as hBN or CaF_2 [TKJ5], see Section 4.4. This demonstrates that the reduction of the defect band width by an increased crystallinity of the gate insulator is a strong lever for increasing the electrical stability of FETs. Independently, graphene, with its continuous tunability of E_F over an interval of nearly 2 eV, provides the largest design freedom. Due to the possibility to tune the Fermi level in graphene by a few 100 meV through moderate doping, a graphene/Al_2O_3 model system was chosen to experimentally verify our stability-based design approach. Thus, in the following the impact of electrostatic doping via the back gate voltage in double gated GFETs on the hysteresis width is analyzed experimentally.

For this purpose, double gated GFETs were fabricated using 90 nm SiO_2 as a back gate oxide and the silicon wafer as a global back gate. The layout of these devices is comparable to Figure 2.3 (d) but with the substrate being used as a back gate. Such a configuration allows to control the doping of the monolayer graphene channel electrostatically via the back gate [38, 526]. In this way, by applying a negative voltage at the back gate of e.g. −20 V, the Dirac voltage of the top gate is shifted towards more positive voltages, corresponding to a higher graphene work function, see Figure 5.11 (a). Conversely, $V_{bg} = 20\,V$ renders the top gate V_{Dirac} more negative, see Figure 5.11 (b), thereby resulting in a smaller graphene work function. Consequently, these GFETs are expected to be more electrically stable at high negative V_{bg} than at high positive V_{bg}.

Therefore, the hysteresis in the top gate $I_D\left(V_{tg}\right)$ curves was characterized by first stabilizing the double gated GFETs at a static V_{bg} and then measuring the hysteresis at top gate different sweep rates. In Figure 5.11 (c) the hysteresis at the top gate is shown for slow sweeps and various back gate voltages ranging from 12 V (orange) down to −40 V. When comparing the measured hysteresis widths as a function of the sweep time and the applied back gate voltage in Figure 5.11 (d), two trends are clearly observed. First, the hysteresis is reduced for fast

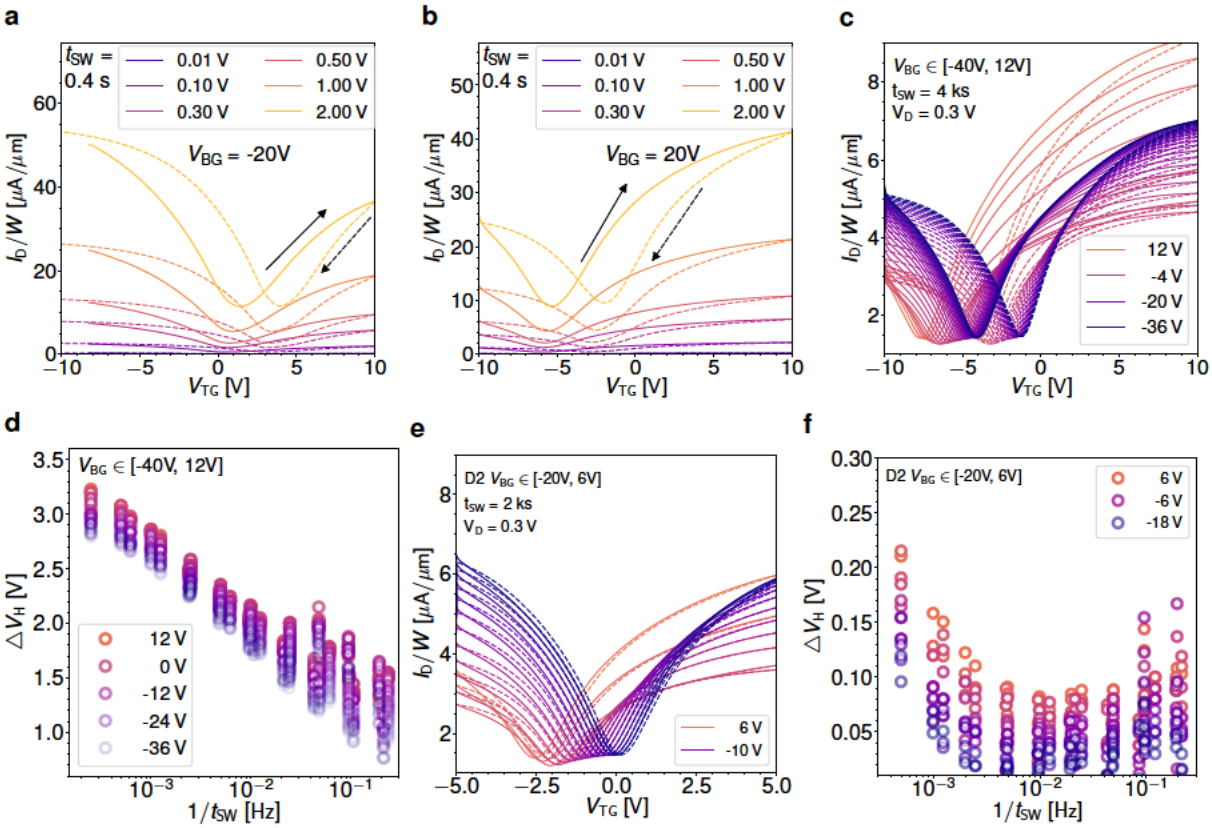

Figure 5.11. The device studied is a double gated GFETs using the silicon wafer as a global back gate with a back gate oxide of 90 nm SiO_2 and a top gate oxide of 40 nm Al_2O_3. It's layout is comparable to Figure 2.3 (d) while also using the substrate as a back gate. **(a)** For these double gated GFETs, I_D-V_G curves recorded at $t_{sw} = 0.4\,s$ are shown at $V_{bg} = -20\,V$, including the backward sweep as dashed lines. **(b)** Transfer characteristics at $V_{bg} = 20\,V$ showing that this back gate bias leads to an electrostatic n-doping of the graphene. **(c)** Slow sweep I_D-V_{GS} curves at $t_{sw} = 4\,ks$ and a top gate sweep range of $V_{tg} \in [-10\,V, 10\,V]$ are compared for different back gate biases with dark blue for $V_{bg} = -40\,V$ and orange for $V_{bg} = 12\,V$, which also correspond to different graphene work functions. **(d)** Respective hysteresis widths ΔV_H are shown as a function of the inverse sweep time for various V_{bg} values. For fast sweeps and the most negative V_{bg}, thus electrostatic p-doping of the GFET, the hysteresis is the smallest. **(e)** Hysteresis in the slow sweep transfer characteristics at $t_{sw} = 2\,ks$ for a smaller top gate sweep range of $V_{tg} \in [-5\,V, 5\,V]$. Here, dark blue represents $V_{bg} = -20\,V$ and orange $V_{bg} = 6\,V$. **(f)** The corresponding hysteresis widths as a function of the inverse sweep time for $V_{tg} \in [-5\,V, 5\,V]$ and various back gate voltages. All graphics in this figure are reproduced from [TKJ3].

sweeps and second, the hysteresis is smallest for the most negative V_{bg}. It is expected that the hysteresis is reduced for high negative back gate voltages, as the work function of the graphene channel is highest for high negative V_{bg}. At high graphene work functions, the Fermi level is located closer towards the lower edge of the defect band in the Al_2O_3 top gate oxide, reducing the probability for charge trapping events. These trends are confirmed when repeating these measurements on a different GFET device D2 using a smaller sweep range of $V_{tg} \in [-5\,V, 5\,V]$ in Figures 5.11 (e) and (f).

Next, a similar measurement protocol of stabilizing V_{bg} at various levels and sweeping V_{tg} at varying rates was repeated 10 times on two different GFETs D1 and D2. In Figure 5.12 (a)

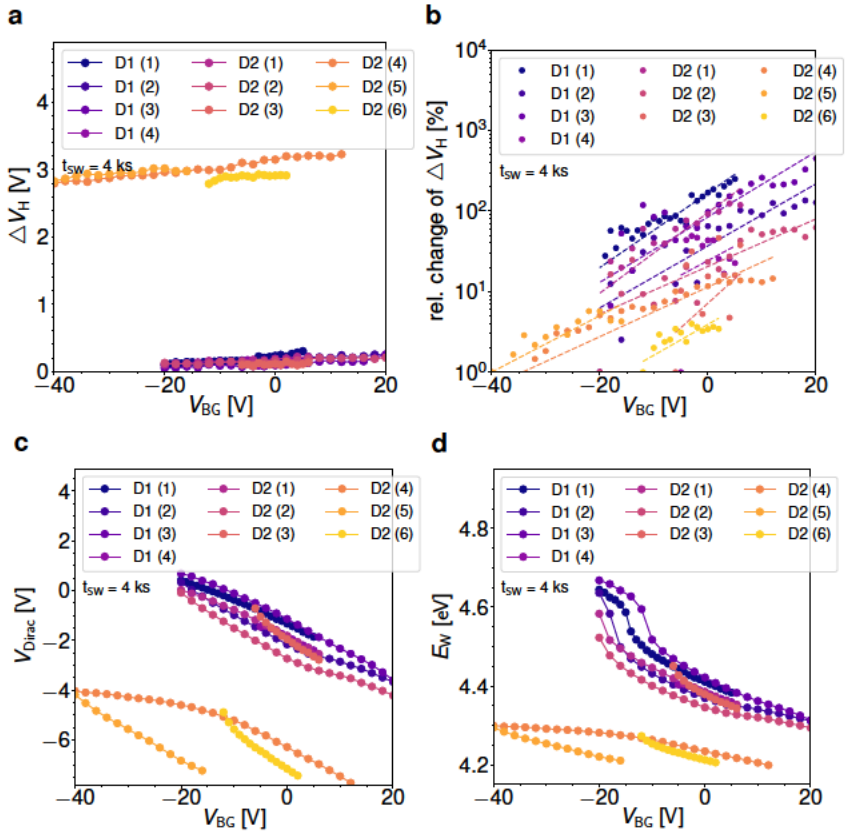

Figure 5.12. **(a)** For many different measurement rounds numbered from (1) to (6) on two double gated GFETs, namely devices D1 and D2, ΔV_H is shown as a function of V_{bg} for the slowest sweep rate of $t_{sw} = 4\,ks$. This shows that the hysteresis width is smallest for high negative V_{bg}, corresponding to p-type doping of the graphene. At the same time, the sweep range of V_{tg} has a strong impact on the overall ΔV_H value as the number of activated border traps is considerably higher for $V_{tg} \in [-10\,V, 10\,V]$ in orange and yellow than for $[-5\,V, 5\,V]$ in blue and purple. **(b)** Thus, the relative change of the hysteresis width as obtained by normalizing ΔV_H to the minimum ΔV_H of every respective trace at $V_{BG,min}$, showing for measurement round 3 on D1, an improvement of up to 450%, thus a factor of 4.5. **(c)** Dependence of V_{Dirac} on V_{bg} for various measurement rounds, demonstrating a certain hysteresis also in the back gate despite slow stepping of V_{bg}. **(d)** Based on the $V_{Dirac}(V_{bg})$ dependence shown in (c) and Equations (5.2) and (5.3) the work function shift achieved through electrostatic doping with the back gate is shown. Measurement round 3 on D1 created the largest E_W shift of 0.34 eV. All graphics in this figure are reproduced from [TKJ3].

the observed ΔV_H is shown as a function of V_{bg} for the slowest sweep rate of $t_{sw} = 4\,ks$. All measurements performed with a larger top gate sweep range spanning $\pm 10\,V$ exhibit a higher absolute hysteresis width at about 3 V, in comparison to the $\Delta V_H = 0.3\,V$ for the small top gate ranges of $\pm 5\,V$, see Figure 5.12 (a). This strong dependence on the top gate sweep range is expected as more oxide traps change their charge state between up and down sweep due to the stronger band bending [TKJ15, 489]. Thus, in order to isolate the impact of the back gate and thus the electrostatic doping on the stability, the hysteresis width is normalized by the smallest hysteresis width measured at the most negative V_{bg}

$$\text{relative change of } \Delta V_H\,[\%] = \frac{\Delta V_H - \Delta V_H(V_{BG,min})}{\Delta V_H(V_{BG,min})}. \tag{5.4}$$

This quantity is shown on a logarithmic scale as a function of V_{bg} in Figure 5.12 (b). Throughout these 10 measurement rounds, there is an exponential dependence of ΔV_H on the applied back gate voltage, as expected from the theoretical calculations presented in Figure 5.10. An improvement by a factor of up to 4.5 is observed for a work function shift of 340 meV. Based on the dependence of V_{Dirac} on V_{bg}, shown in Figure 5.12 (c), the corresponding comparisons of work functions for these measurements was calculated based on Equations (5.2) and (5.3) and presented in Figure 5.12 (d). Overall, an improvement of ΔV_H of about 750 meV/dec is observed when more negative back gate voltages are applied, in good agreement with the theoretical predictions of Figure 5.10 (b). However, in this double gated configuration the full improvement cannot be achieved in every measurement round, as particularly for high V_{bg} a strong modulation of the work function by the back gate is prevented by the charging of oxide traps in the SiO_2. Nevertheless, all hysteresis measurements show that a shift of the graphene work function to higher values, away from the defect band in the Al_2O_3 successfully reduces the amount of electrically active border traps, thereby stabilizing the GFETs.

5.2 Single Defect Analysis in Nanoscaled 2D Transistors

This section is based on the abstract in the conference proceedings and the presentation at

[TKC6] Device Research Conference - Conference Digest DRC 78, 52-53, (2020).

For this presentation, the author has received the Best Student Paper award.

For a better understanding of the atomic nature of the border traps and the physics of the charge trapping processes which cause the ubiquitous hysteresis and BTI in 2D material-based FETs, see Section 5.1, RTN and TDDS measurements on nanoscaled MoS_2 on SiO_2 FETs have been performed [TKC6]. RTN and TDDS are among the very few measurement schemes which can reveal information on the physical configuration of the border traps, see Sections 3.2.2 and 3.2.4. However, in order to enable such an analysis in the first place, only a few electrically active border traps must be located within the active area of the MoS_2 FETs, given by $W \times L$. Here, this condition is referred to as the single defect limit. Under the assumption that the border trap density D_{ot}, defined as the number of border traps per volume [cm^{-3}] and energy range [eV], see Section 4.2.2, is a constant for every device technology, every technology can in principle be scaled down below the single defect limit by sufficiently reducing W and L.

In Figure 5.13 (a) a large-area, bare-channel MoS_2 FET is schematically shown including red, green, and blue spheres in the SiO_2 back gate oxide which represent positively charged, neutral and negatively charged border traps. As several hundreds or up to thousands of border traps are located within the channel area, at any gate biasing and temperature condition several border traps will be active simultaneously. These simultaneous charge trapping events are superimposed to form continuous ΔV_{th} drifts as observed for example in Sections 5.1.1 and 5.1.2. If, however, the device dimensions of the MoS_2/SiO_2 FET are reduced by etching the channel into a small width W and placing the source and drain contacts at a short distance L apart, the number of border traps within the channel is considerably reduced,

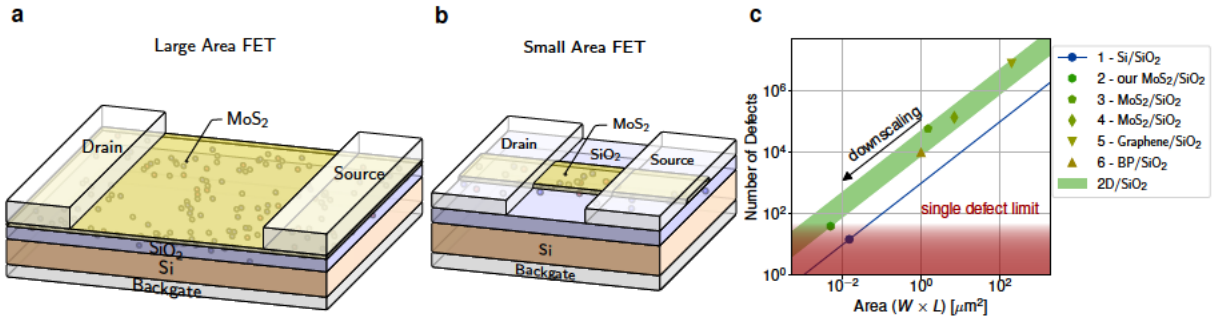

Figure 5.13. **(a)** Schematic layout of a large area FET with an MoS_2 channel and SiO_2 as a back gate oxide with Si as a global back gate. As the active area of the FET is high, the impact of many charge traps is superimposed in continuous ΔV_{th} drifts. **(b)** Layout of the small area MoS_2/SiO_2 FETs investigated in this section. For a constant insulator trap density D_{ot}, the number of electrically active traps in vicinity to the channel is considerably reduced for smaller areas $W \times L$. Therefore, only a number of countable traps are observed as discrete ΔV_{th} steps at a certain V_{GS} and operation temperature. **(c)** As soon as the area of a FET is reduced, the number of defects falls into the red shaded area, the single defect limit, and the impact of single defects can be seen. Every technology has a distinct border trap density D_{ot}, shown as a solid blue line for Si/SiO_2 FETs and a green band for 2D material-based FETs using SiO_2 as a gate oxide. If the dimensions are scaled down, the number of active border traps is reduced along these diagonal lines. Border trap densities shown as symbols are taken from literature, 1-[259], 2-[TKC6], 3-[TKJ15], 4-[TKJ21], 5-[251], 6-[518]. All graphics are adapted from [TKC6].

see Figure 5.13 (b). On such devices, at certain gate biasing and operation temperatures only single defects are activated which cause discrete steps in I_D and ΔV_{th}. Thus, devices with a layout comparable to the schematic shown in Figure 5.13 (b) are used in the following subsections for a RTN and TDDS analysis. In fact, the device shown in Figure 5.13 (b) has device dimensions below the single defect limit which is illustrated in Figure 5.13 (c) for 2D material-based FETs. On a double-logarithmic plot of the number of border traps as a function of the area $W \times L$ every border trap density D_{ot} corresponds to a diagonal line. As industrial silicon technologies exhibit smaller D_{ot}, shown in Figure 5.13 (c) in blue, the single defect limit is reached already for larger areas than for 2D FETs shown in green. However, also for the more defective 2D FETs the single defect limit is reached at around 0.01 μm^2, enabling the RTN and TDDS analysis on MoS_2/SiO_2 FETs of these dimensions in the following.

5.2.1 RTN in MoS_2 Transistors

Here, RTN is measured on bare-channel, nanoscaled MoS_2 FETs using 20 nm of SiO_2 as a back gate oxide. The transistors employ few-layer mechanically exfoliated MoS_2 flakes as a channel which was patterned into widths of 100 nm and 70 nm using plasma etching. The fabrication process of the devices is described in detail in Sections 2.2.1 and 2.2.2, as the investigated FETs were fabricated by the author during a research visit to the Birck Nanotechnology Center at Purdue University in 2019. In Figure 5.14 (a) multiple $I_D - V_{GS}$ characteristics of a FET of a very similar layout, but fabricated earlier [TKJ14] are shown. These transfer characteristics were recorded at $V_{DS} = 0.1$ V and 335 K and show multiple electron trapping and de-trapping events

seen as ΔV_{th} shifts of about 300 mV. As the gate bias increases, the probability for the border trap to capture an electron from the conduction band increases because the energy of the defect level is shifted below E_F. Once the trap is charged it causes a ΔV_{th} shift. If the border traps are located close to the Fermi level at the applied gate bias, stochastic charge trapping and emission processes are observed as steps in the drain current, ΔI_D. This phenomenon is termed RTN, for more details see Section 3.2.2.

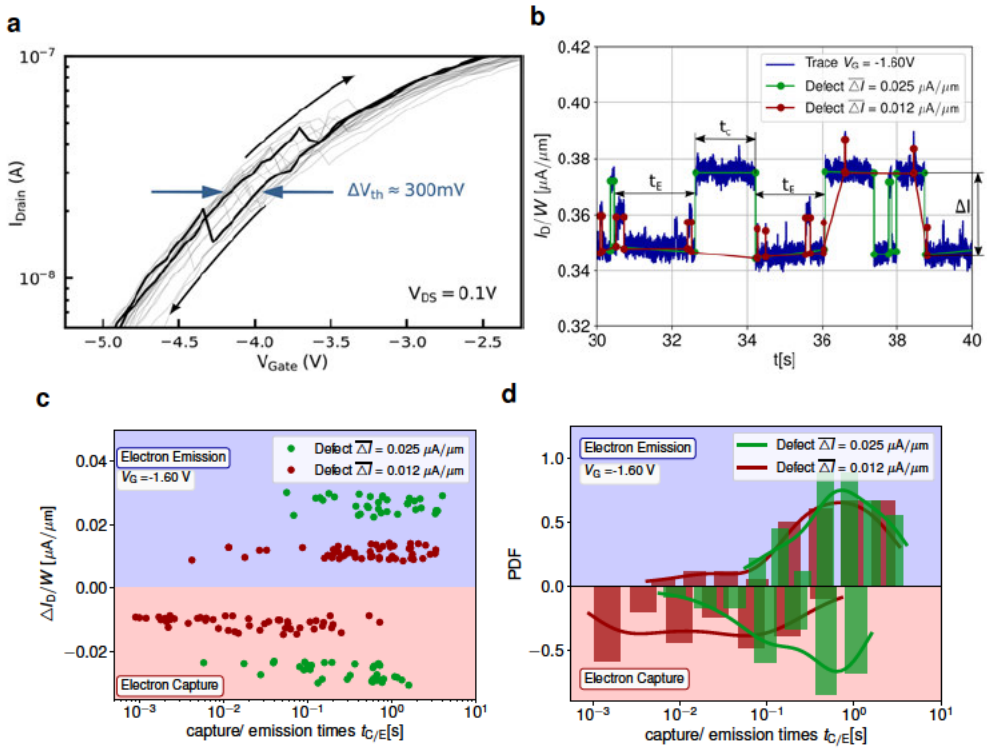

Figure 5.14. **(a)** Impact of a single defect on the drain current of the nanoscale MoS_2 FETs with 20 nm SiO_2 as aback gate oxide. In these I_D-V_{GS} characteristics recorded at 335 K the impact of a single trap is seen in subsequent measurement cycles. This trap changes its charge state during the V_{GS} sweeps, thereby causing a ΔV_{th} shift of about 300 mV. Adapted from [TKJ14]. **(b)** These FETs have a bare channel of $W \times L = 100\,\text{nm} \times 70\,\text{nm}$ with a global Si back gate, see Figure 5.13 (b) and in more detail Figure 2.6. Random Telegraph Noise (RTN) trace as measured at a back gate bias of -1.6 V and a cryogenic temperature of 25 K. A part of the 100 s trace is shown here, allowing for the identification of two atomic defects based on their respective step heights. The defect in green causes step of about 25 nA/µm and the defect in red steps of about 12 nA/µm height. **(c)** Every point corresponds to an electron capture or emission event recorded in the 100 s RTN trace, part of which is shown in (b). Every event is characterized by its capture or emission time (x-axis) and its step height (y-axis) with positive steps being emission and negative steps capture events. **(d)** Probability Density Function (PDF) of the distribution of the capture and emission times of the two defects. The distributions are centered around the capture time constant τ_C and the emission time constant τ_E of the atomic defects. Graphics (b) - (d) are adapted from [TKC6].

A characteristic part of a 100 s RTN trace as measured on the MoS_2/SiO_2 FET at $V_{DS} = 1$ V, $V_{GS} = -1.6$ V and at a cryogenic temperature of 25 K is shown in Figure 5.14 (b). On this device, two independent electron traps were identified which are distinguishable by the magnitude of the drain current steps ΔI_D caused by the charge trapping events. Thus, the respective

step heights are used to differentiate between steps caused by the defect with an average step height of about 25 nA/µm (shown in green) and the defect with an average step height of about 12 nA/µm (shown in red). The capture time t_C is defined as the time between the last emission and the next electron capture event, thus the time spent in the upper charge state, and the emission time t_E is accordingly given by the time between the last capture and next emission event, in effect the time in the lower charge state.

The distribution of the charge capture and emission events is shown in Figure 5.14 (c) where every point corresponds to a single capture and emission event identified in the 100 s RTN trace, part of which is shown in Figure 5.14 (b). Every event is fully characterized by its capture or emission time and the respective step height, serving as the axes of the scatter plot in Figure 5.14 (c), thereby revealing clusters of capture and emission events associated with the observed single defects. For the two atomic defects, the distributions of the capture and emission times are shown in Figure 5.14 (d). Ideally, these distributions should obey a binomial distribution [224]. The centers of the distributions give the capture time constant $\tau_C = \overline{t_{C,i}}$ and the emission time constant $\tau_E = \overline{t_{E,i}}$ of the atomic defects. It is noted that for the defect with higher $\overline{\Delta I_D} \sim 25\,\text{nA/µm}$, the capture and emission time constants are very similar at $V_{GS} = -1.6\,\text{V}$; $\tau_C \sim \tau_E$. In this way, the fingerprint of the atomic defects consisting of $\left\{\overline{\Delta I_D}, \tau_C, \tau_E\right\}$ is fully determined for $V_{GS} = -1.6\,\text{V}$, $V_{DS} = 1\,\text{V}$, and $T = 25\,\text{K}$. In Figure 5.15 this same atomic defect is tracked for varying gate biases.

Figure 5.15 (a) shows part of a 100 s RTN trace recorded on an MoS_2/SiO_2 FET at $V_{GS} = -1.51\,\text{V}$, $V_{DS} = 1\,\text{V}$ and 25 K, again observing the same two defects as detected in Figure 5.14 (b)-(d). All detected steps at $V_{GS} = -1.51\,\text{V}$ are included in the scatter plot in Figure 5.15 (b) and the distribution of the capture and emission times is shown in Figure 5.15 (c). In comparison to Figure 5.14 (d) it can be seen that the capture time constant slightly decreases and the emission time constant slightly increases at higher gate biases.

In Figure 5.15 (d) part of a 100 s RTN trace is shown for a higher gate bias of −1.16 V. At this gate bias the defect with higher $\overline{\Delta I_D} \sim 25\,\text{nA/µm}$ shows a higher emission time constant than capture time constant and is thus mostly in its lower charge state. Indeed, the probability density functions of the capture and emission times in Figure 5.15 (e) confirm that $\tau_E > \tau_C$ at $V_{GS} = -1.16\,\text{V}$ for the defect with the higher step height. In Figure 5.15 (f) the gate bias dependence of the capture and emission time constants is shown for the atomic defect with higher $\overline{\Delta I_D} \sim 25\,\text{nA/µm}$. It can be seen that both τ_E and τ_C depend on the logarithmic scale linearly on the applied gate bias with a small slope. In general, such an exponential dependence is expected as V_{GS} moves the trap level E_T across the Fermi level at the conduction band edge of MoS_2, thereby modifying the barrier height for charge transfer, see Section 3.4.2.

5.2.2 Charge Transfer at Cryogenic Temperatures

In the next step, the RTN measurements as described in detail in Section 5.2.1 for the cryogenic temperature of 25 K are repeated on the same FET for a range of cryogenic temperatures between 10 K and 80 K. Based on these measurements the temperature dependence of electron capture and emission time constants is investigated. In Figure 5.16 (a) the gate bias

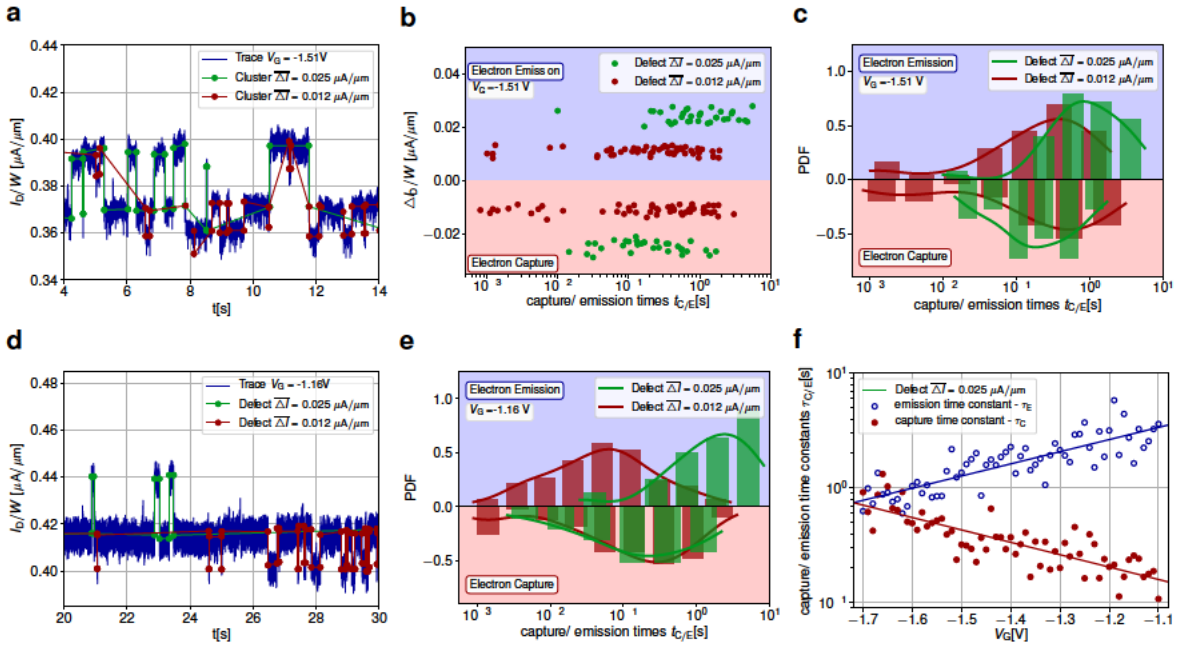

Figure 5.15. **(a)** Part of a 100 s RTN trace at $V_{GS} = -1.51\,V$ and $T = 25\,K$ on the same FET, as the trace analyzed in Figure 5.14 (b)-(d). Again, a defect with a step height of 25 nA/µm in green and another defect with $\overline{\Delta I_D} = 12\,nA/\mu m$ in red are found. **(b)** All steps detected in the 100 s RTN trace shown in (a) are included in the scatter plot showing their step heights and capture and emission time constants. **(c)** PDF showing the distribution of t_C and t_E for the trace at $V_{GS} = -1.51\,V$ and $T = 25\,K$ used to determine τ_C and τ_E. **(d)** Part of a 100 s RTN trace at $V_{GS} = -1.16\,V$ and $T = 25\,K$, showing a much longer emission time in comparison to the capture time for a defect in green with 25 nA/µm. **(e)** This shift of τ_C and τ_E towards more different values can be clearly seen in the PDF of the trace at $V_{GS} = -1.16\,V$. **(f)** Time constants as a function of the applied gate voltage for the defect at $\overline{\Delta I_D} = 25\,nA/\mu m$ at 25 K, with $\tau_E \sim \tau_C$ for smaller gate voltages and $\tau_E > \tau_C$ for higher gate voltages. All graphics in this figure are adapted from [TKC6].

dependence of the time constants is shown at a temperature of 50 K for the defect with a step height of 25 nA/µm. Again, an exponential dependence of the capture and emission time constants on V_{GS} with a comparatively small slope is observed. When comparing the temperature dependencies of the time constants at 25 K, 50 K, and 75 K in Figure 5.16 (b), it can be seen that both capture and emission time constants become smaller for higher temperatures. Thus, for increasing temperatures charge trapping becomes faster, especially charge capture. This trend is in principle to be expected; however, charge trapping becomes faster only very slowly. In fact, for a temperature increase of 50 K for temperatures above room temperature or higher the time constants typically increase over more than 3 orders of magnitude, instead of the less than 1.5 orders of magnitude observed here. This strongly reduced temperature dependence of the capture and emission time constants is expected based on non-radiative multi-phonon transition theory where charge transfer does not freeze out at cryogenic temperatures below 100 K but which instead predicts that charge trapping becomes temperature independent for low temperatures below 50 K [341], see also Section 3.4.2.

At temperatures above room temperature the charge transfer rates for capture and emission times are proportional to a classical Boltzmann factor. At high temperatures the following

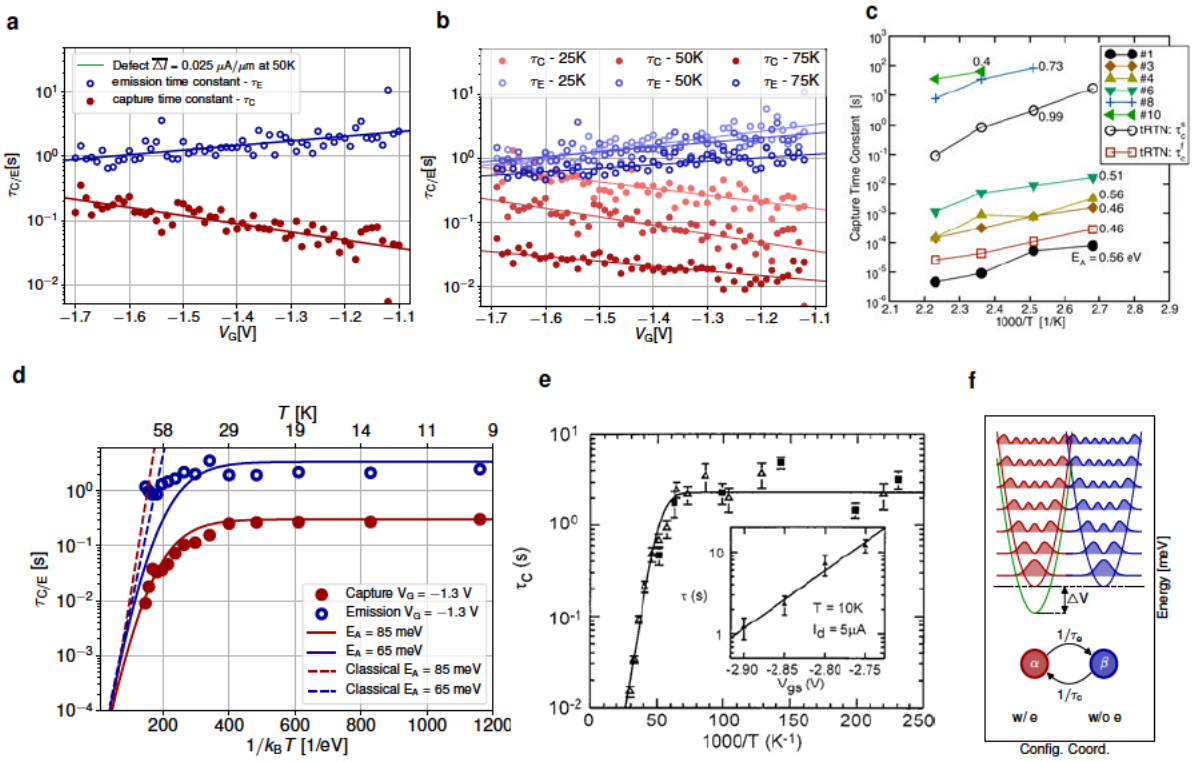

Figure 5.16. **(a)** Time constants as a function of the applied gate voltage for the defect with $\overline{\Delta I_D} = 25\,\mathrm{nA/\mu m}$, as investigated in Figure 5.15, but now at $T = 50\,\mathrm{K}$, revealing that despite the considerable temperature increase the time constants are comparable. **(b)** Bias dependence of the time constants for the defect at 25 nA/µm for various temperatures, showing a small reduction of the time constants for temperatures of 75 K. **(c)** Arrhenius plot of the time constants observed on standard Si/SiON FETs for elevated temperatures between 100 °C and 175 °C. Here, the exponential dependence of the capture time constant according to a Boltzmann factor can be clearly seen from the linear slope of the defects, as reproduced from [262]. **(d)** Arrhenius plot of the time constants for the measurement results at cryogenic temperatures on a nanoscaled MoS_2/SiO_2 FET. The time constants are shown for the atomic defect with $\overline{\Delta I_D} = 25\,\mathrm{nA/\mu m}$ at $V_{GS} = -1.3\,\mathrm{V}$ for temperatures between 10 K and 80 K. In this cryogenic regime the temperature dependence is given by the lineshape function of a non-radiative multi-phonon process, see Equation (3.40b) in Section 3.4.2, which is fitted here to match the measurement results. **(e)** Arrhenius plot of the temperature dependence of the mean capture time as extracted from RTN measurements on Si MOSFETS for $T \in [4.2\,\mathrm{K}, 30\,\mathrm{K}]$ including a fit (solid line), reproduced from [229]. **(f)** Configuration coordinate diagram of the vibronic transition of the atomic defect configuration from a charged (α, red) to a neutral (β, blue) configuration during the charge transfer, see also Figure 3.8 (a). Graphics (a), (b), (d) and (f) are adapted from [TKC6].

expression for the electron capture rate $k_C = 1/\tau_C$ holds if charge exchange with the valence band is neglected

$$k_C = n\theta_n v_{\mathrm{th},n}\sigma_{0,n}\,\exp\left(-\frac{\varepsilon_C^{CB}}{k_B T}\right) \tag{5.5}$$

with the electron density n, the thermal velocity of electrons $v_{\mathrm{th},n}$, the WKB tunneling factor θ_n, the capture cross section $\sigma_{0,n}$, and the energy barrier ε_C^{CB}, compare also Equation (3.44d). Therefore, capture and emission time constants are typically plotted in an Arrhenius plot

as a function of the inverse temperature, where the slope of the linear fit gives the energy barrier ε_C^{CB}, see for example the Arrhenius plot of capture time constants in Figure 5.16 (c). These emission times were measured on Si/SiON FETs using TDDS and RTN measurements at temperatures between 100 °C and 175 °C [262].

However, for the MoS_2/SiO_2 FETs studied here at cryogenic temperatures, capture and emission time constants become temperature independent below 50 K, as can be clearly seen in the Arrhenius plot in Figure 5.16 (d). In this figure, the temperature dependence of the defect with a step height of 25 nA/µm is investigated for a gate bias of −1.3 V with the measured capture times shown as full red and the emission times as empty blue circles. According to NMP theory, the electron capture rates are given by the product of the electron tunneling rate from the conduction band to the defect site and the phonon-mediated transition and reconfiguration of the atoms at the defect site from a neutral to a charged configuration upon electron capture. In the full quantum mechanical description the NMP capture rate in index notation ($k_C = k_{ij}$, as transition between states i and j) is given by

$$k_{ij} = A_{ij}\, f_{ij}^{LSF} = A_{ij} \sum_{\alpha} \frac{\exp\left(-E_{i,\alpha}/\left(k_B T\right)\right)}{\sum_{\gamma} \exp\left(-E_{i,\gamma}/\left(k_B T\right)\right)} \left(\sum_{\beta} |\langle \eta_{i,\alpha} | \eta_{j,\beta} \rangle|^2 \delta\left(E_{i,\alpha} - E_{j,\beta} - \triangle V\right) \right) \tag{5.6}$$

with the electronic matrix element A_{ij} describing the electron tunneling rate and the line shape function f_{ij}^{LSF} containing all phonon interactions between the initial defect configuration α and the defect configuration after charge trapping β. This expression is adapted from Equation (3.40b) in Section 3.4.2. In Figure 5.16 (d) fits of the lineshape function to the experimental data are included as solid lines, showing good agreement of experiment and theory. In this way, an effective energy barrier of around 85 meV for electron capture events and 65 meV for electron emission events was obtained. In addition, the classical charge transfer rates are included as dashed lines in Figure 5.16 (d) revealing a much stronger temperature dependence of the time constants in the classical case. This also demonstrates that the full quantum mechanical case is indeed compatible with classical theory as a limiting case for low temperatures. This leveling-off of the capture and emission time constants below a certain cryogenic temperature was first observed by J. H. Scofield *et al.* in 2000 in small silicon MOSFETs [229]. They observed the capture time constants to become temperature independent below 20 K, see their measurement results and fit function in Figure 5.16(e). However, to the best of the author's knowledge within this work, for the first time, similar behavior on 2D material-based FETs was observed [TKC6].

As predicted by NMP theory, the charge transfer rates to border traps become temperature independent at low temperatures below 50 K. In this temperature regime, the atomic reconfiguration at the defect site is dominated by nuclear tunneling, thus the tunneling of the atomic nuclei through the barriers in the potential energy surface, as illustrated in Figure 5.16 (f). If the border trap has no electron trapped it is in state β, shown in a first approximation as a harmonic oscillator potential including the wave functions of the eigenstates in blue. In order for an electron to be able to be trapped at the border trap, the atomic configuration of the border trap needs to rearrange itself into configuration α. This barrier is overcome via the

energy provided by phonons of the lattice but as the temperature is reduced, the configuration starts to tunnel through the barrier, which can be seen also as the overlap of wave functions in blue and red at energies below the classical energy crossing point. In addition, the parabola corresponding to the negatively charged state α of the border trap can be shifted depending on the applied electric gate field.

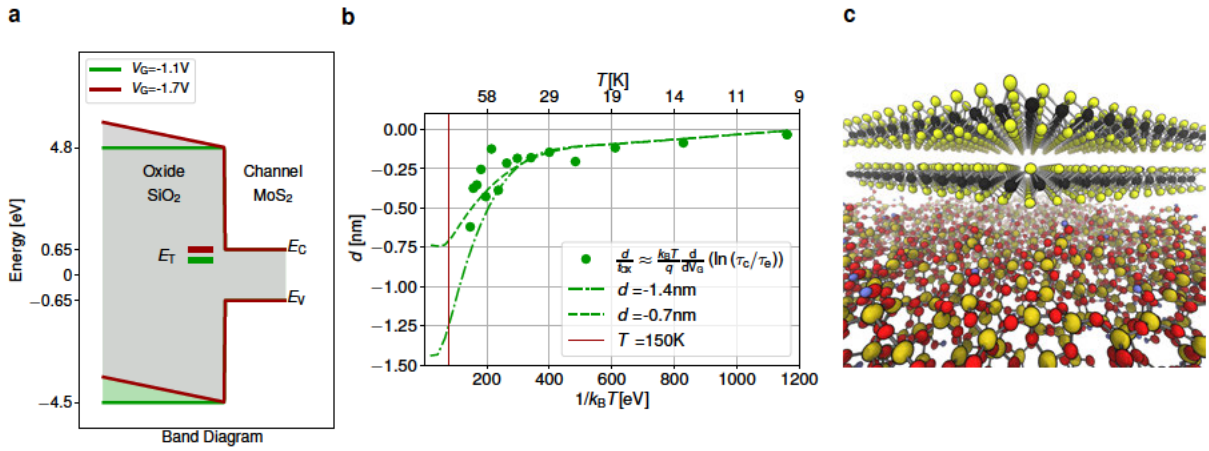

Figure 5.17. **(a)** The trap level E_T of the investigated defect is shifted by applying a gate voltage. Depending on the distance of the defect from the interface with MoS_2, the gate bias dependence will be stronger for defects further in the SiO_2 and weaker for defects directly at the interface. **(b)** Assuming a constant electric field in the oxide, in a classical approximation the ratio of the defect depth d to the oxide thickness t_{ox} can be determined via the relative difference of the bias dependence of τ_E and τ_C. The analyzed defect is roughly less than 1 nm away from the interface. **(c)** Thus, the observed defect is most likely an interface defect located at the highly defective MoS_2 to SiO_2 interface, shown in this schematic. Here, bright yellow represents sulfur atoms, black spheres molybdenum, red, oxygen, dark yellow, silicon and light blue, hydrogen. All graphics in this figure are adapted from [TKC6].

In fact, the defect location in the device determines the gate voltage dependence of the capture and emission times. A defect deep in the oxide has a stronger voltage dependence as the trap level shifts more with an applied gate bias, see Figure 5.17 (a). Under the assumption that the electric field is constant in the oxide, the following relation between the applied gate bias and the energy shift of the border trap (E_T) holds

$$\frac{\mathrm{d}E_T}{\mathrm{d}V_{GS}} = -\frac{qd}{t_{ox}}\left(1 - \frac{\mathrm{d}\psi_S}{\mathrm{d}V_{GS}}\right) \approx -\frac{qd}{t_{ox}}, \tag{5.7}$$

which relates the border trap shift to the ratio of the defect depth d and the thickness t_{ox}.

In addition, based on the classical expression for the charge transfer rates, Equation (5.5), the gate bias dependence of the difference of the capture and emission rates is directly proportional to the energy shift of the border traps

$$\frac{\mathrm{d}}{\mathrm{d}V_{GS}} (\ln(k_C/k_E)) = \frac{1}{k_B T} \frac{\mathrm{d}E_T}{\mathrm{d}V_{GS}}. \tag{5.8}$$

Thus, by inserting Equation (5.8) into Equation (5.7), a classical approximation for the defect depth d is obtained

$$\frac{d}{t_{ox}} \approx \frac{k_B T}{q} \frac{\mathrm{d}}{\mathrm{d}V_{GS}} \left(\ln\left(\tau_C/\tau_E\right)\right). \tag{5.9}$$

This expression is applied to the capture and emission time constants of the defect with a step height of 25 nA/µm and their bias and temperature dependence as shown in Figure 5.16 (b). In this way for every temperature a ratio of d/t_{ox} was calculated and is shown in Figure 5.17 (b) as solid green circles. The dash-dotted lines indicate fits to this data. As Equation (5.9) was derived based on the classical expressions for the charge transfer rates, their applicability to this data set is limited. However, a defect depth d of about 1 nm distance to the oxide interface can be extracted. This location of the border trap is also in good agreement with the small activation energies of the defect of 65 meV and 85 meV, respectively [527]. Thus, the observed border trap is located very close to the MoS_2/SiO_2 interface, which is a highly defective interface. The atomic structure of the MoS_2/SiO_2 interface, where the defect is most likely located, is shown in Figure 5.17 (c).

5.2.3 TDDS in MoS_2 Transistors

In addition to the RTN analysis, time-dependent defect spectroscopy (TDDS) measurements were performed on the nanoscaled MoS_2 FETs with 20 nm SiO_2 as a gate oxide. In comparison with RTN, TDDS measurements have the advantage that (dis-)charging events can be triggered deliberately with a high positive or negative charging voltage at the gate, respectively, thereby considerably extending the gate bias regime accessible for single-defect studies [260]. In Figure 5.18 (a) a TDDS measurement at a cryogenic temperature of 20 K is shown, where a positive stress bias of $V_{GS,stress} = 16\,V$ is applied for 100 s, causing a trap to capture an electron. Immediately after the stress period the gate bias is switched to the recovery bias of $V_{GS,recovery} = 8\,V$ and the current trace is measured. Here, one electron emission event at $t_e = 2.5\,s$ is observed. Subsequently, this measurement cycle is repeated 25 times on the same 70 nm × 70 nm MoS_2/SiO_2 FET. These traces are superimposed in Figure 5.18 (b).

All of the emission events which are observed in the 25 TDDS traces for 100 s stress are characterized by their respective step height and emission time. Based on all these events a spectral map was created in Figure 5.18 (b), showing all detected steps in blue. A subset of these steps was identified to belong to the defect cluster with an average step height of 3.7 nA/µm and these traps are shown in red. Again, the same TDDS measurement sequence consisting of 25 stress and recovery cycles was repeated at increasing operating temperatures. In Figure 5.18 all detected steps at 100 K are shown. At this elevated temperatures, an additional RTN signal is superimposed with the TDDS signal, causing an artifact of the additional defect cluster at higher emission times, where instead the same defect captured and re-emitted the electron. Thus, these steps were not included in the cluster associated with a single atomic defect. This defect's temperature dependence is analyzed in an Arrhenius plot in Figure 5.18 combining measurement data for 20 K, 40 K, 60 K, 80 K, and 100 K. These results also show a temperature independent emission time constant below approximately 40 K and reveal a good fit for the

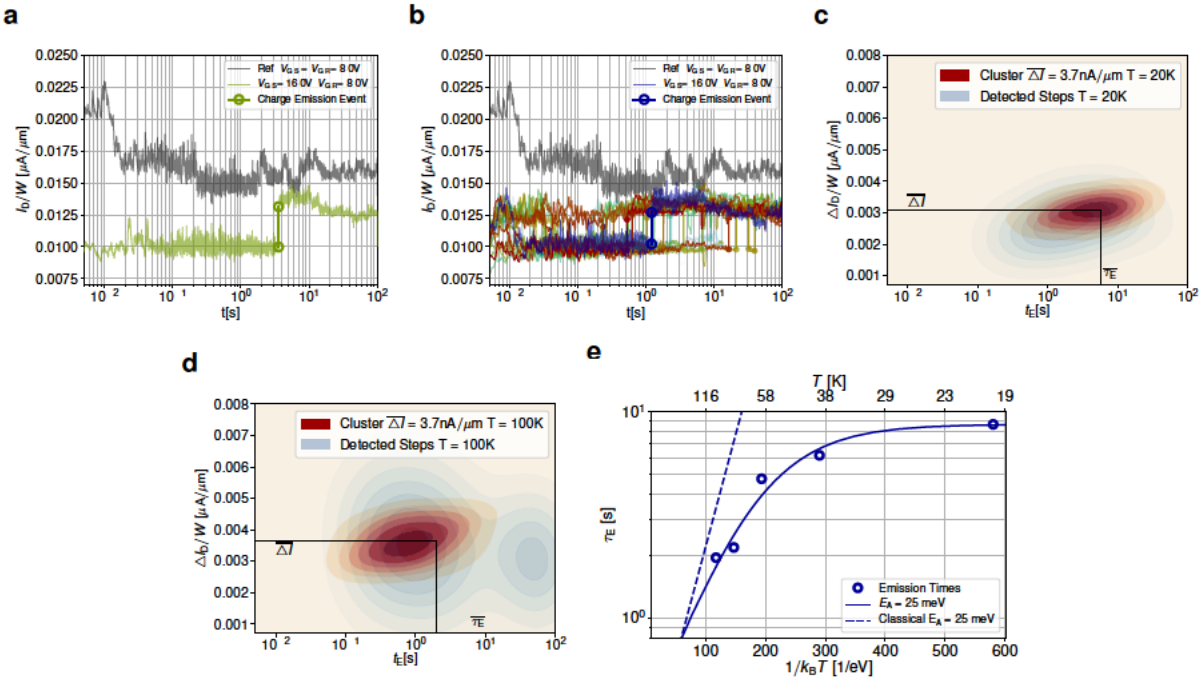

Figure 5.18. **(a)** A positive biased stress pulse of $V_{GS,stress} = 16\,V$ triggers the emission of electrons during the recovery period at $V_{GS,recovery} = 8\,V$ in a TDDS measurement. Here, a single TDDS trace on an MoS_2/SiO_2 FET with an active area of $W \times L = 70\,nm \times 70\,nm$ is shown, including a charge emission at $t_E = 2.5\,s$. The measurement was performed at a cryogenic temperature of 20 K. **(b)** This TDDS measurement in (a) at 20 K uses a stress period of $t_s = 100\,s$ at $V_{GS,stress} = 16\,V$ and monitors recovery at $V_{GS,recovery} = 8\,V$. Exactly this TDDS measurement cycle is repeated 25 times to collect statistics of multiple charge emission events at different t_E. **(c)** All charge emission steps detected during the 25 TDDS traces with $t_s = 100\,s$ shown in (b) are converted to a spectral map of the average step height and emission time. The blue map reflects all detected steps and the red map the cluster of steps at $\overline{\Delta I_D} = 3.7\,nA/\mu m$. **(d)** Detected steps for the TDDS measurement at 100 K. In all detected steps in blue a second cluster appears which is caused by a superposition of an RTN signal on the TDDS trace. This RTN signal is filtered out and only the steps shown in the red map are included in the subsequent evaluation of τ_E. **(e)** Arrhenius plot of the emission time constant determined using TDDS measurements at cryogenic temperatures. Again, only the lineshape function according to NMP theory, see Equation (3.40b), can accurately describe the temperature dependence of the NMP transition in the cryogenic regime. All graphics in this figure are adapted from [TKC6].

lineshape function with an activation energy of 25 meV. Thus, the defect observed with TDDS is most likely located in close vicinity to the MoS_2/SiO_2 interface.

Summing up, both TDDS and RTN measurements demonstrate that charge trapping rates become temperature independent below 50 K and that the charge transfer process at cryogenic temperatures is dominated by nuclear tunneling. As a consequence, charge trapping remains significant in MoS_2 FETs even at cryogenic temperatures and has to be taken into account for device applications at these low temperatures such as FETs for space applications, high-performance computing, and quantum computing [528].

6 Modeling the Operation and Stability of 2D Transistors

A thorough understanding of the physics governing the operation, electrical stability, and degradation in 2D material-based FETs requires a combination of a comprehensive experimental evaluation together with physical models of the device behavior. In the previous chapter, several studies have been discussed which highlight the importance of border traps for 2D FET performance and stable device operation, thereby emphasizing the central role of the semiconductor to insulator interface. Further insights into FET behavior as well as predictions regarding the theoretically achievable FET performance, in particular regarding the suitability of hexagonal boron nitride as a gate insulator for scaled FETs, will be presented in this chapter.

In the first section, the modeling of MoS_2 based transistors will be described. In general, available modeling approaches which are capable of capturing charge transport through FETs are summarized in Section 3.3, ranging in their complexity from the fully quantum mechanical but computationally expensive NEGF models, over classical drift diffusion (DD) models, down to analytic compact models which are usually highly application specific. In this work, MoS_2 FETs are described using technology computer aided design (TCAD) simulations based on classical DD models, as implemented in the simulator Minimos-NT [317]. This classical description has the main disadvantage that it neglects quantum-mechanical effects such as source-drain tunneling in ultimately scaled FETs and fails to describe quasi-ballistic transport and quantization effects in 2D systems. In addition, the density of states in 2D systems which considerably differs from the density of states in 3D systems is not described with full accuracy. Nevertheless, classical simulators are often preferred since they are numerically robust and computationally extremely efficient. Furthermore, they allow one to define complex device structures and geometries which is an invaluable asset for a realistic description of measurement results on prototype devices with complex contact geometries. Most importantly, classical simulators allow for the accurate modeling of charge transfer to border traps by coupling the DD description of the device electrostatics to non-radiative multi-phonon models. The following discussions in this subsection are based mostly on the author's work in [TKJ12, TKJ18].

In the second part of this chapter, the scaling potential and performance limitations of hexagonal boron nitride (hBN) are assessed with a focus on applications in scaled CMOS devices. At present, hBN is the most common layered insulator and is widely considered

to be one of the most promising gate insulators for 2D material-based transistors. In this subsection we review the material parameters of hBN and evaluate its performance limits. These performance limits will be established for the most optimistic scenario, namely for ideal, defect-free hBN. In reality, traps in the hBN will increase the tunneling currents via trap assisted tunneling (TAT), thus the simulation results present a lower limit for the leakage currents. Tunneling currents through thin hBN layers are calculated with an adaptation of the Tsu-Esaki compact model for tunneling currents [334] and a full quantum mechanical description using *ab-initio* DFT calculations in the CP2K framework [288] coupled to the NEGF solver OMEN [529]. All results discussed in this section have been reported by the author in [TKJ2].

6.1 Modeling Molybdenum Disulfide Transistors

Parts of this section (marked by a vertical sidebar) have been published in

[TKJ12] IEEE Journal of the Electron Devices Society 6, 972–978, (2018).

In this section device performance and electrical stability of FETs based on 2D materials are simulated using a drift diffusion based TCAD model [317], for more details see Section 3.3.2. This modeling framework includes a non-radiative multi-phonon model, see Section 3.4.2, to adequately describe the impact of charge trapping events at border traps. Here, the focus is specifically on modeling transistors based on a MoS_2 monolayer as the channel material. A key point for the adaptation of classical DD simulators to novel 2D materials like MoS_2 is to accurately determine their transport and material parameters. While the material parameters of silicon, gallium arsenide, or other conventional semiconductors are well known and have been evaluated using both theoretical calculations and experiments to a high degree of accuracy, the available knowledge about MoS_2 monolayers is at present still incomplete.

Of particular importance for the correct description of charge trapping events is the semiconductor's band gap E_G and its electron affinity χ. These two parameters determine the location of the Fermi level during device operation and, as such, the alignment of the Fermi level to the defect bands in the gate insulator. In turn, this alignment governs the number of electrically active border traps and thereby the electrical stability of the FET, see Section 5.1.3. However, in the past years, there has been some confusion about the precise value of the band gap in monolayer MoS_2. Depending on the utilized measurement or theoretical method the obtained results substantially differ due to the consideration of different physical properties.

For example, the high free electron densities in the orbitals perpendicular to the atomic layer lead to the existence of plasmons and strongly bound excitons [539]. Plasmons are collective oscillations of the free electrons while excitons are quasi-particles of an electrostatically bound electron-hole pair. Therefore, photoabsorption (PA) or photoluminescence (PL) measurements reveal only information on the optical band gap (E_{opt}). For materials with a large excitonic binding energy (E_{exc}) this optical band gap can be substantially smaller than the electronic band gap (E_G), defined as the energy difference between the conduction band minimum and the valence band maximum, $E_G = E_{opt} + E_{exc}$. Photons which are absorbed by

Substrate	Method	Band Gap	E_{opt}	E_{exc}	Reference
-	PS	2.5 eV	1.9 eV	0.6 eV	[530]
SiO_2	STS, PL, PA	2.1 ± 0.1 eV	1.85 ± 0.05 eV	0.2 ± 0.1 eV	[105, 531, 532]
HOPG	STS, PL	2.15 ± 0.1 eV	1.93 eV	0.2 ± 0.1 eV	[533, 534]
-	GGA+GW_0	2.65 eV	-	-	[535]
-	LDA+G_1W_0	2.67 eV	2.04 eV	0.63 eV	[536]
-	LDA+G_0W_0	2.48 eV	2.01 eV	0.47 eV	[537]
Graphene	GGA+G_0W_0	2.43 eV	-	-	[538]

Table 6.1. Comparison of literature values for the band gap of monolayer MoS_2. In addition to the electronic band gap, also the optical band gap (E_{opt}) and the excitonic binding energy (E_{exc}) are given. In the upper part, measurement results are listed and the lower part contains DFT results. The measurement results are mostly smaller than the corresponding DFT results which account for self-energy corrections via the GW approximation. Adapted from [TKJ18].

monolayer MoS_2 create an exciton, but not yet a free electron-hole pair which contributes to charge transport and photocurrent [532]. Nevertheless, there are other measurement methods, such as scanning tunneling spectroscopy (STS) or photocurrent spectroscopy (PS) which directly probe the electronic band gap [530, 533, 534].

At the same time, all experimental methods suffer from a considerable variability in the sample quality of the MoS_2 monolayers depending on the fabrication method used, see Section 2.1. This issue can be avoided when using *ab-initio* DFT calculations to determine the band gap. However, it is generally known that the standard approximations used within DFT (e.g. local density approximation (LDA) or generalized gradient approximation (GGA)) considerably underestimate the band gap for most materials including 2D semiconductors [286]. In order to obtain a better estimate for the band gap of 2D materials, the self energy correction is determined via the GW approximation, where the self energy is given as the product of the Coulomb interaction W of all electrons with the single particle Green's function G [540]. However, the quasi-particle energies calculated within the GW approximation strongly depend on the screened interaction between electrons and thus on the dielectric environment surrounding the 2D layer. Consequently, the band gap of 2D materials depends on the choice of the substrate. In general, for 2D materials that consist of single atomic monolayers, the band gap inherently depends on the surroundings and is no longer a constant material parameter as in bulk semiconductors [519].

In Table 6.1 published values for the band gap of monolayer MoS_2 are compared. Besides the values for the electronic band gaps, also the optical band gaps and the excitonic binding energies are given, where available. The measured electronic band gap, as determined via STS measurements, results in a smaller value for the band gap in comparison to theoretical DFT calculations in combination with the GW approximation for the self-energy correction. In Figure 6.1 the electronic band gap values for monolayer MoS_2 are compared for different substrates. The higher the charge density, and thus the dielectric screening in the direct vicinity to the MoS_2 layer is, the stronger the observed reduction of the MoS_2 band gap. The band gap is therefore highest for suspended MoS_2, see Figure 6.1 (a). When MoS_2 is supported

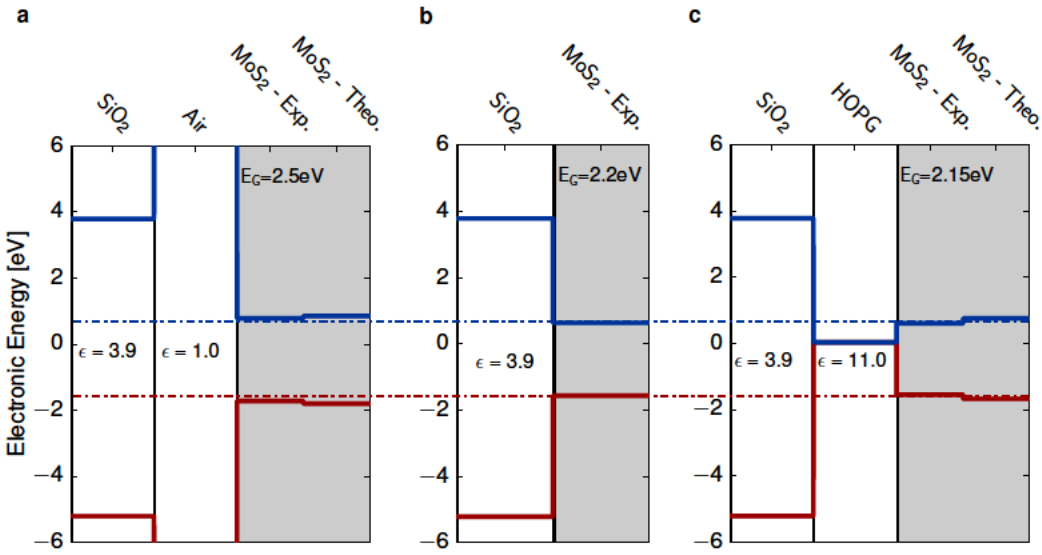

Figure 6.1. **(a)** Schematic band diagram of suspended monolayer MoS_2, where a sufficiently large air gap isolates the MoS_2 layer from the SiO_2 substrate. The band alignment shown is based on [530, 535, 536, 537]. **(b)** Band diagram of MoS_2 on an SiO_2 substrate showing the band alignment according to [105, 531]. The dash-dotted lines are guides to the eye indicating the band gap on SiO_2. **(c)** On a highly oriented pyrolytic graphite (HOPG) substrate with strong dielectric screening and a high permittivity, the band gap of monolayer MoS_2 is smaller than on SiO_2 or for suspended layers [533, 534, 538]. All graphics in this figure are adapted from [TKJ18].

by SiO_2, its bandgap decreases, see Figure 6.1 (b), and it decreases even more for MoS_2 on highly oriented pyrolytic graphite (HOPG), see Figure 6.1 (c).

In the following, the focus will be on MoS_2 on SiO_2, as the simulated FETs use 90 nm SiO_2 as a back gate oxide. For MoS_2 on SiO_2 an electron affinity of approximately -3.85 eV is obtained [456, 541]. Further material parameters required for drift diffusion simulations, are the effective electron and hole masses, which are determined by the curvature of the parabolas used to approximate the band structure close to the respective minimum and maximum. In monolayer MoS_2 these extrema are located at the K-point, rendering it a direct semiconductor. Effective masses in MoS_2 are about 0.55 m_0 for both electrons and holes [540]. In addition to the band alignment and the effective masses, also the dielectric constant or permittivity of a material can be calculated using DFT. However, for 2D materials quantum confinement within the monolayer plane leads to a small and highly non-local dielectric function [541]. This anisotropy is directly reflected in the dielectric constant with a higher in plane than out of plane dielectric constant [360, 542]. For the TCAD simulations of MoS_2 performed in the following, an out of plane dielectric constant of about 5.5 was used [542]. All MoS_2 material parameters which can be calculated using DFT and are required for drift diffusion simulations are summarized in the first part of Table 6.2.

Table 6.2 contains all material parameters which are required for accurate simulations of MoS_2 based FETs. The first section contains parameters which are extracted from the theoretically calculated band structure of MoS_2. The second section contains material parameters which are strongly influenced by defects in the channel region and are thus process dependent. For these parameters, only meaningful ranges are given according to literature, within which

Parameter	Value/Range	Reference
Transport band gap (E_G)	2.2 ± 0.1 eV	[531, 537, 538, 541]
Electron affinity (χ)	-3.85 ± 0.09 eV	[537, 538, 541]
Eff. rel. permittivity (ϵ_r^{eff})	5.5 ± 0.9	[542, 543]
Work func.diff.(Ti/Au) (E_W)	[0.05, 0.2] eV	[544]
Mobility (μ)	[0.1, 100] cm^2/Vs	[40, 173, 188]
Den. of interface traps (D_{it})	$[10^{12}, 10^{13}]$ $cm^{-2}eV^{-1}$	[386]

Table 6.2. Material parameters of monolayer MoS_2 on SiO_2 which serve as input parameters for DD based TCAD simulations. The parameters in the first section are extracted from the band structures as calculated with DFT, the parameters in the second section depend strongly on the defects in the semiconductor and thus on the processing conditions. Therefore, these parameters served as fitting parameters and were adjusted to reproduce the measurement data. Adapted from [TKJ12].

the values should be chosen. At the current stage of 2D material research, with no generally acknowledged and standardized processing conditions, but instead multiple competing methods, see Section 2.1, these parameters, the work function difference E_W to the contact metals, the mobility μ, and the density of interface traps D_{it}, have to be treated as fitting values and are adjusted to every batch of devices separately.

After having established the material parameters and parameter ranges for monolayer MoS_2, the general simulation methodology using DD based TCAD [317] is verified against measured characteristics. These measured characteristics were recorded on bare-channel back gated monolayer MoS_2 FETs with 90 nm thermal SiO_2 as a back gate insulator with a device layout comparable to the layout shown in Figure 2.3 (a). A detailed description of the device fabrication and measurement methods used have been reported in detail elsewhere [TKJ21] and are only briefly summarized here. MoS_2 monolayers were exfoliated on top of a SiO_2 on Si wafer and titanium/gold electrodes were deposited for source and drain contacts, forming a FET with dimensions of $W = 6.8\,\mu m$ and $L = 1\,\mu m$. A DD based TCAD simulator is justified for these FETS, as their lateral dimensions are in the micrometer range. Thus, there is a large number of scattering centers in the channel region resulting in scattering-dominated charge transport in the diffusive regime. In Figure 6.2 (a) the measurement data from the large-area monolayer MoS_2 FET are compared with simulation data obtained from a drift diffusion simulation and a ballistic simulation based on the top of the barrier model [325]. The top of the barrier model is a compact model to describe ballistic transport in nanoscaled FETs, see Section 3.3.3. This comparison highlights the importance of scattering events in these large-area prototype MoS_2 FETs, as ballistic transport predicts eight orders of magnitude higher current saturation levels than the currents observed experimentally. For these large area MoS_2 based FETs, drift diffusion based TCAD simulations provide an efficient tool to describe current transport. Its main drawback in this context is that the density of states in the 2D layer is not accurately described, an error which is assumed to be small enough to be neglected in the following.

A central material parameter in the diffusive transport regime is the mobility μ which is inversely proportional to the average time interval between scattering events and the effective masses of the charge carriers, see Sections 3.1.3 and 3.3.2. In the highly defective MoS_2

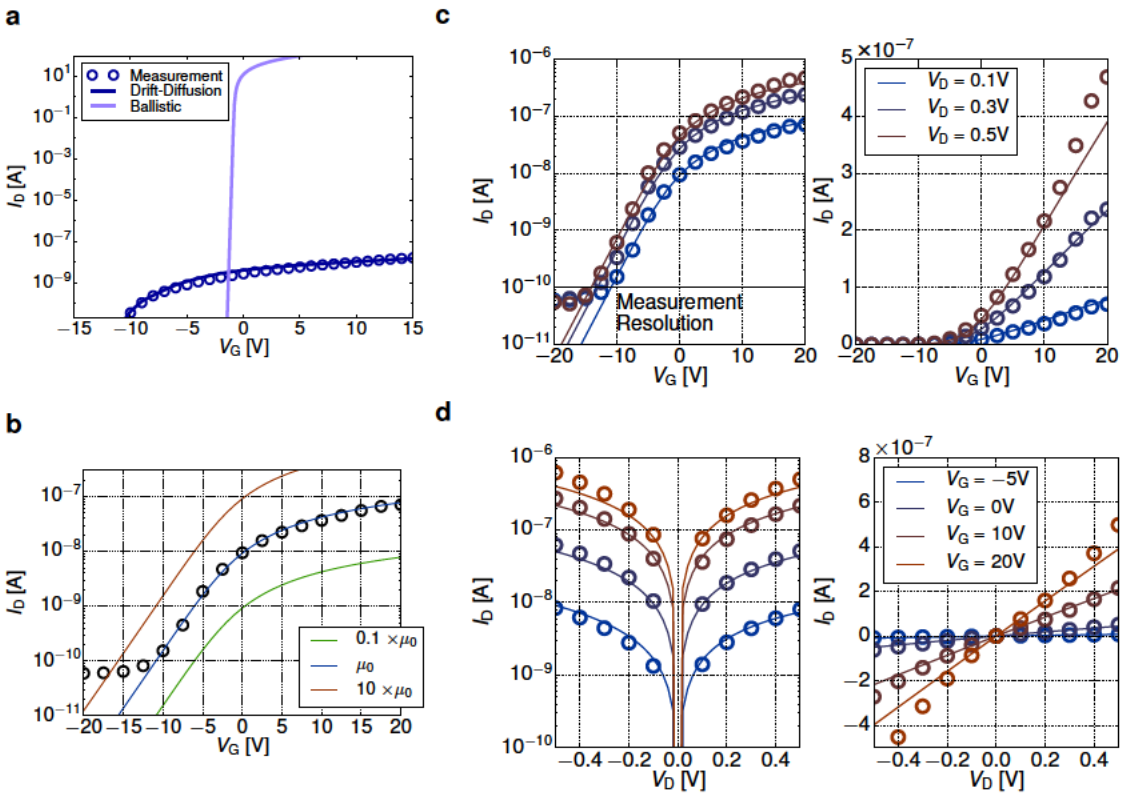

Figure 6.2. **(a)** Comparison of drift diffusion and ballistic simulations for MoS_2 FETs. Circles correspond to measured $I_D - V_{GS}$ characteristics on bare-channel monolayer MoS_2 FETs using 90 nm SiO_2 as a back gate oxide. The device layout is comparable to Figure 2.3 (a) and the active area amounts to 7 µm^2, reproduced from [TKJ18]. **(b)** Impact of the mobility on $I_D - V_{GS}$ characteristics obtained using DD based TCAD simulations [317]. In the scattering dominated transport regime, the mobility is a key parameter to which I_D is directly proportional. **(c)** When using the parameters listed in Table 6.2, excellent agreement between measured transfer characteristics shown as circles and simulated curves, given as solid lines, is achieved. **(d)** Drift-diffusion simulations capture the electrostatics of monolayer MoS_2 on SiO_2 FETs well, providing good agreement of the output characteristics. Graphics in Figures (b)-(d) are reproduced from [TKJ12].

prototypes investigated here, impurity scattering at interface traps is most likely the dominant contribution which limits the observed mobility [40]. In Figure 6.2 (b) the impact of the mobility on the simulated transfer characteristics is shown. According to the approximation for the drain current in the linear regime, see Equation (3.1), the drain current is directly proportional to the mobility, a relation well fulfilled in this instance.

In Figure 6.2 (c) and (d) the agreement between measurement data and DD simulations is presented. The MoS_2/SiO_2 FETs were characterized within a gate voltage range of $V_{GS} \in [-20\,V, 20\,V]$ and a drain voltage range of $V_{DS} \in [-0.5\,V, 0.5\,V]$. In the transfer characteristics in Figure 6.2 (c), circles represent measurement points. Note that the saturation of the current below 0.1 nA has no physical meaning, but is caused by the limitations of the measurement equipment used. The drift diffusion model is capable of capturing all features of both the transfer characteristics and the output characteristics in Figures 6.2 (c) and (d) on a logarithmic scale as well as on a linear scale.

6.1.1 Contact Models

Accurate modeling of the Schottky barriers at the source and drain contacts in MoS_2 FETs is a vital component in the TCAD simulations shown in Figure 6.2. Contrary to silicon MOSFETs, where highly doped junctions lead to the formation of Ohmic contacts, most 2D material-based prototypes, which includes the MoS_2/SiO_2 FETs investigated here, are intrinsic semiconductors without any doped regions. Thus, at the interface between the metal contacts and the MoS_2 layer, Schottky barriers form. The modulation of the Schottky barrier heights and widths at the contacts by the gate bias allows to switch these 2D FETs on and off [171, 173], see Section 2.3 for more details.

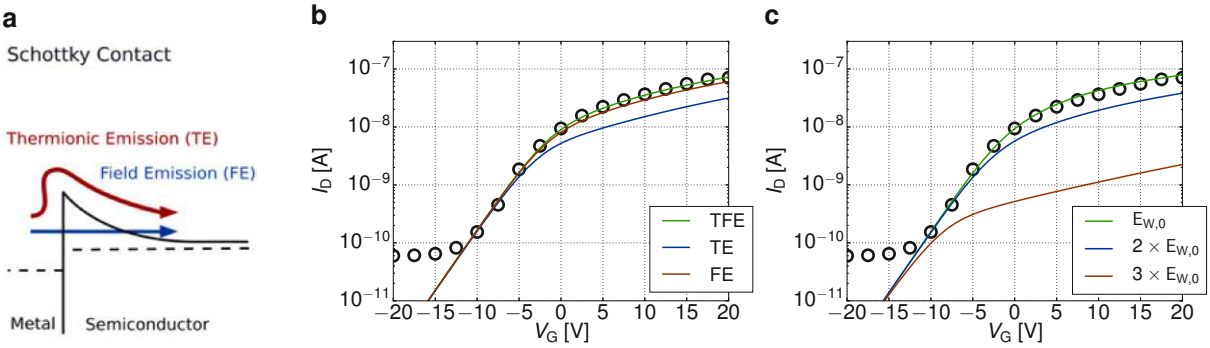

Figure 6.3. **(a)** Schematic illustration of the two contributions to the current across the Schottky barriers at source and drain contacts of MoS_2 FETs. Thermionic emission (TE) describes electrons injected over the barrier and field emission (FE) specifies the tunneling current through the energy barrier. **(b)** Impact of the Schottky barrier model on the simulated $I_D - V_{GS}$ characteristics. In particular in the on-state the contribution of field emission needs to be considered. Circles represent the measured currents and solid lines the simulation results. **(c)** Impact of the Schottky barrier height E_W on the $I_D - V_{GS}$ characteristics, showing a reduction of the on current by multiple orders of magnitudes for increased barrier heights. Graphics (b) and (c) are reproduced from [TKJ12].

In Figure 6.3 (a) the band diagram of the metal semiconductor junction at a Schottky contact is shown. Here, the dashed line indicates the location of the Fermi level in the metal and the semiconductor including an applied bias, respectively. The Schottky barrier height is given by the work function difference E_W between the metal and the MoS_2 layer according to Equation (2.1). In addition, the different contributions to the current across the Schottky barrier are indicated, thermionic emission (TE) in red and field emission (FE) in blue. Their combination leads to a thermionic-field emission (TFE) current. Thermionic emission refers to the thermionic current flow over the energy barrier, as described by Equation (2.2) and field emission is the tunneling current through the barrier, as given by Equation (2.3) [184, 545].

In Figure 6.3 (b) the different contributions to the drain current in the MoS_2/SiO_2 FETs are shown, demonstrating that TE currents dominate in the on-state of the devices. For all simulation results presented in the following, the TFE model was used to describe the current across the Schottky barriers at source and drain. In Figure 6.3 (c), the impact of the work function difference is illustrated, demonstrating that even small variations of the Schottky barrier height can decrease the saturation current level by several orders of magnitude.

6.1.2 Impact of Interface Traps

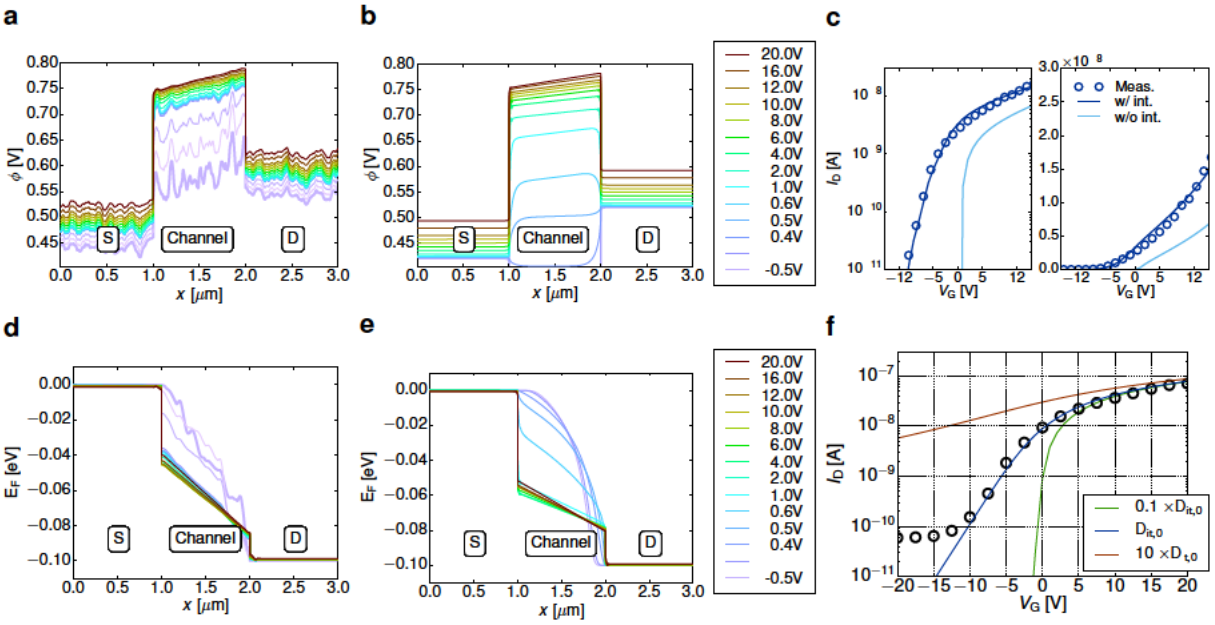

Figure 6.4. **(a)** Simulated electrostatic potential across the channel of MoS_2 FETs using 90 nm SiO_2 as a back gate oxide including the impact of interface traps via the SRH model, see Section 3.4.1. For the simulated FETs, the channel is 1 µm long, $V_{DS} = 0.1$ V is applied and the gate voltage is varied from 20 V, where the channel is completely turned on in dark red, to −0.5 V directly below V_{th} in light purple. **(b)** Electrostatic potential in the MoS_2 channel without any interface traps. **(c)** Impact of the interface traps on the $I_D - V_{GS}$ characteristics simulated with DD based TCAD [317]. **(d)** Location of the Fermi level E_F as a function of the applied gate voltage, if interface traps are included using the SRH model. Close to V_{th} the Fermi level moves away from the conduction band edge into the MoS_2 band gap. **(e)** Fermi level in the MoS_2 channel for varying V_{GS} without including interface traps. Graphics (a) - (e) are adapted from [TKJ18]. **(f)** Impact of the interface trap concentration D_{it} on the $I_D - V_{GS}$ characteristics, showing a strong influence on the subthreshold swing, see also Section 4.2.1. Reproduced from [TKJ12].

In the drift diffusion based TCAD simulations presented here the impact of interface traps was considered by using the Shockley-Read-Hall (SRH) model, see Section 3.4.1. In this model the interface traps serve as recombination centers for charge carriers and, whenever charged, disturb the electrostatics of the transistor. As the free electron densities in 2D materials are high and the band gap of 2D materials is large, charge recombination effects are less of a concern in comparison to silicon technologies. However, the electrostatic doping by the interface traps is essential, as the current flows directly at the interface in 2D materials. The impact of charged interface traps on the potential in the channel of an MoS_2/SiO_2 FET is shown in Figures 6.4 (a) and (b). In Figure 6.4 (c) it is shown that the charging of interface traps leads to a shift of the threshold voltage and to an increased subthreshold swing.

When considering the impact of charged interface traps on the location of the Fermi level in the MoS_2 channel in Figures 6.4 (d) and (e), it becomes apparent that in the on-state of the MoS_2 FET the Fermi-level is pinned. Only as the device is switched off, the charged interface traps locally affect E_F. In Figure 6.4 (f) it is shown that the density of interface traps D_{it} strongly

affects the subthreshold slope in accordance with Equation (4.3). The density of interface traps in MoS_2 FETs was evaulated experimentally using CV measurements by Takenaka *et al.* [386] and $1/f$ noise measurements by Vu *et al.* [385], for more details see Section 4.2.1.

6.1.3 Modeling the Hysteresis

After having successfully developed a model to describe the current through an MoS_2/SiO_2 FET in the steady-state, the next step towards modeling the hysteresis are transient simulations, where border traps are taken into account using the NMP model [341], see Section 3.4.2. Even though several groups claim that charge trapping at interface defects is responsible for the hysteresis [546, 547], here it is argued that, in accordance with previous works [TKJ15, TKJ21, 518], charge trapping events at border traps are the main source. This is corroborated by the the fact that the largest hysteresis is observed for the longest sweep time, see also Section 5.1.1. In addition, according to the SRH model in monolayer MoS_2 with a band gap of 2.2 eV, a maximum time constant of 1 µs is obtained for a typical capture cross section of $1 \times 10^{-15}\,\mathrm{cm}^2$, thus the charge trapping at interface traps is too fast to explain the observed hysteresis.

Moreover, border traps are located at a finite distance from the interface, the most important ones for the charge transfer processes lying typically within the first few nanometers [9]. This leads to an increased bias dependence, as observed in the hysteresis in MoS_2 FETs. The enhanced bias dependence of charge trapping in the oxide in comparison to charge trapping at the interface is illustrated in Figure 6.5. Interface traps provide trap levels inside the band gap, thus as the Fermi level sweeps across the band gap for increasing gate voltages, interface traps become discharged. This charging process is five orders of magnitude faster than the sweep time, thereby effectively reducing the subthreshold slope. Once the Fermi level reaches the conduction band edge (roughly at $V_{GS} \approx V_{th}$), it remains roughly pinned there due to the high concentrations of injected electrons. In a first approximation there are no trapping and detrapping events at interface states above the threshold voltage, which is confirmed by comparing the charge state of the interface traps in Figures 6.5 (b) and 6.5 (c). However, for increasingly positive gate voltages, the oxide defect band is bent downwards, leading to more trapping events in the oxide, consistent with the experimentally observed increase in the hysteresis for increased high levels of the gate voltage $V_{GS,H}$ [TKJ15]. The charge capture and emission events for gate voltages above the threshold voltage cause an effective shift of the entire $I_D(V_{GS})$, which produces the observed hysteresis.

For the modeling of the hysteresis we use the four-state NMP model, see Section 3.4.2. The model does not only account for the energy barriers for electron transfer, as is usually done when using the SRH model, see Section 3.4.1, but it also considers the energetic relaxation of the structure around the defect, where the electron is captured or emitted [224]. Depending on the microscopic nature of the defect, which has been studied in detail for SiO_2 based on Si/SiO_2 FETs [348, 422], one usually discusses either hole or electron trapping events. As the charge transfer process is exactly the same in both cases, the two processes can only be distinguished by the charge change of the trapping defect in the oxide, which either goes from positive to neutral (hole/donor-like trap) or from neutral to negative (electron/acceptor-like

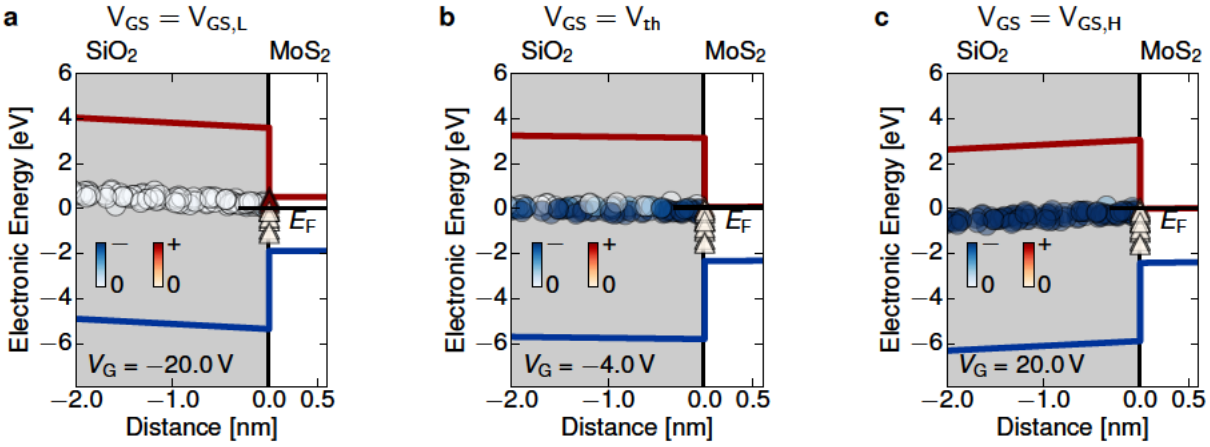

Figure 6.5. **(a)** Band diagram of the MoS_2/SiO_2 FET showing the location of donor-like interface traps (red triangles) and of the acceptor-like oxide defect band (blue circles) [418, TKC12] responsible for the hysteresis. For gate voltages below the threshold voltage $V_{GS,L}$ as shown here, E_F moves across the band gap and interface traps are discharged. **(b)** Band diagram of the MoS_2/SiO_2 FET at V_{th} where several border traps in the SiO_2 are already charged. **(c)** The majority of border traps in SiO_2 is negatively charged in the on-state at $V_{GS,H}$. All graphics are adapted from [TKJ12].

trap), see also Section 5.1.1. Therefore, the difference between electron and hole traps is only visible in an offset of the transfer characteristic, as it only changes the balance of fixed charges.

In order to explain the hysteresis in MoS_2 FETs the two defect bands of SiO_2 are used, which are already known from silicon technologies [TKJ13, 418, TKC12, 548], with the first one being a donor-like hole trapping band located at $\langle E_T \rangle \pm \sigma_{E_T} = 4.6 \pm 0.3\,\text{eV}$ below the conduction band edge of SiO_2 [548], and the second one being an acceptor-like electron trapping band at $\langle E_T \rangle \pm \sigma_{E_T} = 3.0 \pm 0.2\,\text{eV}$ below the conduction band edge of SiO_2, see Table 4.1. The second defect band has already been observed for Si-based devices with dielectric gate stacks [418, TKC12] and has been used in our previous works for the modeling of the hysteresis and of bias-temperature instabilities in FETs based on MoS_2 [TKJ15, TKJ21] and black phosphorus [518]. The first defect band is located in the lower half of the band gap of monolayer MoS_2 and does not contribute to the degradation in n-type FETs, where the Fermi level only scans across the upper half of the band gap. Therefore, only the second defect band needs to be taken into account and is shown in Figure 6.5.

Besides the bias dependence of the charge trapping process, the second important aspect is the dynamic behavior of the responsible defects, as determined by the NMP model. A trap can only contribute to the hysteresis if it captures an electron at a high gate voltage and maintains its charge until the low level of the gate voltage is reached. This means that the electron capture time constant (τ_C) of the respective trap has to be smaller than the electron emission time constant (τ_E) at high gate voltages and vice-versa. For identifying the traps which contribute to the hysteresis, the important voltage level is $V_{th} \approx -4\,\text{V}$, where the hysteresis is extracted. If $\tau_E < \tau_C$ holds for $V_{GS} < V_{th}$ and $\tau_E > \tau_C$ for $V_{GS} > V_{th}$, this trap can in principle contribute to the hysteresis.

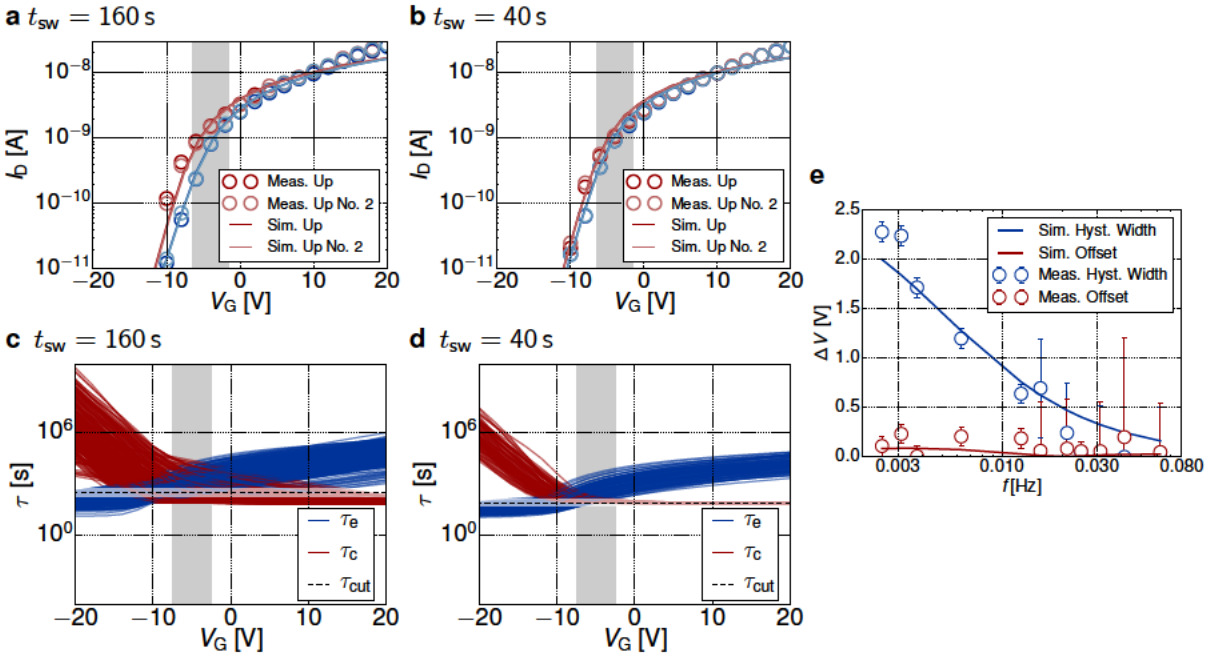

Figure 6.6. **(a)** Comparison of the simulated hysteresis (solid lines) to the measured hysteresis (circles) on monolayer MoS_2/SiO_2 FETs. For a sweep time of 160 s the hysteresis is large with the up sweep shown in red having a smaller V_{th} and the down sweep in blue a higher V_{th}. **(b)** A reduced hysteresis is observed at $t_{SW} = 40$ s and accurately reproduced in transient DD simulations coupled to an NMP model to describe charge transfer to border traps. **(c)** Voltage dependence of the time constants of the border traps for a selected set of defects which contributes to the observed hysteresis for a sweep time of 160 s. The cut-off time is determined via $\tau_{cut} = 2t_{sw}$. **(d)** At the smaller sweep time of 40 s, fewer border traps have time constants in the respective range and can contribute to the observed hysteresis, thereby reducing the hysteresis width. **(e)** Hysteresis width (extracted between up- and down-sweep (blue)) and the offset (extracted between two up- or two down-sweeps for different measurement rounds (red)) as a function of the sweep frequency. The error bars report the minimum error of the measurement process given by the voltage step ΔV used to record the I_D (V_{GS}) curves. The hysteresis width decreases quickly for fast sweeps. Adapted from [TKJ12].

In Figures 6.6 (a) and (b) the simulated hysteresis for two different sweep rates is shown and compared to measurement data. There were two subsequent measurement rounds to demonstrate that the hysteresis is a reproducible phenomenon and there is no general drift of the characteristics interfering with the hysteresis. The simulation results, obtained within the scope of this work, clearly corroborate the previously observed PBTI-like hysteresis [TKJ21]. In this context, PBTI-like hysteresis means that for the down sweep the $I_D - V_{GS}$ characteristic is shifted towards higher threshold voltages, comparable to the threshold voltage increase during PBTI stress. Alternatively, such a hysteresis is termed clockwise.

When comparing Figures 6.6 (a) and (b) there is an apparent dependence of the hysteresis width on the sweep frequency. In fact, the traps contributing to the hysteresis at different frequencies are not the same. The time for one up-sweep or one down-sweep ($2t_{sw} = 1/f$) sets to a first approximation an upper limit (τ_{cut}) for the time constants of the contributing traps. If either $\tau_E < \tau_{cut}$ at the maximum negative V_G or $\tau_C < \tau_{cut}$ at the maximum positive

V_G, this trap can change its charge state for the first time towards the end of the up sweep and for the second time towards the end of the down sweep. If this condition is not fulfilled, it is very unlikely that this trap changes its charge state at all during the sweeping process. In addition, the trap also must not change its charge state too quickly. To be precise, it cannot contribute to the hysteresis if it captures a charge before the hysteresis width is measured at $V_{GS} = V_{th}$. This corresponds to meeting the condition $\tau_C > t(V_{th})$ at the threshold voltage, with $t(V_{th})$ being the sweep time until the threshold voltage is reached.

In Figures 6.6 (c) and (d) the bias dependence of the time constants of all traps fulfilling all of the above mentioned criteria, and thus causing the hysteresis, are displayed. The electron capture time shows a larger bias dependence than the emission time. At shorter sweep times, fewer defects meet the criteria, reducing the hysteresis width. To quantify the hysteresis phenomenon, the hysteresis width at the threshold voltage for all measured sweep frequencies is extracted. In Figure 6.6 (e) the hysteresis width is shown as a function of the sweep frequency for the measurements and for the simulations. The error bars indicate the minimal measurement errors given by the voltage stepping used in the measurements. Additionally, the offset between subsequent measurement rounds is displayed to make sure that no permanent shift of the characteristics interferes with the hysteresis. Good agreement between measured and simulated data is obtained, demonstrating that the presented simulation methodology captures the time behavior of the hysteresis phenomenon correctly.

6.2 Modeling Leakage Currents through Gate Insulators

Parts of this section (marked by a vertical sidebar) have been published in

[TKJ2] Nature Electronics 4, 98–108, (2021).

In this section the leakage currents through scaled gate insulators are studied and the current blocking potential of different insulators is compared. As described in Section 4.1, insulators in modern FETs should be thinner than 1 nm equivalent oxide thickness (EOT) in order to provide good gate control. At the same time, in order to ensure a small standby power consumption, the gate leakage current density should stay below the low-power limit of $1.5 \times 10^{-2}\,\mathrm{Acm}^{-2}$ [28, 364], for a supply voltage of $V_{DD} = 0.7\,\mathrm{V}$ being applied at the gate [21].

In the following an analysis is provided on which gate insulators for 2D material-based FETs are, in theory, capable of providing such low gate leakage currents at a small EOT. Here, a theoretical lower limit for the gate leakage currents is established in the case of a defect-free insulator. In reality, defects in the insulator can frequently lead to current densities above this lower limit if trap assisted tunneling currents dominate the leakage [366], in particular in highly defective insulators for 2D FETs. However, an analysis of the ideal situation is of critical importance as it yields the ultimate performance limit of the respective material. These results rely only on inherent material properties which cannot be altered by improving the material quality via breakthroughs in the synthesis methods, but only by resorting to a different material system.

Arguably, hexagonal boron nitride is widely considered to be the most promising insulator for 2D material-based devices. Numerous studies have demonstrated the potential of hBN when used as a substrate and gate insulator in FETs at the proof-of-concept level, where thick insulators are employed [67, 472, 549]. There is, however, only a limited number of studies about the suitability of hBN as an insulator at the scaling limit with a thickness of one to six atomic layers (0.33 nm – 2 nm) [86, 218, 550]. Here, the performance limits of hBN in its ultrathin form are analyzed by calculating the tunneling currents through hBN, using the intrinsic material properties of single-crystalline, multilayer hBN.

6.2.1 Adaptations of the Tsu-Esaki Model for hBN

Tunneling currents were simulated for a system of three layers of hBN corresponding to an EOT of 0.76 nm according to the present technology node [21]. The hBN layers were placed between a gold electrode with a work function of 4.7 eV and a p-doped silicon layer (acceptor doping density $N_A = 10^{18}\,\mathrm{cm}^{-3}$, donor doping density $N_D = 10^{10}\,\mathrm{cm}^{-3}$), thereby forming a metal-insulator-semiconductor (MIS) structure. The current density through this structure was calculated using the Tsu-Esaki model [334], as implemented in Comphy [TKJ13]. Within this model the tunneling transmission probability is approximated by a Wentzel-Kramers-Brillouin (WKB) factor and the expressions for the electron current are given in Equations [1] - [3] in Figure 6.7 (a). Similar expressions are also valid for the hole current, i.e. for carrier transport between the Si valence band and the metal.

In general, the Tsu-Esaki model describes the process of electron/hole tunneling from the conduction/valence band of one contact, e.g. a metal, to that of another contact, e.g. a semiconductor, while both contacts are separated by an energy barrier formed by an insulator, see Figure 3.7 in Section 3.3.3. Within the Tsu-Esaki model, the curvature of the conduction and valence bands in the insulator are accounted for in the effective tunneling masses. In comparison, the standard application of the Comphy framework is to calculate charge transfer rates to border traps in the insulator according to NMP theory. One important factor which contributes to these rates is the tunnel coefficient $\theta_e(E)$, see Equation (3.44d), calculated using the WKB approximation to obtain analytic expressions for triangular (Fowler-Nordheim tunneling) and trapezoidal (Direct tunneling) shaped energy barriers. This WKB tunneling factor was adapted here to describe tunneling as part of the Tsu-Esaki formula. Another central aspect of the Tsu-Esaki model is the supply function $N_e(E)$, which critically depends on the calculation of the Fermi levels at both contacts. In Comphy the Fermi level at the channel/insulator interface is calculated by solving the Poisson equation employing a Newton iteration. Within this context, the space charge per unit area as a function of the surface potential is derived from an analytic expression assuming charge neutrality deep in the bulk semiconductor [207]. The doping concentrations, work function differences, and the insulator capacitance determine in this calculation the Fermi level as a function of gate bias. Both quantities, the tunneling coefficient and the supply function, are subsequently numerically integrated with respect to the energy over the entire valence and conduction bands for electrons and holes respectively to arrive at the current density $J_e(E)$. The gate bias dependent tunneling current is finally obtained by repeating the integration for each voltage

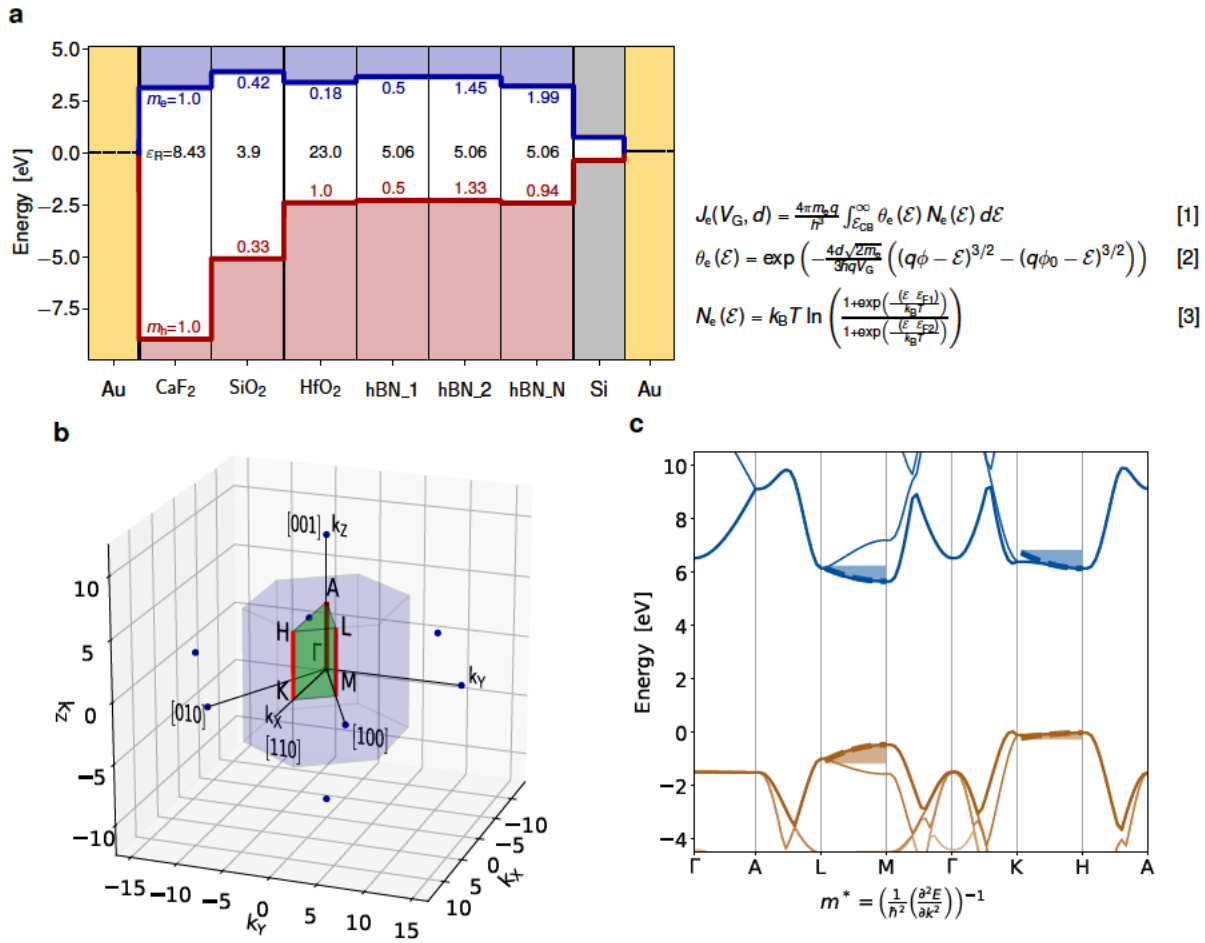

Figure 6.7. **(a)** On the left hand side the band diagram of the components of a metal insulator semiconductor (MIS) system consisting of a gold electrode, an insulator, e.g. hBN, and silicon is shown. The band alignment of hBN is compared with other insulators and several plausible material parameters of hBN are given with hBN_N denoting the material parameters calculated and used in DFT + NEGF calculations. On the right hand side the Tsu-Esaki equations are shown, which describe the electron contribution to the direct tunneling current density J_e through an insulating barrier. Here, θ_e is the WKB electron tunnel coefficient, N_e the electron supply function, E_{CB} the conduction band edge energy, E_{F1} the Fermi level in the metal, and E_{F2} the Fermi level in the semiconductor. **(b)** Hexagonal first Brillouin zone of hBN, shown in the momentum space spanned by k_x, k_y, and k_z with all high symmetry points labeled. The two valleys contributing to the transport in the z direction are highlighted in red, the H → K and M → L valleys. **(c)** The hBN band structure, calculated with the HSE06 functional, is shown. It can be seen that the bands along H → K and M → L, which contribute to vertical transport, are comparatively flat. The definition of the effective mass m^* is included and the parabolas corresponding to the effective masses are shown as dashed lines. All graphics in this figure are adapted from [TKJ2].

step. Within the semi-classical picture purely quantum mechanical effects like quasi bound states in a strongly inverted channel are neglected and the effective masses are approximated by single parameters. Nevertheless, the Tsu-Esaki model has shown good agreement with steady state measurements of tunneling currents in a variety of applications ranging from Si CMOS technology [551] to tunnel junctions [552] [553] and it offers the advantages of reduced computational costs for a small number of model parameters.

In the Tsu-Esaki model, the tunneling current depends most strongly on the parameters in the exponential WKB factor, given in Equation [2] in Figure 6.7 (a), and as such on the insulator thickness (d), the applied voltage (V_{GS}), the material parameters of the energy barrier heights (ϕ, ϕ_0), and on the effective tunneling masses for electrons (m_e) and holes (m_h). Another material parameter that indirectly affects the layer thickness is the dielectric constant which defines the equivalent oxide thicknesses (EOT = $\epsilon_R/\epsilon_{R,SiO_2} d_{SiO_2}$). Here, an experimentally determined value for the dielectric constant of hBN of $5.06\epsilon_0$ is used, which has served as reference value for many years [457], even though DFT calculations have recently been used to calculate a smaller theoretical value of $3.76\epsilon_0$ [360]. The discrepancy between these values is unclear and the use of the higher value aligns with the aim of presenting the best case scenario, thus the lowest possible estimate for the tunnel leakage currents through hBN.

The band diagrams for hBN, according to various plausible sets of material parameters, are shown in Figure 6.7 (a) in comparison to other commonly used insulators, namely the conventional amorphous oxides SiO_2 and HfO_2 and the ionic fluoride CaF_2, which was recently proposed as a gate insulator for 2D material-based FETs [TKJ7], see Section 4.4. In addition, in Table 6.3 the material parameters of hBN are explicitly listed and the parameter trends required for efficiently suppressing a direct tunneling current are included. For minimizing the tunneling current, the offsets for both valence and conduction bands must be large to ensure high energy barriers, the effective masses must be large, and the dielectric constant also must be as high as possible, as this corresponds to a large physical layer thickness for a given EOT, even though this needs to be balanced against high charge carrier mobilities in the semiconductor.

It is important to note that, based on this semi-classical methodology, only a range of tunneling current estimates through hBN can be provided, shown as a blue shaded area in Figure 6.9. This is a direct consequence of the empirically derived parameters for the effective tunneling masses for electrons and holes are important, but these empirical parameters have barely been studied in the past. Thus, two sets of parameters are used here. The first set of small tunneling masses, corresponding to high currents, is based on reference [356], where the tunneling masses were calibrated to experimental data. We hypothesize that the agreement achieved in this work was likely due to a severe underestimation of the effective tunneling masses which control the tunneling current which compensates for the neglect of TAT in the model. This set of tunneling masses is used for simulations of hBN_1. The second set of high tunneling masses, corresponding to small currents, is adapted from reference [368], where the effective masses were extracted from DFT calculations of the band structure of bulk hBN. This set is used for the simulations of hBN_2.

In any case, the calculation of the effective tunneling masses for out of plane transport through hBN, based on the DFT band structure, is complex and comparatively inaccurate for two main reasons. First, two valleys contribute to the out of plan transport in bulk hBN, the M→L and H→K valleys. These two valleys are highlighted in red in the depiction of the hexagonal first Brillouin zone of hBN in Figure 6.7 (b). Second, the band structure of hBN along the M→L and H→K orientations is nearly flat, which corresponds to high tunneling masses but also leads to large uncertainties in the extraction of the effective masses from bands with a

Trend	Parameter			Value	Reference	Used for
↑	bandgap	E_G		5.95 eV	[455][554]	hBN_1, _2
				5.63 eV	-	hBN(NEGF)
-	electron affinity	χ		1.14 eV	[456]	hBN_1, _2
				1.3 eV	[555]	-
				1.59 eV	-	hBN(NEGF)
↑	dielectric const.	ε		5.06 ε_0	[457]	hBN_1, _2
				3.76 ε_0	[360]	-
↑	electron mass	m_e	-	0.5 m_0	[356]	hBN_1
			-	1.45 m_0	-	hBN_2
			(M→L)	2.21 m_0	[368]	-
			(M→L)	2.31 m_0	-	hBN(NEGF)
			(H→K)	1.45 m_0	-	hBN(NEGF)
↑	hole mass	m_h	-	0.5 m_0	[356]	hBN_1
			(M→L)	1.33 m_0	[368]	hBN_2
			(M→L)	1.48 m_0	-	hBN(NEGF)
			(H→K)	4.38 m_0	-	hBN(NEGF)

Table 6.3. Material parameters of bulk hBN. In the leftmost column the trends for suppressing tunnel leakage currents are highlighted, where ↑ stands for as high as possible and – for not specifiable in general. The tunneling masses are given as multiples of the electron mass m_0. Adapted from [TKJ2].

small curvature. The band structure, as calculated by HSE06 [556], is shown in Figure 6.7 (c), where the comparatively flat bands along these two orientations can be seen and parabolas corresponding to the effective masses are shown. This small curvature directly originates from the layered structure of hBN and as such from the high inherent anisotropy of a layered material. Therefore, the effective electron mass is most likely overestimated in [368] and was adapted here to a smaller, more plausible value based on the currents we simulated with *ab initio* methods, as explained below. The wide blue shaded area in Figure 6.9, which spans in some regions more than 4 orders of magnitude, demonstrates the importance of future studies on extracting effective tunneling masses for electrons and holes through hBN.

6.2.2 Coupled DFT and NEGF Model

In order to avoid the problem of calculating effective masses and to increase the accuracy of the estimated currents through defect-free hBN, the current through Au-hBN-Si structures was also calculated using a non-equilibrium Green's functions (NEGF) approach in combination with DFT, see Section 3.3.1. These calculations were performed by our collaborators at ETH Zürich. In these full-band transport simulations the Hamiltonian and overlap matrices of the structure are first calculated with the CP2K package [288] based on the HSE06 hybrid functional [556]. These matrices are then loaded into the quantum transport solver OMEN [529] to obtain the current-voltage characteristics of the MIS gate stack based on the same electrostatic potentials as used in the semi-classical WKB case.

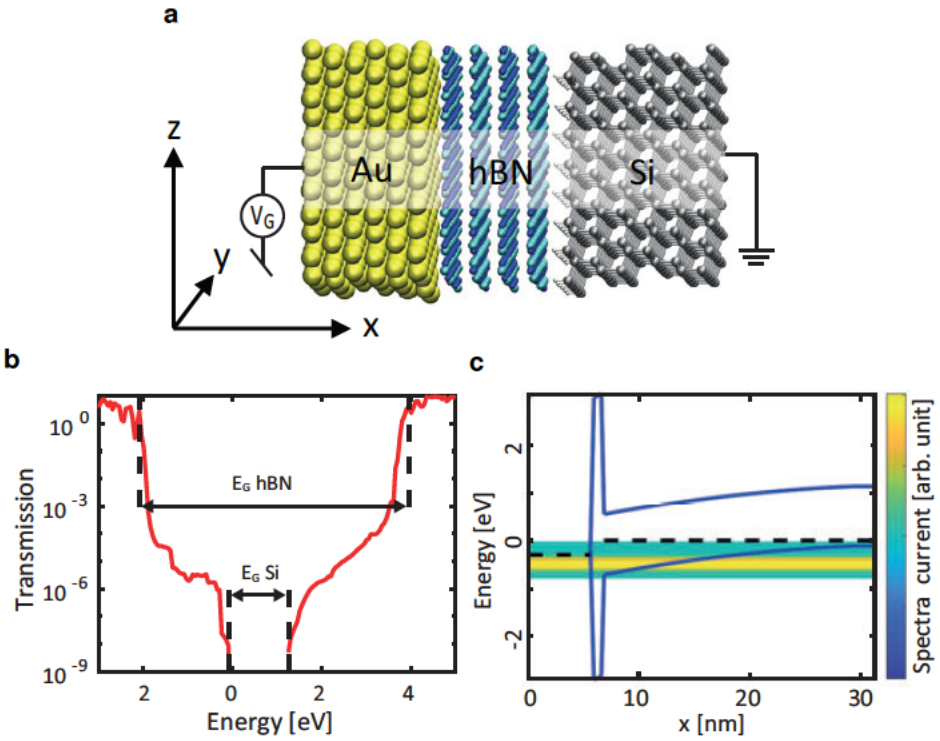

Figure 6.8. **(a)** Atomistic representation of the (111)Au-hBN-(111)Si MIS stack used in the DFT and quantum transport simulations. Au, B, N, and Si atoms are shown as yellow, blue, cyan, and gray spheres, respectively. A gate bias is applied across the MIS stack that is oriented along the x-axis. **(b)** Transmission function as a function of the energy through the MIS structure shown in (a) at a gate voltage of $V_{GS} = 0.3\,V$. The Fermi energy is set to 0 eV. The black dashed lines indicate the band edges of the hBN and Si regions where band gaps for hBN/Si of 5.9 eV/1.26 eV, respectively, are found. **(c)** Energy- and position-resolved current density through the hBN at $V_{GS} = 0.3\,V$. The spectral current density is shown as a heat map with yellow indicating high current densities and blue small current densities. The dashed black lines refer to the Fermi energy of the Au gate electrode to the left and the Si substrate to the right. The solid blue line shows the band diagram of the MIS stack. All graphics in this figure are adapted from [TKJ2].

The device geometry for the DFT calculations is shown in Figure 6.8 (a). This structure was created by first stacking individual slabs of each material on top of each other with a distance of 0.3 nm between them. The (111)Au slab was 1.6 nm thick and consisted of 189 atoms. Then, two to four layers of hBN, each measuring ~0.33 nm and containing 57 atoms, were added on top of the (111)Au contact. The structure was completed by a hydrogen passivated (111)Si slab of a thickness of 1.6 nm and composed of 144 Si and 12 H atoms. In this manner, a hexagonal unit cell was formed with a side length of 1.33 nm. In the next step, the positions of all atoms within the MIS stack were relaxed at the DFT-D3 level [557] with the CP2K code [288] using PBE functionals [558] for a Brillouin zone sampling at a 2x2x1 k-point mesh. During the geometry optimization process, atoms were free to move along all directions with the restriction that the size and shape of the cross section spanned by the y-z plane in Figure 6.8 (a) were kept constant. Thus, the out-of-plane cell length along x in Figure 6.8 (a) adjusted itself automatically. In this way, the distances between the materials were optimized to minimize the total energy of the system, leading to relaxed (111)Au-hBN and hBN-(111)Si interfaces.

On this relaxed structure, DFT calculations with CP2K were performed to extract the Hamiltonian H and overlap S matrices. Both H and S matrices were subsequently loaded into the OMEN quantum transport solver [529] to compute the current-voltage characteristics of the system in the ballistic limit, thus without any energy or momentum relaxation and no scattering processes. Because of the large device dimensions and the large design space to explore, self-consistent Schrödinger-Poisson calculations with OMEN were computationally too expensive. Rather, the same electrostatic potential profiles as in the WKB case were used in the quantum transport simulations as well. In Figure 6.8 (b) the transmission function through the (111)Au-hBN-(111)Si structure with four layers of hBN is shown for a gate voltage $V_{GS} = 0.3\,V$. As the HSE06 hybrid functional was used in Si and hBN, reasonable band gap values of 1.26 eV for Si and 5.9 eV for hBN could be observed. In Figure 6.8 (c) the corresponding energy-and position-resolved spectral current map is depicted, together with a band diagram of the different material regions.

6.2.3 Performance Projection of the Tunnel Current through hBN

The calculated tunneling currents through hBN using both approaches, DFT+NEGF and the Tsu-Esaki current range, are in good agreement, as can be seen in Figure 6.9 (a). Only for small gate voltages the tunneling current is underestimated by the range obtained from the Tsu-Esaki model. When comparing the leakage currents through hBN with tunnel currents through other insulators it becomes clear that at a small EOT of 0.76 nm the gate leakage through hBN is slightly lower than through SiO_2. However, both are orders of magnitude higher than through the high-k dielectric HfO_2 or through crystalline CaF_2 [TKJ6]. It is expected that in real samples employing any of these materials, the currents will likely be higher than reported here because the impact of trap-assisted tunneling is neglected. This serves the purpose of establishing a lower limit of theoretically attainable tunneling currents. Thus, in the best case scenario, tunneling currents through hBN will be orders of magnitude higher than, for example, through the high-k dielectric HfO_2.

In addition, the tunneling current was calculated as a function of EOT for a fixed electric gate field and a fixed applied gate voltage, corresponding to the two scaling laws, Dennard scaling [22] and constant voltage scaling [23]. In Figure 6.9 (b) the tunneling current density is shown as a function of EOT for constant electric gate fields of 2 MV/cm for negative gate voltages, corresponding to a p-type transistor and in Figure 6.9 (c) for positive voltages, thus an n-type FET. It can be clearly seen that hBN is not suitable as a gate insulator in a p-type FET for scaled devices with EOT <1 nm, as the gate leakage current exceeds the low-power limit by more than one order of magnitude. If the leakage currents are above the low-power limit, the off-state currents, and thus the power consumption of the device, are too high for applications in consumer electronics. This observation was made for the current technology node and will be even worse for future nodes, where the insulator thickness will be scaled down even further. Similar conclusions can be drawn from a comparison of the tunneling currents as a function of the EOT for a constant negative voltage of −0.7 V in Figure 6.9 (d) and for a positive voltage of 0.7 V in Figure 6.9 (e), corresponding to a p-type and n-type FET of the current technology node [21]. The simulations predict substantial leakage currents even

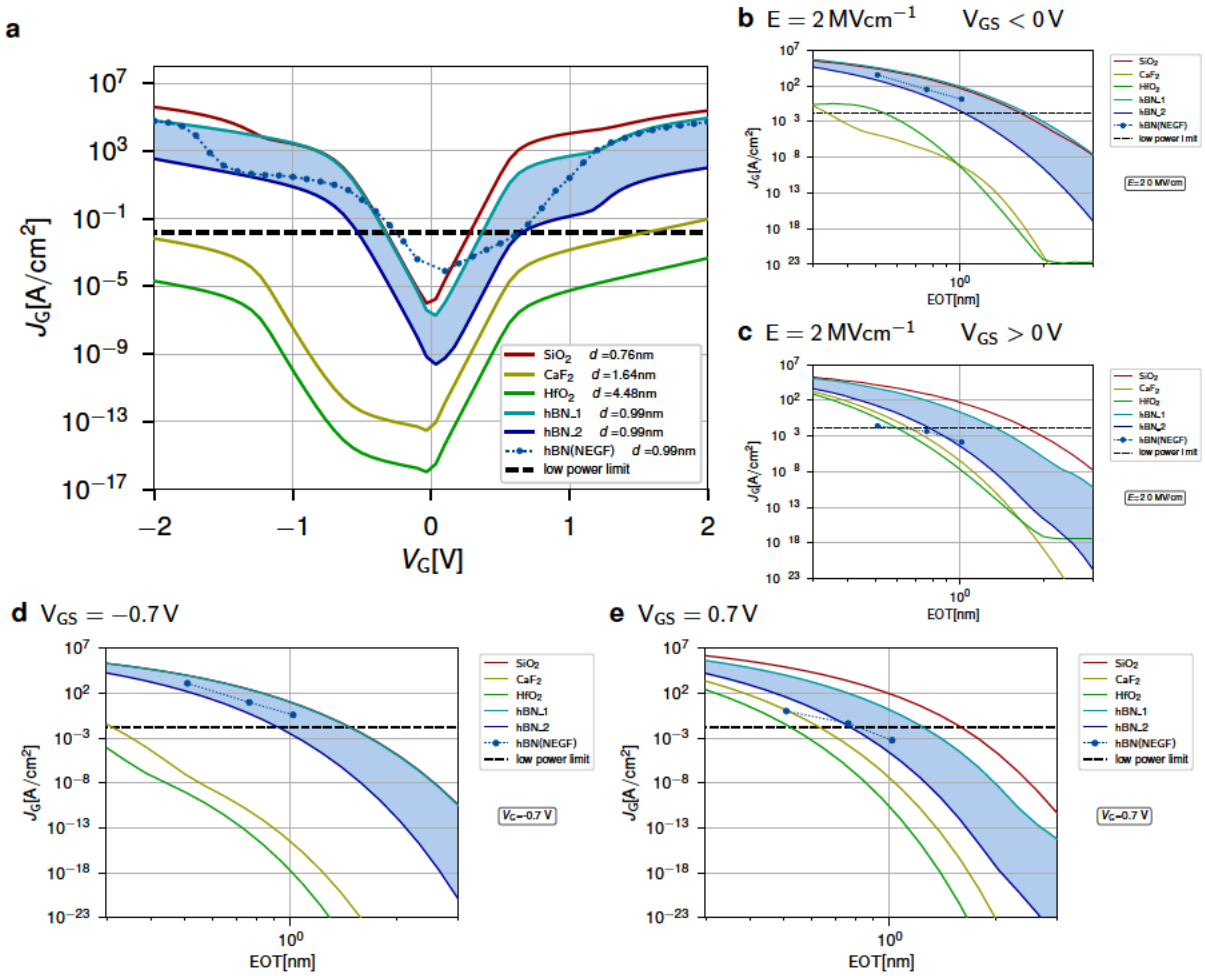

Figure 6.9. **(a)** Comparison of the tunneling current density J_G through the MIS gate stack of Au/insulator/Si as a function of the applied gate voltage V_G. Currents are given for a constant EOT of 0.76 nm, corresponding to three atomic layers of hBN. hBN_1 and hBN_2 stand for two different sets of material parameters used, as shown in Figure 6.7 (a). In addition, *ab-initio* simulation results are included as solid blue circles connected by a dashed line. **(b)** Current densities at a constant gate insulator field of 2 MVcm^{-1} for a p-type transistor as a function of the EOT. Leakage currents through various insulators are compared at a negative gate bias $V_{GS} < 0$ V at a constant gate field, illustrating Dennard scaling for a p-type FET. **(c)** Current densities as a function of the EOT are compared at a fixed gate field of 2 MVcm^{-1} and positive gate bias $V_{GS} > 0$ V, showing the leakage current increase if a n-type transistor is scaled down according to Dennard scaling. **(d)** Current densities are compared for different gate insulators at a constant negative gate bias of $V_{GS} = -0.7$ V, which illustrates constant voltage scaling for a p-type transistor. **(e)** Current densities are compared at a constant positive gate bias of $V_{GS} = 0.7$ V, showing the leakage current increase for constant voltage scaling of a n-type transistor. All graphics in this figure are adapted from [TKJ2].

through defect-free hBN when negative voltages are applied due to the small band offset for holes of only about $\phi_h = 1.9$ eV and the comparatively small tunneling masses for holes in the M→L and H→K valleys of hBN.

It is worth noting that the calculated tunneling current densities depend on the choice of the metal gate, since the work function of one contact changes. This is an advantage of the Tsu-

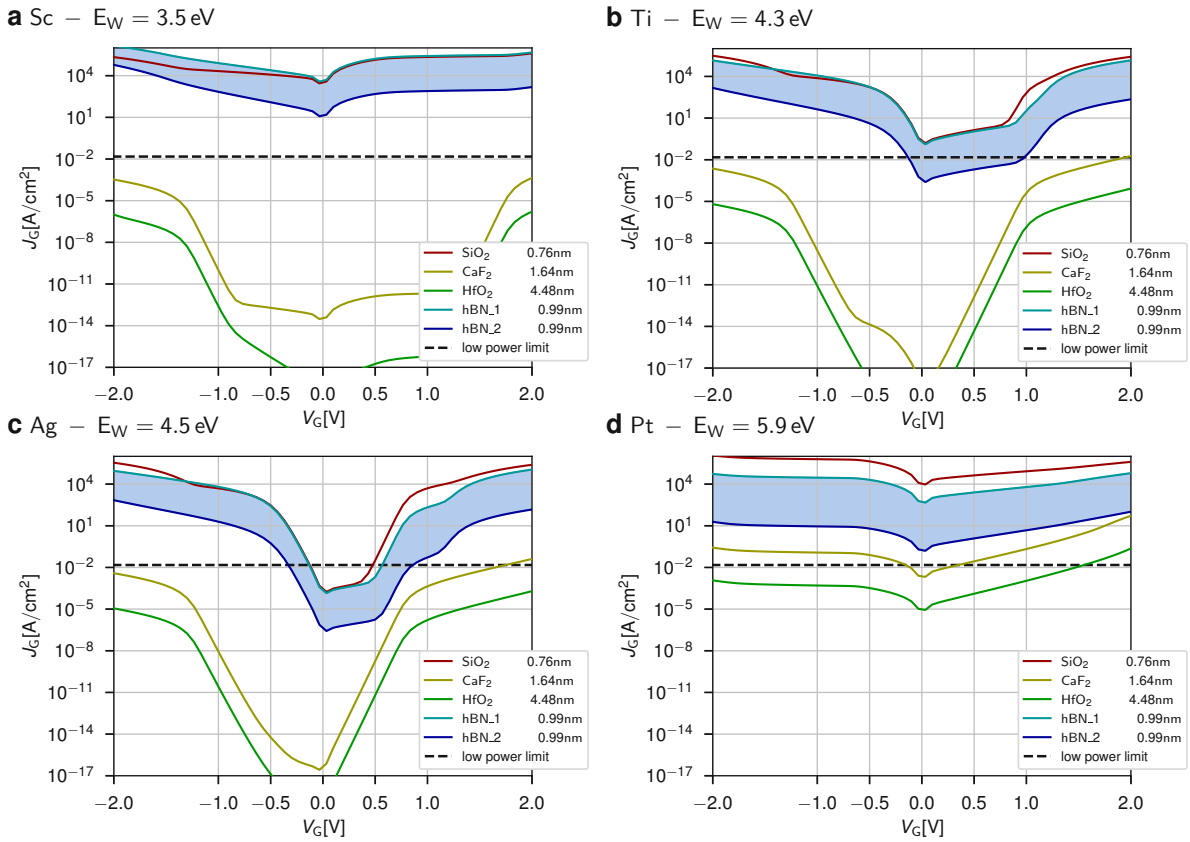

Figure 6.10. **(a)** Estimated tunneling current density through a MIS gate stack of Sc/insulator/Si for different insulators as a function of the applied gate voltage. In comparison to Figure 6.9 (a) Sc is used instead of Au, which has a considerably lower work function at 3.5 eV, leading to much higher current densities through SiO_2 and hBN. **(b)** Current densities through a MIS gate stack with Ti as a metal gate with $E_W = 4.3$ eV. **(c)** Current densities for a Ag gate electrode with a work function of 4.5 eV, close to the work function of Au at 4.7 eV. **(d)** Current densities for a Pt gate electrode with a high work function of 5.9 eV result in considerably higher gate leakage currents for all the insulators compared. All graphics in this figure are adapted from [TKJ2].

Esaki model, that the impact of the metal work function on the calculated leakage currents can be easily investigated by recalculating the currents for varying gate metals. Thus, in Figure 6.10 (a) the tunneling current densities are shown as a function of the applied gate voltage for scandium contacts with a small work function of 3.5 eV. When using this gate contact material the tunneling current densities are particularly high for SiO_2 and hBN. As the work function increases to 4.3 eV in titanium in Figure 6.10 (b) or to 4.5 eV in silver in Figure 6.10 (b), the tunneling current densities decrease with the smallest currents being observed for gold contacts with a work function of 4.7 eV, as shown in Figure 6.9. For considerably higher work function metals like platinum at 5.9 eV in Figure 6.10 (d), the tunneling current densities are exceedingly high for all insulator materials compared here. Most importantly, the best case scenario is the usage of Au as a metal gate, as this corresponds to the smallest observed tunneling currents.

All comparisons shown here demonstrate that there is in general a shortage of insulators which provide sufficient leakage current blocking potential for continued down-scaling of

transistors and insulators. Among all insulators currently available, hBN is particularly ill-suited for being used as a scaled gate dielectric for *p*-type devices and shows a performance slightly worse than most insulators for *n*-type devices at operation voltages below 1.0 V and above this regime the current through hBN dramatically increases.

One possible solution to this lack of scalable insulators would be to change the operation regime and use smaller supply voltages where only steep-slope devices can operate. In conventional MOSFET devices the subthreshold swing of a FET cannot be smaller than the Boltzmann limit of 60mV/decade at room temperature, determining a minimum operation voltage of about 0.7 V for sufficient on/off current ratios. In order to overcome this limit the device operation principles must be modified. Approaches which could achieve this goal exploit a constrained injection energy window for charge carriers such as tunnel FETs [369], a non-monotonic variation around the Fermi energy in the density-of-states as an energy filter [46], or an insulator which creates a negative capacitance of the gate stack, such as a ferroelectric, thereby amplifying the surface potential of the channel [371]. All these steep-slope devices allow for a supply voltage below 0.5 V where also hBN could serve as a gate insulator. In addition, hBN can also be used for applications where tunneling through the layer is required as part of the device design, such as a tunneling barrier in a tunnel FET based on a graphene/hBN heterostructure [550].

7 Conclusions and Outlook

This thesis outlines a number of advancements to the current state-of-the-art in 2D material-based FETs. Based on the comprehensive experimental analysis of FET performance for both large-area FETs and nanoscaled FETs, which is accompanied by thorough physical modeling of device operation and degradation, we have gained several insights. Above all, the collected data suggests that, at the moment, the most critical obstacle towards large-scale industrial applications of 2D material-based FETs is the lack of suitable gate insulators.

Parallels can be drawn to the early days of solid state transistors in the late 1950s, where it was the lack of a stable semiconductor surface that prevented enhancement mode operation for FETs, a problem that was solved by thermally grown amorphous SiO_2 on silicon. Nowadays, 2D semiconductors offer in principle defect-free van der Waals surfaces, but unless they are combined with a suitable insulator that also provides defect-free crystalline surfaces, a high-quality van der Waals interface cannot be formed. In addition, the insulator needs to reduce charge trapping as well as effectively blocking currents and providing good stability for thin physical layers at high electric fields. As at the moment no insulating material fulfills all these criteria, current 2D material-based FET prototypes cannot realize their theoretically predicted potential and fall short in terms of performance, electrical stability, and reliability. Unquestionably, in comparison to the 1960s, the demands on the materials and technologies involved are much higher. At present, the goal is to fabricate transistors at the atomic scale, thereby coming close to the ultimate physical limitations. Therefore, new materials like 2D materials and new device concepts like tunnel FETs, cold source FETs, and ferroelectric FETs are explored. However, such fundamental modifications to the well-established processes give rise to numerous new questions and challenges. The overarching goal is to produce faster, cheaper and more reliable nanoelectronics to connect people. In this regard, this thesis makes a small contribution to the collaborative efforts of the research community to bring ultrascaled 2D material-based FETs closer to the market.

In the first part of this chapter, the main results of this thesis are summarized and the main conclusions highlighted. This part is followed by an outlook about open research questions and possible future steps.

7.1 Conclusions

As stated above, this thesis aims to contribute to the solution of a key problem for 2D material-based FETs, namely, to the identification of a suitable gate insulator for 2D FETs. Towards this end, first, clear criteria are developed in Chapter 4. Of these criteria, scalability is the first requirement suitable gate insulators for 2D transistors must meet. Thus, they need to provide excellent gate control at a small EOT while maintaining acceptable leakage current levels through these ultrathin layers. As a next requirement, the densities of electrically active interface traps and border traps in the gate insulator need to be considerably reduced. Finally, the third requirement summarizes the constraints caused by the technological integration of 2D FETs into circuits. In this context, uniform deposition of top gate insulators and tunable threshold voltages are needed as well as symmetric nMOS and pMOS transistors for CMOS integration.

Against this background, several selected challenges for insulators for 2D FETs are investigated in detail in this thesis. In Section 5.1, a comprehensive experimental analysis of the electrical stability and reliability of large-area 2D material-based FETs is presented based on both hysteresis and BTI measurements. These measurement methods provide two complementary views on the border traps that are electrically active in 2D FETs. These border traps are charge traps within the gate insulator that are located at a distance of up to 2 nm away from the interface. It was shown that two partially overlapping subsets of border traps cause the observed hysteresis and BTI. To be precise, the applied biasing voltages, biasing times, and operation voltages determine which subset of border traps is activated. Moreover, if the energetic location of the defect bands in the insulator is far away from the location of the Fermi level in the channel, charge trapping is considerably reduced.

Based on these insights, a novel stability-aware design strategy is suggested and verified in Section 5.1.3. This strategy aims to maximize the energetic distance between the location of the Fermi level in the channel and the defect bands in the gate insulator by carefully selecting the right combination of 2D semiconductor and insulator, or by shifting the graphene work function away from the defect bands via doping. It was revealed that in conventional amorphous oxides with broad defect bands, the hysteresis and BTI can be improved by one order of magnitude with a considerable Fermi level shift. However, it is expected that in crystalline insulators with much narrower defect bands, improvements by several orders of magnitude can be achieved already for small Fermi level shifts.

Further insights into the physics of the charge transfer processes to border traps in 2D material-based FETs were gained in a comprehensive analysis of RTN and TDDS at cryogenic temperatures down to 10 K, see Section 5.2. This analysis uses nanoscaled MoS_2 on SiO_2 FETs that have been fabricated by the author. Because of the small active channel area of these devices, single charge trapping events can be seen as discrete steps in the drain current. Based on the analysis of the capture and emission time constants and step heights of the charge traps, invaluable information about the atomic nature of the defects and the physical properties of the involved charge trapping processes are collected. It is observed that for cryogenic temperatures below 100 K, the time constants do not follow an Arrhenius law but instead

become temperature independent. These results demonstrate that, at cryogenic temperatures, the atomic rearrangement of the nuclei at the defect site is not mediated by phonons, but dominated by nuclear tunneling, as predicted by the non-radiative multi-phonon model. Therefore, charge trapping at border traps remains a central challenge for applications at cryogenic temperatures, such as quantum computing, high-performance computing, or space operation. From the experimental results described above, we conclude that improvements in the electrical stability and reliably of 2D material-based FETs require dedicated efforts to tailor the prevalence and activity of border traps in the system. This could be achieved via stability-aware device design or via material engineering of high quality crystalline van der Waals interfaces.

Our experimental findings are complemented by thorough physical modeling of the electrostatics of prototype 2D material-based FETs and charge trapping events therein. In Section 6.1, commercial drift-diffusion based TCAD models that are routinely used for silicon FET design, are adapted to FETs using MoS_2 as a channel material. This adaptation includes a thorough evaluation of the material parameters of this layered semiconductor, the implementation of a model for the Schottky barriers at the metal source and drain contacts, and the use of a well-established model for charge trapping at interface traps, as the interface trap densities are high in prototype MoS_2 FETs.

Based on the accurate reproduction of the electrostatics of MoS_2 FETs in a two-dimensional model, the hysteresis dynamics of these devices are analyzed in Section 6.1.3. These dynamics are explained to full satisfaction based on charge trapping events at border traps in the SiO_2 back gate oxide that are described using a non-radiative multi-phonon model. It is demonstrated that, as the sweep time for the entire hysteresis measurement is reduced, fewer border traps can contribute and the hysteresis width decreases. In a hysteresis measurement, only those border traps are activated which capture charges during the up-sweep but do not emit them before the end of the down-sweep. In this way, the modeling results shed light on the underlying physics, showing how the observed hysteresis width reflects the overall distribution of time constants of border traps and their bias activation.

After this in-depth analysis of charge trapping at border traps in the gate insulator, the requirement for maintaining low leakage currents through ultrathin gate insulators is studied in detail in Section 6.2. In particular, a theoretical lower limit of the gate leakage current density is established for a number of potential gate insulators at a small equivalent oxide thickness, as required by the current technology node. In this section, the ideal scenario is evaluated by calculating the direct tunneling currents through a defect-free structure, thus in real devices the leakage currents are expected to exceed these lower boundaries. In the comparison of leakage currents through various gate insulators, we focused on hBN, a layered insulator that is widely considered as the most promising gate insulator for 2D material-based FETs. However, hBN suffers from a small dielectric constant and small band offsets to the valence bands of most 2D semiconductors. Therefore, despite an unavoidable uncertainty in the effective masses for electronic transport orthogonal to the layered structure, calculations based on the semi-classical Tsu-Esaki model reveal that hBN is most likely unsuitable as a gate insulator in scaled pMOS devices. These trends are confirmed by a fully quantum mechanical

model of DFT calculations coupled to NEGF transport simulations. Throughout all scaling regimes, hBN is unsuitable for pMOS devices as gate stacks of six hBN layers or less cannot sufficiently block tunnel currents, rendering hBN unsuitable for applications in scaled CMOS. Thus, hBN can serve as a substrate or gate insulator only for those 2D nanoelectronic devices that do not require scaling, for example sensors or neuromorphic devices. Alternatively, hBN could be used in novel device concepts that allow for a considerable reduction of the supply voltage like cold-source FETs or tunnel FETs, where it could also serve as a tunnel barrier.

In summary, the high concentrations of border traps in amorphous oxides and the typically wide defect bands cause electrical instabilities during the operation of 2D material-based FETs and considerably degrade their reliability. In this work, a stability-based design approach was suggested that could be used to avoid defect bands in amorphous oxides. However, the defect bands in novel crystalline insulators like hBN, mica or CaF_2 are expected to be much narrower, allowing for more substantial and comparatively easily accesible stability and reliability improvements. Nevertheless, it was shown that hBN cannot satisfy the stringent scaling requirements for modern ultrascaled CMOS logic applications as excessive leakage currents flow through thin hBN layers. Therefore, the question regarding the best gate insulator for ultrascaled 2D material-based FETs cannot be answered yet. Promising candidates that need to be evaluated in the future are layered insulators aside from hBN, e.g. Mica or TiO_2, native oxides to 2D semiconductors, e.g. Ta_2O_5, HfO_2 or Bi_2SeO_5, or ionic fluorides, e.g. CaF_2, see Section 4.4.

7.2 Outlook

In the future, the performance of various gate insulators for 2D material-based FETs should be evaluated according to the criteria formulated here. Depending on the insulator analyzed, the challenges are different and for most insulator candidates the available data currently does not go beyond a few early proof-of-concept studies. For example, the widely used amorphous high-k oxide HfO_2 can block gate leakage currents well [TKJ2], and the ALD growth of HfO_2 as a top gate oxide was demonstrated on TMDs with PTCDA as a seed layer [359]. However, for the combination of MoS_2 and WSe_2 with HfO_2 as top gate oxide, considerable charge trapping at border traps is expected, as the band edges are aligned within the HfO_2 defect bands. Additionally, the interface of HfO_2 with vdW semiconductors is of poor quality and contains many interface traps. In contrast, an enhanced electrical stability would be expected for BP FETs or HfS_2 FETs using HfO_2 [TKJ3]. However, these predictions need yet to be verified. In addition, it remains unclear whether a single PTCDA layer at the interface can screen charge traps in the amorphous oxide or whether it can ensure a high mobility in the 2D channel despite the prevalent remote-phonon scattering in HfO_2 [412], see Section 4.2.1. Based on a similar notion, Agarwal *et al.* [559] have suggested to use a combined gate stack of hBN and HfO_2 as a gate insulator, thereby benefitting from the good van der Waals interface with hBN and simultaneously blocking the tunnel currents with HfO_2. However, there is yet no scalable fabrication method for such gate stacks in a top gated design. Furthermore, it remains to be seen whether a good trade off can be reached between low trap densities in the close vicinity to the 2D channel while maintaining an overall small EOT of the gate stack.

When looking for layered insulators that could satisfy all requirements for the gate stack based on a single material, only little is known about alternative layered insulators such as Mica or TiO_2. There are few proof-of concept devices using Mica as a gate insulator [476, 479] and no device demonstrations yet using TiO_2 [480]. Thus their scaling potential, the prevalent defect densities in these materials and options for top gate integration are unexplored. In comparison, native oxides to 2D semiconductors have been investigated in more detail. For example Bi_2SeO_5, the native oxide to the 2D semiconductor Bi_2O_2Se exhibits good device performance for top gated devices and allows for selective patterning of the oxide [443]. However, up to now, the use of this gate insulator was limited to the exotic semiconductor Bi_2O_2Se, that shows purely n-type operation. In addition, there is no information about charge trapping dynamics and defect bands in Bi_2SeO_5 or about the electrical stability and reliability of such devices. In a similar manner, if HfO_2 is used as a native oxide to $HfSe_2$, initial studies suggest high densities of border traps that cause inferior reliability of the FETs [441]. A promising candidate for a gate insulator to 2D FETs is the ionic insulator CaF_2 as a crystalline material that forms a quasi van der Waals interface with layered 2D crystals [TKJ7, TKJ6]. The electrical stability and reliability of MoS_2 FETs with CaF_2 as gate insulator is superior in comparison to other 2D based FETs [TKJ7, TKJ8], however hitherto only back gated devices have been fabricated. Thus, the top gate integration of CaF_2 is the central challenge for this material system.

In general, for all above-mentioned insulators, no single-defect studies have yet been performed. Up to now, all RTN and TDDS studies on 2D material-based FETs were performed on transistors using SiO_2 as a gate oxide [TKC6, TKJ14, 235], see Section 5.2. However, these methods are among the few experimental techniques that can provide direct information about the location and atomic nature of the dominant charge traps. Thus, it is expected that single defect studies on 2D FETs using HfO_2 or CaF_2 will reveal important insights into the location of the border traps both spatially and energetically. With respect to the modeling of 2D material-based devices, TCAD models can describe the impact of single defects at different locations throughout the channel, thereby locating the defects that were observed in single-defect studies. It should be noted that future studies should take the high anisotropy of the permittivity of 2D materials into account [360]. In addition, modeling based on both semi-classical TCAD models as well as NEGF can be used to evaluate the impact of short-channel effects on ultrascaled 2D FETs, devoting special attention to the role the insulator plays in effects such as fringing-induced barrier lowering in high-k dielectrics [560]. What is more, theoretical models can be used to analyze the impact of contact dimensions and geometries on the device performance of nanoscaled FETs.

Another research question concerns the tunnel currents through van der Waals gate stacks. For example, the tunnel currents through combined hBN/HfO_2 gate stacks have not yet been investigated. In addition, combinations of various TMDs and insulator candidates for 2D material-based FETs can be explored in terms of their respective leakage currents, verifying the most important combinations with a combined DFT and NEGF approach. Moreover, the tunnel current models could be extended to account for trap assisted tunneling via insulator defects. These models would be able to describe measured tunnel leakage currents, thereby gaining more information about the defect bands in novel insulators like hBN or CaF_2.

In summary, there are numerous open research questions that build upon the insights reported in this thesis. Future studies will hopefully shed more light on the question of suitable gate insulators for 2D nanoelectronics and provide further insights into charge trapping dynamics at border traps. Notably, while this thesis focuses on scaled FETs for CMOS logic circuits, many concepts can also be used in memory elements or sensors. For example, the sensitivity of the threshold voltage to the density of adsorbed gas molecules in bare-channel 2D FETs can serve as a sensing signal in highly sensitive gas sensors [561]. Alternatively, the large hysteresis in 2D FETs can be used in neuromorphic circuits where short gate pulses have been used to mimic neurotransmitter release [562]. Therefore, the understanding of charge trapping processes in 2D FETs developed within this thesis can be used to design novel 2D material-based nanoelectronic devices for promising future applications in various fields, among them sensors and neuromorphic computing.

A Estimation of the Doping Level in MOCVD grown MoS_2

As discussed in Section 2.1.2, MoS_2 films can be p-doped during MOCVD growth by introducing $NbCl_3$ powder as a precursor for Nb-doping at an upstream location to the growth substrate. In order to study the conductivity as well as the homogeneity of the sample doping, FETs based on doped MoS_2 samples were fabricated and characterized. For the sake of simplicity, a back gated device design with a global back gate, comparable to the layout shown in Figure 2.3 (a), was chosen using 90 nm of SiO_2 as a back gate oxide. Based on the measured transfer characteristics of 23 FETs, the approximate doping levels were extracted using equations of classical semiconductor theory, see Section 3.1.1. These calculations, that form the basis for the data shown in Figures 2.2 (d) and (e), are provided in the following in detail.

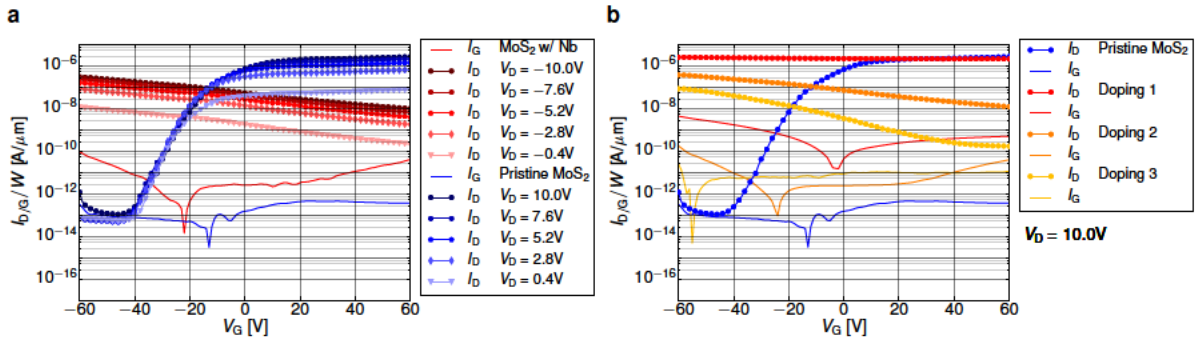

Figure A.1. a Transfer characteristics of MoS_2 FETs based on a pristine, undoped MoS_2 layer (blue) in comparison to a Nb-doped layer (red). Both samples were grown using MOCVD at 650 °C. Here, the drain current I_D is shown as symbols and the gate current as solid lines. In the doped FETs clear p-type behavior is observed, but also a considerable amount of shunting. **b** I_D (V_{GS}) characteristics of MoS_2 FETs based on a Nb-doped MoS_2 film, illustrating the variation of the doping levels across the film. All characteristics were measured on one MoS_2 film that was grown using MOCVD at 650 °C. Both graphics in this figure are adapted from [TKJ10].

In Figure A.1 (a) the transfer characteristics of MoS_2 FETs based on pristine and Nb-doped films are compared. It is apparent, that doping with Nb results in a pronounced p-type doping and a considerable loss of gate control over the channel. This weak gate modulation of the drain current is caused by shunting. Due to the heavy doping levels the gate partially loses control over the top part of the channel in the back-gated device configuration. Thus, this topmost portion of the semiconducting channel acts as a shunt. The thickness of this shunt

varies depending on the thickness of the MoS_2 layer used and on the doping density and is estimated in this particular FET to be around one monolayer of MoS_2. In this way, the shunting dramatically reduces the on/off current ratio from 10^7 to about 30.

However, the doping varies considerably throughout the a MOCVD grown MoS_2 film, as can be seen in Figure A.1 (b). As a result, the shunt current $I_{D,shunt}$, thus the minimum current level through the sample for the highest applied positive gate voltages, varies between 10^{-10} A/μm and 10^{-6} A/μm. These variations in the shunt current that span four orders of magnitude, indicate considerable variations in doping levels across the MoS_2 film. Subsequently, the shunt currents are used to estimate the doping level at different locations of the MOCVD grown MoS_2. First, the constant-criterion is used to determine the threshold voltage, see Equation 3.6, and the peak transconductance method is used to obtain an estimate for the mobility, see Equation 3.11. Furthermore, in a first order approximation, the following relation for the shunt current holds [563]

$$I_{D,shunt} = \mu \frac{W}{L} V_{DS} q N_A \left(t_{body} - W_{DM}\right) = \mu \frac{W}{L} V_{DS} q N_A t_{shunt}, \tag{A.1}$$

with the doping density N_A, the body thickness of the MoS_2 t_{body} and the depletion width W_{DM}. Here, the depletion width is given by [207]

$$W_{DM} = \sqrt{\frac{4\varepsilon_{semi}\, k_B T\, \log\left(N_A/n_i\right)}{q^2 N_A}}, \tag{A.2}$$

thus it depends on the doping density N_A, alongside the permittivity of the MoS_2 ε_{semi}, the temperature T and the intrinsic charge carrier concentration n_i. In consequence, the extracted doping density will strongly depend on the thickness of the semiconducting channel t_{body}, which was evaluated using AFM measurements to amount to about 6 atomic layers, thus 3.9 nm.

All in all, Equations (A.1) and (A.2) form an implicit equation for N_A, as the shunt current, the mobility, the drain bias and the MoS_2 thickness are known, that is evaluated numerically for the transfer characteristics measured on the MoS_2 flake. It should be noted, that this approximation works well for high doping levels and thick layer thicknesses. However, for the lower doping concentrations on an MoS_2 layer of only 3.9 nm thickness, the calculated thickness of the shunted layer t_{shunt} becomes unphysically small and is thus fixed to the thickness of one monolayer at 0.65 nm. Additionally, based on the doping density N_A, the percentage of Mo atoms x_{Nb} that were replaced with Nb during growth can be calculated using the relation

$$x_{Nb} = \frac{\sqrt{3}}{2} a^2 c N_A \tag{A.3}$$

with the lattice constants $a = 0.312$ nm and $c = 1.2$ nm of hexagonal MoS_2 [564].

For all characteristics shown in Figure A.1 (b), the calculated data and extracted doping densities are listed in Table A.1. From the extracted material parameters given in Table A.1, the values for I_{on} and μ are strongly impacted by the Schottky barriers at the Ni contacts to the

Quantity	Unit	Pristine MoS_2	Doped locat. 3	Doped locat. 2	Doped locat. 1
$I_{D,shunt} = I_{off}$	A/μm	10^{-13}	10^{-10}	10^{-8}	2×10^{-6}
I_{on}	A/μm	2.6×10^{-6}	8.2×10^{-8}	3.5×10^{-7}	2.4×10^{-6}
I_{on}/I_{off}	-	10^7	500	30	1
μ	cm^2/Vs	0.22	0.007	0.022	0.034
t_{shunt}	nm	0	0.65	0.65	2.2
W_{DM}	nm	3.9	3.25	3.25	1.7
N_A	cm^{-3}	-	4×10^{17}	10^{19}	4.7×10^{20}
x_{Nb}	%	-	0.004	0.1	5

Table A.1. Extracted data and calculated doping levels for the four characteristics shown in Figure A.1 (b). The doping is given for three different locations of a Nb-doped MOCVD grown MoS_2 film in comparison to an undoped MOCVD grown MoS_2 film.

MoS_2 channel and thus do not reflect the intrinsic material properties, see also Section 2.3.1. In the same way the doping levels N_A were calculated for 23 fabricated FETs on different locations of the Nb-doped MoS_2 flake and are shown in Figures 2.2 (d) and (e).

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List of Publications

Scientific Journals and Book Contributions

[TKJ1] S. Das, A. Sebastian, E. Pop, C. J. McClellan, A. D. Franklin, T. Grasser, **T. Knobloch**, Y. Illarionov, A. V. Penumatcha, J. Appenzeller, Z. Chen, W. Zhu, I. Asselberghs, L.-J. Li, U. E. Avci, N. Bhat, T. D. Anthopoulos, and R. Singh. "Transistors Based on Two-Dimensional Materials for Future Integrated Circuits." In: *Nature Electronics* 4 (2021), pp. 786–799. DOI: 10.1038/s41928-021-00670-1.

[TKJ2] **T. Knobloch**, Y. Illarionov, F. Ducry, C. Schleich, S. Wachter, K. Watanabe, T. Taniguchi, T. Müller, M. Waltl, M. Lanza, M. I. Vexler, M. Luisier, and T. Grasser. "The Performance Limits of Hexagonal Boron Nitride as an Insulator for Scaled CMOS Devices Based on Two-Dimensional Materials". In: *Nature Electronics* 4 (2021), pp. 98–108. DOI: 10.1038/s41928-020-00529-x.

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[TKJ18] **T. Knobloch**, G. Rzepa, Y. Illarionov, M. Waltl, D. Polyushkin, A. Pospischil, M. Furchi, T. Mueller, and T. Grasser. "Impact of Gate Dielectrics on the Threshold Voltage in MoS_2 Transistors". In: *ECS Transactions* 80.1 (2017), pp. 203–217. DOI: 10.1149/08001.0203ecst.

[TKJ19] X. Song, F. Hui, **T. Knobloch**, B. Wang, Z. Fan, T. Grasser, X. Jing, Y. Shi, and M. Lanza. "Piezoelectricity in Two Dimensions: Graphene vs. Molybdenum Disulfide". In: *Applied Physics Letters* 111.8 (2017). DOI: 10.1063/1.5000496.

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Conference Proceedings

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[TKC2] Y. Illarionov, **T. Knobloch**, K. Smithe, M. Waltl, R. Grady, D. Waldhoer, E. Pop, and T. Grasser. "Anomalous Instabilities in CVD-MoS_2 FETs Suppressed by High-Quality Al_2O_3 Encapsulation". In: *Device Research Conference - Conference Digest, DRC*. Columbus, OH, 2020, pp. 150–151.

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[TKC6] **T. Knobloch**, J. Michl, D. Waldhoer, Y. Illarionov, B. Stampfer, A. Grill, R. Zhou, P. Wu, M. Waltl, J. Appenzeller, and T. Grasser. "Analysis of Single Electron Traps in Nanoscaled MoS_2 FETs at Cryogenic Temperatures". In: *Device Research Conference - Conference Digest, DRC*. 2020, pp. 52–53.

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[TKC8] M. Gillinger, **T. Knobloch**, M. Schneider, and U. Schmid. "Harsh Environmental Surface Acoustic Wave Temperature Sensor Based on Pure and Scandium doped Aluminum Nitride on Sapphire". In: *Proceedings of Eurosensors*. Vol. 1. 10. Paris, 2017, p. 341. DOI: 10.3390/proceedings1040341.

[TKC9] Y. Illarionov, G. Rzepa, M. Waltl, **T. Knobloch**, J. Kim, D. Akinwande, and T. Grasser. "Accurate Mapping of Oxide Traps in Highly-Stable Black Phosphorus FETs". In: *2017 IEEE Electron Devices Technology and Manufacturing Conference, EDTM 2017 - Proceedings*. 2017. DOI: 10.1109/EDTM.2017.7947532.

[TKC10] **T. Knobloch**, G. Rzepa, Y. Illarionov, M. Waltl, D. Polyushkin, A. Pospischil, M. Furchi, T. Mueller, and T. Grasser. "Impact of Gate Dielectrics on the Threshold Voltage in MoS_2 Transistors". In: *Meeting of the Electrochemical Society (ECS)*. Vol. 14. National Harbor, MA, 2017, p. 837.

[TKC11] **T. Knobloch**, G. Rzepa, Y. Illarionov, M. Waltl, F. Schanovsky, M. Jech, B. Stampfer, M. Furchi, T. Muller, and T. Grasser. "Physical Modeling of the Hysteresis in MoS_2 Transistors". In: *European Solid-State Device Research Conference*. 2017. DOI: 10.1109/ESSDERC.2017.8066647.

[TKC12] G. Rzepa, J. Franco, A. Subirats, M. Jech, A. Chasin, A. Grill, M. Waltl, **T. Knobloch**, B. Stampfer, T. Chiarella, N. Horiguchi, L. Ragnarsson, D. Linten, B. Kaczer, and T. Grasser. "Efficient Physical Defect Model Applied to PBTI in High-κ Stacks". In: *IEEE International Reliability Physics Symposium Proceedings*. 2017. DOI: 10.1109/IRPS.2017.7936425.

Master Thesis

[TKT1] **T. Knobloch**. "Characterization and Physical Modeling of Degradation in MoS_2 Transistors". MA thesis. Technische Universität Wien, 2016.

Curriculum Vitae

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Academic Career and Positions

since 10/2016	Researcher (Universitätsassistent), TU Wien PhD thesis: *Understanding the Limitations of 2D Material Based Field-Effect Transistors Related to the Gate Insulator*, supervisor Prof. Dr. Tibor Grasser
05-11/2019	Visiting Scholar at Birck Nanotechnology Center, Purdue University, USA supervisor Prof. Dr. Joerg Appenzeller
10/2016	Master's degree in Microelectronics, TU Wien, with distinction Thesis: *Characterization and Physical Modeling of Degradation in MoS_2 Transistors*
10/2014	Bachelor's degree in Technical Physics, TU Wien, with distinction Thesis: *Characterization of Iridium, Tantalum and Aluminium Oxide Thin Films for Applications in High Temperature Sensors*

Main Areas of Research

Theresia Knobloch's main scientific focus lies on fabrication, experimental characterization, design and modeling of devices based on 2D materials. In this research field, she primarily studies the stability of 2D material-based field-effect transistors with a particular focus on nanoscaled devices and the role the insulators play for device performance. She has ample experience in the modeling of devices, in particular in TCAD modeling and model devel-

opment, electrical device characterization and cleanroom fabrication. At the institute for microelectronics, she coordinates public outreach activities like the open house day and actively engages in events like “Long Night of Research”.

Additional Academic Achievements

	Invited Speaker
in 07/2021	Ioffe Institute, St. Petersburg, Russia
in 10/2017	Meeting of the Electrochemical Society(ECS), National Harbor, Maryland, USA
	Awards and Scholarships
2021	IEEE Electron Devices Society PhD Student Fellowship
2020	Best Paper Award at the Device Research Conference, Columbus, Ohio, USA
2019	Marietta Blau Scholarship, Austrian Federal Ministry of Science
	Marshall Plan Scholarship, Marshall Plan Foundation
	Christiana Hörbiger Award, TU Wien
2018	Scholarship for Scientific Work Abroad, TU Wien
2017	Award of Appreciation for Outstanding Scientific Achievements for one of the 50 Best Diploma Theses, Austrian Federal Ministry of Economy and Research
	Study Award, SEW Eurodrive Foundation
	Faculty Price, Faculty of Electrical Engineering, TU Wien
2012-2016	Merit-based Scholarships (annual), TU Wien
	International Research Experience
05/2019 - 11/2019	Birck Nanotechnology Center, Purdue University, USA
	Visiting Scholar: *The Impact of Dielectric Defects on 2D FETs*
08/2018 - 11/2018	Birck Nanotechnology Center, Purdue University, USA
	Visiting Scholar: *MOSFETs based on 2D Materials*
02/2017 - 03/2017	Insitute of Functional and Soft Materials, Soochow University, China
	Visiting Scholar: *Reliability of Devices based on 2D Materials*
	Reviewing Activities
since 2019	ACS Nano, Applied Surface Science
since 2018	Journal of Applied Physics, IEEE Transactions on Electron Devices
since 2017	Journal of Mathematics in Industry, SISPAD Conference