DISSERTATION

Modeling of Defect Related Reliability Phenomena in SiC Power-MOSFETs

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Abstract

The quality of the interface between semiconductor and insulator material has always played a major role for the functionality of a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). This also applies to silicon carbide (SiC) MOSFETs which show superior properties when used as switches in power conversion applications. However, electrically active defects on an atomic scale located near the SiC/SiO_2 interface determine the stability of the device parameters and increase its on-state losses due to a perturbation of the electrostatics upon being charged. The kinetics of these charge transfer processes are strongly influenced by the applied bias and surrounding temperature, hence summarized under the term Bias Temperature Instability (BTI). While the total defect density at the interface has been significantly reduced, by e.g., the introduction of nitrogen-containing post-oxidation anneals, which led to improved channel carrier mobility and stability of the threshold voltage, the exact nature of these defects is still unknown. Another detrimental effect caused by oxide defects are enhanced gate leakage currents, which are enabled by the traps acting as charge transition centers, termed Trap-Assisted Tunneling (TAT) currents. Since both effects are widely accepted to be caused by inelastic tunneling processes, the underlying charge transfer reactions can be described by the Non-Radiative Multi-Phonon (NMP) model. While the application of this model has revealed many details of the charge transfer kinetics and led to the identification of a few potential defect structures in Si MOSFETs, its application to SiC MOSFETs has not been successfully demonstrated. One reason for this is the large defect density, which hampers defect parameter extraction by conventional methods. Therefore, a novel Effective Single Defect Decomposition (ESiD) algorithm is applied in combination with the reliability simulation framework Comphy to simulate the measured transient threshold voltage shifts caused by charge transfer at a large ensemble of defects, which is characterized in various lateral channel MOSFETs. The obtained defect parameters are then compared for their consistency over several SiC technologies and with those reported from ab-initio calculations for suspected defect structures. Additionally, a new two-state NMP based TAT modeling approach is presented in this work, including charge hopping between defects. This novel model is then applied to successfully explain TAT currents obtained in SiC/SiO_2 MOSCAPs. Further verification of the model with widely studied TAT currents measured employing capacitors based on ZrO_2 allows to draw conclusions about the nature of these charge transition centers in both binary oxides. A defect parameter comparison to those obtained from DFT calculations of models from a defect class, so called polarons, results

in excellent agreement, rendering polarons a likely defect candidate responsible for TAT. Finally, features of both reliability threats, BTI and TAT, are reasonably well explained by two-state NMP charge transfer kinetics in SiC-based MOSFETs. The extracted defect parameters suggest a few structural defects as the root-cause of reliability issues in SiC MOSFETs due to their consistency with ab-initio based parameter extraction.

Kurzfassung

Eine zentrale Rolle für die Funktionalität des Metal Oxide Semiconductor Field-Effect Transistors (MOSFET) spielt seit jeher die Qualität des Materialüberganges zwischen Halbleiter und Isolator. Das gilt auch für Silizium Carbid (SiC) basierte MOSFETs, welche herausragende Eigenschaften für die Verwendung als Schalter in Spannungsumrichtern mit sich bringen. Die Stabilität der Bauteilparameter wird dabei von mikroskopischen Defekten nahe dem SiC/SiO_2 Übergang beeinflusst, die sich elektrisch laden können, was zu einer Erhöhung des Leitungswiderstandes als Folge der elektrostatischen Störung führt. Die Kinetik dieser Ladungstransferprozesse wird dabei wesentlich von der angelegten Gate-Spannung und der Umgebungstemperatur beeinflusst, weshalb der Effekt als Bias Temperature Instability (BTI) bezeichnet wird. Obwohl die Defektdichte am Materialübergang durch einen Passivierungsprozess in Stickstoffmonoxid angereicherter Umgebung erheblich reduziert wird, wirken sich Defekte immer noch nachteilig auf die Lebenszeit von Transistoren aus. Trotz intensiver Forschung ist die chemische Struktur der elektrisch aktiven Defekte noch immer nicht geklärt. Eine weitere nachteilige Auswirkung von Oxiddefekten kann deren Rolle als Transmissionszentren für sogenannte Trap-Assisted Tunneling (TAT) Ströme sein. Beide Effekte, BTI und TAT, resultieren aus inelastischen Tunnel-Ladungsprozessen welche mit Hilfe der Non-Radiative Multi-Phonon (NMP) Theorie beschrieben werden können. Während dieses Model erfolgreich für die detailierte Beschreibung der Ladungstranferkinetik in Silizium basierten MOSFETs verwendet wurde und zur Identifikation zahlreicher struktureller Defektkandidaten geführt hat, blieb dessen Anwendung in SiC MOSFETs bisher aus. Einer der Gründe dafür ist die große Vielzahl und hohe Dichte an Defektstrukturen, die die Extraktion von Bauteil- und Defektparametern mit herkömmlichen Methoden erschweren. Aus diesem Grund wurde die sogenannte Effective Single Defect Decomposition (ESiD) für die Defektparameter Bestimmung in Kombination mit dem Zuverlässigkeitssimulator Comphy verwendet, um die gemessene zeitabhängige Schwellenspannungsverschiebung in verschiedenen lateralen MOSFETs zu reproduzieren. Die auf verschiedenen SiC MOSFET Technologien extrahierten Defektparameter werden anschließend mit Hilfe von Dichtefunktionaltheorie (DFT) berechneten Werten verglichen. Zusätzlich wurde im Rahmen dieser Dissertation ein neues zwei-Zustands-NMP Model zur Beschreibung von TAT Strömen entwickelt, welches den Ladungstransfer zwischen den Defekten berücksichtigt. Mit diesem Model können TAT-Ströme in SiC/SiO_2 MOSCAPs erfolgreich erklärt werden. Zusätzlich wird die Modellierung anhand von bekannten Tunnelströmen in Kondensatoren mit

Zirconiomoxid (ZrO_2) als Dielektrikum verifiziert. In beiden Oxiden lassen sich die Tunnelströme mit Defekten erklären, deren NMP Parameter exzellent mit jenen die sich aus DFT Rechnungen für sogenannte Polaronen ergeben, übereinstimmen. Zusammenfassend lassen sich beiden Zuverlässigkeitsphänomene, BTI und TAT, in SiC MOSFETs durch Ladungstransfers zu und von Defekten anhand des NMP Models erklären. Die dabei verwendeten Parameter können auf Konsistenz mit DFT Rechnungen geprüft werden, wodurch eine Eingrenzung auf einige wenige Defektkandidaten ermöglicht wird.

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List of Abbreviations

AER	Active Energy Region
BJT	Bipolar Junction Transistor
BTI	Bias Temperature Instability
CET	Capture Emission Time
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pumping
CV	Capacitance-Voltage
DFT	Density Functional Theory
DPI	Defect Probing Instrument
DT	Direct Tunneling
DUT	Device Under Test
EDMR	Electrically Detected Magnetic Resonance
eMSM	extended Measure Stress Measure
EPR	Electron Paramagnetic Resonance
ESiD	Effective Single Defect Decomposition
ESR	Electron Spin Resonance
FET	Field-Effect Transistor
FN	Fowler Nordheim
HCD	Hot Carrier Degradation
IGBT	Insulated Gate Bipolar Transistor
MEA	Multi-Exponential Analysis
MIM	Metal Insulator Metal
MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
MOSCAP	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MSM	Measure Stress Measure
NMP	Non-Radiative Multi-Phonon
OTF	On-The-Fly
PDA	Post Deposition Annealing
PEC	Potential Energy Curve
PES	Potential Energy Surface
POA	Post Oxidation Annealing
RTN	Random Telegraph Noise
SiC	Silicon Carbide
4H-SiC	4H-Silicon Carbide
SILC	Stress Induced Leakage Current
SIMS	Secondary Ion Mass Spectroscopy
SNR	Signal-to-Noise Ratio
SRH	Shockley-Read-Hall
TAT	Trap-Assisted Tunneling
TCAD	Technology Computer-Aided Design
TDDB	Time-Dependent Dielectric Breakdown
TDDS	Time-Dependent Defect Spectroscopy
WKB	Wentzel-Kramers-Brillouin
XPS	X-ray Photoelectron Spectroscopy

Chapter 1

Introduction

The 2021 Intergovernmental Panel on Climate Change (IPCC) [1] report clearly states the urgent necessity to achieve a climate-neutral energy budget within the next decades. Hence, the ever-growing market of renewable energy production will further gain importance in the near future. Not only solutions for a carbon-free energy production but also approaches for a more efficient grid transport and therefore power conversion is among the highest priorities to meet the requirements of climate-neutrality with at the same time increasing power consumption. Electrical power conversion primarily requires a transformation of the voltage level and frequency, which is achieved by time-division of the input signal and transferring the energy into passive elements, e.g. an inductive coil on the output side. This signal partitioning requires an electrical switch, which is commonly realized by a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) or an Insulated Gate Bipolar Transistor (IGBT). Despite the significant improvements of the conversion efficiency that have been achieved in such devices based on silicon substrates, inevitable limits in the reduction of static and dynamic switching losses, as a consequence of the material properties of Si, have to be faced. These limits have been identified decades ago [2] and alternative substrate materials have attracted the attention of scientists and industry. These are so called wide-band gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), that exhibit superior properties for power electronics to improve the conversion efficiency, have already made their way as substrate material into commercially available devices. Moreover, "exotic" substrate materials such as gallium oxide (Ga_2O_3) or diamond (C) promise further improvement in terms of power conversion efficiency and may fully replace Si-based power switches in the near future.

1.1 MOSFETs in Power Conversion Applications

The growing importance of renewable energy in total power consumption, as shown in the left panel of Figure 1.1, requires high efficiency for converting the voltage and frequencies at the generation and/or consumer site, as for instance at locally installed photo voltaic (PV) panels, to those required for the power grid. The task of finding the

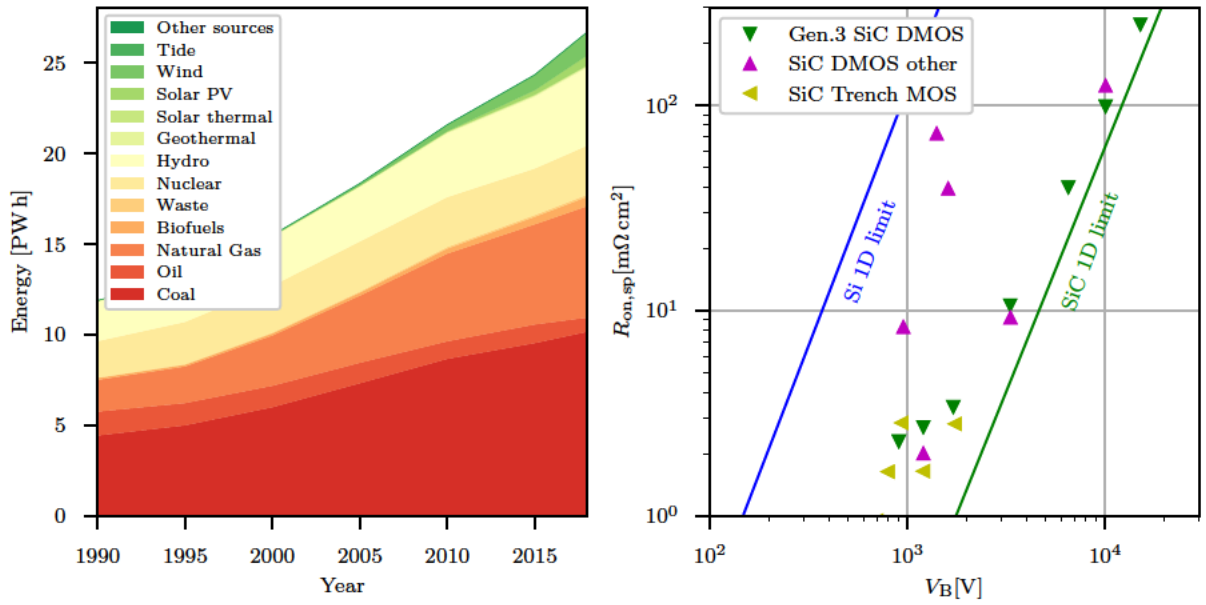

Figure 1.1. Electrical energy production **(left)** has more than doubled in the last 30 years, while renewable sources have increased their share of total energy production (data taken from [3]). Thus, advanced electronic systems become increasingly important. SiC MOSFETs when used as switches for power conversion circuits offer higher conversion efficiency **(right)**, as a lower static on resistance can be achieved for a given voltage class, as shown for the third generation SiC DMOS technology of Cree Inc. [4] and for other SiC-DMOS and trench design SiC-MOSFETs (reproduced from [5]).

most suitable material for power conversion switches depends on many aspects of the application (e.g., voltage/power class, switching frequency) and eventually is limited by production costs, i.e. the economical feasibility of the production line that is used for the desired substrate material. Therefore, various materials and their impact on device properties have been studied in the past decades. A selection of the most important properties for power devices in general and those of SiC in particular are presented in the upcoming sections.

1.1.1 Materials

The natural limit of the minimum static on-state losses of a power switch built from a semiconductor material is defined by the relation of the blocking voltage V_B, that it is able to withstand, while at the same time sustaining a minimum (ideal) specific on-state resistance

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon_s \mu_n E_C^3}. \tag{1.1}$$

A comparison of the natural limits for Si and SiC substrates together with already available SiC MOSFET technologies that exceed the Si limit is presented in Figure 1.1.

By considering Baliga's figure of merit [6]

$$\mathrm{BFOM} = \varepsilon_s \mu_n E_C^3 = \frac{4V_B^2}{R_{on,sp}}, \tag{1.2}$$

which relies on the material parameters electrical permittivity ε_s, the electron mobility μ_n and the critical field strength E_C, the static power handling capabilities of an ideal device employing different substrate materials can be compared. Additional to the static losses, in a switching mode device with area A the dynamic losses for a switching frequency f at gate bias V_G are added to the total conversion losses [2]

$$P_{loss} = \underbrace{I^2 \frac{R_{on,sp}}{A}}_{\text{static}} + \underbrace{C_{in,sp} A V_G^2 f}_{\text{dynamic}} \tag{1.3}$$

with the specific input capacitance $C_{in,sp} = \varepsilon_s E_C / \left(2\sqrt{V_G V_B}\right)$. With these quantities Baliga defined a high frequency operating device figure of merit, termed Baligas high frequency figure of merit (BHFFOM), by [2]

$$\mathrm{BHFFOM} = \frac{1}{R_{on,sp} C_{in,sp}}. \tag{1.4}$$

Johnson earlier formulated a FOM for the fundamental trade-off between a transition frequency within a channel length L and for a carrier saturation velocity v_{sat} with $f_T = v_{sat} / (2\pi L)$ and the power handling capability defined by the breakdown voltage across the channel $V_B = E_C L$ as [7]

$$\mathrm{JFOM} = f_T V_B = \frac{v_{sat}}{2\pi E_C}. \tag{1.5}$$

Besides the electrical material properties, heat management plays an important role in order to operate the power switch in a feasible temperature regime. Therefore, Keyes defined a figure of merit as [8]

$$\mathrm{KFOM} = \lambda \sqrt{\frac{c v_{sat}}{4\pi\varepsilon_s}} \tag{1.6}$$

with the specific thermal conductivity λ and the speed of light c to compare the heat dissipation limitations of the substrate material of power devices. Shenai *et. al* later proposed different thermal figures of merit depending on the heat dissipation coupling of the power device, rather than just taking bulk properties into account [9]. While Keys, Baligas, Johnsons and Shenais figures of merit mainly compare the bulk material properties of the substrate materials, Kim [12] tried to take the impact of the output capacitance in a conversion circuit with a certain input voltage into account to define a new high frequency figure of merit (NHFFOM) by extending the approach of Baliga [2]. Moreover, Huang [13] defined a figure of merit (HDFOM) for comparing unipolar

Par.	Si	GaAs	SiC	GaN	β-Ga_2O_3 [10]	C (diamond)	Unit
ε_r	11.7	12.9	9.76	8.9	10	5.7	1
E_G	1.12	1.42	3.26	3.39	4.85	5.5	eV
E_c	0.3	0.4	1	4	8	10	$MV\,cm^{-1}$
μ_n	1400	8500	900	1000	300	2000	$V\,cm^{-1}\,s^{-1}$
λ	1.5	0.55	3.7	2.1	0.2	6	$W\,cm^{-1}\,K^{-1}$

Table 1.1. Comparison of relevant parameters for substrate materials considered in power conversion devices, also shown in Figure 1.2 **(right)**. Si-based power MOSFETs are still widely manufactured, while SiC and GaN based devices steadily increase their market share in their respective voltage classes. Data taken from [10, 11].

switching devices based on the product of R_{on} and Q_{GD}, two quantities that can be obtained from measurements, assuming that the switching losses are dominated by the gate drain charge Q_{GD}. In the same work, also the Huang chip area FOM (HCAFOM) is defined as HCAFOM = $\varepsilon\sqrt{\mu}E_c^2$, whereby a higher FOM stands for less chip area necessary to sustain the same critical fields when conducting the same current density.

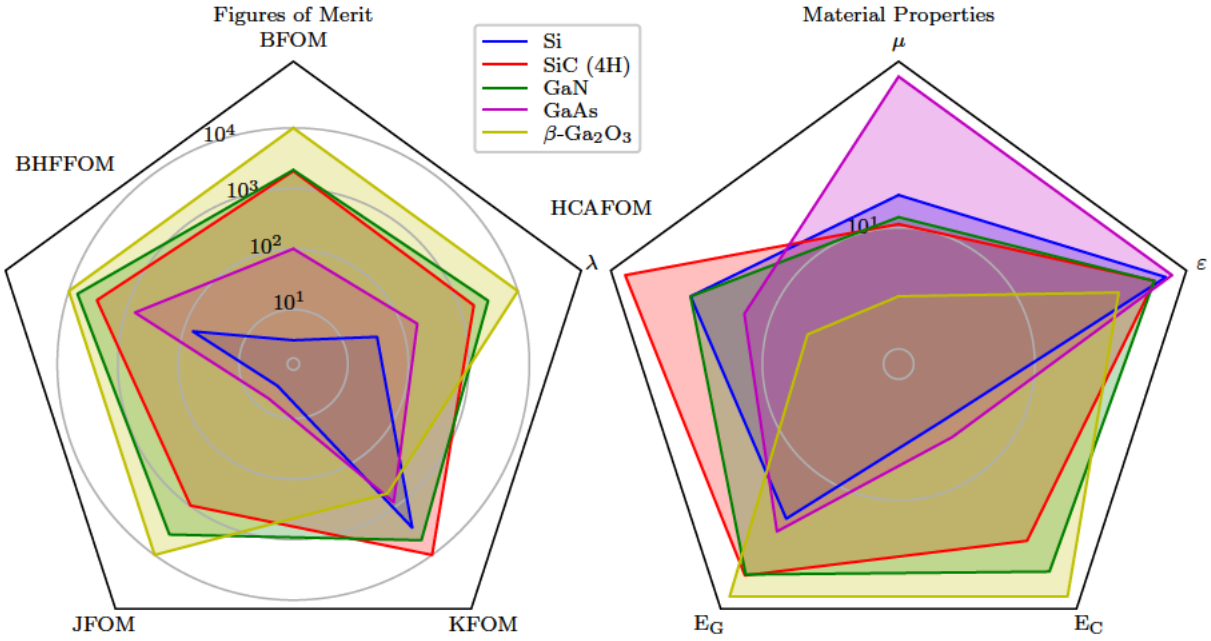

Figure 1.2. Figure of merits **(left)** and material properties **(right)** of different wide-band gap materials are compared. SiC and GaN as substrate materials offer advantages for applications in medium to high voltage and high frequency classes, respectively, and both have already been introduced in commercial devices. While novel materials such as β-Ga_2O_3 show record breaking FOMs, material processing is hindering their introduction in commercial devices, an aspect that is not taken into account by most FOMs. Note that for the spider diagram representation the FOMs and material properties have been normalized to the maximum value of each quantity (multiplied by a constant factor).

Most of the FOMs purely consider bulk material properties, as listed in Table 1.1 for mature conventional (Si, GaAs) and wide band-gap (SiC, GaN) as well as more exotic

semiconductor materials (C, β-Ga_2O_3), and do not take into account process-ability and properties arising from their compatibility to potential insulators. Apparently, SiC does not provide record breaking FOMs and also the bulk material properties are not exceeding those of e.g. GaN, except for heat conductivity, as shown in Figure 1.2. However, its ability to grow native SiO_2 and the availability of high quality substrates together with mature device processing techniques at reasonable cost outperforms GaN. Also, potential future candidates such as diamond within the medium to high blocking voltage class are far from large scale wafer level production at this point in time. For instance, β-Ga_2O_3 with its wider bandgap and higher critical field strength promises even better breakdown voltage to on-resistance ratio compared to both GaN and SiC. Therefore, it has been suggested as a suitable substrate material candidate for power devices within recent research works. However, p-doping of the material is particularly challenging due to the band-structure of β-Ga_2O_3 and has not been demonstrated yet [10]. With the largest bandgap and a high electron mobility as well as superior thermal conductivity, diamond is well suited for harsh conditions such as high temperatures and blocking voltages. However, the high chemical stability of the material leading to these properties poses severe challenges for device processing.

1.1.2 From MOSFETs to SiC Power Switches

A key step in the development of conventional MOSFETs has been the continuous improvement of the quality of the interface between the channel substrate material and the insulating layer. The electrically active "interface states" forming at the semiconductor-oxide transition region were the main reason that it took more than another three decades from Lilienfeld's discovery of the field effect [14] until the first working MOSFET was demonstrated [15]. Thus, bipolar junction transistors (BJT) were the first to be used for logic circuits. However, with the introduction of annealing process steps MOSFETs outperformed BJTs and stand today at the heart of almost every electronic application. The basic working principle of a MOSFET is to modulate the conductivity of a channel, i.e. the density of free minority charge carriers in a thin layer situated in between two contact regions with opposing doping concentration compared to the channel. These are termed source and drain contacts and the modulating terminal is known as gate contact. The "set-in" gate bias point for forming this inversion layer, which opens a percolation path between the source and drain terminals, is defined as the threshold voltage V_{th}. Interface traps and defects within the oxide in the vicinity of the channel, often referred to as near-interface traps (NITs) or border states, severely distort the device electrostatics and can lead to a drift of V_{th} when charged. By passivation of the Si surface and the interface to its stable native oxide SiO_2, stable device operation can be achieved which has led to the success of integrated Si/SiO_2 Complementary Metal Oxide Semiconductor (CMOS) processors.

An analogous development can be observed when looking at the history of the SiC MOSFET. Once SiC as bulk substrate material has been available in adequate quality for utilization in semiconductor devices in the 1990s [16, 17, 18], bipolar diodes were

available soon afterwards in 2001 [19]. However, it took almost another decade until the first commercially available SiC MOSFETs entered the semiconductor device market in 2010 [20]. Since then, SiC MOSFETs have gained significant market share in the sector for devices with 0.9 to 15 kV blocking voltage [4]. An important milestone for the sucess of Si-based MOSFETS has been the improvement of the Si/SiO_2 interface. Therefore, the interface properties have been studied over decades to optimize the interface carrier mobility and the threshold voltage stability by reducing the amount of electrically active defects, with e.g. forming gas anneals, in the vicinity of the channel. Such anneals have not shown to reduce the density of traps for SiC based MOSFETs with SiO_2 used as an insulator. Thus, efforts to reduce the defect densities have just recently been successful by improving the annealing process in nitrogen enriched ambient after oxide deposition [21]. Even though this led to a significant reduction of the SiC/SiO_2 interface defect densities, it is still the determining factor for power loss improvement, as scattering at the remaining interface and border states reduces the carrier mobility and thereby dominates R_{on}. Thus, to date large efforts towards a more detailed understanding of the electrical properties of the defects at the interface region, such as presented within this work, have been made. Before discussing the reliability threats caused by defects in more detail, the bulk SiC properties and MOSFET device fabrication will be outlined in the next two sections.

1.1.3 Silicon Carbide Material Properties

Carborundum, as silicon carbide is termed natively, is stoichiometrically composed by an equal number of Si and C atoms. Among the various polytypes in which SiC can crystallize [22], the four layered hexagonal (4H-SiC) polytype has been instituted in commercially available SiC power-switches. In the notation of Ramsdell, the polytype is denoted by the number of Si-C bilayers within the unit cell, shown in Figure 1.3, and the crystal system (H for hexagonal), hence 4H-SiC. Due to its superior mobility and breakdown values, the 4H- has ousted the 6H-SiC polytype as substrate material for power MOSFETs [23]. Therefore, this polytype is referred to throughout this work, unless otherwise noted. The stacking sequence of SiC is shown together with crystal planes and translation vectors, which are technologically relevant for modern MOSFET architectures, in Figure 1.3. A 1/2 hexagonality can be seen for the 4H polytype, with half of the bilayers crystallyzing on hexagonal sites within the unit cell. The two lattice constants for the 4H crystal structure are given by $a_0 = 3.0789$ Å, $c_0 = 10.082$ Å. The covalent Si-C bond has a binding energy of $E_b = 4.6$ eV, with a weak ionicity, as the valence electrons localize closer to the carbon atom (c.f. electro negativity: C: 2.5, Si: 1.8).

The electronic band structure of 4H-SiC exhibits an indirect bandgap of 3.26 eV [26] at room temperature from the Γ (top valence band) to M (minimum conduction band) point and features $M_c = 3$ conduction band minima within the first Brillouin-zone. The temperature dependence of the bandgap due to thermal expansion can be described by

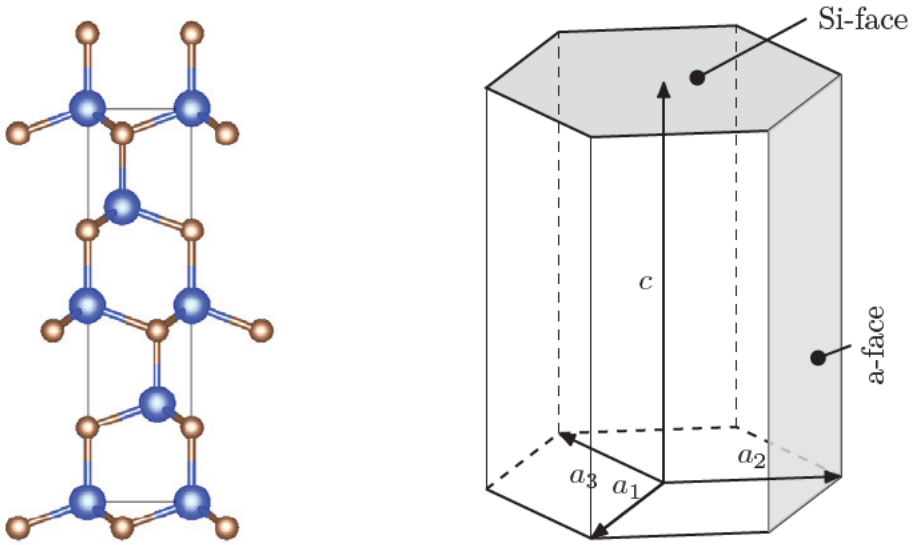

Figure 1.3. Unit cell of 4H-SiC **(left)** with equal number of C (brown) and Si (blue) atoms, reproduced from [24, 25], is shown together with technologically relevant crystal planes in SiC MOSFETs and translation vectors **(right)**. Note the Si-face (0001)-plane is typically the terminating surface in lateral and the a-face $(11\bar{2}0)$-plane in vertical MOSFETs.

the Varshni model [27]

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T+\beta} \tag{1.7}$$

with $\alpha = 3.5 \times 10^{-4}\,\mathrm{eV\,K^{-1}}$, $\beta = 1.1 \times 10^{3}\,\mathrm{K}$ and $E_G(0) = 3.285\,\mathrm{eV}$ [28, 29].

Due to the hexagonal crystal structure, the effective masses in the perpendicular and parallel planes to the c-axis exhibit a strong anisotropy. The parallel electron effective mass measured by cyclotron resonance is given by $m_{\parallel} = 0.31 m_0$, while the perpendicular mass is given by $m_{\perp} = \sqrt{m_{M\Gamma} m_{MK}} = 0.48 m_0$. Hole effective masses were extracted with $m_{\parallel} = 1.75 m_0$ and $m_{\perp} = 0.66 m_0$ [30, 31]. By applying the concept of density of states (DOS) effective masses for electrons and holes $m^*_{de,dh}$, the effective DOS in conduction and valence band is given by [32]

$$N_C = 2M_C \left(\frac{m^*_{de} kT}{2\pi\hbar^2}\right)^{3/2} \tag{1.8}$$

$$N_V = 2 \left(\frac{m^*_{dh} kT}{2\pi\hbar^2}\right)^{3/2}. \tag{1.9}$$

As the calculated effective DOS is not exactly proportional to $T^{3/2}$, the effective masses need to be modeled as temperature dependent too. The thermal DOS effective masses

calculated by using the $k \cdot p$ method [33] have been fitted with polynomials [34]

$$m^*_{\mathrm{de}}(T)/m_0 = m^*_{\mathrm{de}}(0) + a_{\mathrm{e}}T + b_{\mathrm{e}}T^2 + c_{\mathrm{e}}T^3 + d_{\mathrm{e}}T^4 \tag{1.10}$$

$$m^*_{\mathrm{dh}}(T)/m_0 = \frac{1 + a_{\mathrm{h}}T + b_{\mathrm{h}}T^2 + c_{\mathrm{h}}T^3 + d_{\mathrm{h}}T^4}{1 + e_{\mathrm{h}}T + f_{\mathrm{h}}T^2 + g_{\mathrm{h}}T^3 + h_{\mathrm{h}}T^4} \tag{1.11}$$

for the application in device simulations.

Moreover, the carrier mobilities show anisotropic values parallel and perpendicular to the c-axis, with about 20 % higher mobilities in the parallel direction. Note that at room temperature ionized impurity scattering is the limiting mechanism for mobility in bulk SiC and can be described by the Caughey-Thomas equation [35]

$$\mu_{\mathrm{e,h}} = \frac{\mu_{0,\mathrm{e,h}}}{1 + \left(\frac{N_{\mathrm{D}}+N_{\mathrm{A}}}{N_{\mathrm{e\,h}}}\right)^{l_{\mathrm{e,h}}}} \tag{1.12}$$

with $\mu_{0,\mathrm{e}} = 1020\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $\mu_{0,\mathrm{h}} = 118\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, $N_{\mathrm{e}} = 1.8 \times 10^{17}\,\mathrm{cm^{-3}}$, $N_{\mathrm{e}} = 2.2 \times 10^{18}\,\mathrm{cm^{-3}}$ and the doping ratio exponents $l_{\mathrm{e}} = 0.6$ and $l_{\mathrm{h}} = 0.7$. Note that these values are given for high purity SiC grown by epitaxy and will be decreased in bulk SiC grown by sublimation due to scattering at the increased numbers of point and stacking defects. At higher temperatures the acoustic phonon and inter-valley scattering become the dominant scattering mechanisms and the doping concentration dependence of the mobilities decreases.

1.1.4 Fabrication and Properties of SiC MOSFETs

A first step for the successful fabrication of commercially available SiC MOSFETs was the production of largely defect free SiC substrate wafers. A solution growth of large area bulk SiC ingots, which is the standard technique used for Si wafer production, imposes many challenges such as low solubility of C even at large temperature. Additionally, a high pressure (e.g. 100 bar) under inert Ar conditions is required and the reaction of the melt with the graphite crucible can not fully be omitted, which requires the development of other wafer production methods. Seeded-sublimation growth has been established to grow bulk ingots making reasonable quality SiC wafers of up to 150 mm diameter available. In this boule growth method, sintered poly-crystalline SiC is typically sublimed within a graphite crucible. The sublimed source species then move towards a seed crystal of the intended poly-type with high crystalline quality, due to a defined temperature gradient within the crucible. A surface reaction and crystallization step at the lower temperature seed crystal leads to the desired controlled poly-type crystal growth. The crucible is thereby heated to $T \approx 2300$ to 2400 °C, while the seed temperature is about 100 °C lower. Exact process control is required during crystal growth as defect formation energies for stacking, dislocation, and point defects are relatively low for the desired 4H-SiC polytype. Inert gas is introduced during the crystal growth to minimize impurity incorporation and by consideration of reaction kinetics

and thermodynamics, performance-limiting defects in the bulk SiC have been significantly reduced in the past [36, 37]. However, to achieve the required crystal quality, i.e. defect free poly-type preserved grown SiC with controlled doping and thickness, homoepitaxy has become an essential growth technique for the production of SiC devices that can compete with their Si-based counterparts. The lightly doped drift layer on top of the heavy doped substrate used as the drain contact is grown by chemical vapor deposition (CVD) technique employing silane (SiH_4) and propane (C_3H_8) or ethylene (C_2H_4) as precursors. The employment of a 4° off-axis angle on the substrate allows to perfectly rebuild the required stacking sequences of the hexagonal polytypes [38, 39].

With high quality substrates available, the most important process steps for the production of MOSFETs on SiC substrates are outlined further. High energy ion-implantation is used to form doping regions of n- and p-type conductivity, as a diffusion process is not applicable due to the significantly smaller diffusion constants of dopands within SiC [40] compared to Si. After the implantation, the damaged rough SiC surface is typically carbonized forming a carbon cap for subsequent mass production steps [41]. High-temperature post-implantation anneals are required for higher dose implantation for successful lattice recovery and doping activation. Aluminum is typically used as p-type dopand, while Phosphorus or Nitrogen are used for n-type doping. Al incorporates into the SiC lattice either on a hexagonal or cubic Si site with ionization energy $E_A \approx 200\,\text{meV}$, which results in only a fraction of dopands ionized even at room temperature. With $E_D \approx 60\,\text{meV}$ for both, P substituting a Si on a cubic site and N for C on a hexagonal site, these dopands can be considered ionized at room temperature at low concentration (i.e. $< 10^{16}\,\text{cm}^{-3}$). The fraction of ionized dopands is given by

$$N_D^+ = \frac{N_D}{1 + g_D \exp\left(\frac{E_D - E_F}{k_B T}\right)} \tag{1.13}$$

$$N_A^- = \frac{N_A}{1 + g_A \exp\left(\frac{E_F - E_A}{k_B T}\right)}. \tag{1.14}$$

with the degeneracy factors $g_{A,D}$ determined by the band-structure of the host material and the Fermi level E_F. $N_{A,D}$ denote the maximum electrically active doping concentration, i.e. the concentration of the fully ionized dopands.

A major advantage above other compounds, e.g. GaN, is that SiC can be thermally oxidized to form a high quality oxide, i.e. SiO_2, for MOS devices and a passivation layer for SiC surfaces. The dry oxidation process is described by the reaction

$$2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO. \tag{1.15}$$

A similar amount of bulk SiC as for Si, namely 46 %, is consumed for the SiO_2 growth, i.e. 10 nm SiO_2 are grown by consuming 4.6 nm SiC. It has to be mentioned that a dry thermal oxidation of SiC is time consuming and it takes more than 6 h to grow a 50 nm thick SiO_2 layer, as typically required for power switches, on the (0001)-terminated face at $T = 1150\,°\text{C}$ [42]. The oxidation process is strongly anisotropic and about ten times

faster on the a-face surface at the same T when compared to the oxidation of Si-face surfaces. This implies also strong oxide thickness variation along a trench MOSFET, i.e. smallest thickness on top and bottom of the trench and thicker at the sidewalls. Besides the strong anisotropy in growing rate at different surfaces, dry thermal growth leads to increased carbon incorporation at the interface as O_2 in-diffusion and CO out-diffusion are reported to be the rate limiting mechanisms in thick SiO_2 layers [42]. Oxide growth via atomic layer deposition (ALD) can resolve the anisotropy problem and additionally increases the interface stability [43]. However, it is an unfeasible process step for economic power device processing due to the long duration required to grow thick oxides. Therefore, the oxide deposition via a low-pressure chemical vapor deposition (LPCVD) employing tetra-ethyl-ortho-silicate (TEOS) as a precursor [44, 45] offers an alternative with the additional benefit of a reduced thermal budget at the gate stack.

However, as is the case for silicon MOSFETs, the interfacial strain and stoichiometric disorder at the transition region to the bulk amorphous oxide leads to electrically active unsaturated dangling bonds, e.g. $P_{b,0}$-centers for Si/SiO_2. In Si-MOSFETs, these defects are passivated by a forming gas (H_2) ambient annealing process step, thereby reducing the number of interface traps from $D_{it} \approx 10^{13}\,cm^{-2}\,eV^{-1}$ [46] to $D_{it} < 10^{10}\,cm^{-2}\,eV^{-1}$ [47]. Unlike for Si surfaces and the Si/SiO_2 interface, hydrogen passivation has not shown to significantly reduce the interface trap density for SiC/SiO_2 MOS structures [48]. Only the implementation of a Post Oxidation Annealing (POA) or Post Deposition Annealing (PDA) step in nitrogen enriched ambient has lead to a sufficient reduction of interface traps at the SiC/SiO_2 transition region and enough stability for surface passivation [20]. Typically, nitridation of the interface can be achieved in ambients containing nitrous oxide NO_2, nitric oxide NO or ammonia NH_3 at temperatures of above 1300 K. However, even with years of POA and PDA optimization, the $D_{it} \approx 10^{11}\,cm^{-2}\,eV^{-1}$ observed in SiC MOSFETs is still two orders of magnitude higher than in Si-technologies.

The high interface trap density also dominates the channel electron mobility due to electron scattering at these charged defects. In bulk 4H-SiC the dominant scattering mechanisms are acoustic and intervalley scattering for lightly doped ($N_D = 3.5 \times 10^{15}\,cm^{-3}$) regions. For increased doping densities of $N_D = 7.5 \times 10^{17}\,cm^{-3}$, as approximately used for channel doping concentrations, neutral impurity and invervalley scattering dominate at room temperature and above, resulting in an electron mobility of about $\mu_e \approx 400\,cm^2\,V^{-1}\,s^{-1}$ at room temperature, as extracted by Hall measurements and theoretical calculations [49]. This value decreases to about $50\,cm^2\,V^{-1}\,s^{-1}$ at a temperature of 100 K. However, as shown in Figure 1.4, when extracting mobility values from $I_D(V_G)$ characteristics at different temperatures for lateral (Si-face) MOSFETs, an opposing trend is observed, with increasing Ghibaudo mobilities [50] for higher T at significantly smaller absolute values. This behavior can mainly be explained by reduced Coulomb scattering at higher T, due to less interface charge trapped [51]. Also, a strong correlation of the reduced mobility with large interface trap densities has been extracted

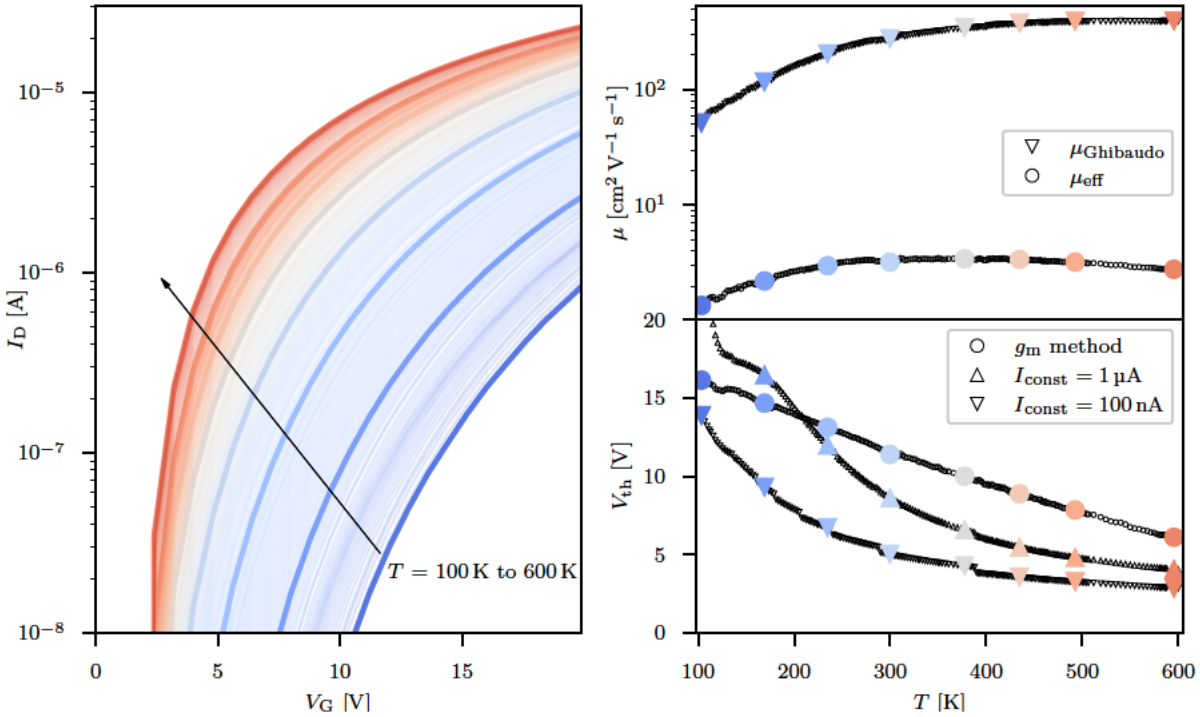

Figure 1.4. $I_D\,(V_G)$ characteristics for lateral Si-face (0001) n-MOSFETs with L=8 µm, W=100 µm and d_{ox} = 70 nm gate oxide with NO-POA for varying temperature in the range of 100 to 600 K **(left)**. The channel mobilities **(top, right)** are extracted by the method of Ghibaudo [50] and with the effective mobility equation [23]. The threshold voltage is extracted by a constant current method and the maximum g_m method **(bottom, right)**.

on different SiC surface termination planes at the interface to SiO_2 [23]. Thus, it has been revealed that the a-face surface shows larger mobilities compared to the Si-face, due to reduced interface trap densities close to the SiC conduction band edge [52]. Therefore, UMOSFET (or trench) architectures with a vertical channel along the a-face crystal plane, contrary to DMOSFETs with channel planes along the Si-face as shown in Figure 1.5, have been introduced by manufacturers recently.

Additionally, channel counter doping by donor incorporation (for n-channel MOSFETs) has been studied extensively, with e.g. N, P, Sb and Ba incorporated in a thin layer at the SiC/SiO_2 interface [53, 54]. The effect of these thin counter-doping layers is a electrostatic potential screening that leads to smaller field strengths required to build up the same inversion layer carrier density and also less surface scattering. In turn, higher low field channel mobilities can be observed, with diminishing effect at higher fields [53].

1.2 Reliability of MOSFETs

As outlined in the previous section, the introduction of the forming gas anneal has established a process step to enable the passivation of the majority of interface defects between bulk Si and amorphous SiO_2 (a-SiO_2), allowing the fabrication of highly stable MOSFETs. However, with the continuous down-scaling of CMOS transistors to

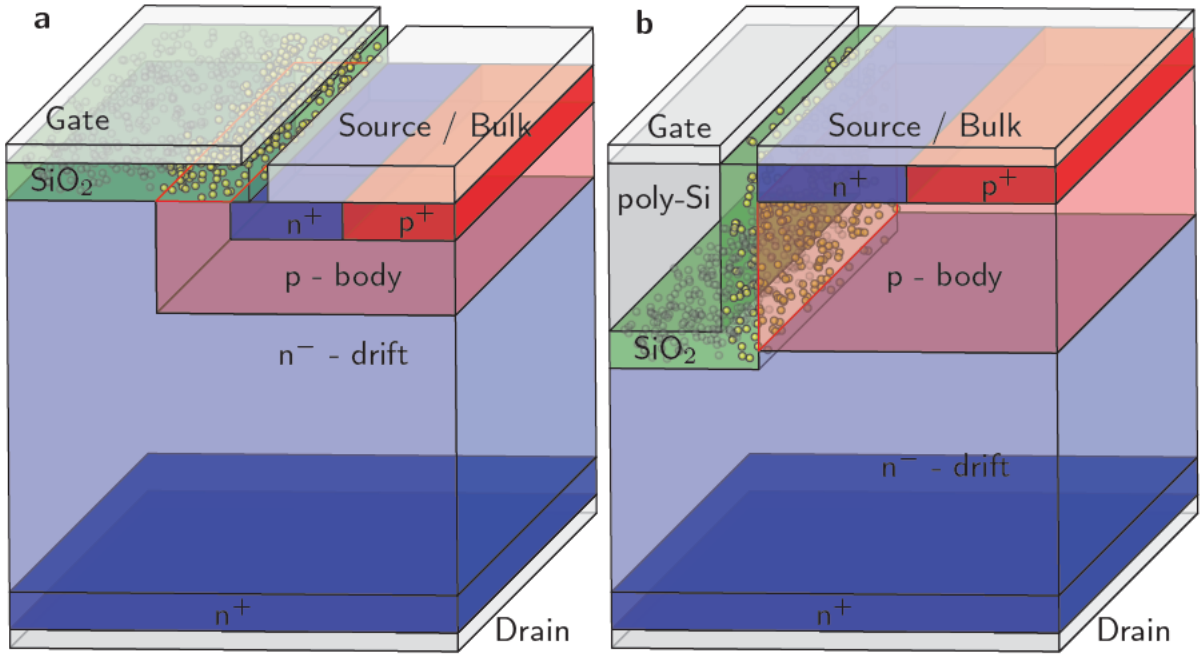

Figure 1.5. Sections of a DMOSFET (a) and an UMOSFET (b) are shown with cuts along the vertical symmetry axis of the devices. A tens of nm thick oxide is deposited on the trench sidewalls. The channel surface area along the SiC $(01\bar{1}2)$ plane in the trench case and along the (0001) plane in the DMOSFET case are highlighted in red. While highest channel mobility values are reported along the vertical interface orientation, charge trapped at interface and bulk-oxide defects, schematically indicated by yellow balls, severely reduce channel mobility compared to bulk values at both surfaces. In order to simplify the device representations, details such as passivation doping and correct aspect ratios are spared out.

a few nanometer channel length and only a small number of atomic layers thin gate dielectrics, the impact of charges captured at single electrically active defects located in the vicinity of the channel has become more pronounced. Due to the perturbation of the electrostatics upon charge capture, a single defect can eventually lead to failure of a MOSFET. The device parameter alteration effects due to these charge trapping events are summarised under the term Bias Temperature Instability (BTI). Next to BTI, enhanced electric field strengths in the lateral channel direction from the source to drain contact can lead to breakage of previously passivated dangling bonds. This bond breakage is a result of carriers with high kinetic energies scattering at the interface region, thereby creating defect states which then can capture and emit charge. Thus, the mechanism is referred to as Hot Carrier Degradation (HCD). Also, the effect of carriers tunneling through the insulating layer via hopping at pre-existing oxide defects, termed Trap-Assisted Tunneling (TAT) leads to enhanced leakage current resulting in additional power losses. Furthermore, as a consequence of TAT, defects within the bulk oxide can be created or high energetic carriers multiply due to impact ionization at large stress oxide field strengths. These additional leakage current following from these events are referred to as Stress Induced Leakage Current (SILC) and eventually lead to oxide breakdown. This failure mechanism is typically characterized by Time-

Dependent Dielectric Breakdown (TDDB) experiments. In the following, the role of BTI, gate leakage currents and HCD on the reliability of MOSFETs will be briefly outlined and the state of the art of research on these topics will be discussed.

1.2.1 Bias Temperature Instabilities

The alteration of the characteristic parameters of a MOSFET, e.g. flat band voltage V_{fb}, threshold voltage V_{th}, carrier mobility μ and sub-threshold slope SS, is known to be accelerated by enhanced temperature and gate bias stress. Therefore, these deviation phenomena have been collected under the term Bias Temperature Instability (BTI) [55]. BTI has been first described in the late 1960s by Miura *et. al* [56]. The stabilization of silicon surfaces [57] was the main research focus at that time, and the first BTI characterization attempts have been related to the mechanisms of ion impurity diffusion and thermally assisted tunneling [58, 59]. The main features observed were the power-law like development of the shifts of the threshold voltage based on empirical parameters, i.e. a time exponent n of about 0.2, thermal activation with activation energies up to 0.2 eV and voltage acceleration with exponents m in the range of 2 to 3 [60, 61]. Based on these observations, an expression for ΔV_{th} was given by [60]

$$\Delta V_{\mathrm{th}}\left(t, V_{\mathrm{G}}, T\right) = A t^{n} V_{\mathrm{G}}^{m} \mathrm{e}^{\frac{E_{\mathrm{A}}}{k_{\mathrm{B}} T}} \tag{1.16}$$

with a constant prefactor A and the activation energy E_{A} as fitting parameters. This method is easy to apply and is therefore still widely used, however, it fails to connect the degradation with the underlying physical mechanisms and additionally implies an infinite degradation trend because no saturation of the ΔV_{th} is considered. Moreover, the expression was derived from observations of negative BTI (NBTI) in Si-based pMOSFETs and cannot be generally applied to positive BTI (PBTI) or BTI observations on different technologies. For example, if more than one dominating trapping mechanism is prevalent, different slopes for the time evolution of ΔV_{th} may be observed which cannot be captured by this simple model. Therefore, in the past decades more sophisticated models have been developed to describe the underlying physical mechanisms more accurately. Heiman *et. al* connected threshold voltage shifts in Metal Oxide Semiconductor Capacitor (MOSCAP)s to charge trapped in the oxide [62], applying a Shockley and Read like kinetic statistics [63]. This modeling approach, however, only considers elastic tunneling of charge carriers from the channel to the defect. From the 1970s on, also reaction and diffusion limited regimes of the NBTI degradation were frequently proposed to originate the effect [64, 65]. In the latest version of this model, interface defect creation at high oxide field strengths has been proposed. This stems from hydrogen that is released causing additional dangling bonds at the interface (reaction), followed by hydrogen diffusion and accumulation in the oxide (diffusion) [66]. Since direct release of hydrogen is energetically unfavorable, a more realistic approach supported by DFT calculations suggests the release of hydrogen from a reservoir, e.g.

dopands in the Si substrate, which can then lead to depassivation of the interfacial Si-H bonds [67].

After correlating 1/f noise with discrete RTN signals in small area MOSFETs as discovered by Ralls *et. al* [68], a different approach to a reaction-diffusion model was presented by Kirton and Uren, who modeled the single defect charge transitions in the context of the Non-Radiative Multi-Phonon (NMP) framework [69, 70]. Tewksbury later first modeled threshold voltage shifts in MOSFETs applying the NMP theory to charge transitions involving oxide defects [71, 72]. Both, RTN and V_{th} shifts are therein explained by an inelastic tunneling process at pre-existing oxide defects. It took more than another decade until Grasser's two stage model [73] based on [74] was the first attempt to model both, a recoverable and a permanent component of BTI as observed in Si/SiO_2 systems. The recoverable part (stage 1) is explained by the formation of E′-centers from oxygen vacancies which can be charged and discharged. The permanent part (stage 2) is described with a 3-state model and caused by the de-passivation of $P_{b,0}$-centers triggered by charged E′-centers.

Further experimental observations on charge capture and emission events of single defects in small area devices such as Time-Dependent Defect Spectroscopy (TDDS) [75] studies and Random Telegraph Noise (RTN) [76] measurements initiated the refinement towards a four-state defect model for the recoverable component, which is able to explain both single charge transfer events in small area and the superposition of such in a defect ensemble in large area devices [77, 78]. This extension allowed for the description of phenomena like fixed/switching traps [79], and anomalous, temporary and reversal RTN [80]. The explanation of such details in RTN, i.e. charge trapping kinetics at a single defect, requires the existence of meta-stable defect states, which has been shown to be consistent with ab-initio studies for a number of suspected defect candidates [81]. Therefore, besides charge trapping is still not accepted as the unique mechanism causing BTI [82], the NMP model has provided deep physical insight into charge trapping as the origin of BTI.

BTI on SiC power MOSFETs has been characterized early after the development of wide-bandgap devices, with a focus on the time-dependence after bias-stress [83, 84] and its temperature dependence [85]. These works mainly extracted ΔV_{th} after bias stress as a function of the stress time by evaluating the V_{th} based on post stress $I_{\text{D}}\,(V_{\text{G}})$ measurements, thereby acknowledging the strong read-out time dependence of V_{th} after a stress phase within in their measurements. Later Okayama *et. al* [86] discovered an accelerated recovery when negative bias stress is applied after a positive stress phase. This mechanism can be explained by reduced emission times of previously trapped electrons during the negative bias phase. Reduced ΔV_{th} was also observed at elevated T, speculating that this effect evolves from ion diffusion [85], thereby neglecting the possibility of accelerated recovery at higher T [87]. The role of nitrogen passivation in NO containing ambient leading to an improved interface stability, i.e. less electron charge trapping, has been also studied [88] and the first structural defect candidates, i.e. interface states with more than 0.6 eV below the SiC conduction band together with

nitrogen related defects and oxygen vacancies, have been proposed [89]. Switching bias stress experiments for equal positive and negative bias revealed negative V_{th} shifts and therefore higher stability of trapped holes compared to a unipolar bias stress [90]. While comparisons between BTI in Si and SiC MOSFET are drawn frequently and might be valid due to the same nature of oxide defects [CSC1, CSC2], it was also emphasized that the interpretation of BTI measurements with state-of-the-art characterization methods developed for Si MOSFETs can be misleading [91, 92, CSJ1] when applied to SiC MOSFETs due to the wide distribution of the defect capture and emission time constants. Puschkarsky *et. al* conducted detailed BTI experiments under AC and DC gate bias stress, revealing accelerated temperature recovery [93] leading to seemingly less degradation at increased T. Furthermore, an accurate model to reproduce the extracted charge trapping kinetics with activation energy maps has been demonstrated [94, 87]. Additionally, recently a frequency independent switching cycle dependence of ΔV_{th} at bipolar gate bias operation in trench MOSFETs has been reported [95, 96, 97], however, not been explained by a physical mechanism. Note that a similar effect has been noticed in Si-based MOS devices employing SiO_2 as an insulator before and has been explained by the gate-sided hydrogen release model [98, 99].

Besides the detailed experimental studies conducted to characterize BTI in SiC MOSFETs for more than a decade, a physical defect-centric modeling approach to consistently describe the charge trapping mechanisms at the device level has not been presented so far. This gap from experimental observation to device modeling with defect bands that can be compared to parameters obtained by ab-initio methods from defect candidates is aimed to be narrowed down within this thesis [CSC1, CSJ2, CSC3].

1.2.2 Gate Leakage Currents and Oxide Breakdown

The charge blocking capability under electric fields of an ideal insulator within a MOSFET is intrinsically limited by its band offsets, i.e. the energetic barriers defined by the conduction and valence band edges of the substrate to those of the insulator, as well as the thickness of the dielectric layer. With ongoing scaling of insulators in CMOS technology Fowler Nordheim (FN) and direct tunneling (DT) currents, a result of charge carriers being able to tunnel through the energetic barrier given by the insulator, lead to detrimental on- and off-state losses. This intrinsic limitation can further be decreased by the presence of charge traps in real devices. Next to the capture of charge in the oxide and the resulting perturbation of the electrostatics across the MOS structure (c.f. BTI), defects in the insulator can also act as charge transition centers between the channel and the gate electrode. This so-called Trap-Assisted Tunneling (TAT) emerges from the same inelastic charge tunneling mechanism as in the case of BTI as will be outlined in the following.

Conduction via defects within the band gap of a semiconductor material acting as transition or recombination centers have been early studied and described by Mott [100]. The modeling efforts have later been extended by Miller and Abrahams to describe charge hopping in doped crystalline semiconductors [101]. While these early modeling

approaches considered purely elastic tunneling processes, Schenk *et. al* developed a model for defect with deep trap levels to band transitions accompanied by a multi-phonon relaxation [102], which was later extended by Herrmann *et. al* to model leakage currents through MOSFETs used for memory applications [103]. This model represents to date the core of most TAT modeling approaches based on NMP theory [104, 105, 106, 107]. Later, the TAT model of Schenk *et. al* has been further refined and extended to model thermally activated leakage currents through high-κ dielectrics used in MOSFETs by the group of Larcher [108, 109, 110, 111]. It should also be noted that a full quantum mechanical description of TAT currents within the NMP theory, as presented e.g. in [112, 113, 114], is most rigorous and necessary at for instance cryogenic temperatures [115]. However, its application on a device level simulation is often prohibitively expensive due to its large computational cost and often not necessary within the typical device operating temperature range, as will be discussed in Chapter 4.

In SiC MOS structures, thermally activated gate leakage currents below the FN regime have been observed recently [116, 117, 118] and were suspected to be trap-assisted with further conduction to the insulator conduction band [119, 120]. Thereby, a "sweet spot" of a defect band in spatial and energetic dimension enables this current conduction via traps. A close investigation of this hypothesis by physical modeling of these charge transitions will be presented within this thesis.

Increased FN, DT, and TAT currents at high stress oxide fields can further lead to defect creation by high energetic carriers, e.g. impact ionization [121] within the oxide. The resulting increased defect density following the oxide field stress further exaggerates gate leakage currents, hence termed Stress Induced Leakage Current (SILC) [122, 123]. It was already discovered in the 1980s that the resulting current was caused by thermally assisted tunneling from the channel to newly created defects [124, 125, 126]. Thereafter, the ongoing oxide degeneration eventually leads to a breakdown of the insulating capability by forming permanently conducting filaments, which is typically characterized by transient current measurements at increased bias and temperature stress within the TDDB method. Already in 1973, defect creation was suggested to be the responsible mechanism for TDDB, with a distinct oxide thickness dependence, predicting a stronger impact for thinner oxides [127]. While modeling attempts have focused on impact ionization for both SILC and TDDB [128, 129], the structural reconfiguration of defects could also explain the formation of leakage paths in the oxide and was able to explain correlation of single steps in gate tunneling currents and drain currents [130].

1.2.3 Hot Carrier Degradation

Contrary to BTI, the more permanent device parameter (V_{th}, μ, SS) alteration due to HCD is attributed to defect creation at the Si/SiO_2 interface in Si-based MOSFETs. While the effects of BTI are extracted at high gate and low drain bias, which leads to a uniform oxide field distribution and low energetic carriers across the lateral MOSFET channel coordinate, HCD is typically characterized at the high drain bias and low gate bias regime, as shown in Figure 1.6. In this regime highly energetic, hence termed

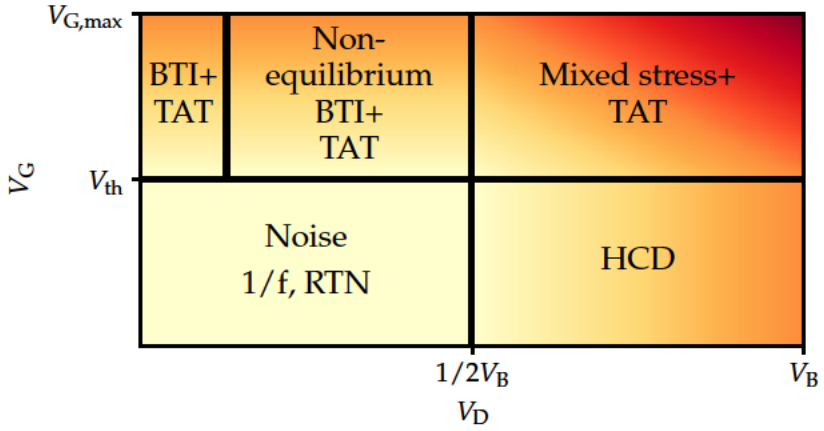

Figure 1.6. The different reliability mechanisms are shown for their relevance over the V_G and V_D regimes. Contrary to BTI which is typically studied for small V_D and enhanced V_G, HCD is observed at the opposite bias regimes, i.e. small V_G at large V_D. For both, small V_G and V_D, it is possible to characterize RTN in small area, and 1/f noise in large area devices, respectively. A mix of HCD and BTI is observed if both terminal biases are increased above their nominal operation values. Figure adapted from [131].

"hot" carriers, can exchange energy with the surrounding heat bath, i.e. excite certain phonon modes, which in turn can lead to the breakage of the Si-H passivation bond at the interface and therefore the creation of electrically active amphoteric dangling bond defects, the so called $P_{b,0}$-centers. As has been shown by Jech *et. al*, utilizing ab-initio calculations, this process needs to overcome high energetic barriers and thus can be explained by a resonant phonon mode excitation caused by non-equilibrium energetic carriers [132]. Also, the effect of high energetic non-equilibrium carriers in the interaction with oxide defects at BTI stress conditions has been investigated, resulting in a unified parameter free model for both BTI and HCD (mixed-mode) regimes [131]. The work of Jech *et. al* emphasized the importance of considering HCD and BTI for an accurate description of the Si/SiO_2 MOSFET degradation over typical device lifetimes.

While the impact of HCD in Si-based MOSFETs on device degradation is undisputed, only little attention has been paid to this effect in SiC MOSFETs. First studies on the effect of HCD stress in SiC MOSFETs revealed changes in the photon emission spectra of the investigated devices [133]. However, it was not possible to extract small relative changes of interface defect densities at already large absolute levels with electrical measurements after HCD stress. With the introduction of more stable NO annealed devices, a significant change of defect densities was observed after HCD stress by performing Charge Pumping (CP) measurements [134]. A clear identification of a defect candidate at the interface such as the $P_{b,0}$-center in Si/SiO_2 MOS structures or K_N at the insulator/Si interface of SiON devices [135] was not possible by Electrically Detected Magnetic Resonance (EDMR) measurements [136]. However, an N related defect was suggested to be responsible for the observed increase in the EDMR signal following hot-carrier stress. Determination of the HCD and the role of interface bond breakage in SiC MOSFETs is not as straight forward as in Si-based devices due to the

different nature of the interface and a multitude of possible defect configurations and therefore remains unclear to date [137].

1.3 State of the Art, Motivation and Outline

With the application of the NMP theory for oxide and interface defects in MOS devices in combination with device simulation in modern TCAD frameworks, charge trapping has been identified as the main mechanism responsible for BTI as well as TAT in mature Si based technologies. The investigation of single charge transfer events in small area devices allowed to consistently link these reliability threats to RTN and potential defect candidates that are responsible for charge trapping have been identified by parameter comparison with those obtained from ab-initio calculations. With many electrically active defects at the SiC/SiO_2 interface and an increased number of potential defect candidates due to the enhanced stoichiometric complexity compared to Si-based MOSFETs, electrically measured shifts of the threshold voltage ΔV_{th} have not been linked to defect parameters and compared with such derived by ab-initio methods for SiC based devices yet. BTI in SiC MOSFETs, so far, has only been described by empirical power-law interpolation, completely lacking a physical interpretation. A more advanced approach by using activation energy maps can also not connect BTI to a specific physical mechanism and therefore create a link between the data and a potential defect candidate even though charge trapping is widely acknowledged as the main reason for BTI in SiC MOSFETs.

Therefore, in this work, BTI as well as TAT observed in different SiC/SiO_2 MOS structures is characterized and reproduced by employing an efficient simulation framework with a physical charge trapping model. The obtained defect parameters are then compared to those calculated by ab-initio methods.

This Chapter 1 has provided an overview of the benefits of using SiC as substrate material in power MOSFETs at medium to high voltage classes by laying out its material properties. SiC MOSFET processing and state of the art architectures are briefly discussed, followed by the introduction of the most relevant reliability threads in MOSFETs in general and in particular due to the detriments of the SiC/SiO_2 interfacial region compared to the mature Si/SiO_2 system.

In Chapter 2 of this work, experiments to extract the charge transfer kinetics by electrical characterization methods are discussed with a special focus on the peculiarities that arise when applying methods established in Si technologies to SiC MOSFETs.

Chapter 3 contains an overview of defect candidates that have been identified in both bulk oxide and the transition region to bulk SiC with ab-initio methods. Suspected defect candidates that are located in the transition layer between these two materials include such that potentially form due to the introduction of N containing precursors during the interface annealing process step.

Within Chapter 4, the NMP model, which has widely been established for describing charge transfer reactions at defects in Si, SiGe and novel two-dimensional material based

MOSFETs, is reviewed. One focus is put on the defect parameter extraction using the novel Effective Single Defect Decomposition (ESiD) method which enables to find defect parameters efficiently based on a non-negative least squares optimization scheme. The application of this optimized method becomes a necessity due to the large number of defect candidates in the oxide and in the transition layer at the SiC/SiO_2 interface, resulting in an significantly enhanced defect parameter space, compared to the Si/SiO_2 system. Furthermore, an efficient modeling approach will be introduced to describe charge transfer reactions between a reservoir and a defect as well as between two defects. This extension is essential for the simulation of TAT currents with percolation paths involving multiple defects. The two different non-adiabatic reactions can be described with a single defect parameter set that can be consistently converted into each other. After discussing the limitations of this novel model, the incorporation into trap-assisted tunneling current calculations in MOS stacks will be presented. With this model implemented in Comphy, the relevance of defect to defect charge transfer will be explored in parameter space for a hypothetical defect band in SiC/SiO_2.

Finally, the results of the investigations conducted in this thesis are presented in Chapter 5. First, V_{th} shifts extracted via various BTI degradation measurements on large area lateral test structures are modeled with a set of physical defect parameters with the two-state NMP transition rates as implemented in the reliability simulator Comphy. Afterwards the defect parameters are compared to such extracted on Si based MOSFETs and vertical channel (trench) SiC MOSFETs. By making use of the efficiency of the ESiD approach to handle a large set of data for defect parameter extraction, a comparison of three DMOS technologies is demonstrated, with both DC and application relevant bipolar AC stress signals. Details of SiC MOSFET specific degradation, e.g. accelerated charge emission at higher temperature leading to seemingly smaller ΔV_{th} and the increased stability of bipolar gate bias operation, are explored by the calibrated simulation framework. An extrapolation of ΔV_{th} and R_{on} up to typical device lifetimes of about ten years at room temperature and medium oxide fields based on the extracted parameters at stress conditions is shown at operating bias and temperature for static AC signals.

Additionally, TAT currents are modeled in SiC/SiO_2 stacks as well as Metal Insulator Metal (MIM) capacitors employing ZrO_2 as insulating layer for different regimes of TAT. The simulations reveal details of the tunneling mechanisms, such as spatial and energetic resolution of conduction via the traps. Finally, the parameters obtained thereby are compared to those computed with DFT for polarons in both binary oxides.

Both novelties, the first-time defect-centric modeling of BTI data in SiC/SiO_2 MOSFETs and TAT currents in the same system employing the NMP model with increased accuracy compared to previous methods demonstrate the advantage of using physical defect parameters that can be compared to ab-inito calculated parameters of the electrically active structural defects. At the same time, the efficiency necessary to handle large defect ensembles when compared to empirical modeling approaches can be maintained with the ESiD algorithm.

A concluding chapter and an outlook are finally presented. Possible applications and extensions of the hereby presented novel modeling methods are outlined.

Chapter 2

SiC MOSFET Reliability Characterization

Within this chapter an overview of techniques to extract device parameters, e.g. the threshold voltage V_{th} and flat-band voltage V_{fb}, based on electrical characterization methods is presented. Furthermore, widely employed measurement schemes to extract the device parameter degradation, namely the drift of the threshold voltage ΔV_{th} over time and gate leakage currents I_G, are introduced. Additionally, the custom-built measurement tools used to extract the data presented in this work are discussed and the advantages and drawbacks of the setups outlined. Finally, the peculiarities of the presented methods when applied for reliability characterization of SiC MOSFETs are highlighted, based on the findings presented in [138, 94, CSJ1].

2.1 Electrical Characterization Methods

An important device parameter that can be altered during device operation is the threshold voltage V_{th}. It is loosely defined as the bias state at which a significant conducting channel is formed at the MOS interface. Another important MOSFET parameter is the subthreshold-slope $SS = \partial V_G / \partial \log(I_D)$ as it is decisive for defined switching between ON and OFF state within a small gate bias range. Additionally, the transconductance $g_m = \partial I_D / \partial V_G$ is mostly related to the carrier mobility which is correlated to scattering at interface defects [139]. In practice, electrical characterization methods are used to extract these parameters as well as to track aging of these parameters during stress experiments. An overview of the most important extraction methods for MOSFETs is given in this section, with focus on V_{th} extraction and its variation over time due to bias and temperature stress, the two most dominant parameters for BTI.

2.1.1 Transfer Characteristics

The transfer-characteristics is defined as the relation of the drain current I_D over the gate bias V_G recorded at a constant drain bias V_D and can be used to extract the current

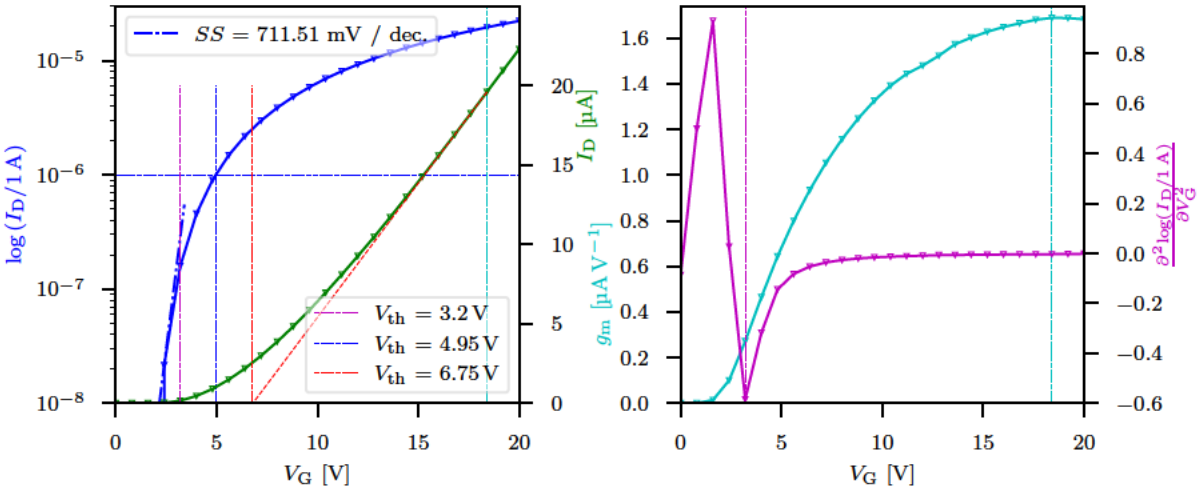

Figure 2.1. The extraction of V_{th} **(left)** is shown with a constant current of $I_D = 1\,\mu A$ (blue), the linear extrapolation (red) and the second derivative method (magenta) for a lateral SiC-MOSFET test structure with W × L = 100 × 8 µm^2 and $V_D = 0.1\,V$ at elevated T = 550 K (c.f. Figure 1.4). Additionally, the computed trans-conductance g_m with its maximum value marked and the second derivative of the logarithmic drain current with the required minimum are also shown **(right)**.

state of device parameters at the time of measurement. It is typically recommended to sweep the gate bias V_G of the Device Under Test (DUT) and measure I_D at each bias point as fast as possible. This aims to minimize the duration of an applied oxide stress field during the sweep to suppress the impact of defects with shorter capture and emission time constants compared to the sweep duration as much as possible. As a consequence, fast sweeps conserve the pristine device state. As the theoretical definition of V_{th}, the exact equilibrium of majority and minority carriers in the conducting channel of a MOSFET [32], cannot be experimentally accessed, other definitions of V_{th} are required for its experimental extraction [140]. Most frequently, V_{th} is accessed via the transfer characteristics of the MOSFET by applying a constant source-drain current criterion

$$V_{th|I_{D,const}} = V_{G|I_D=const}. \tag{2.1}$$

The current I_D is thereby typically chosen to be scaled by the device geometry with

$$I_D = I_{ref}\frac{W}{L} \tag{2.2}$$

at a constant V_D when comparing MOSFETs with different channel geometries. $I_{ref.}$ is typically chosen to result in a drain current within the sub-threshold region of the transfer characteristics. The ease of application of the method and a low extraction variability, when used for wafer scale device V_{th} variations, make the constant current method suitable for the extraction of ΔV_{th} over time [141].

Alternative methods use the trans-conductance

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{G}}} \tag{2.3}$$

to determine V_{th} from the $I_{\mathrm{D}}\left(V_{\mathrm{G}}\right)$ characteristics. For example, the linear extrapolation method uses the gate voltage for the maximum transconductance $g_{\mathrm{m,max}}$ to extrapolate to zero drain current. By subtracting V_{D} / 2 from the resulting intersection gate bias, V_{th} is obtained as [142]

$$V_{\mathrm{th},g_{\mathrm{m,lin}}} = \frac{I_{\mathrm{D}|g_{\mathrm{m,max}}}}{g_{\mathrm{m,max}}} - V_{\mathrm{G}|g_{\mathrm{m,max}}} - \frac{V_{\mathrm{D}}}{2}. \tag{2.4}$$

The second derivative method allows for a better comparison with the theoretical value of V_{th} by defining the gate bias at the minimum of the second derivative of the logarithmic drain current as threshold voltage [143]. Figure 2.1 shows a comparison of the extraction methods for a lateral SiC-MOSFET with a simple architecture, i.e. no JFET or drift-region are present contrary to a DMOS or trench design. Hence, these test structures allow for solely characterizing the channel degradation. A large variation of ΔV_{th} = 3.55 V between the presented extraction methods on this technology emphasizes the importance of using a unique definition of the V_{th} extraction method when comparing absolute V_{th} values, especially in SiC technologies.

The parameter extraction methods described above have been established for mature Si technologies and it is implicitly assumed that during the bias sweep the transistor parameters do not change. However, this assumption does not generally hold true for other material systems, such as two-dimensional channel based transistors [144] and SiC/SiO_2 MOS structures [145]. Both systems show a distinct transfer-characteristic hysteresis, as a result of charge that is captured during the bias up-sweep and not emitted during the down-sweep. This asymmetry of the capture and emission processes leads to a shift of the transfer characteristics to more positive voltages during the subsequent down-sweep (in the case of a nMOS), as shown in Figure 2.2. The peculiar shape of the hysteresis depends on the device temperature, as well as the voltage sweep rate and start and end bias of the sweep [CSC4, CSJ3].

2.1.2 Capacitance Voltage Measurements

The measurement of the small-signal capacitance of a MOS stack is a widespread technique to obtain unknown information about the transistor gate stack, i.e. oxide thickness, doping densities, poly-Si gate-depletion and permittivity. Additionally, variation of the measurement parameters and comparison of the resulting changes in shape of the Capacitance-Voltage (CV) curves allows for extraction of defect properties. For CV measurements, a DC voltage is applied at the gate contact and superimposed with a sinusoidal AC signal with a small amplitude. The bulk contact of a MOSCAP (or all terminals - source, drain and bulk - in case of a MOSFET) remains grounded. Initially,

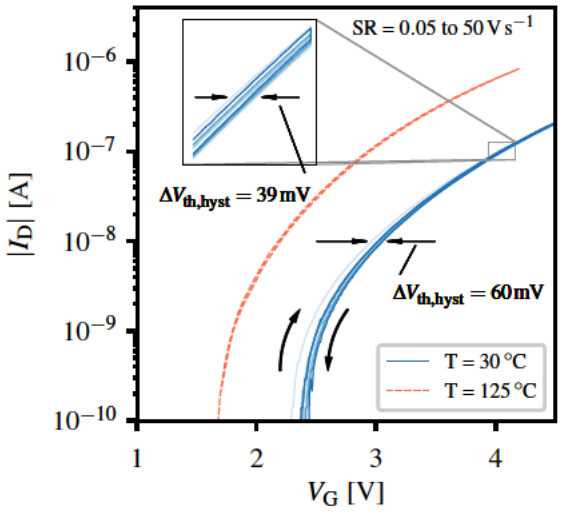

Figure 2.2. Transfer characteristic hysteresis is shown for a narrow gate bias up- and down-sweep of lateral SiC/SiO_2 MOSFET test structures. A distinct hysteresis can be measured at room temperature, depending on the voltage sweep-rate, while at higher temperatures the effect becomes less pronounced (originally published in [CSC1]).

the DC bias is swept typically from the accumulation to the strong inversion regimes. At each DC step the gate current is recorded over a number of AC periods and the measured gate current signal is modulated by the applied gate voltage signal to compute the impedance of the MOS stack from the phase shift and signal amplitudes. Furthermore, in subsequent measurements, the frequency of the applied AC signal is often varied from the kHz to MHz regime. Thus, depending on the charge transfer kinetics of defects in the oxide and/or at the interface, the shape of the CV curve may change. When a high number of defects, which exhibit charge capture and emission times in the range of the gate sweep duration, is present also a distinct hysteresis in the CV characteristics may be observed, as is the case in SiC MOSFETs. As shown in Figure 2.3, the CV measurement is considerably influenced by defects at low frequencies and significantly deviates from the ideal (defect free) case.

In Si MOS devices, the quasi static CV measurement allows for the extraction of the surface potential over the gate bias $\psi_s(V_G)$, c.f. (4.57) and (4.58). This method is not straight-forward to apply in SiC MOS devices due to the large deviation from the ideal CV characteristic, as is compared for in Figure 2.3. Thus, in order to reproduce the measurement, a transient self-consistent computation of the Poisson equation, taking the occupation of the defects into account, is required to obtain the SiC MOS CV shape. Note that such self-consistent simulations are computationally expensive and are thus often omitted.

Based on CV measurements, a number of methods to extract interface trap densities have been developed, e.g. Terman-, Conductance- or the High-Low method. However, these methods have been established based on observations in Si-based MOSFETs and are based on assumptions such as for example that defects may only be charged and

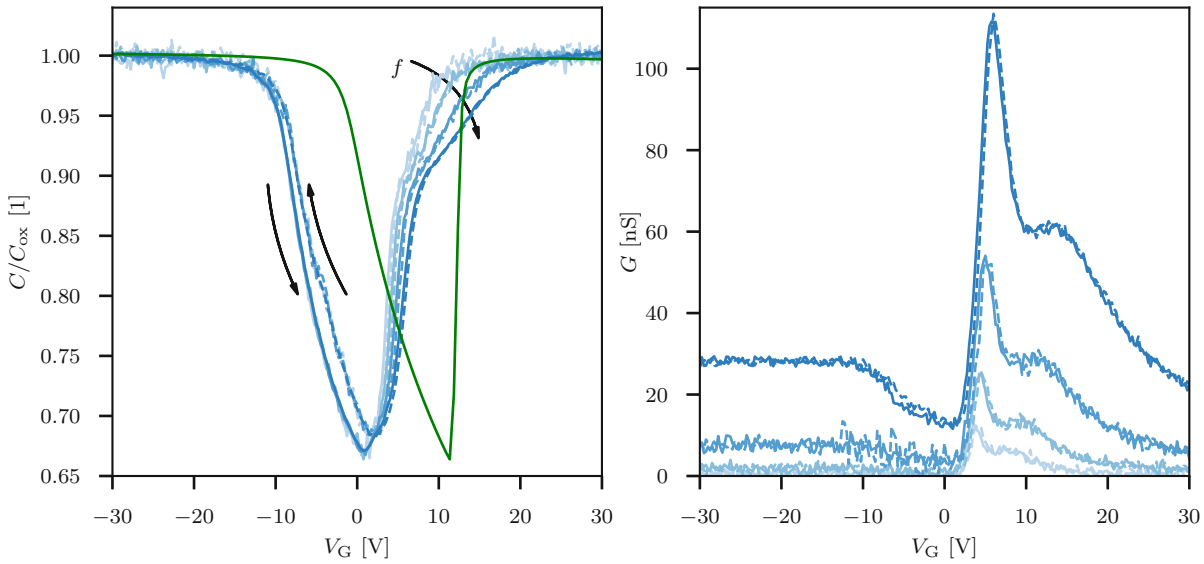

Figure 2.3. Capacitance **(left)** and conductance **(right)** of a lateral SiC MOSFET measured in gated diode configuration [146, 147] at low frequencies of f = 2, 4, 8 and 16 kHz are shown for sweeps from accumulation to strong inversion **(blue - solid)** subsequently and vice versa **(blue - dashed)**. Compared to the ideal (defect free) curve **(green)** calculated by solving the Poisson equation numerically for the gate stack, the impact of fixed charge and dynamic charge exchange becomes clearly visible. The whole characteristics is shifted towards negative biases (fixed positive charge) and the reduced steepness of the accumulation and inversion branches is likely a result of the large number of interface defects.

discharged below a certain AC signal frequency. Additionally, these assumptions often rely on the prerequisite that the defects simply follow Shockley-Read-Hall like transition kinetics. Thus, these methods are not directly applicable to SiC MOSFETs and have to be adapted if considered for application with SiC MOSFET [23].

2.1.3 Measure-Stress-Measure Schemes

As indicated by the name, the Measure Stress Measure (MSM) schemes consist of three phases. After an initial minimally-intrusive measurement of the pristine device state (typically with a $I_D(V_G)$ curve recorded within a small bias range), the DUT is stressed at elevated electric fields, temperature or irradiation compared to regular device operation conditions. This stress phase aims to accelerate device parameter degradation compared to regular operation, in order to be able to obtain the degradation within a reasonable experimental time. Following the stress phase, the device state is measured again and the quantities of interest are compared with their initial state. A regular MSM sequence typically consists of multiple stress and measure phases that are applied subsequently. In the extended MSM (eMSM) scheme [148], the recovery of the device parameters, i.e. V_{th}, mobility or channel conductivity in case of continuous I_D measurement, is monitored over a period of time during the measurement phase. Furthermore, the schemes can vary in terms of the duration and amplitude of the bias stress applied. For instance, in the constant voltage stress (CVS) scheme the stress duration (and al-

ternatively also the measurement duration) is extended within each subsequent stress phase maintaining a constant stress bias. Conversely, in the ramped voltage stress (RVS)

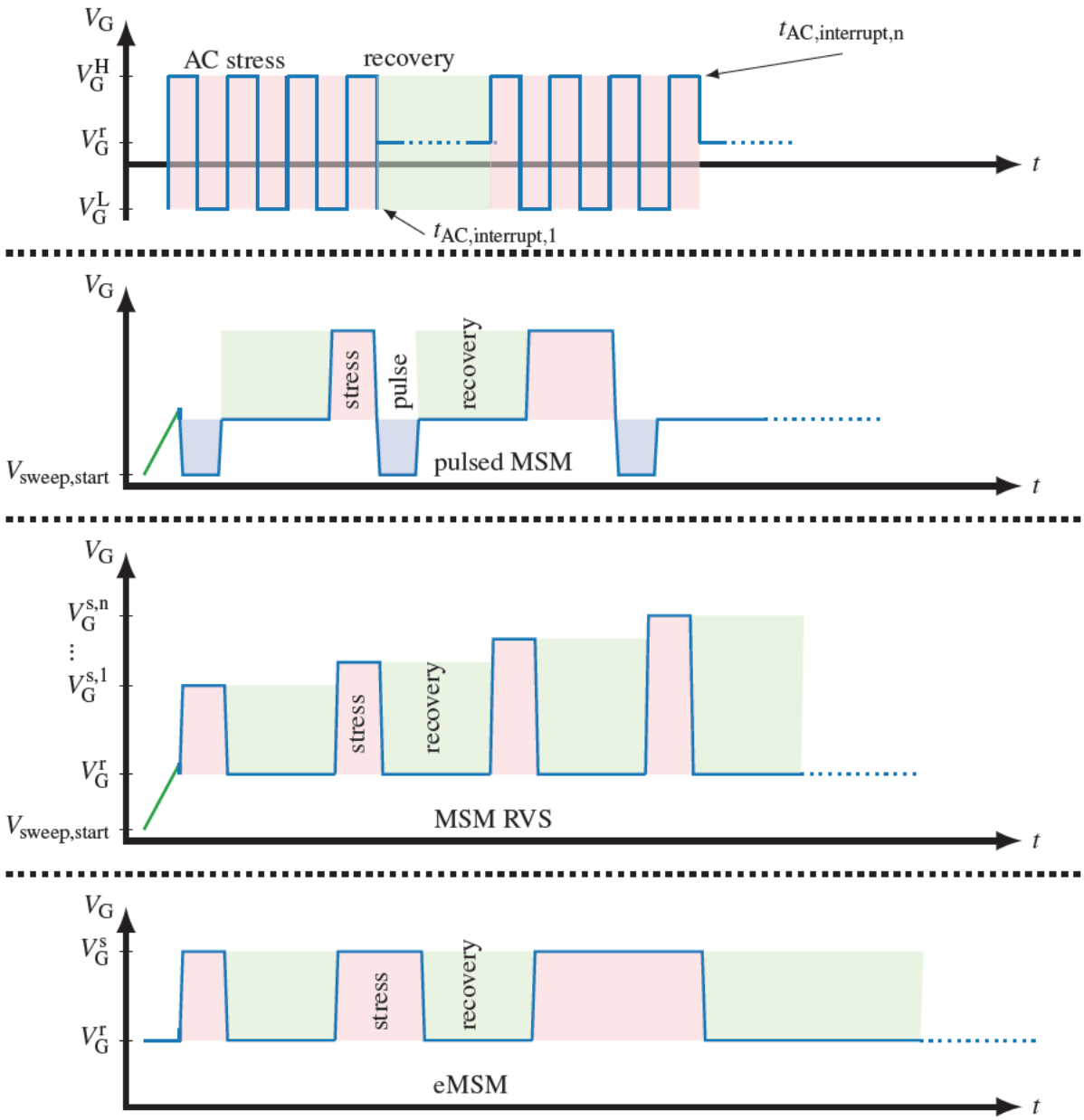

Figure 2.4. Different bias stress MSM schemes used throughout this work are shown. The CVS eMSM sequence **(bottom)** consists of stress phases of constant gate bias with subsequently increased duration. Conversely, in the RVS scheme **(bottom, center)** the stress time is kept constant while the stress bias is increased after each recovery phase. A pulsed MSM sequence **(top, center)** allows to (partly) separate fast from more permanent degradation in SiC technologies. The AC stress scheme **(top)** is used to study V_{th} shifts during operation relevant AC conditions, by interrupting the AC signal at different intervals in the AC duty cycle. (partly taken from [CSJ2])

scheme [149], the stress duration is kept constant, while the bias is increased at each stress phase. In order to investigate the degradation at operation relevant AC conditions, a variation of the CVS-MSM scheme replacing the constant DC stress by a digital AC

stress signal was proposed and demonstrated in [87]. The scheme allows to investigate the short time V_{th} variation by interrupting the AC signal at different points during an AC duty cycle. A combination of both, CVS and RVS schemes, has also been suggested and termed accelerated capture emission (ACE) measurement pattern [150]. Within this scheme, the stress voltage and periods are increased subsequently, and also the read-out bias is varied from inversion to accumulation regime during one readout phase. This results in an accelerated charge capture and emission within the experimental time window compared to individual CVS and RVS schemes. For further optimization of the efficiency of the experiment, a variation of the eMSM scheme including temperature ramps to accelerate the device recovery has been proposed [93]. Figure 2.4 gives an schematic overview about the different MSM schemes used throughout this work. The major drawbacks of the MSM methods are the lack of information about device degradation during the stress phase, as well as the inherent measurement delay when switching from stress to recovery bias. Even with ultra-fast measurement setups [151] this delay exceeds 1 µs. As a consequence, depending on the technology investigated, a major part of the faster device recovery remains inaccessible.

To overcome this drawback and to investigate degradation during the stress phase the On-The-Fly (OTF) method, also known as three-point or non-relaxation characterization method [152, 153], has been proposed. The channel conductance is obtained by recording the drain current, while pulsing the gate bias with small variations around the stress voltage level (typically at three points), with a small drain bias applied. This allows to record the change of the operation point of the transfer characteristics with minimum interruption of the stress phase. However, as only selected points of the $I_D(V_G)$ can be measured, the interpretation of the results becomes challenging and capture events with smaller transition times due to the inevitable gate bias switching delay, are not accessible by this technique. OTF extractions of ΔV_{th} during bias stress have been conducted for PBTI [154] and NBTI [155] in SiC MOSFETs revealing significantly larger V_{th} shifts compared to MSM studies.

2.1.4 Single Charge Transfer Measurements

The characterization methods (MSM, OTF) presented above are mainly employed to characterize continuous degradation and recovery of large area MOSFETs. These devices typically show a continuous recovery signal of the channel conductivity after being subjected to bias and temperature stress. The change in device behavior is a result of the superposition of many single charge emission events from a large ensemble of defects that has been charged within the stress phase. With ongoing down-scaling of the device geometry to a few nm technology nodes, the number of electrically active defects has reduced to a few single traps within the vicinity of the channel area in modern CMOS transistors. At the same time the impact of a single defect on the channel conductivity has increased with the reduced active channel area [156]. These circumstances (reduced number of defects and decreased conductivity upon charging) allow to study single charge capture and emission events in small area transistors. By

extracting the statistically distributed properties of these events, e.g. charge capture and emission time constants, many details about the charge transfer kinetics can be revealed. Commonly, two measurement techniques are employed for the extraction of the charge capture and emission events. Both methods are based on measuring fluctuations of the channel conductivity, i.e measuring the drain-source current at a constant drain and gate bias.

In the TDDS method [75], the statistical distribution of the single charge emission events is analyzed based on a large number N of repeated gate bias stress and measure sequences, typically $N \approx 100$ is used. Within this method, each defect can be identified by its step height η, which is dependent on the defects lateral and perpendicular position relative to the current percolation path. In contrast to the charge emission times, the capture times are not directly accessible, but can be derived from the average defect occupancy for the applied stress time, which is changed subsequently. The method is applicable for defects with asymmetric capture and emission times at the applied bias and temperature conditions. Due to the large number of repetitions required to extract statistical properties, the time window for the recovery trace extraction has to be limited to about $t_{\text{recovery}} < 1\,\text{ks}$ to yield reasonable experimental times [157]. The TDDS applied to a Si based MOS technology has revealed two different types of defects, termed fixed and switching emission time constant traps [75, 79]. The explanation of the latter requires an additional meta-stable defect state, which has been one of the main requirements for the development of the four-state defect model [73, 77].

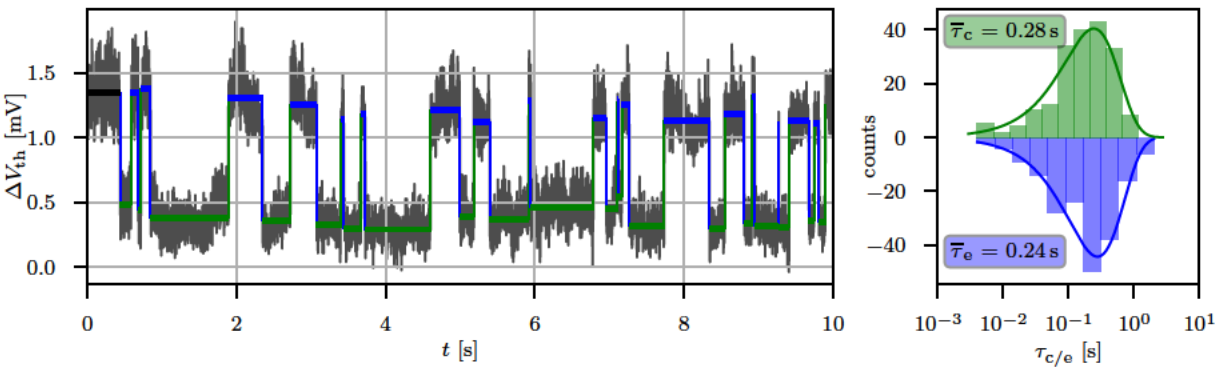

Figure 2.5. First 10 s of an RTN signal are shown as extracted on a nMOSFET at $T = 9\,\text{K}$ **(left)**. The electron capture (green) and emission (blue) times $\tau_{c/e}$ and events $\eta_{c/e}$ are highlighted. The transition times are exponentially distributed as shown in the histograms and Gaussian fits (lines) **(right)**. (originally published in [CSC5])

Measuring RTN signals in small area devices allows to study defects with similar capture and emission time constants $\tau_c \approx \tau_e$ within a single measurement trace. This is typcially the case when the Fermi-level of the channel is aligned to the thermodynamic trap level E_T of the defect. Figure 2.5 shows an exemplary RTN signal and analysis of a Si-based MOSFET conducted at cryogenic temperatures. This study revealed that RTN in the CMOS devices used in quantum computing control circuits does not freeze out, contrary to defects responsible for BTI. It has to be noted, that as is the case for TDDS

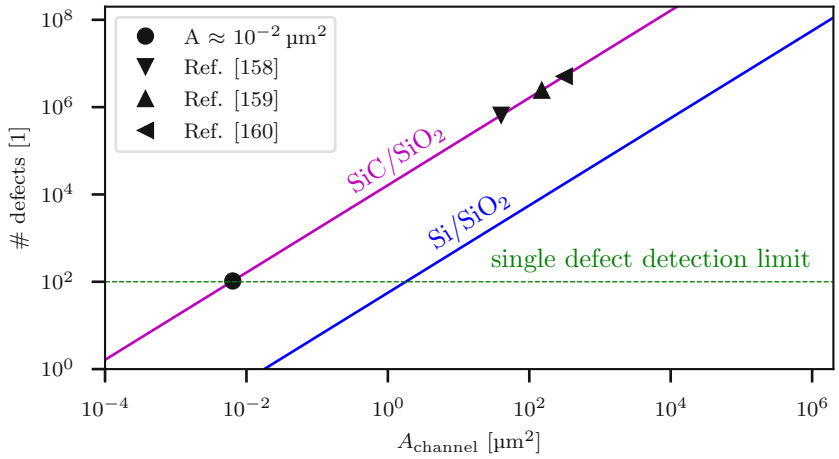

Figure 2.6. A comparison between the scaling requirements for single defect analysis in Si/SiO_2 and SiC/SiO_2 MOS gate stacks is shown. The interface state densities for calculating the number of defects for a given active channel area were chosen as $N_{it,Si} = 5 \times 10^9\,eV^{-1}\,cm^{-2}$ and $N_{it,4H-SiC} = 5 \times 10^{11}\,eV^{-1}\,cm^{-2}$ inline with values reported in literature. SiC MOSFETs produced for harsh environment CMOS applications reported in literature [158, 159, 160] (triangular symbols) with the smallest available channel areas contain still numbers of defects which are magnitudes above those required for single defect detection.

signal evaluation, a large Signal-to-Noise Ratio (SNR) is required to reliably detect the individual steps of a RTN signal.

Defect analysis by the RTN technique has been used to obtain charge transfer kinetics of defects in various MOS material systems, including standard Si-based [138], two-dimensional channel [161] and also wide bandgap substrate materials as GaN [162]. However, to date, no such studies have been conducted in a SiC/SiO_2 MOSFET. There are no obvious limitations that would obstruct the technique from its application, however, no devices with channel areas small enough to reveal single defect charge transfer events have been fabricated so far. The main reason for this is that SiC devices are mainly intended for power electronic applications where there is no requirement for scaled devices. An approximation of the minimum channel scaling required for RTN analysis in SiC MOSFETs is given in Figure 2.6, together with experimental small area SiC transistors reported in literature. The extrapolation of the device area together with a typical SiC MOSFET interface defect density shows that scaling of these structures by about another four orders of magnitude could allow for SiC/SiO_2 channel single defect studies.

The noise spectra of individual RTN signals of single defects that are superimposed in large area devices manifests itself in a $1/f$ like behavior [70]. Such spectra have been measured and analysed in SiC MOSFETs [163, 164]. The authors suggest that the origin of the low-frequency noise is solely interface defect related by comparing the data with charge-transition levels used in TCAD and compared to such obtained by ab-inito calculations.

2.2 Peculiarities of SiC MOSFET Characterization

As discussed in Chapter 1, a large number of electrically active defects in the vicinity of the conducting channel typically implies, among other detriments, instabilities of the device characteristics. Defect densities of approximately two orders of magnitude higher as compared to Si-based devices [20] bring along many challenges for the characterization of device parameters and the extraction techniques developed for Si-based MOSFETs, e.g. distorted CV-measurements for the extraction of the surface potential or additional readout delays in MSM sequences. As these techniques are impaired by alterations due to the continuous charging and discharging of the defects, a few considerations need to be taken into account, in order to make extracted quantities (like V_{th}) comparable (partly noted in [94]):

- As the application of any small external bias to the device terminals will alter its pristine characteristics, the full device history should be noted and taken into account for the extraction of ΔV_{th}.
- The pristine device state should be recorded as fast as possible using the narrowest bias range required, to minimize changes to the device during the initial characterization, a step that generally serves as the reference for further analysis.
- Measurement delays for recording ΔV_{th} need to be kept as short as possible. To extract operation relevant shifts of V_{th} at AC gate signals in the kHz regime, the measurement delay needs to be kept in the µs regime. For the extraction of faster degradation components at room and operation relevant temperatures (elevated due to self-heating), additional extraction at low temperature needs to be conducted. This is possible due to the strong temperature dependence of the defects time constants [165].

In order to make the extraction and degradation of V_{th} from measurement data more comparable among different SiC MOSFETs, Rescher *et. al* proposed a so called pre-conditioning scheme [91, 92]. Within this scheme a defined gate bias pulse in the MOSFETs accumulation regime is applied after the device is stressed and before V_{th} is read out. This pulse at typically negative biases (for a nMOS transistor) leads to accelerated emission of electrons that had been are captured during a pBTI stress phase. Most of the defects that are responsible for short term degradation emit previously captured electrons, and only a more permanent part of V_{th} degradation remains. Consequently, only defects with significantly larger charge emission time constants remain charged before V_{th} read out. While this scheme has the advantage of a more "stable" V_{th} read out, as the V_{th} value extracted is less dependent on the exact read out time after the stress phase, a large fraction of V_{th} instability is not captured by the scheme. This bears the advantage of making extracted absolute V_{th} values more comparable between different technologies and within industry standard stress tests, in which many devices are stressed in parallel and readout subsequently at varying read out times. On the other hand, if the scheme is used to reproduce charge trapping kinetics in simulations,

the charge transfer kinetics need to reproduce also the pre-conditioning scheme, instead of using the measured V_{th} directly for the PBTI simulation, e.g. [166].

In the work of Feil *et. al* [CSJ1], the impact of a gate voltage pulse on the extraction of device parameters has been investigated in detail for different commercially available SiC MOSFETs. The time dependence of the readout of absolute parameter values like V_{th}, R_{on} or g_m is quantified with typical errors of more than 10 % for common measurement readout delays and the dependence on pulse length and pulse bias is discussed. It is also shown that the pre-conditioning method can be advantageous to characterize long-term instabilities of V_{th}, i.e. classical BTI. However, it does require a careful calibration of the pulse length and width to remove the fully reversible fast recovering part of both electron and hole trapping that is inevitable in the scheme. For each technology investigated, the ideal readout close to charge trapping equilibrium can be calibrated to lie within the first milliseconds of the readout [CSJ1].

In this work the effect of a depletion or accumulation bias pulse on defects with slow and fast capture and emission times is reproduced by a transient simulation in Section 5, thereby capturing the pre-conditioning charge transfer kinetics. The full transient simulation of the whole stress and measurement scheme, including initial $I_D(V_G)$ curves, is therefore the rigorous approach to cover the widespread charge transfer kinetics within SiC based MOSFETs in a physical simulation.

2.3 Measurement Setups

Extracting the channel conductance is most frequently performed by one of the two measurement principles shown in Figure 2.7. The constant gate voltage scheme uses a trans-impendance amplifier configuration to measure the source-drain current through the channel which is converted to a voltage proportional to the current by the amplifier circuit. The main advantage of this principle is its simplicity and high stability. However, the recorded change of the drain current has to be converted back to a threshold voltage shift by an initially recorded $I_D(V_G)$ characteristics (see 2.1.1). Changes in the subthreshold-slope SS and trans-conductance g_m of the transistor transfer characteristic during the experiment are thereby neglected and can lead to erroneous ΔV_{th}.

In the constant drain current method a feedback loop to the transistor gate from the amplifier output ensures constant conductance (at constant drain bias) in the channel, with the advantage that changes in the trans-conductance and shape of the $I_D(V_G)$ do not lead to additional error due to post-processing utilizing an initially recorded characteristics. However, the circuit requires a setup designed in a way that stable operation due to the feedback loop is guaranteed at all measurement conditions, which requires additional passive elements [138]. Within this work, two custom built setups have been used. One is based on the constant voltage scheme, and termed Defect Probing Instrument (DPI) [167], and the other one on the constant current feedback loop method designed by Reisinger *et. al* [151]. Note that a comparison of the DPI with commercially available general purpose measurement instruments shows superior SNR

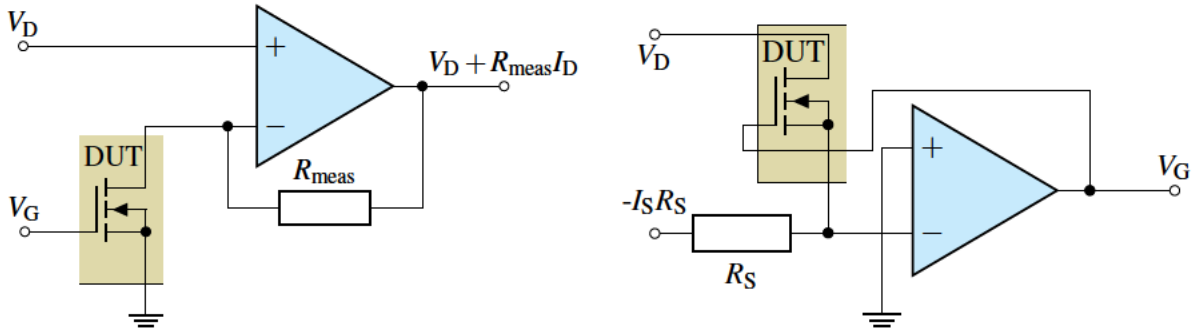

Figure 2.7. The basic measurement principles for the change of channel conduction are shown. In the constant gate voltage scheme **(left)** the operational amplifier is configured as a trans-impendance amplifier. At constant applied gate bias, the output voltage of the amplifier stage is proportional to the drain current. At the constant drain current configuration **(right)**, a constant source current is forced through the channel ajdusted with the source resistor. The feedback loop ensures that the gate bias is adjusted in a way that the drain current is constant (reproduced from [138]).

at higher current resolution. The minimum measurement delay depends on the chosen gain region and is limited by the gain bandwidth product of the measurement region, with $t_{delay} \approx 100\,\mu s$ at the highest resolution selected [167]. In the feedback loop setup, this delay is determined by the settling time of the output voltage of the OPAMP with a minimum of $t_{delay} \approx 1\,\mu s$ [151].

2.4 Magnetic Resonance Methods

Besides electrical device characterization, physical characterization methods allow to gain insight into the nature of the defects at the MOS interfacial and insulator layers. As such the Electron Spin Resonance (ESR) or Electron Paramagnetic Resonance (EPR) spectroscopy based on [168, 169] has served to identify $P_{b,0}$ and E′ centers as defects in the Si/SiO_2 system. The measurement technique is based on the Zeeman effect that relates the spin energy state change ΔE of an electron with an externally applied magnetic field B_0. Two spin states within an orbital exhibit an energy difference in opposing direction. In order to change its spin state, the electron has to absorb a photon of energy $h\nu$. Thus the fundamental EPR resonance equation yields

$$h\nu = g\mu_B B_0 \tag{2.5}$$

in which μ_B is the Bohr magneton and g the g-factor associated with the interaction of both the external field B_0 and local magnetic fields due to spin-orbit coupling. In the experimental setup, the sample is placed within a Helmholtz coil to generate a homogeneous magnetic field and a spectrometer employing a microwave radiation source, a resonance cavity and a detector. The absorption spectrum is measured over varying B_0 which gives a unique fingerprint of the electron spin state transition, which can be uniquely related to theoretical calculations of atomic configurations employing

unpaired electrons. This is typically achieved by extracting the g factor at the measured field and frequency of the absorption line according to (2.5). Since the spin-orbit coupling is theoretically well understood, the g-factor of the unpaired electron can be associated with a specific orbital.

A variant of EPR spectroscopy is the Electrically Detected Magnetic Resonance (EDMR) characterization method [170]. Thereby the energy levels of electron donors and acceptors are extracted by switching the spin with a microwave pulse (same principle as in EPR). The recombination current that occurs when the electron moves to a lower energy state (which is possible after spin change due to Pauli's exclusion principle) and recombines with a hole is detected. This technique allows for the detection of only a very small number of defects within a sample.

2.5 Summary

Typically used MOSFET parameter extraction methods have been presented in this chapter, with focus on large area transistor BTI characterization. Due to the large density of fast traps in SiC MOSFETs, compared to their Si counterparts, it is essential to record the full device history of the DUT starting from its pristine state. If the discussed preconditioning schemes are applied, they also need to be considered within a transient simulation. Gate stack parameter extraction from CV curves and their correct reproduction by simulation require fully self-consistent computational schemes, which limits their usability for ideal device electrostatic calibration, compared to Si-based MOSFETs, and one needs to fall back to the exact knowledge of doping profiles and gate oxide thickness for simulating SiC MOSFETs.

Chapter 3

Defects in SiC Field Effect Transistors

Advances in material and process engineering have enabled the production of pure crystalline Si with negligible distortions to the ideal crystal structure. An ongoing challenge is the deposition of a suitable insulator ensuring a high quality interface. Although the lattice mismatch at the interface between the bulk Si and its native oxide leads to electrically active defects, i.e. Si dangling bonds or P_b centers, these can be passivated by hydrogen atoms in a forming gas annealing step, leading to a chemically stable material system. On the contrary, as outlined in Chapter 1, the quality of the SiC crystal available at wafer scale still suffers from stacking faults, dislocations and point defects. Furthermore, the chemical composition of the SiC/SiO_2 interface is less understood, compared to its mature Si/SiO_2 counterpart. While forming gas anneals do not show a significant passivation effect in SiC/SiO_2 systems, annealing in nitrogen containing ambients successfully reduces the number of electrically active defects. However, the exact chemical mechanism of this passivation effect is still debated. Within bulk amorphous SiO_2, potential defect candidates have been identified and studied in detail by atomistic simulations employing ab-inito calculations. In this chapter an overview is provided of the relevant defect types and their properties in bulk SiO_2 and at the SiC/SiO_2 interface as calculated with Density Functional Theory (DFT). It has to be noted that the widespread terminology suggested by Fleetwood [171], which categorizes defects in interface, border and oxide traps is not strictly followed throughout this work. This is because a clear separation of the electrically active defects by its spatial distance to the interface, which would require a sub-nanometer resolution characterization, cannot be provided by the experimental extraction or transient device simulations available.

3.1 Defects in Bulk Silicon Dioxide

Amorphous SiO_2 (a-SiO_2) has been studied in great detail due to its importance in semiconductor technology. Among electrical, optical and structural properties, a number of electrically active defect types have been studied using electrical, magnetic resonance or optical characterization methods, as described in Chapter 2. Experimentally, param-

agnetic defects are often characterized by magnetic or spin resonance measurements. Within α-quartz, the so-called E_1' center, in which the prime denotes that one is electron involved in the measurement signal and 1 evolves from arbitrary enumeration, has been identified by EPR measurements already in the 1950s [172]. The **oxygen vacancy (OV)**, which naturally forms during the oxidation of silicon, with densities depending on the oxidation process parameters like temperature and pressure, has been suspected early on as a candidate to explain the ESR and EPR spectra for E_γ' centers in a-SiO_2 (which is the equivalent to E_1' in the crystalline material) [173, 174]. However, it took until the late 1990s to connect the EPR data with structural properties derived from ab-initio calculations. Thereby an excellent agreement of the experimentally determined hyperfine structure with the calculated OV [175] was obtained. In its neutral state, the two Si atoms with the missing two-coordinated O bind together, thereby forming a Si-Si dimer. If one of the binding electrons is removed, e.g. by the application of an external electric field, the defect will eventually relax to its stable positive state which can be detected with ESR and EPR measurements due to the spin of the single remaining electron at the defect site. The defect can exist in multiple states, e.g. in its stable state the Si atom can eventually bind to a back oriented O atom after moving through the plane spanned by the three adjacent O atoms, thereby forming a puckered configuration, c.f. Figure 3.1 (top) state 1 and 2 [176]. This transition is accomplished via a meta-stable state (1′, 2′) which is reached by a purely thermally activated structural re-configuration. The existence of such meta-stable states is supported by experimental observation of anomalous RTN [80], which justifies the applicability of a four-state NMP model to describe the kinetics of charge capture and emission of OVs in detail. Additionally, to the E_γ' EPR signal, the origin of another EPR signal obtained in a-SiO_2, the so-called E_δ', is not fully understood and has been associated with a re-bonded OV or a multi-vacancy defect [174]. Note that recent results suggest that the OV is not considered responsible for charging mechanisms related to PBTI and NBTI in Si/SiO_2 transistors employing thin insulating layers [178]. To the contrary, the tails of the distributions of their thermodynamic charge transfer levels calculated by DFT are within the energetic range that are scanned in SiC/SiO_2 MOSFETs during operation and stress experiments for both BTI regimes. However, the trap-level distribution of the OV appears energetically more favourable in the PBTI regime as shown in Figure 3.1 (bottom). Furthermore, the relaxation energies for the PBTI relevant transitions -/0 and 0/- as extracted from DFT are asymetrically distributed around 2 eV [177], which is within a reasonable range to link to experimentally observable charge transition kinetics and well agrees with NMP parameter ranges extracted from MSM measurements, as will be shown in Chapter 5. High formation energies of about 7.6 eV [177] at low densities of 10^{14} to $10^{17}\,cm^{-3}$ extracted by EPR measurements [179, 180] on the other hand oppose the relevance of OVs for PBTI. However, increased densities could be observed in thicker and deposited oxides. Since the thermal budget for processing SiC MOSFETs is typically higher compared to Si transistors, different densities may be expected.

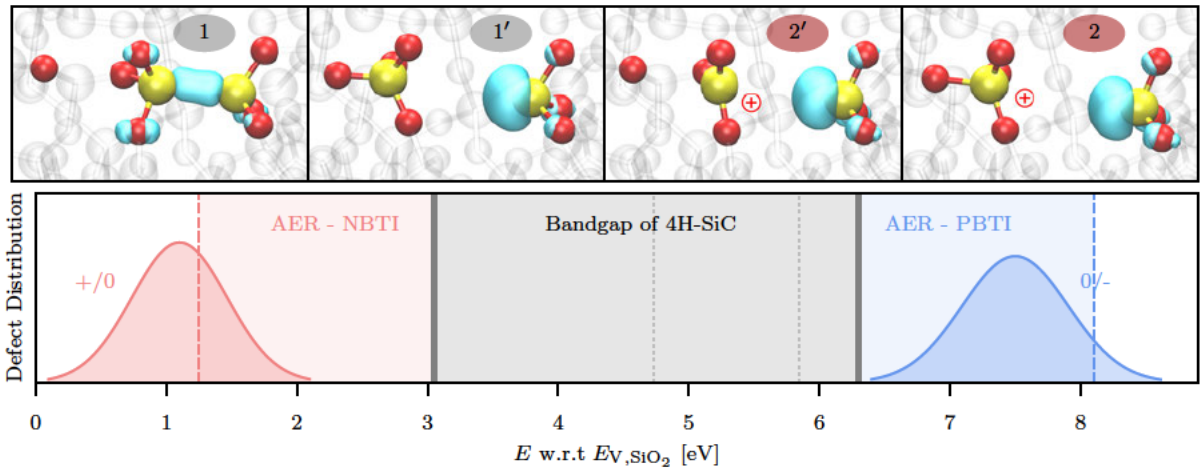

Figure 3.1. Oxygen vacancy in different charge states and configurations **(top)**. The neutral (1) and positive (2) stable states are shown together with meta-stable states (1′,2′). The transition from neutral state 1 to positive state 2 occurs upon emission of one of the electrons in the Si-Si bond (2′) and the following structural relaxation, in which the Si atom moves through the plane spanned by the O atoms and bonds to a back-oriented O atom (2). The distribution of +/0 and 0/- charge transfer levels predicted by DFT calculations [81, 177]**(bottom)** renders the OV a potential defect candidate for both NBTI and PBTI in the SiC/SiO_2 MOS structure. The AERs (dashed) are calculated for $E_{ox} = 5\,MV\,cm^{-1}$ at 3 nm distance from the interface. (partially reprinted and modified from [178])

At oxygen vacancies embedded in a locally partially recrystallized SiO_2 structures, the charge-transfer levels (CTLs) for the +/0 transition are shifted towards the oxide valence band edge, as calculated by hybrid functional DFT [181], rendering OVs potential defect candidates responsible also for NBTI in SiC MOSFETs. The shift of the CTL upon the structural change of the OV from the neutral dimer state 1 to its positive state 2 upon hole capture could also explain the positive charge built up upon bipolar stress in p-type MOSCAPs, i.e. long-term NBTI and PBTI subsequently, as suggested by Shen *et. al* [90]. Hole capture in both n-type and p-type SiC MOSCAPs has been linked to the OV within their work.

Another defect candidate for electron capture in bulk a-SiO_2 is the **intrinsic electron trap**, or **polaron** [182], shown in Figure 3.2. It stems from an intrinsic site in the SiO_2 network at which an electron may spontaneously localize at elongated O-Si-O bonds with bond angles $> 132°$. The large density of these precursor sites of $N_T = 5 \times 10^{19}\,cm^{-3}$ estimated from their formation probability and their calculated thermodynamic trap level at $E_T = 2.8\,eV$ below the SiO_2 conduction band edge make the defect a suitable candidate for electron trapping [182, CSC1]. Experimentally, the intrinsic electron trap is often linked to photon-stimulated electron tunneling measurements of shallow electron traps [183], in which a large defect density of $10^{13}\,cm^{-2}\,eV^{-1}$ is extracted with an E_T of 0.1 eV below the conduction band edge of 4H-SiC in SiC/SiO_2 MOS devices. It should be noted that a similar precursor site was calculated with DFT also for other binary oxides, i.e. ZrO_2 and HfO_2 [184]. Within this work, the intrinsic electron trap is linked with TAT currents measured in SiC/SiO_2 MOSCAPs. Therefore, the calculations of

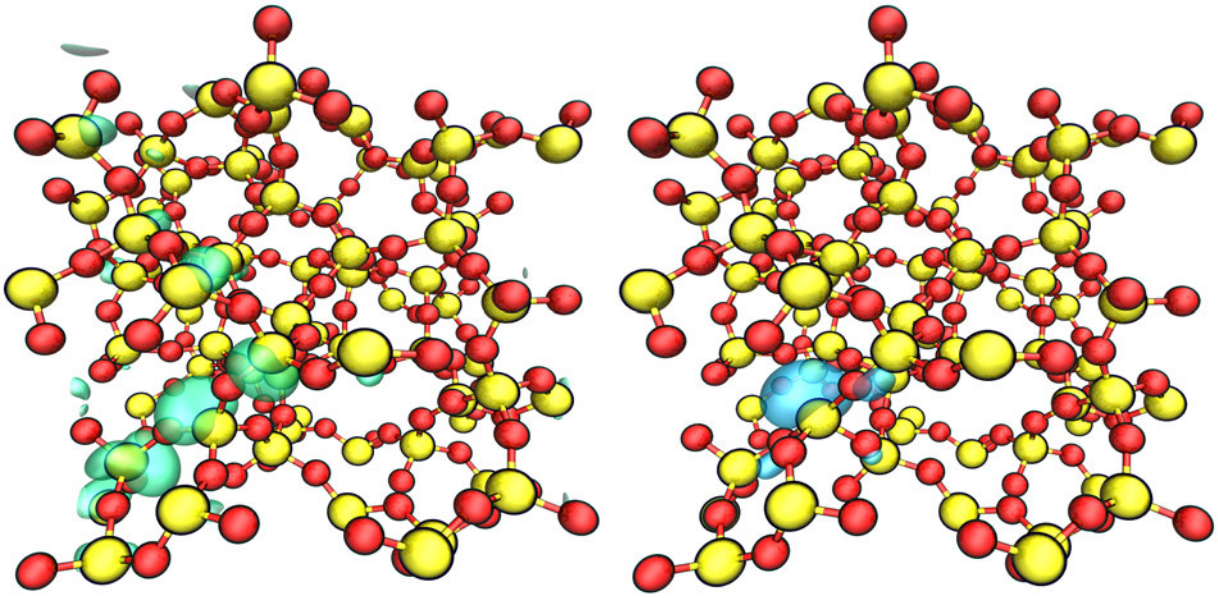

Figure 3.2. Ball-and-stick model of the a-SiO_2 network with Si atoms (yellow) and oxygen atoms (red). An intrinsic electron trap is shown with a partly localized lowest unoccupied molecular orbital (LUMO) at an elongated O-Si-O bond **(left)**. Upon electron capture, the wavefunction collapses onto the bond, which undergoes structural relaxation and further opens up the bond angle to reach values close to 180°, as can be seen from the intrinsic electron trap in its negative charge state, which is characterized by its highest occupied orbital (HOMO) **(right)**.

El-Sayed *et. al* [182] are extended to observe statistical relevant parameter distributions of the thermodynamic defect level and relaxation energies. Additionally, the same class of intrinsic traps can be linked to tunneling currents in ZrO_2 based MIM capacitors within the NMP modeling framework Comphy, as will be discussed in Chapter 5.

3.2 Defects at the Silicon Carbide / Silicon Dioxide Interface

The enhanced Active Energy Region (AER) in the SiC/SiO_2 material system compared to the Si/SiO_2 case allows additional bulk-SiO_2 defects to become charged/discharged in SiC MOSFETs. Additionally, different types of interfacial defects have to be considered. A large number of physical and electrical characterizations as well as theoretical studies on the structural properties of the SiC/SiO_2 interface have been published in the past 25 years. Within the sub-stochiometric transition layer between semiconductor and oxide, as shown for an ideal atomistic model in Figure 3.3, the accumulation of carbon in clusters during oxidation has been early suggested to be responsible for deep defects states [187, 188]. However, experimentally no significant amount of excess carbon could be measured by Electron Energy Loss Spectroscopy (EELS), Secondary Ion Mass Spectroscopy (SIMS) (Figure 3.3 (right)) and X-ray Photoelectron Spectroscopy (XPS) studies after re-oxidation and nitridation of the interface [189]. Instead, acceptors

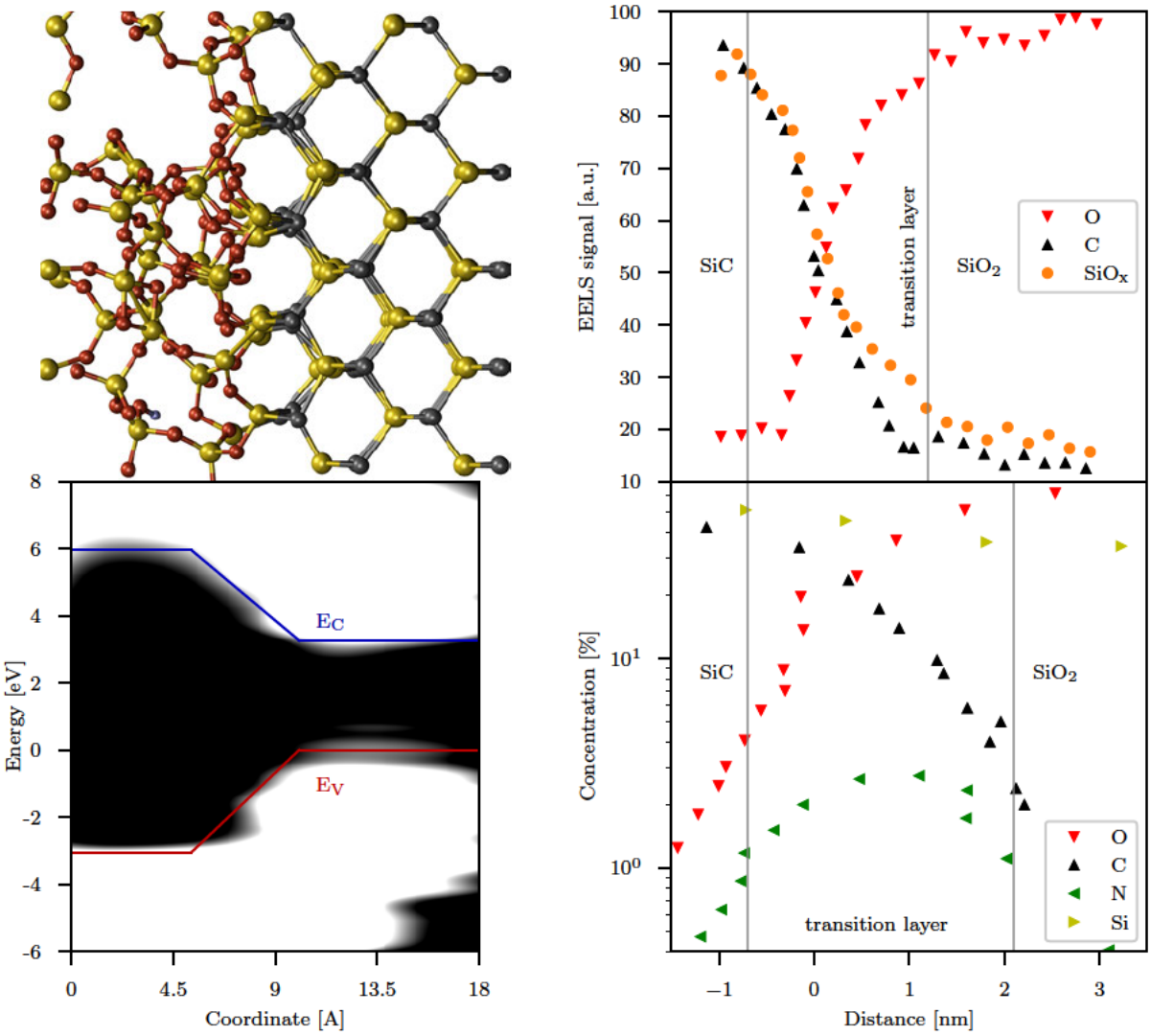

Figure 3.3. The interface transition region is shown schematically with a ball-and-stick model **(top, left)** and the progression of the bandedges **(bottom, left)**. The transition region of 5 Å from the bulk SiC to SiO_2 has been calculated employing classical MD combined with DFT [185]. Additionally, EELS data [186] **(top, right)** of NO post-deposition annealed SiO_2 is compared to SIMS data [118] **(bottom, right)**. For better comparability, the SIMS data has been spatially aligned to the EELS signals at the sub-stochiometric layer between bulk SiC and SiO_2.

like carbon interstitial and oxygen bound dimer states have been suggested as suitable defect candidates by ab-initio calculations, as their trap levels lie close to the SiC conduction band edge [190]. The increased complexity of the chemical composition which is induced by additional elements like C and N at the SiC/SiO_2 interface region allows for a number of other potential defect candidates. Some of these have been theoretically studied in the framework of DFT employing a hybrid functional in addition to hydrogen related defects by Devynck *et. al* [191]. Their results render the Si_2-C-O structure a suitable defect candidate, which can form when a CO molecule replaces an O atom in the SiO_2 network. This defect is expected to occur at high defect densities

and exhibit CTLs close to conduction band edge of SiC, as experimentally measured by photon stimulated tunneling and electrical characterization by Afanasev *et. al* [183]. In later works, carbon-dangling bonds ($P_{b,C}$ centers), analogously to the $P_{b,0}$-centers in Si/SiO_2, have been suggested by comparison of EDMR spectra with those calculated for $P_{b,C}$ defects [192, 193, 194] as interface states with energy levels deep within the SiC bandgap. During Si oxidation, these dangling bonds natively form from strain release during the SiC oxidation process and structurally consist of a carbon atom back-bonded to three silicon atoms with an unsaturated bond directed towards the interface.

The detailed structural interface analysis of Woerle *et. al* [195] includes various physical characterization methods, e.g. EELS, Photo-Luminescence (PL) and local- Deep Level Transient Spectroscopy (DLTS) on thermally oxidized SiC/SiO_2 samples with different surface roughnesses. Their results suggest that an abrupt transition from SiC to SiO_2 is only possible on atomically flat surfaces, which is also supported by EELS and scanning transmission electron microscopy (STEM) measurements on SiC MOSFETs with low-temperature deposited oxide layers and comparison to ab-initio calculations for abrupt transitions [196, 197]. Therefore, in this work, linearly interpolated transition regions for the energetic band-edges within 5 Å, as shown in Figure 3.3 **(bottom, left)**, are used within the simulations conducted.

3.3 The Role of Hydrogen

Although, as discussed in Chapter 1, forming gas anneals for interface passivation have not improved the interface of the SiC/SiO_2 system, hydrogen may still play a role in defect formation and inevitably is introduced through other process steps, e.g. through Silan (SiH_4) which is used as precursor for the poly-Si gate contact formation, poly-Si/SiO_2 interface passivation after deposition in forming gas or through the precursor TEOS upon oxide formation via CVD. Rescher has shown by measuring CV characteristics of MOSCAPs after certain process steps (process splits), that an accumulation of positive charges, i.e. protons, is especially pronounced after the annealing step which follows the interlayer dielectric deposition [198]. A promising approach to describe the dissociation of hydrogen at passivated interfacial bonds at the poly-Si interface under stress conditions is provided by the gate-sided hydrogen release model [98]. The model is capable of describing both the recoverable and the permanent component of BTI in Si-MOSFETs. At its core, this model is based on the assumption that hydrogen related defects, such as the **hydrogen bridge (HB)** or the **hydroxyl-E′ center (HE′)**, can release their hydrogen which can then diffuse through the insulator and eventually create defects at another oxide site or create new dangling bonds by forming H_2 by releasing the H atom of a previously passivated P_b center. Note that both the HB and HE′ defects can form from H atoms which rapidly diffuse through SiO_2 due to small diffusion barriers at low temperatures [199]. In the case of HB, additionally an interaction with an OV [200] is required, thus reducing its formation probability. However, both the formation of HB and HE′ is likely in the SiO_2 network upon availability

of the precursor sites with CTLs for +/0 and 0/- within the SiC bandgap or close to the band edges and relaxation energies distributed between 1 to 3 eV [81, 177]. Thus, just like in Si based MOSFETs, the role of hydrogen related defect structures cannot be neglected when electrically active defect candidates in bulk a-SiO_2 are studied in SiC MOSFETs.

3.4 Nitrogen Related Defects

Optimizing the SiC/SiO_2 interface by POA or PDA in nitrogen containing ambients, i.e. NO, NO_2 or NH_3, has lead to a considerable improvement of the mobility and reduction of deep interface states, as discussed in Chapter 1. However, a significant amount of N can directly be observed at the interface after annealing as reported in several studies [201, 118, 197]. This accumulation of N in the transition region between SiC and SiO_2 is correlated with an increased defect density close to the SiC conduction band [201, 52]. Another source of N is its implantation as an electron donor in the source and drain region. In N implanted regions, the $N_C V_{Si}$ has been suggested as deep level defect responsible for dopant-deactivation [202]. This motivated theoretical studies on the incorporation of N close to the SiC/SiO_2 interface using ab-initio methods. These first-principle studies have suggested that N can passivate large amounts of both silicon and carbon dangling bonds effectively [203], however, with the trade-off that states in the lower half of the band-gap are formed by a resulting threefold N, leading to positive charge accumulation. Increased hole trap densities have also been reported due to the incorporation of NO at the interface from capacitance measurements and first-principle calculations [204]. Both studies suggest an increase of positive charge accumulation in an Si-C-N-O or even Si-C-N-O-H transition layer, consistent with the shift of the ideal device characteristics towards more negative gate bias, c.f. Figure 2.3.

The incorporation of NO or NH into well known bulk-SiO_2 defects such as the intrinsic electron trap and the oxygen vacancy has been modeled with DFT by Mistry *et. al* [205]. These studies revealed that the incorporation of NO^- can passivate the intrinsic electron trap, thereby potentially reducing the available concentration of these defects for electron trapping.

The studies of Higa *et. al* on dry-oxidized and nitrided interfaces revealed a drastic reduction of the $P_{b,C}$-center's EDMR signal for short term POA and is especially pronounced on a- and m-face interfaces [206]. However, over-nitridation leads to an increased EDMR signal that has been related to the so called K_N-center, which is a silicon dangling bond that forms on a Si atom that is bonded to three N atoms. These K_N-centers are also observed in plasma nitrided oxides (PNO), while a similar EDMR spectrum is observed for such defects in Si_3N_4 and referred to as *K*-center [135, 207].

In summary, nitrogen plays a two-fold role for the stability of the SiC/SiO_2 interface. Its importance for the passivation of interfacial defects is widely acknowledged and POA in N containing ambients has been established for industrial production. On the

other hand, potential defect candidates that could arise from N incorporation at the interface are not clearly identified.

3.5 Summary

As only briefly outlined in this chapter, the variety of defect candidates that potentially form in SiC/SiO_2 structures is much larger compared to Si/SiO_2. Their calculated thermodynamic trap levels are distributed over the whole oxide band gap. Moreover, as the active energy regions for negative and positive transistor operation show, almost the entire SiO_2 band gap can be scanned by deliberately altering the gate bias, suggesting that thermodynamic charge transitions are possible with almost any candidate proposed. The introduction of another atomic species in the substrate compared to pure Si, namely carbon, gives rise to the formation of additional carbon-dangling bonds at the interface to its native oxide with defect levels in the upper half of the SiC band-gap. Those are likely passivated to a large fraction by N, which when incorporated is also suspected to form traps with defect levels suitable for positive charge accumulation and also form acceptor like states close to the SiC conduction band edge. In Chapter 5, the parameters, i.e. thermodynamic trap level, relaxation energies and defect densities, obtained from ab-initio calculations of most likely defect candidates to explain charge transfer reactions causing BTI and TAT in SiC/SiO_2 structures are compared with those used for defects in the presented device simulations.

Chapter 4

Modeling of Charge Transfer Reactions at Defects in MOS devices

While the previous chapters discuss the relevance of BTI and TAT, the experimental characterization of the degradation mechanisms and the microscopic structure of defects considered to be responsible for the observed phenomena, in this chapter models to describe the underlying physical processes, i.e. charge transfer reactions, will be presented. Previous works have revealed that inelastic tunneling processes are essential to describe many experimentally observed features of BTI, RTN and TAT. However, the amorphous nature of the deployed insulating layers results in broad distributions of structural defect properties, and hence also the charge transfer kinetics of defects extends over many orders of magnitude in time. The extraction of physically meaningful defect properties from detailed models employing a number of parameters, e.g. the 4-state NMP model, becomes arbitrarily cumbersome, especially in large area devices, where only the macroscopic response of a defect ensemble is experimentally accessible. This becomes even more challenging when dealing with materials which can host a plethora of distinct defect types as is the case for SiC based power MOSFETs. Therefore, the modeling approaches presented in this work target the description of physical charge transfer reactions based on defect parameters that can be linked to experimentally inferred parameters as well as theoretical ab-intio calculations of particular defect candidates. In particular the methods presented here for simulation and defect parameter extraction have been developed with a focus on computational efficiency, in order to allow for the explicit treatment of a large number of defects across a wide parameter space.

4.1 From State Diagrams to the Master Equation

As already discussed in Chapter 3, within the 4-state defect model a point-defect can dwell in one of two stable (1, 2) or two meta-stable states (1′, 2′). As indicated in Figure 4.1 (left) for an electron trap, the states (1, 1′) denote the neutral and (2, 2′) the negative charge states. Thermal transitions within the same charge state are

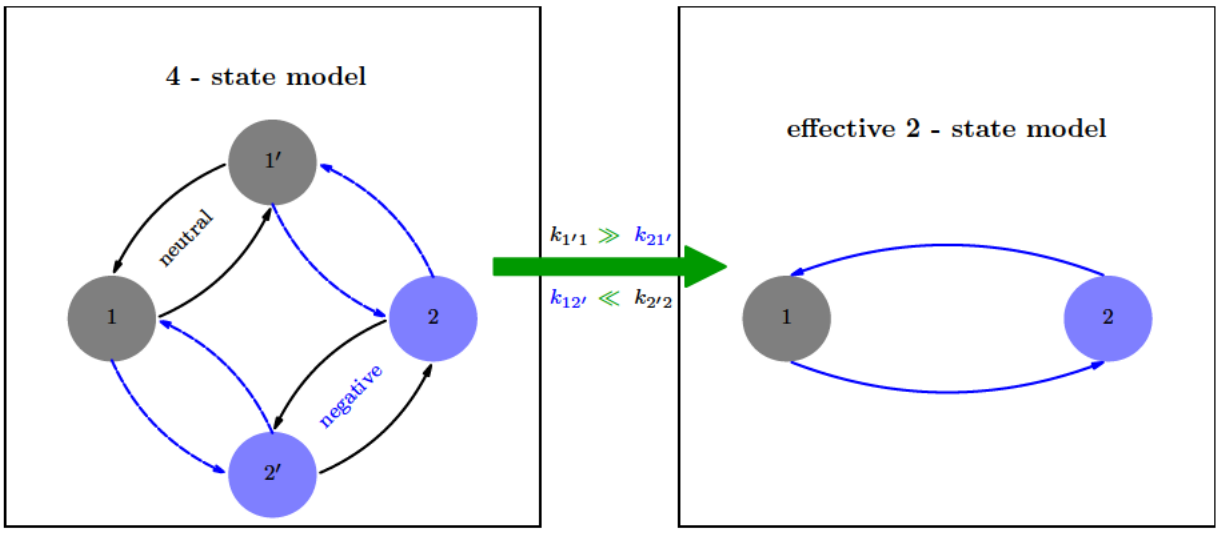

Figure 4.1. A detailed description of the charge transfer kinetics requires to include meta-stable defect states for many defect structures leading to a 4-state Markov chain **(left)**. However, often a reduction to an effective 2-state diagram **(right)** can be justified, e.g. in case the meta-stable states are experimentally not observable in large-area devices or the transition rates k_{ij} between stable and meta-stables states (black), stemming from purely thermally activated reactions, are much faster than the charge transfer transitions (blue).

linked to structural relaxation of the defect without the need for an additional charge transfer to occur, hence such transitions are not directly detectable experimentally. However, certain observations in single-defect measurements like switching traps [79] or anomalous/temporal RTN [80] prove the existence of additional meta-stable states. When dealing with a large ensemble of defects as is typically the case for large area devices, these details do not play a significant role and a reduction of the four state model to an effective two state model shown in Figure 4.1 (right) is justified [208]. This holds also true when modeling defects like polarons, which are not expected to exhibit meta-stable states. Additionally, the purely thermally activated transitions from meta-stable to stable states are often much faster than the charge transfer transitions, e.g. considering typical bias conditions, where the barriers for charge transfer are higher than thermal barriers of about 0.25 to 0.5 eV in the case of HB or HE′-center defects in SiO_2 [165].

In general, the temporal evolution of the charge state occupation of a defect is of particular interest. In order to compute the probability of a state to be occupied or change its occupation within a certain time, the basic assumption is that the transition rates k_{ij} from state i to state j are independent of the defect's occupation history and only depend on the state in which the defect currently dwells. This is the key assumption for modeling the state transitions within a Markov chain and is justified as the time-scale for reaching the equilibrium configuration after a charge transfer (typically within a few ps) to and from a defect is much faster than typical transition rates ranging from µs to ks and above. With this assumption of memory-less transitions, the defect's charge state can be described using a simple state machine, which can be mathematically described

by a time-continuous discrete Markov process with the probability P of changing the state X from i to j within the time Δt [209]

$$P\left\{X_{t+\Delta t} = j | X_t = i\right\} = k_{ij}\Delta t + \mathcal{O}\left(\Delta t^2\right). \tag{4.1}$$

On the other hand, the probability of remaining in state i is given by

$$P\left\{X_{t+\Delta t} = i | X_t = i\right\} = 1 - P\left\{X_{t+\Delta t} \neq i | X_t = i\right\} = 1 - \sum_{i \neq j} k_{ij}\Delta t + \mathcal{O}\left(\Delta t^2\right). \tag{4.2}$$

By using the law of conditional probabilities and taking the limit to infinitesimal time steps, the evolution of the probability to be in state i is given by the following differential equation:

$$\frac{\partial P_i}{\partial t} = \lim_{\Delta t \to 0} \frac{P_i\left(t + \Delta t\right) - P_i\left(t\right)}{\Delta t} = \sum_{j \neq i} P_j k_{ji} - P_i k_{ij}. \tag{4.3}$$

The entire system is then described by the so-called Master equations, a set of coupled linear differential equations, given by

$$\dot{\vec{P}} = \boldsymbol{K}\vec{P} \tag{4.4}$$

with the coefficients of the rate matrix $\boldsymbol{K}$

$$K_{ij} = \begin{cases} k_{ji} & , i \neq j \\ -\sum_{l \neq i} k_{il} & , i = j. \end{cases} \tag{4.5}$$

Note that at all times the total occupation has to be conserved, i.e.

$$\sum_i P_i = 1 \tag{4.6}$$

has to hold. This condition is preserved from the initial state $\vec{P}\left(0\right)$ within the Master equation [210] and by solving (4.4) the occupation probabilities at all times t can be computed as

$$\vec{P}\left(t\right) = \exp\left(\boldsymbol{K}t\right)\vec{P}\left(0\right). \tag{4.7}$$

For Markov processes with a ring topology as constituted within the 4-state model (or reduced state models) the rate matrix $\boldsymbol{K}$ is sparse with only two off-diagonal elements, which significantly reduces numerical computation efforts for solving (4.7). For the simple case of a two-state defect model the steady state solution $(t \to \infty)$ for the occupation probability of state 1 reads

$$P_1\left(\infty\right) = \frac{k_{21}}{k_{12} + k_{21}} \tag{4.8}$$

and the temporal evolution of the occupation probability is given by an exponential decay function, i.e.

$$P_1(t) = P_1(\infty) + [P_1(0) - P_1(\infty)] \exp\{-t(k_{12} + k_{21})\}. \tag{4.9}$$

For an ensemble of N non-interacting defects their occupations can be simply computed individually by using (4.7), if their initial occupations and transition rates are known.

To include the possibility of a charge transfer between individual defects, the transition rates in (4.3) have to include the rates from and to each other defect and therefore depend on the occupation of all other defects. By assuming a two-state Markov process and denoting $f_i = P_{1,i}$ with i running over N defects, a non-linear system of coupled Master equations with components

$$\frac{\partial f_i}{\partial t} = k_{\text{in},i}(\vec{f})\,(1 - f_i) + k_{\text{out},i}(\vec{f})\,f_i \tag{4.10}$$

results. The in- and out-rates at each defect are then given by

$$k_{\text{in},i}(\vec{f}) = \sum_{j \neq i}^{N} k_{ji} f_j \tag{4.11}$$

$$k_{\text{out},i}(\vec{f}) = \sum_{j \neq i}^{N} k_{ij}\,(1 - f_j)\,. \tag{4.12}$$

Note that (4.10) is fundamentally different compared to the previous case of a single defect treated in (4.3) and (4.4), as it refers to a defect occupation probability in a state system in which $\sum_i^N f_i \neq 1$. An efficient algorithm for solving the non-linear system of ordinary differential equations (ODE) as required for calculating charge hopping currents within a two-state NMP model will be presented in Section 4.5. In the following sections, physical charge transitions rates for charge transfer between defects and carrier reservoirs, as well as between defects, are derived.

4.2 The Shockley-Read-Hall Model

In their original work, Shockley and Read, as well as Hall, derived rates for non-radiative recombination of excess electrons and holes [63, 211] in bulk semiconductors, introduced either by light or carrier injection via defects, as shown in Figure 4.2 (left). For non-degenerated semiconductors the total rate for electron capture was derived as [63]

$$k_{\text{c},n} = \left[1 - \exp\left(\frac{E_\text{T} - E_{\text{F},n}}{k_\text{B} T}\right)\right] f_{p,\text{T}}\, n C_n. \tag{4.13}$$

Thereby n denotes the electron density, $f_{\text{p,T}}$ the hole occupation of the trap ($f_{p,\text{T}} = 1 - f_{n,\text{T}}$) and $C_n = v_\text{T}\sigma_n$, v_T stands for the thermal carrier velocity and σ_n is the capture

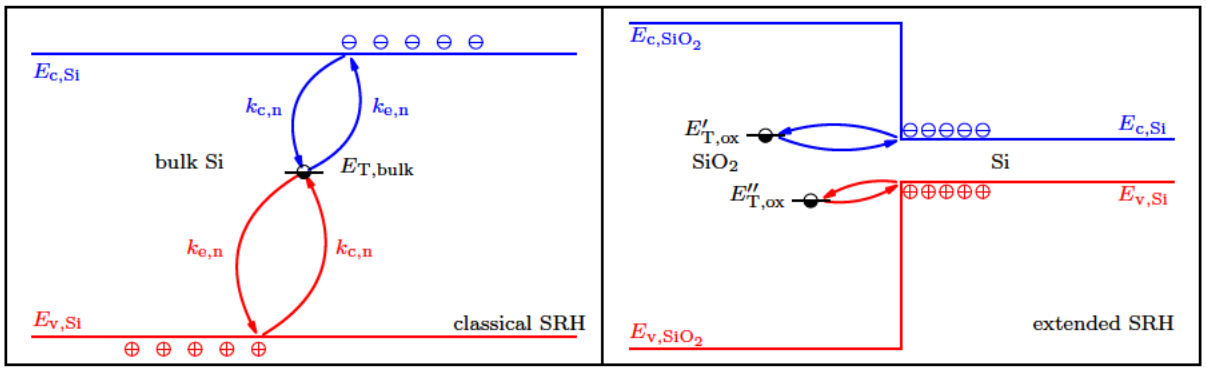

Figure 4.2. The classic SRH model was derived for the calculation of recombination (generation) rates of electrons and holes within a non-degenerate bulk semiconductor **(left)**. Later it was extended to account for charge trapping in interface and oxide defects **(right)** by simply adding a tunneling probability factor to the transition rates [62].

cross section. This factor describes the probability of electron capture per unit time, which is equivalent to the influx for a certain defect volume. The rates for electron emission $k_{e,n}$, hole capture $k_{c,p}$ and hole emission $k_{e,p}$ can be analogously derived. Under steady-state conditions, the capture and emission rates are equal, leading to the well known SRH recombination rate

$$R_{SRH} = \frac{C_n C_p \left(pn - p_1 n_1\right)}{C_n \left(n + n_1\right) + C_p \left(p + p_1\right)}. \tag{4.14}$$

This model can be extended to describe electron trapping at interface defects from the semiconductor conduction band. Using Boltzmann statistics, the transition rate reads

$$k_{c,n} = k_0 \exp\left(\frac{E_T - E_c}{k_B T}\right), \tag{4.15}$$

with $k_0 = \sigma_n v_{th} N_c$, where N_c denotes the effective density of states in the semiconductor conduction band. This model is still widely used for calculating interface trap densities from different device characterization methods [147], but also to calculate transient V_{th} shifts caused by charge capture and emission at interface and oxide defects [212]. In order to treat charge transfer rates to oxide defects, the energetic barrier (see Figure 4.2 right) at the oxide interface between the defect and the semiconductor has to be taken into account. It is usually included in (4.15) by simply introducing a tunneling probability ϑ to the prefactor [62]. However, it should be noted that this modeling approach only accounts for elastic tunneling processes, thereby fully neglecting any energetic exchange of the charge carrier with the surrounding phonon bath upon the charge transfer reaction. The reason for the success of the SRH model for the extraction of interface trap densities was recently demonstrated by Ruch *et. al* [213] by comparing it to NMP theory for interface defects ($P_{b,0}$-centers), with small relaxation energies. As will be derived in the next section, these relaxation energies E_R determine the strength of electron-phonon coupling, i.e. small E_R typically is a consequence of weak electron-phonon coupling. As a result, the obtained interface trap density spectra of

both modeling approaches as extracted via CP experiments are very similar, in contrast to such calculated for defects with larger E_R [213].

4.3 Non-Radiative Multi-Phonon Theory

As discussed in the previous section, the SRH model fails to describe charge transfer to and from oxide defects due to its purely elastic tunneling character that results in a "tunneling front" from the gate channel into the oxide and underestimation of defect charge transition time constants in thin oxides [77]. The missing model component within the SRH picture is the structural transformation of the defect upon charge capture. In order to compute exact transition rates for both radiative and non-radiative transitions, a full quantum mechanical treatment of the defect and the surrounding phonon bath is required [214]. However, such an approach is computationally unfeasible when applied to a large ensemble of defects with a wide variation of structural properties, as is the case in large area power MOSFETs with amorphous insulators. In this section, the detailed derivation of classical NMP transition rates from the exact quantum mechanical solution as given by Waldhoer [215] will be iterated. In such a form, the NMP model allows for transient computations for a large defect ensemble as is required to study charge trapping on a device level. It should be noted that these classical approximations of the transfer rates have shown to be able to capture the main features of charge trapping related effects in a large number of Si-based [216], as-well as novel 2D [144] and wide-band gap devices [162, 217]. Unlike in radiative transitions, in which the excess energy to overcome an energetic barrier is induced by a photon, both the energetic activation of the carrier and the dissipation of the excess energy upon relaxation to the final state's equilibrium configuration is due to interaction with multiple phonons. Therefore, for the derivation of the non-radiative multi-phonon transition rates, both electronic states ψ and vibrational states η as well as their mutual interaction have to be considered. By using the simplifications induced by the Born-Oppenheimer approximation [218], the transition rates from an initial vibronic state $|\psi_i \otimes \eta_\alpha\rangle$ to a final state $|\psi_j \otimes \eta_\beta\rangle$ can be calculated with Fermi's Golden Rule [219]

$$k_{i\alpha,j\beta} = \frac{2\pi}{\hbar}|M_{i\alpha,j\beta}|\delta\left(E_{j\beta} - E_{i\alpha}\right) \tag{4.16}$$

with the state eigenenergies $E_{i\alpha}$, $E_{j\beta}$ and the matrix element

$$M_{i\alpha,j\beta} = \langle \psi_i \otimes \eta_\alpha | \hat{H}' | \psi_j \otimes \eta_\beta \rangle . \tag{4.17}$$

Within the Born-Oppenheimer approximation, the first order perturbation Hamiltonian $\hat{H}'$ can be separated in an electronic $\hat{H}'_e$ and vibrational $\hat{H}'_v$ part. This approximation is justified due to the large difference in timescales, at which the electrons and nuclei respond to changes of their coordinates and momenta within the system and the matrix

element becomes [215]

$$\begin{aligned} M_{i\alpha,j\beta} &= \langle \psi_i \otimes \eta_{i\alpha} | \hat{H}'_{\mathrm{e}} + \hat{H}'_{\mathrm{v}} | \psi_j \otimes \eta_{j\beta} \rangle \\ &= \langle \eta_{i\alpha} | \eta_{j\beta} \rangle \langle \psi_i | \hat{H}'_{\mathrm{e}} | \psi_j \rangle + \langle \psi_i | \psi_j \rangle \langle \eta_{i\alpha} | \hat{H}'_{\mathrm{v}} | \eta_{j\beta} \rangle \\ &= \langle \eta_{i\alpha} | \eta_{j\beta} \rangle \langle \psi_i | \hat{H}'_{\mathrm{e}} | \psi_j \rangle . \end{aligned} \tag{4.18}$$

Due to the orthogonality of the different electronic wave-functions, the second term in (4.18) vanishes and the matrix element is determined by the overlap integral of initial and final vibrational states multiplied by the electronic matrix element, as stated by the Franck-Condon principle [220, 221].

As for typical operating conditions a large number of different vibrational modes will contribute to the overall rate, the thermal average over all partial rates (4.16) needs to be considered. With the initial state assumed to be in thermal equilibrium this results in the expression of the rate by a product

$$k_{ij} = A_{ij} f_{ij} \tag{4.19}$$

with A_{ij} being the electronic matrix element describing the electronic coupling between the defect wavefunction and the charge reservoir. The line-shape function f_{ij} describes the vibrational interactions in the classical high temperature limit, in which the difference between the vibrational energies $\Delta E_{i\alpha}$ is much smaller then the thermal energy $k_{\mathrm{B}}T$ and the classical barrier ε_{ij} defined by the crossing point between the Potential Energy Surfaces (PESs) of the initial and final state (c.f. Figure 4.3), i.e. $\Delta E_{i\alpha} < k_{\mathrm{B}}T < \varepsilon_{ij}$, and can be approximated by [215]

$$f_{ij} = \gamma_{ij} \exp\left(-\frac{\varepsilon_{ij}}{k_{\mathrm{B}}T} \right) . \tag{4.20}$$

The exponential term typically dominates f_{ij}, whereas the prefactor γ_{ij}, which depends on the particular PES shape, can be neglected [215].

Up to this point, the NMP formalism is fairly general. In order to reduce the complexity introduced by considering a full PES, the harmonic approximation of the one-dimensional Potential Energy Curve (PEC) of the neutral and negative state at their energetic minimum is used, as shown in Figure 4.3 (left). While, the PES shape is in general arbitrarily complex, the assumption of parabolic PECs has been shown to deliver a reasonably accurate approximation for important defect candidates in Si MOSFETs [215, 222]. For the calculation of charge transfer in MOSFETs, the rates (4.19) need to be calculated for the interaction with a carrier reservoir, which can be the channel conduction (valence) band or the gate contact. As the most relevant degradation mechanism for power switch applications is PBTI in a nMOSFET, the rates are derived for charge transfer between the channel conduction band and a defect, as shown in Figure 4.3 (right). The system's total energy in the neutral defect state is given by

$$V_0\left(q, E_{\mathrm{el}}\right) = V_{0,\mathrm{cb}}\left(E_{\mathrm{el}}\right) + V_{0,\mathrm{min}} + c_0\left(q - \Delta q\right)^2 \tag{4.21}$$

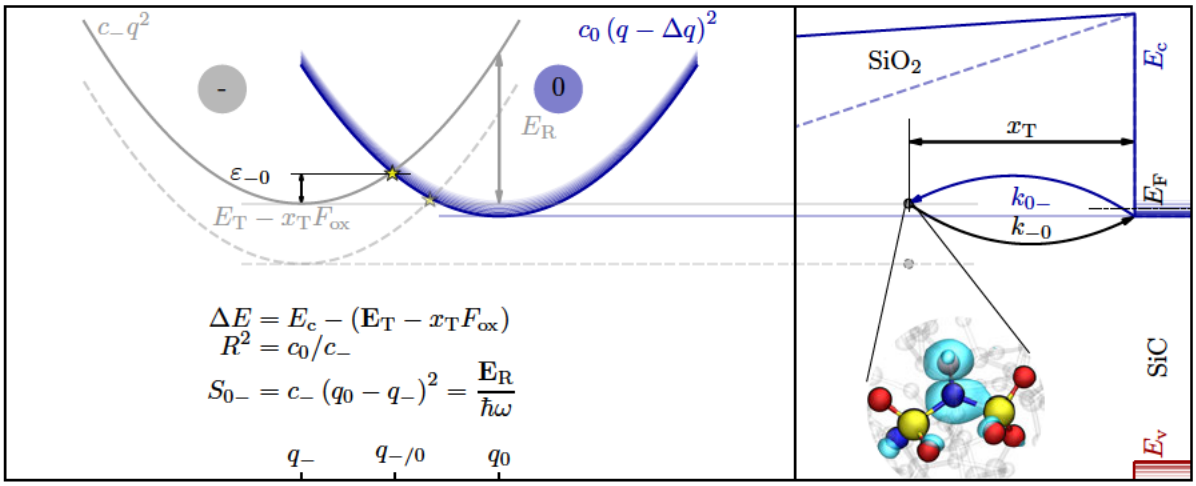

Figure 4.3. Harmonic approximations of the Potential Energy Curves (PECs) of two defect states along the dominant reaction coordinate q for charge transfer between the channel conduction band and the defect. In the classical high temperature limit the barriers ε_{-0} and ε_{0-} are determined by the intersection point. These barriers are uniquely defined by the relaxation energy E_R, the trap level E_T relative to the conduction band edge E_c and the curvature ratio R. Note that the minima of the parabolas shift relative to each other with different field strength across the oxide (c.f dashed lines).

with the curvature c_0 of the neutral PEC and the reaction coordinate difference between the minima $\Delta q = q_0 - q_-$. The energy of the electron E_{el} in the channel conduction band is included in the first term $V_{0,cb}$ and as indicated in Figure 4.3 each band state the electron can dwell in results in a separate PEC for the neutral state. When an electron with energy E_{el} is captured from the conduction band, the defect becomes negatively charged and the total energy reads [215]

$$V_- (q) = V_{0,cb} - E_{el} + V_{-,min} + c_- (q)^2 . \tag{4.22}$$

As only energy differences are relevant for calculating the transition rates, $V_{0,cb}$ cancels out. With the additional definition of the thermodynamic trap level $E_T = E_c - V_{0,min}$ the transition rate (4.19) becomes a function of E_{el} and E_T as [215]

$$k_{0-} (E_{el}, E_T) = A_{0-} (E_{el}, E_T) f_{0-} (E_{el}, E_T) . \tag{4.23}$$

For a continuous energy state reservoir an integration over the energy space is required yielding [215]

$$k_{0-} (E_T) = \int_{E_c}^{\infty} A_{0-} (E, E_T) D_c (E) f_n (E) f_{0-} (E, E_T) dE. \tag{4.24}$$

Thereby D_c denotes the density of states in the conduction band and the electron (hole) occupation f_n (f_p) of the reservoir needs to be weighed by Fermi-Dirac statistics [215]

$$f_n(E) = 1 - f_p(E) = \frac{1}{1 + \exp\left[(E - E_F) / (k_B T)\right]}. \tag{4.25}$$

Finally, to solve the integral (4.24) over the band states, further approximations are necessary, in order to reduce the numerical expense. First, by using the bandedge approximation, which assumes that the carriers within a semiconductor are predominantly located around the bandedges, the matrix elements and line-shape function can be factored out of the integral [215]

$$k_{0-}(E_T) = A_{0-}(E_c, E_T) f_{0-}(E_c, E_T) \int_{E_c}^{\infty} D_c(E) f_n(E) dE. \tag{4.26}$$

The left over terms in the integral simply yield the electron concentration

$$n = \int_{E_c}^{\infty} D_c(E) f_n(E) dE. \tag{4.27}$$

Furthermore, the electronic matrix element A_{ij} is typically approximated by a simple tunneling factor [78], which is reasonable given the strong localization of the defect wave functions [215]. This approximation yields [76]

$$A_{0-} = v_{th,n} \sigma_n \vartheta, \tag{4.28}$$

with the electron thermal velocity $v_{th,n}$, the capture cross section σ_n and the tunneling probability, which is typically calculated by using a Wentzel-Kramers-Brillouin (WKB) approximation [223], which gives analytical expressions for trapezoidal and triangular barriers. Together with the line-shape function in the classical limit, we arrive at the analytical expression for the electron capture rate from the conduction band edge [215]

$$k^c_{0-}(E_T) = n v_{th,n} \sigma_n \vartheta \exp\left(-\varepsilon_{0-} / (k_B T)\right) \tag{4.29}$$

Analogously and by using the relation $f_p(E) = f_n \exp\left((E_F - E) / (k_B T)\right)$ the electron emission rate is given by [215]

$$k^c_{-0}(E_T) = n v_{th,n} \sigma_n \vartheta \exp\left((E_F - E_T - \varepsilon_{-0}) / (k_B T)\right). \tag{4.30}$$

In the same fashion analytical rates for electron capture (emission) can be calculated for the interaction with the channel valence band k^v_{0-} (k^v_{-0}) and the gate contact k^g_{0-} (k^g_{-0}). The total capture and emission rates for solving the Master equation (4.4) are then given by the sum of all capture and the sum of all emission partial rates. As can be seen from the equations (4.29) and (4.30), the rates are dominated by the barriers $\varepsilon_{0-}, \varepsilon_{-0}$, which can be analytically calculated from the intersection point of the PECs in the harmonic

approximation (c.f. Figure 4.3) by [77]

$$\varepsilon_{-0} = E_{\mathrm{R}} \left(\frac{1 - R\sqrt{1 + (R^2 - 1)\, E_{0-}/E_{\mathrm{R}}}}{R^2 - 1} \right)^2 \tag{4.31}$$

with the relaxation energy E_{R} and the square root of curvature ratio $R = \sqrt{c_0/c_-}$. The reverse barrier ε_{0-} can be calculated by $\varepsilon_{0-} = \varepsilon_{-0} - E_{0-}$ with the energetic difference between the PECs minima $E_{0-} = E_{\mathrm{c}} - E_{\mathrm{T}} - x_{\mathrm{T}} F_{\mathrm{ox}}$ and F_{ox} the electric field strength within the oxide. The left panel of Figure 4.3 thereby illustrates how the minima of the PECs are shifted relative to each other by applying F_{ox} across the oxide in the gate stack, which imposes the gate bias dependence of the energy barriers. Note, that this is the main difference of the Grasser two-stage NMP model, compared to the Kirton and Uren model [70], which extended the SRH model by a bias independent Boltzmann factor, which is only a good approximation in the case of interface defects [77].

4.4 Two-State NMP Model for Trap-Trap Interaction

Up to this point, charge transfer between a reservoir and a defect has been described, while defect to defect charge transfer has been neglected. However, there are strong indications [224, CSJ4] that "charge hopping" between defects in dielectrica can lead to enhanced leakage currents in semiconductor devices.

4.4.1 Parameter Transformation

Therefore, with the goal of efficient computational models in mind, an approach to calculate defect to defect charge transfer will be presented. To minimize the parameters needed for a full-scale computation of both defect/reservoir and defect/defect NMP charge transfer reactions, as well as to contain the defect properties represented by the PECs for defect to reservoir charge reactions, as shown in Figure 4.3, a harmonic two-state PEC for defect/defect reaction will be derived from the corresponding defect/reservoir interaction.

The top two panels of Figure 4.4 represent the harmonic approximation for two-state PECs for two individual defects A and B, which can be denoted by repeating (4.21) and (4.22) with a negative state 1 and neutral state 2 by

$$V_1^{\mathrm{A,B}}(q) = V_{1,0}^{\mathrm{A,B}} + c_1^{\mathrm{A,B}} q^2 \tag{4.32}$$

$$V_2^{\mathrm{A,B}}(q) = V_{2,0}^{\mathrm{A,B}} + c_2^{\mathrm{A,B}} \left(q - \Delta q^{\mathrm{A,B}} \right)^2. \tag{4.33}$$

Under the assumption of linearly independent defect/reservoir state PECs and negligible relaxation of the charge reservoir, together with the requirement of $R^{\mathrm{A,B}} = 1$, a superpostion of the individual PECs yields an effective PEC for defect/defect charge reaction (detailed discussion about limitations and requirements is given in Section

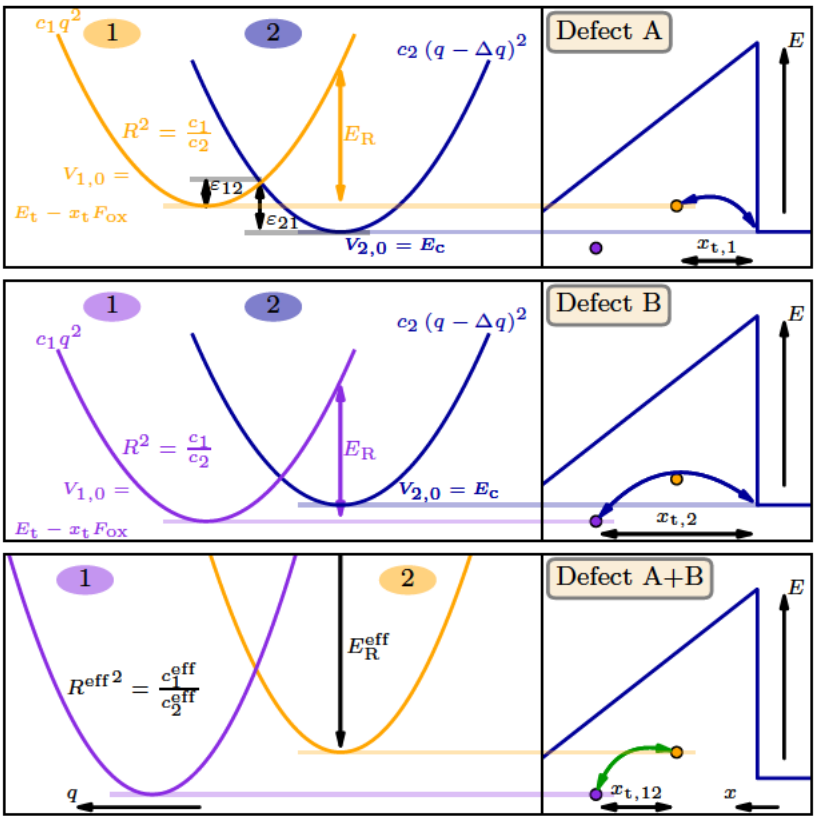

Figure 4.4. The PECs of two individual defects **(top)** and **(center)** are shown for charge transfer from/to the channel conduction band. Superposition of the two PECs results in an effective PEC **(bottom)** to calculate barriers for charge transfer between the defects. Assuming negligible reservoir relaxation, the effective parameters R^{eff} and E_R^{eff} are fully determined by the parameters of the individual defect/reservoir PECs. (taken from [CSJ4]))

4.4.2). For deriving the defect/defect transition PECs, the minima $V_{2,0}^{A,B}$ of the reservoirs in both reservoir/defect PECs are assumed to be the conduction band edge E_C of the semiconductor channel substrate. When an electron is transferred from defect A to B, the charge state of A changes from negative to neutral, while B changes its state from neutral to negative simultaneously. The superpostion for PECs of the individual states of defect A and B, together with a transformation of the reaction coordinate accordingly, results in the effective defect/defect charge transfer PEC

$$V_1^{\text{eff}}(q) = V_1^{B}(q) + V_2^{A}(-q) \tag{4.34}$$

$$V_2^{\text{eff}}(q) = V_1^{A}(-q) + V_2^{B}(q)\,. \tag{4.35}$$

State 1 thereby represents the state in which an electron dwells at the site of defect A (negatively charged) while defect B resides in its neutral state. The effective state 2 represents the opposite charge states. By inserting (4.32) and (4.33) into (4.34) and (4.35)

and subtracting $V_{2,0}^{\mathrm{A,B}} = E_{\mathrm{C}}$ from both equations, the effective states read

$$V_1^{\mathrm{eff}}(q) = V_{1,0}^{\mathrm{B}} + c_1^B q^2 + c_2^{\mathrm{A}}\left(\Delta q^A - q\right)^2 \tag{4.36}$$

$$V_2^{\mathrm{eff}}(q) = V_{1,0}^{\mathrm{A}} + c_1^A q^2 + c_2^{\mathrm{B}}\left(q - \Delta q^B\right)^2. \tag{4.37}$$

Thereby the energy reference level is shifted by $V_{2,0}^{\mathrm{A,B}}$, which is allowed as only energetic differences are of interest. By applying a quadratic extension and shifting the reaction coordinate by $\Delta q_1^{\mathrm{eff}} = -\left(c_2^{\mathrm{A}}\Delta q^{\mathrm{A}}\right)/c_1^{\mathrm{eff}}$ with $c_1^{\mathrm{eff}} = c_1^B + c_2^{\mathrm{A}}$ the equation is brought to the form of (4.33):

$$V_1^{\mathrm{eff}}(q) = V_{1,0}^{\mathrm{B}} - s_1 + \left(c_1^{\mathrm{B}} + c_2^{\mathrm{A}}\right)q^2 \tag{4.38}$$

$$V_2^{\mathrm{eff}}(q) = V_{1,0}^{\mathrm{A}} - s_2 + \left(c_1^{\mathrm{A}} + c_2^{\mathrm{B}}\right)\left(q + \Delta q^{\mathrm{eff}}\right)^2 \tag{4.39}$$

with $\Delta q^{\mathrm{eff}} = \Delta q_2^{\mathrm{eff}} - \Delta q_1^{\mathrm{eff}}$. Note that the shifts of the minima of the harmonic oscillators

$$s_1 = c_2^{\mathrm{A}}\left(\Delta q^{\mathrm{A}}\right)^2 - \frac{\left(c_2^{\mathrm{A}}\Delta q^{\mathrm{A}}\right)^2}{c_1^{\mathrm{eff}}} = c_2^{\mathrm{A}}\left(\Delta q^{\mathrm{A}}\right)^2\left(1 - \frac{c_2^{\mathrm{A}}}{c_1^{\mathrm{eff}}}\right) \tag{4.40}$$

$$s_2 = c_2^{\mathrm{B}}\left(\Delta q^{\mathrm{B}}\right)^2 - \frac{\left(c_2^{\mathrm{B}}\Delta q^{\mathrm{B}}\right)^2}{c_2^{\mathrm{eff}}} = c_2^{\mathrm{B}}\left(\Delta q^{\mathrm{B}}\right)^2\left(1 - \frac{c_2^{\mathrm{B}}}{c_2^{\mathrm{eff}}}\right) \tag{4.41}$$

are a result of different curvatures in the original PECs and vanish for the case of identical curvature ratios. The parameters R^{eff} and $E_{\mathrm{R}}^{\mathrm{eff}}$, which uniquely define the effective PEC, are readily described by the parameters used in (4.33) for defect/reservoir interaction yielding

$$R^{\mathrm{eff}} = \sqrt{\frac{c_1^{\mathrm{eff}}}{c_2^{\mathrm{eff}}}} = \sqrt{\frac{c_1^{\mathrm{B}} + c_2^{\mathrm{A}}}{c_1^{\mathrm{A}} + c_2^{\mathrm{B}}}}, \tag{4.42}$$

$$E_{\mathrm{R}}^{\mathrm{eff}} = c_1^{\mathrm{eff}}\Delta q^{\mathrm{eff}2} = c_1^{\mathrm{eff}}\left(\frac{c_2^{\mathrm{A}}\Delta q^{\mathrm{A}}}{c_1^{\mathrm{eff}}} + \frac{c_2^B\Delta q^{\mathrm{B}}}{c_2^{\mathrm{eff}}}\right)^2. \tag{4.43}$$

The case of two identical defects with $R^{\mathrm{A}} = R^{\mathrm{B}}$ and $E_{\mathrm{R}}^{\mathrm{A}} = E_{\mathrm{R}}^{\mathrm{B}}$ results in $R^{\mathrm{eff}} = 1$ and $E_{\mathrm{R}}^{\mathrm{eff}} = 2E_{\mathrm{R}}^{\mathrm{A,B}}$, which intuitively states that twice the energy is exchanged with the thermal bath upon electron transfer from defect to defect (as both sites undergo structural relaxation), compared to the defect / reservoir case. It has to be noted that it is inherently assumed that the carrier reservoirs are not undergoing structural relaxation upon charge capture or emission. Thus, $c_2^{\mathrm{A}} = c_2^{\mathrm{B}}$, which due to $R^{\mathrm{eff}} = \sqrt{\left(R^{\mathrm{A}} + 1\right)/\left(R^{\mathrm{B}} + 1\right)}$ is only a function of the curvature ratios of the defect PECs and with the restriction of $R^{\mathrm{A}} = R^{\mathrm{B}} = 1$ the effective ratio is also $R^{\mathrm{eff}} = 1$ for non-identical defects with $E_{\mathrm{R}}^{\mathrm{A}} \neq E_{\mathrm{R}}^{\mathrm{B}}$.

By calculating the barriers with the effective parameters according to (4.31) and following the derivations given in Section 4.3, using a discrete density of states at E_{T} with the trap density N_{T}, the analytical expressions for the rates for defect/defect charge

transfer are

$$k_{12,21}\left(f_{1,2}, E_{\mathrm{T};1,2}\right) = N_{\mathrm{T}}\left(E_{\mathrm{T};1,2}\right) f_{1,2} v_{\mathrm{th},n,\mathrm{ox}} \sigma \vartheta \exp\left(-\varepsilon_{12,21} / \left(k_{\mathrm{B}} T\right)\right). \tag{4.44}$$

The fundamental advantage of the transformation of the PECs from the defect/reservoir to the defect/defect interaction case is the reduced parameter set, as only one reaction coordinate diagram needs to be parameterized. These parameters can be readily compared to such derived from DFT computations for suspected defect candidates [81]. However, the superposition of defect states can only be considered valid within the limits that are discussed in the following section.

4.4.2 Limitations

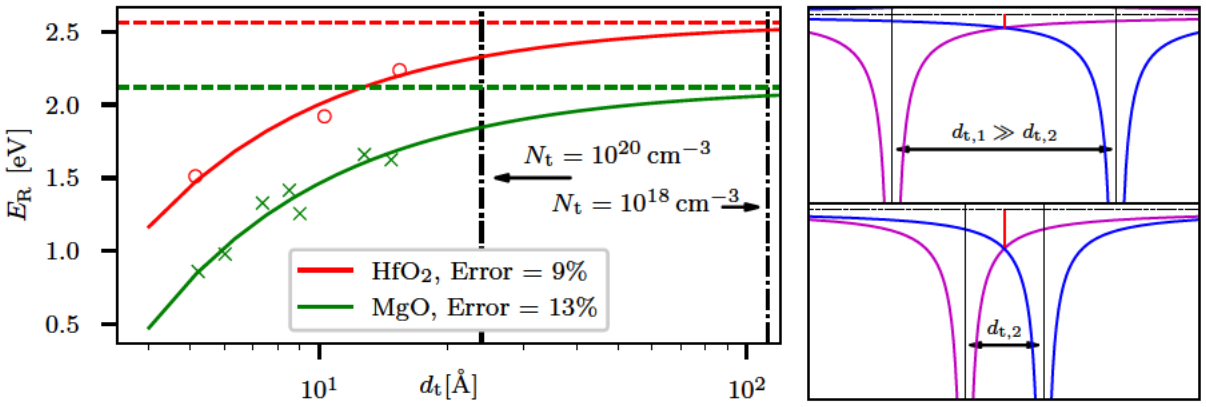

Figure 4.5. Large defect densities and therefore low average distances between the defects lead to a strong coupling, resulting in a reduced relaxation energy and energetic barriers for defect to defect charge transfer, as calculated by constrained-DFT for defects in HfO_2 [225] and MgO [226] **(left)**. A schematic for one-dimensional Coulomb potentials with large **(top, right)** and small distance **(bottom, right)** between the defects illustrates the exponential barrier reduction (red) with decreasing distance (taken from [CSJ4])

As mentioned in the previous section, a superposition of defect/reservoir charge transfer PECs is strictly valid for linearly independent potentials only. For the exact quantum mechanical solution, a Coulomb interaction term needs to be considered in the electronic Hamiltonian of the many-body Schrödinger equation. By using constrained DFT including exact Hartree-Fock exchanges, the reduction of the relaxation energies of the potential energy surfaces for defect to defect electron transfer has been calculated as a function of their mutual distance for defects in MgO [226] and HfO_2 [225]. The results of these calculations are reprinted in Figure 4.5 together with an extrapolation to large distances using a Marcus-like functional of the form [226]

$$E_{\mathrm{R}} = E_{\mathrm{R},\infty}\left(1 - C/d_{\mathrm{t}}\right). \tag{4.45}$$

$E_{\mathrm{R},\infty}$ was thereby calculated for fully decoupled defects in the dilute limit. The fitting constant C has the physical meaning of a cavity (for ions in solvents in the original

work of Marcus), however, this interpretation may not apply for electron transfer in solids [227]. Nonetheless, the general form of E_R as a function of distance as given in (4.45) can still be considered valid. The results show that even at large defect densities of $N_t = 10^{20}\,\mathrm{cm}^{-3}$ corresponding to low average distances calculated when assuming close-packed spheres

$$d_t = \frac{1}{\sqrt{2}}\left(\frac{4}{N_t}\right)^{\frac{1}{3}} \approx 2.3\,\mathrm{nm}, \tag{4.46}$$

the relative errors due to E_R reduction are about 10 %.

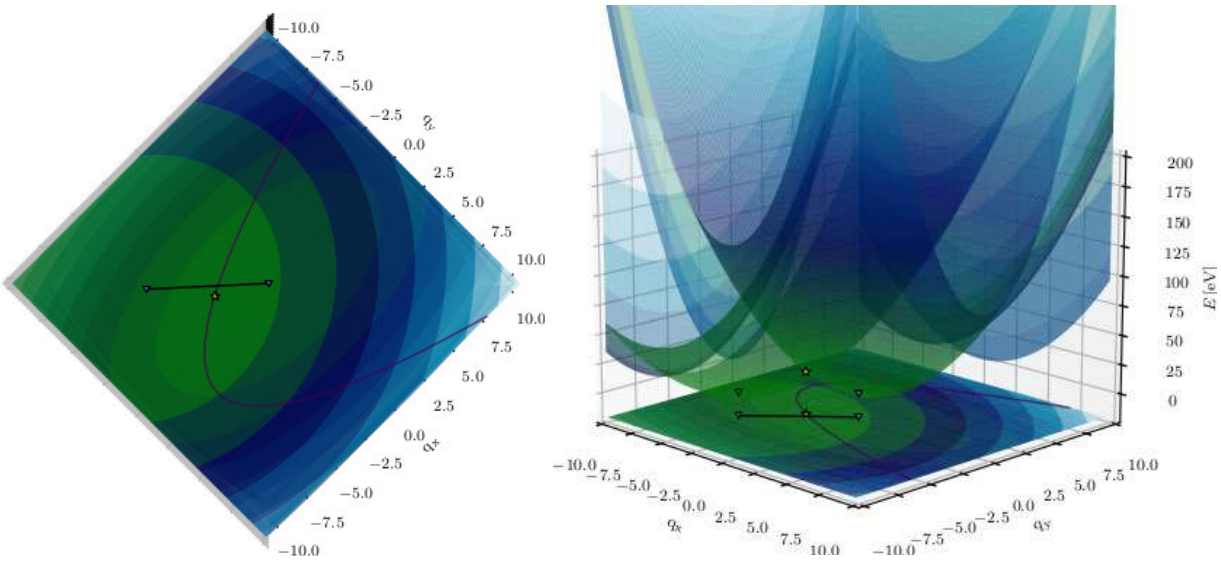

Figure 4.6. A two dimensional representation of the PES, with harmonic approximations in both lateral reaction coordinates q_x and q_y, illustrates a slight offset of the energetic minimum of the transition point (star) between the two state minima, compared to the intersection of the one-dimensional approximation (direct line), resulting in enlarged barriers.

Another restriction for the PECs superposition in Section 4.4.1 is given by the requirement of the curvature ratios satisfying $R^A = 1/R^B$. This seems quite restrictive, however, recent DFT investigations for defects in SiO_2 show that the curvature ratios are close to 1 and hence fulfill this restriction. Besides this case study in SiO_2, $R = 1$ is also well justified and a frequently used approximation for defects in other materials [228, 229, 114]. Additionally, if the requirement is not met, the minimum energy crossing point of both two-dimensional PESs does not lie on the direct line between the two minima of the states, as shown in Figure 4.6. A correct calculation of the intersection point would then require the calculation of the energetic minimum of the transition point of the two dimensional PES, which exceeds the acceptable computational effort for a device reliability study by far.

Additionally, the choice of $R = 1$ prevents a cross-correlated defect parameter search for R and E_R, when trying to fit experimental data, as will be outlined in Section 4.8. With the NMP model for defect to defect charge transfer outlined and keeping its

limitations in mind, the next section will present its application for the calculation of trap-assisted leakage currents.

4.5 Efficient Framework for MOS Gate Leakage Currents

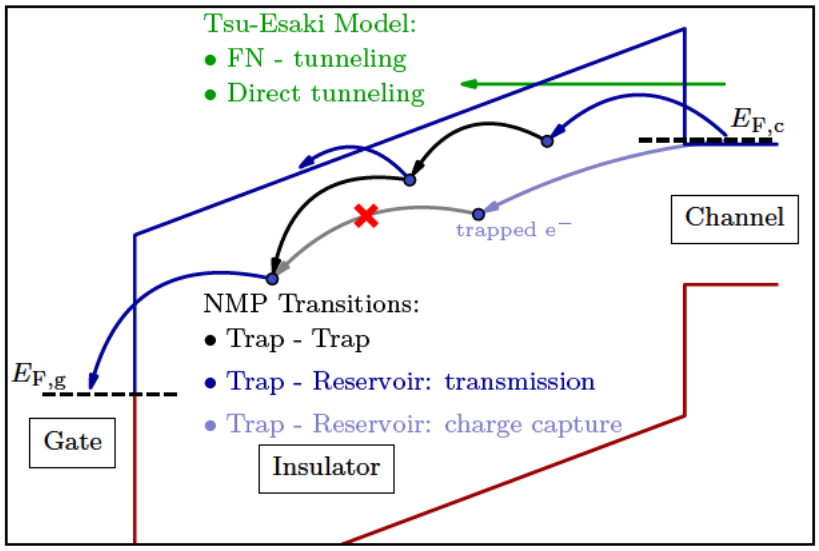

Figure 4.7. Different gate leakage current mechanisms can be observed in a MOS gate stack. Fowler-Nordheim and direct tunneling currents (green) are the dominating leakage mechanism in thin and mostly defect free dielectrics. In more defective oxides, trap assisted tunneling over multiple (black) or single defects (blue) can be measured in addition to transient charge trapping currents (taken from [CSJ4]).

As stated in Chapter 1, several leakage current mechanisms through the dielectric in a gate stack are possible. In Figure 4.7, the most common tunneling mechanisms are schematically shown, with direct and Fowler-Nordheim Tunneling currents through an energetic barrier and trap assisted currents via one or multiple defects. In this section, a standard model for calculating currents through energetic barriers together with a derivation for the charge hopping mechanism following [230] based on a generalized Ramo-Shockley theorem [231] will be re-framed to be applicable for a MOS gate stack.

4.5.1 Tsu-Esaki Model

The tunneling current through an energetic barrier that separates two electrodes can be computed with the so called Tsu-Esaki formalism [232], in which the current density at the semiconductor channel for electrons and holes is expressed as

$$J_{\mathrm{TE},e} = \frac{4\pi m_e q_0}{h^3} \int_{E_{\mathrm{CB}}}^{\infty} \vartheta_{\mathrm{WKB}}(E)\, N_e(E)\, \mathrm{d}E \tag{4.47}$$

$$J_{\mathrm{TE},h} = \frac{4\pi m_h q_0}{h^3} \int_{-\infty}^{E_{\mathrm{VB}}} \vartheta_{\mathrm{WKB}}(E)\, N_h(E)\, \mathrm{d}E. \tag{4.48}$$

with the effective electron density of states (hole) mass $m_{e(h)}$ in the semiconductor in the plane parallel to the interface [233], the elementary charge q_0, the Planck constant h, a tunneling probability ϑ and the so-called supply function N. Assuming Fermi-Dirac statistics at both contacts, the supply function for electron tunneling is given by

$$N_e(E) = k_B T \ln\left(\frac{1+\exp\left(-\frac{E-E_{F1}}{k_B T}\right)}{1+\exp\left(-\frac{E-E_{F2}}{k_B T}\right)}\right). \tag{4.49}$$

In order to efficiently calculate the tunneling probability, the WKB approximation can be applied for thin and energetically high barriers as [223]

$$\vartheta_{WKB}(E) = \exp\left(-\frac{4\pi}{h}\int_{x_1}^{x_2}\sqrt{2m_{e,diel}\left(W(x)-E\right)}dx\right) \tag{4.50}$$

with $m_{e,diel}$ denoting the effective electron mass in the dielectric. Thereby, the integral is

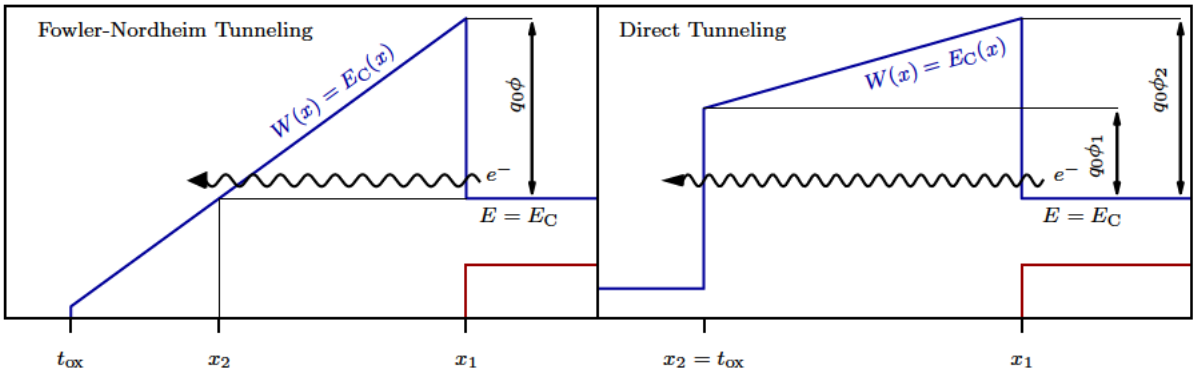

Figure 4.8. A triangular energetic barrier with the height $q_0\phi$, as typically observed at high field strengths F_{ox} and thicker oxides, eventually leads to FN-like tunneling **(left)**, with the electron tunneling to the oxide conduction band. A trapezoidal barrier, typically seen for thin oxides at medium F_{ox}, leads to direct tunneling (DT), where the electron has to tunnel through the oxide layer **(right)**.

carried out from position x_1 to x_2 over the energetic barrier with shape $W(x)$. In the case of a triangular barrier, as shown in Figure 4.8 (left), (4.50) evaluates to the commonly known FN formula for electron tunneling [234]

$$\vartheta_{WKB}(E) = \exp\left(-\frac{4\sqrt{2m_e}}{3\hbar q_0 F_{ox}}\left(q_0\phi - E\right)^{\frac{3}{2}}\right) \tag{4.51}$$

with the potential barrier ϕ, the electron energy E and the electrical oxide field strength $F_{ox} = (V_G - \phi_s)/t_{ox}$. Also, for a trapezoidal barrier (Direct Tunneling (DT)) as shown in Figure 4.8 (right) with the barrier heights $\phi_2 > \phi_1$ an analytic expression evaluates to

$$\vartheta_{WKB}(E) = \exp\left(-\frac{4\sqrt{2m_e}}{3\hbar q_0 F_{ox}}\left(\left(q_0\phi_2 - E\right)^{\frac{3}{2}} - \left(q_0\phi_1 - E\right)^{\frac{3}{2}}\right)\right). \tag{4.52}$$

From (4.48) and (4.50) it can be seen that the material parameters, i.e. the energy barrier and effective tunnel masses, within the exponent in the WKB factor strongly influence the current density in the inversion and accumulation regime, in which the supply function (4.49) is non-zero. Together with the exact knowledge of the oxide thickness t_{ox} and the dielectric constant ε, these parameters determine the accuracy of the Tsu-Esaki computation.

Upon careful parameter calibration, the capability of the model to calculate accurate tunneling currents through defect free dielectrics has been demonstrated. By considering this best case scenario, the suitability of dielectrics for new material combinations has been demonstrated with our implementation in Comphy for a large number of compounds considered as insulators for two-dimensional channel materials in [CSJ5]. It was thereby found that hexagonal boron-nitride (hBN), which was often proposed as dielectric for 2D materials, does not meet the requirements of low gate leakage current for pMOS fabrication even in the defect-free case [CSJ5]. As for real devices the leakage current is eventually further enhanced due to trap-assisted tunneling, the next section outlines the calculation of such a hopping current.

4.5.2 Charge Hopping Model

As for a charge hopping current the local current density does not fulfill the continuity condition, i.e. charges "vanish" at one defect site and "pop up" at another instantaneously. In this case, the current at the gate contact can be written as [230]

$$I_{\mathrm{G}} = -\int_{\partial D_{\mathrm{G}}} \left(\vec{J} + \frac{\partial \vec{D}}{\partial t}\right) \cdot \mathrm{d}\vec{A} \tag{4.53}$$

with the integral taken over the device surface at the gate contact area ∂D_{G}. By selecting a test-function $h_{i=\mathrm{G}}$ as the solution of the Laplace equation at the gate contact and $h_i = 1$ for all other contacts and by using the divergence theorem, the integral over the whole device volume reads [230]

$$I_{\mathrm{G}} = -\int_D \boldsymbol{\nabla} \cdot \left[h_i \left(\vec{J} + \frac{\partial \vec{D}}{\partial t}\right)\right] \mathrm{d}V = -\int_D \underbrace{\boldsymbol{\nabla} h_i \cdot \left(\vec{J} + \frac{\partial \vec{D}}{\partial t}\right)}_{=0} + h_i \boldsymbol{\nabla} \cdot \left(\vec{J} + \frac{\partial \vec{D}}{\partial t}\right) \mathrm{d}V. \tag{4.54}$$

The left term in the right hand side integral thereby vanishes due to the choice of h and a conduction current of $\vec{J} = \vec{0}$ at the contact. Due to the local violation of the continuity condition in the Pauli-Master equation [235], the current is not divergence free and is given on a one-dimensional grid between points i and j as

$$\boldsymbol{\nabla} \cdot \left(\vec{J} + \frac{\partial \vec{D}}{\partial t}\right) = q_0 k_{ji} \left(1 - f_j\right) f_i \tag{4.55}$$

by using (4.10) with $f_{i/j}$ being the occupations of the two trapping sites. For a bias difference of $V_G - \phi_s$ between gate and channel interface, the test function evaluates to $h_i = \frac{x_i - x_j}{t_{ox}}$ with the oxide thickness t_{ox}. Inserting (4.55) into (4.54) the current at the gate contact evaluates to the generalized Shockley-Ramo theorem [236, 231], which yields the displacement currents observed at the gate due to each charge movement within $\mathcal{D}$, to

$$\begin{aligned} I_{G,TAT} = & \underbrace{C_{ox}\frac{dV_G}{dt}}_{\text{displacement current}} + \underbrace{q_0 \sum_i^N k_{e,i,gate} f_i - k_{c,i,gate}\left(1 - f_i\right)}_{\text{single-TAT current}} \\ & + \underbrace{q_0 \sum_i^N \sum_{j \neq i}^N k_{e,ij} f_i \left(1 - f_j\right) \frac{x_i - x_j}{t_{ox}}}_{\text{multi-TAT current}} \\ & + \underbrace{q_0 \sum_i^N \left[k_{c,i,channel}\left(1 - f_i\right) - k_{e,i,channel} f_i\right] \left(1 - \frac{x_i}{t_{ox}}\right)}_{\text{charge trapping current}} \end{aligned} \tag{4.56}$$

with the oxide capacitance $C_{ox} = \varepsilon_{ox} WL / t_{ox}$. The rates in (4.56) consist of both reservoir to defect interactions for the TAT current and charge trapping current contributions and defect to defect rates for the multi-TAT current contribution. This charge hopping current model has been implemented in Comphy, as will be discussed in the next section.

4.6 Compact Physics Framework (Comphy)

The development of the Compact Physics Framework (Comphy) [208, 216] aimed at reducing the computational effort needed to extract the large number of parameters as required for detailed BTI models, i.e. the four-state NMP or the GSHR model which are partly implemented in commercial TCAD frameworks [237, 238, 239]. However, it has been demonstrated that the mean BTI degradation observed in large area MOSFETs can be explained physically with a two-state NMP model, which requires only a reduced defect parameter set. Comphy and its implementation of the two-state model have been initially applied to reproduce the degradation for a large number of process splits with gate stacks employing SiO_2 and HfO_2 including different gate contact materials [240]. As a large ensemble of defects can be handled efficiently, it makes the framework particularly suitable for calculating BTI in SiC-MOSFETs, allowing for the extraction of physical defect parameters by using established material parameters. In the following, the main physical models for providing the electrostatic quantities required to calculate the charge transfer kinetics and transient ΔV_{th} will be outlined. Also, the extension of the framework for efficiently calculating gate leakage currents employing the models presented in the previous section will be presented.

4.6.1 Electrostatic Quantities

In order to calculate the effective trap level of a defect relative to the channel carrier reservoirs, the relation of the applied gate bias to the surface potential at the channel / oxide interface needs to be known. Therefore, by assuming a uniform doping concentration and charge neutrality exists deep in the bulk semiconductor (far away from the interface), the approximation of the surface charge Q_s as a function of the surface potential φ_s can be used, which reads [32]

$$Q_\mathrm{s}\left(\varphi_\mathrm{s}\right) = \pm\frac{\sqrt{2}k_\mathrm{B}T}{q_0 L_\mathrm{D,e}} \sqrt{\frac{p_0}{n_0}\left(e^{-q_0\varphi_\mathrm{s}/\left(k_\mathrm{B}T\right)} + q_0\varphi_\mathrm{s}/\left(k_\mathrm{B}T\right) - 1\right) + \left(e^{q_0\varphi_\mathrm{s}/\left(k_\mathrm{B}T\right)} - q_0\varphi_\mathrm{s}/\left(k_\mathrm{B}T\right) - 1\right)}. \quad (4.57)$$

Thereby, $L_\mathrm{D,e} = \sqrt{k_\mathrm{B}T\varepsilon_\mathrm{s}/\left(n_0 q_0^2\right)}$ denotes the electron Debye length, ε_s the semiconductor permittivity and n_0, p_0 the carrier concentrations at thermal equilibrium, which are derived from the doping concentrations $N_\mathrm{A}, N_\mathrm{D}$ and the band gap E_G [208]. In the case of a charge free insulator, the potential drop across the gate stack is given by

$$V_\mathrm{G} = \frac{Q_s\left(\varphi_\mathrm{s}\right)WL}{C_\mathrm{ox}} + \varphi_\mathrm{s} + \frac{\Delta E_\mathrm{W}}{q_0} \quad (4.58)$$

with the work-function difference ΔE_W between the gate and channel materials. As the inverse relation $\varphi_\mathrm{s}\left(V_\mathrm{G}\right)$ is required to calculate the channel electrostatic quantities like Fermi-Level E_F and carrier densities n, p with employing the Joyce-Dixon approximation [241], (4.58) is solved numerically for φ_s employing an iterative scheme. Figure 4.9 shows a comparison of the approximations used in Comphy to a full numerical solution of the Poisson equation across a poly-Si/SiO_2/SiC stack with a Finite-Volume method and Fermi-Dirac statistics.

4.6.2 Threshold Voltage Shift

With the surface potential derived in the previous section, the Fermi-Levels in the channel and gate are known and can be used to calculate the transition rates (4.29) and (4.30) for each input tuple $\left(V_\mathrm{G}, t, T\right)$. These allow the computation of the transient defect occupancy $p(t)$ using (4.9). By using a simple charge sheet approximation [242, 72], the perturbation of the potential due to N defects reads

$$\Delta\varphi = -q_0 C_\mathrm{ox}\sum_i^N p_i\left(1 - \frac{x_\mathrm{T,i}}{t_\mathrm{ox}}\right) \quad (4.59)$$

with x_T being the distance of the defect from the channel/oxide interface.

Often a solution of the occupation for AC signals is sought in order to calculate ΔV_th within circuit simulations. Therefore, an efficient numerical solution for the occupations

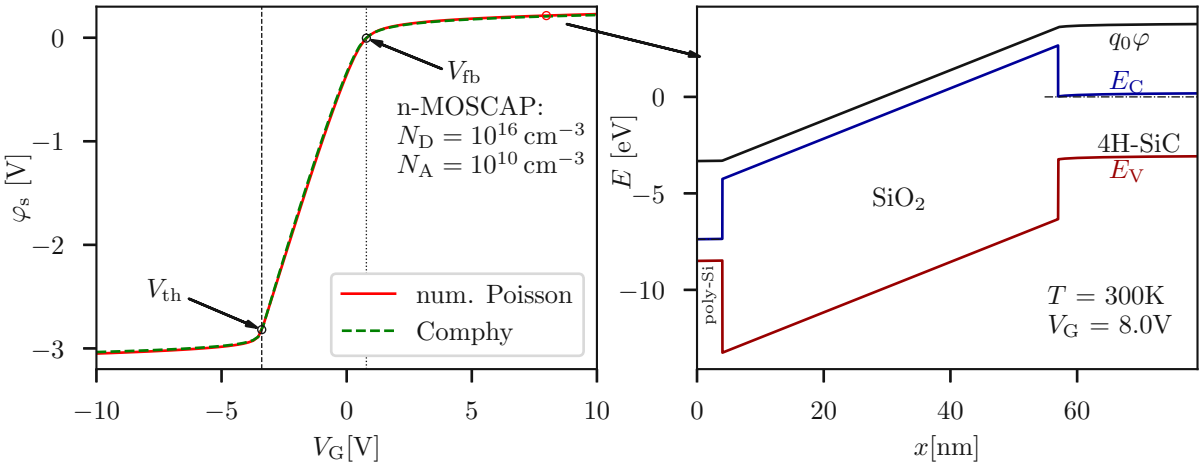

Figure 4.9. Comparison of the numeric solution of the Poisson equation for $\varphi_s\,(V_G)$ of a n-MOSCAP with a charge free oxide shows good agreement with the efficient approximations used in Comphy **(left)**. The full numeric solution of the Poisson equation employing Fermi-Dirac statistics is shown in a band diagram for strong accumulation **(right)**.

given by a two-state Master equation for arbitrary shaped periodic two-level bias signals has been proposed by Giering *et. al* [243]. For the special case of a periodic digital gate AC signal with period $t_p = 1/f = t^H + t^L$ at biases V_G^H at high level and V_G^L at low level an analytical expression, evaluated after n periods, can be found by [208]

$$p_2\left(t_0 + nt_p\right) = p_2\left(t_0\right) P_1\left(t_0 + t_p, t_0\right)^n + \frac{1 - P_1\left(t_0 + t_p, t_0\right)^n}{1 - P_1\left(t_0 + t_p, t_0\right)} P_2\left(t_0 + t_p, t_0\right) \tag{4.60}$$

with

$$P_1\left(t_0 + t_p, t_0\right) = \exp\Big(- \left(k_{12,H} + k_{21,H}\right) t^H - \left(k_{12,L} + k_{21,L}\right) t^L \Big), \tag{4.61}$$

$$\begin{aligned} P_2\left(t_0 + t_p, t_0\right) = &- \frac{k_{12,H}}{\left(k_{12,H} + k_{21,H}\right)} \left(e^{-(k_{12,H}+k_{21,H})t^H} - 1 \right) \\ &- \frac{k_{12,L}}{\left(k_{12,L} + k_{21,L}\right)} \left(e^{-(k_{12,L}+k_{21,L})t^L} - 1 \right) e^{-(k_{12,H}+k_{21,H})t^H}. \end{aligned} \tag{4.62}$$

The availability of an analytic expression to calculate the defect occupation for periodic AC signals allows for efficient extrapolation of the device degradation ΔV_{th} and therefore ΔR_{on} under operating conditions as will be shown in Section 5.1.6.

4.6.3 Gate Leakage Current Computation

Irrespective of the fact that the Poisson equation is only solved in one dimension within the Comphy framework, the derivation of the correct spatial tunneling distance d_T requires a three dimensional defect distribution. Therefore, based on the input quantities defect density N_T and average defect number $\overline{N}$ that should be sampled, a volume with $V_i = A_i t_{diel}$ is defined that fulfills $V = \overline{N}/N_T$. The dielectric thickness

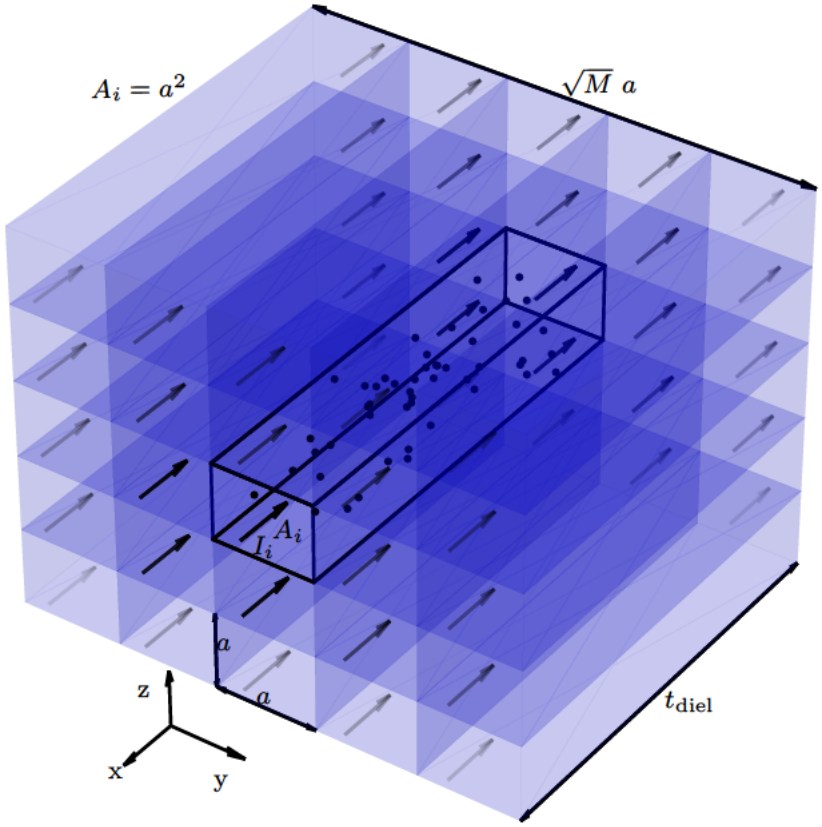

Figure 4.10. To account for the amorphous nature of the most common gate insulators, the defects in Comphy are sampled in three dimensional slabs, with boundaries on the gate contact and channel interface. The volume $V = a^2 t_{\text{diel}}$ of the slabs is calculated to contain a given mean number of defects $\overline{N}$ for a density N_{T}, with the actual number of traps N being Poisson distributed within the M slabs. (taken from [CSJ4])

is fixed by the gate stack input quantities, and $A_i = a^2$ a square area. Within this volume, the defects are sampled using a Monte-Carlo scheme according to their uniform spatial and normally distributed energetic parameters. To avoid low defect densities, in particular those which lead to d_{T} below 1 nm, defects that result in smaller d_{T} to any neighboring defect are removed from the drawn sample and re-drawn, i.e. rejection sampling is implemented. The actual number of defects N within a slab is further sampled based on a Poisson distribution, as such is observed in small area devices [244, 156], with probability of N defects within the slab given by

$$P(N) = \frac{\mathrm{e}^{-\overline{N}}\overline{N}^{N}}{N!}. \tag{4.63}$$

For the energetic defect parameters (E_{T},E_{R}) samples are drawn based on a normal distribution with ($\sigma_{E_{\text{T}}}$, $\sigma_{E_{\text{R}}}$). The expectation values and variations of the current density and threshold voltage shifts can then be calculated from repeating the simulation on M slabs, as schematically shown for the simulation space in Figure 4.10.

The computation of the currents in steady state is based on solving the coupled system of equations (4.10) for zero derivative, which reads

$$k_{\text{in},i}\left(\vec{f}\right)\left(1-f_i\right) = k_{\text{out},i}\left(\vec{f}\right) f_i \tag{4.64}$$

with the total in and out rates $k_{\text{in},i}$ and $k_{\text{out},i}$ at each defect i, which consist of reservoir and defect interaction rates. Therefore, for each step k with the input tuple (t_k, $V_{\text{G,k}}$, T_k) all rates as described in Section 4.4 are computed and (4.64) is solved with a Newton scheme. For the transient case, the equation is discretized with an implicit Euler scheme, resulting in the occupations as

$$f_{i,k} = \left[\left(1-f_{i,k}\right) k_{\text{in},i,k-1}\left(\vec{f}_{k-1}\right) - f_{i,k} k_{\text{out},i,k-1}\left(\vec{f}_{k-1}\right)\right]\left(t_k - t_{k-1}\right) + f_{i,k-1}. \tag{4.65}$$

The discrete equation can then again be solved with a Newton scheme and the resulting occupations together with the individual rate contributions. With the occupations, the TAT current (4.56) can be evaluated ant the total gate current sums up from the contributions of the TAT and band-to-band current $I_{\text{G,TE}}$ (Tsu-Esaki) (4.48) to a total gate current

$$I_{\text{G,tot}} = I_{\text{G,TAT}} + I_{\text{G,TE}}. \tag{4.66}$$

With the full modeling framework at hand to compute both TAT currents via single and multiple steps, the significance of a charge transition between two contacts via multiple defects in terms of its contribution to a total leakage current will be evaluated in the following section.

4.7 The Multi-TAT Regime

A multi-TAT current or charge hopping current with charge transitions involving numerous defects, has been suggested to contribute to gate leakage currents in a number of previous works [126, 245, 110, 224]. However, multiple mechanisms can lead to leakage currents, and the importance of multi-TAT has not been quantified in terms of its contribution to these total leakage currents. In this section, by using the physical model for calculating charge hopping currents as described in the previous sections, a quantification of the multi-TAT conduction shall be given. Thus, in order to analyze the requirements of a material stack employing a defective dielectric layer for multi-TAT to significantly contribute to a total leakage current density, it is necessary to analyze the average number of defects $\langle N \rangle$ which act as charge transition centers. Therefore, $\langle N \rangle$ is defined as

$$\langle N \rangle = \frac{\sum_i I_{i,\text{min}} N_i}{\sum_i I_{i,\text{min}}} \tag{4.67}$$

with $I_{i,\min}$ being the minimum current between two defects or reservoir and defect and N_i denoting the number of defects within the path i. The summation is carried out over all possible percolation paths and divided by the total current.

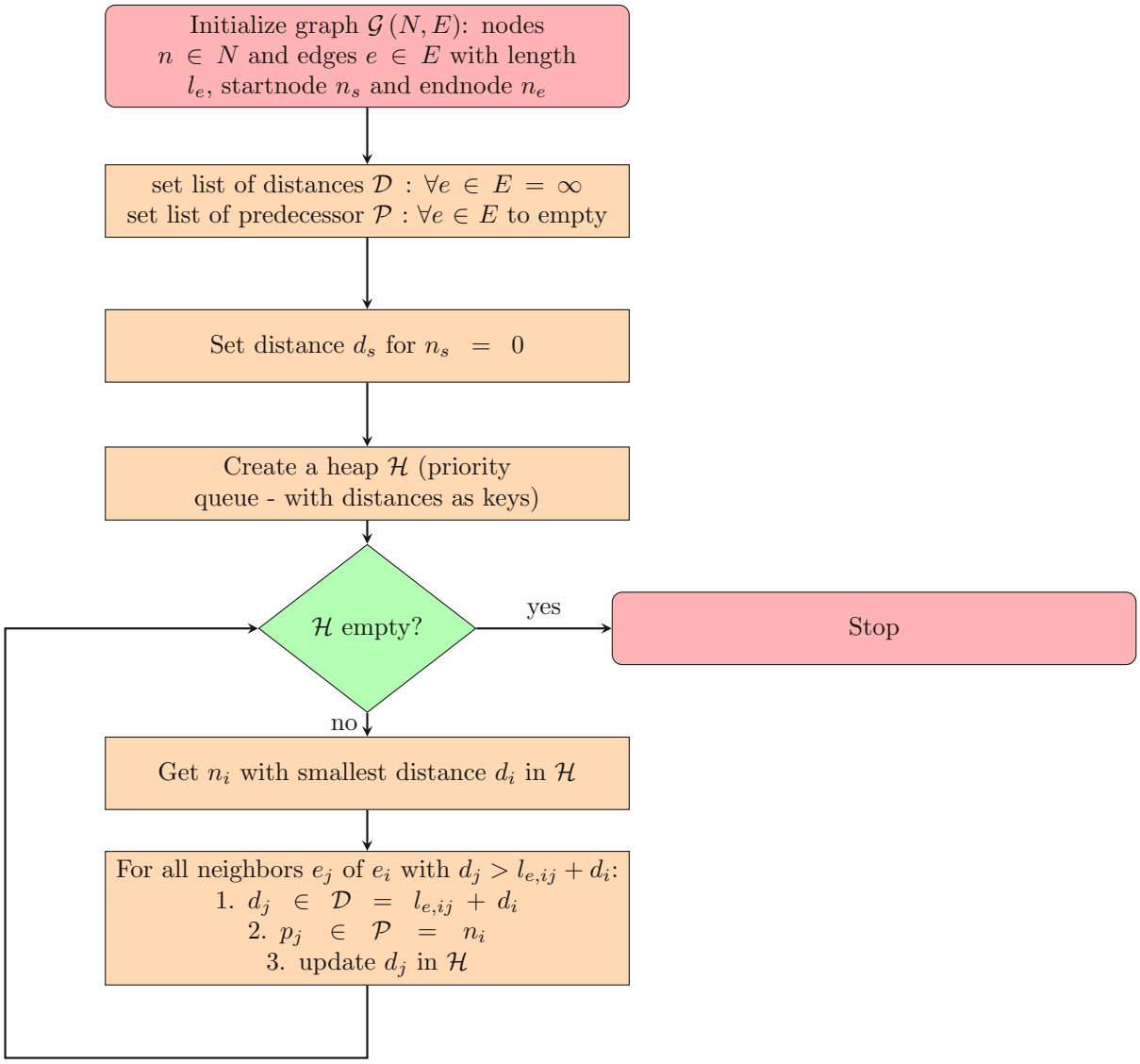

Figure 4.11. Flow diagram of the Dijkstra algorithm employing a heap as priority list. The utilization of a heap reduces the complexity to $\mathcal{O}(|N|\log|N| + |E|)$ [246]. The algorithm stops if the heap $\mathcal{H}$ is empty, i.e. the distance to all nodes has been calculated. The length of the list of distances to the end node n_e (gate) is equivalent to the number of defects in the TAT current percolation path.

For that, all individual percolation paths i and their contribution I_i to the total current need to be identified. In order to efficiently identify the path with the largest, second largest and so on contribution path finding algorithms, as mainly used for instance in navigation systems, provide a perfect solution. Therefore, the single-source shortest-path algorithm of Dijkstra [247] is used in an adapted way to calculate all percolation paths and the number of contributing defects in each. Hence, after calculating the charge transitions between all defects and the reservoirs for a certain (V_G,t,T) as described in Section 4.3 in a post- processing step, a graph connecting all the defects is created to

execute the algorithm. Each defect represents a node of the graph, with the channel representing the starting and the gate the end node. Since a shortest path algorithm is used, a distance metric on this defect connection graph needs to be introduced. As the search should identify the dominant current paths, the Markov transition probabilities are used as the metric on the graph. Thus, the edges between the nodes representing the current that is conducted in between the defects are weighed by the inverse of the multi-TAT terms of (4.56), i.e. Markov transition probabilities. In the same way the edges that connect the nodes with the starting node are weighed by the inverse of the charge trapping term and the ones connected to the gate by the TAT current term.

The algorithm is shown in the flow diagram in Figure 4.11 and first initializes two lists $\mathcal{D}$ and $\mathcal{P}$ that are required in the standard form of the algorithm to store the distances of the start node to the actual node. Within $\mathcal{D}$, the shortest path is stored and $\mathcal{P}$ represents a list with the preceding nodes in that path. The Dijkstra algorithm is then started by setting the distance to the start node at n_s to $d_s = 0$. For increasing the performance to $\mathcal{O}\left(|N|\log|N| + |E|\right)$ [246], with N nodes and E edges, a Fibonacci heap $\mathcal{H}$ is used with the keys of the nodes n_i being the distances d_i from the starting node.

The priority list is then reduced in each iteration by removing the node n_i with the smallest distance, and updating all adjacent node distances and setting their predecessors to n_i. In the next step, the heap is updated with the new distances and n_i is removed. From the final list of predecessors of the end node n_e, the shortest path is read with the number of nodes being the defects in the percolation path. For the purpose of extracting all percolation paths, the edge with the smallest weight, i.e. smallest current $I_{i,\mathrm{min}}$, is then removed from the initial graph and the number of nodes is weighed by this current. This ensures charge conservation, as can be easily seen from Kirchhoff's law within the network, i.e. missing current contributions or double counting are ruled out. The procedure is then repeated until no path can be found from n_s to n_e. With all paths i analyzed for the contributing defects N_i percolating the minimum current I_min within the path the average defect number as a measure of multi-TAT relevance can be calculated by (4.67).

Applying this algorithm to the example shown in Figure 4.12, one ends up with four conducting paths (removing the minimum edge of each dominant path ensures charge conservation, i.e. no double counting of currents) sorted by the order of their extraction:

- Channel - 1 - Gate with $I_\mathrm{min} = \frac{1}{4} I_\mathrm{tot}$
- Channel - 1 - 3 - Gate with $I_\mathrm{min} = \frac{1}{3} I_\mathrm{tot}$
- Channel - 1 - 2 - Gate with $I_\mathrm{min} = \frac{1}{4} I_\mathrm{tot}$
- Channel - 1 - 2 - 3 - Gate with $I_\mathrm{min} = \frac{1}{6} I_\mathrm{tot}$

This example shows, that the algorithm does not necessarily find the path conducting the largest fraction of the total current, as the weighing of edges is conducted by the Markov transition probability instead of the resistivity. However, the exact ordering of

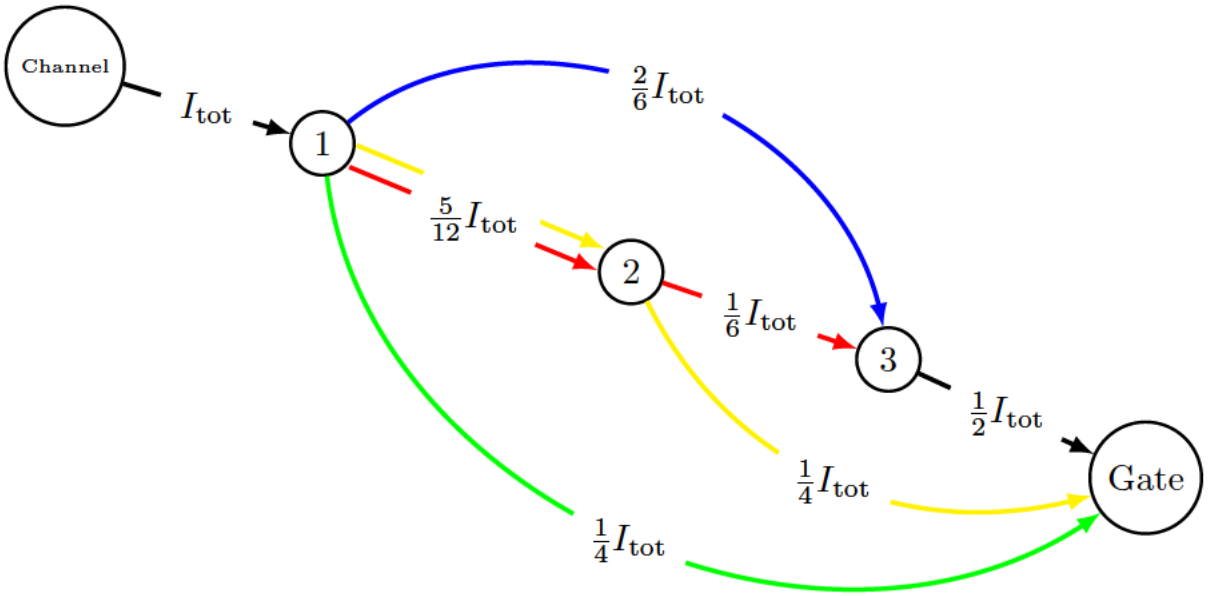

Figure 4.12. A simple exemplary conduction path graph is shown to demonstrate the principle of the algorithm employed to extract the average number of defects that are responsible for the overall TAT percolation paths. The conducting path with the largest current contribution (blue) is thereby not necessarily identified first, which is the only path with one defect in this example (green).

the paths is irrelevant for the computation of the average defect number, which for the example by employing (4.67) reads:

$$\langle N \rangle = \frac{1}{4} \times 1 + \frac{1}{3} \times 2 + \frac{1}{4} \times 2 + \frac{1}{6} \times 3 \approx 2.33. \tag{4.68}$$

With the percolation path analysis at hand, the properties of a gate stack and the defects within the insulator that lead to a relevant multi-TAT current shall be discussed. Therefore, a poly-Si/SiO_2/Si gate stack is employed with a single defect band. Three oxide thicknesses with 5, 10 and 20 nm, with the defect band located at $E_T = 0.95$ eV with respect to the Si mid-gap are investigated. This specific selection of the energetic position of E_T allows for electrons being captured from the channel at small to medium oxide field strengths due to its small relative distance to the Si conduction band and reduces the probability of the electron to be directly emitted to the oxide conduction band due to the relatively centered position within the SiO_2 band-gap. A constant number of defects $\overline{N} = 50\,\text{nm}^{-1}$ is introduced in the oxide layer, resulting in 250, 500 and 1000 defects used within each simulation, respectively. As the relative distance of the effective defect levels between individual defects is determined by E_T and its distribution, the most relevant parameters for enabling multi-TAT transitions are given by E_R and the distance between the defects, i.e. the defect density. In order to study their impact, these parameters are varied from $E_R = 0.3$ to 1.5 eV and $N_T = 10^{18}$ to $10^{20}\,\text{cm}^{-3}$. Note that the

relaxation energy refers to the defect/reservoir transition and the transformed E_R for defect/defect transitions is approximately a factor of two higher, see Section 4.4.1. The NMP parameters and ranges of this fictive defect band are summarized in Table 4.1. For all three gate stacks, bias sweeps from $V_G = 0\,V$ to $V_{G,max} = 5$, 10 and 20 V were

Band	$\langle E_T \rangle$	σ_{E_T}	$\langle E_R \rangle$	σ_{E_R}	$x_{T,max}$	N_T
multi-TAT	0.95 eV	0.1 eV	0.3 to 1.5 eV	0.1 eV	-	10^{18} to 10^{20} cm^{-3}

Table 4.1. NMP defect band used in SiO_2 with varying $\langle E_R \rangle$ and N_T

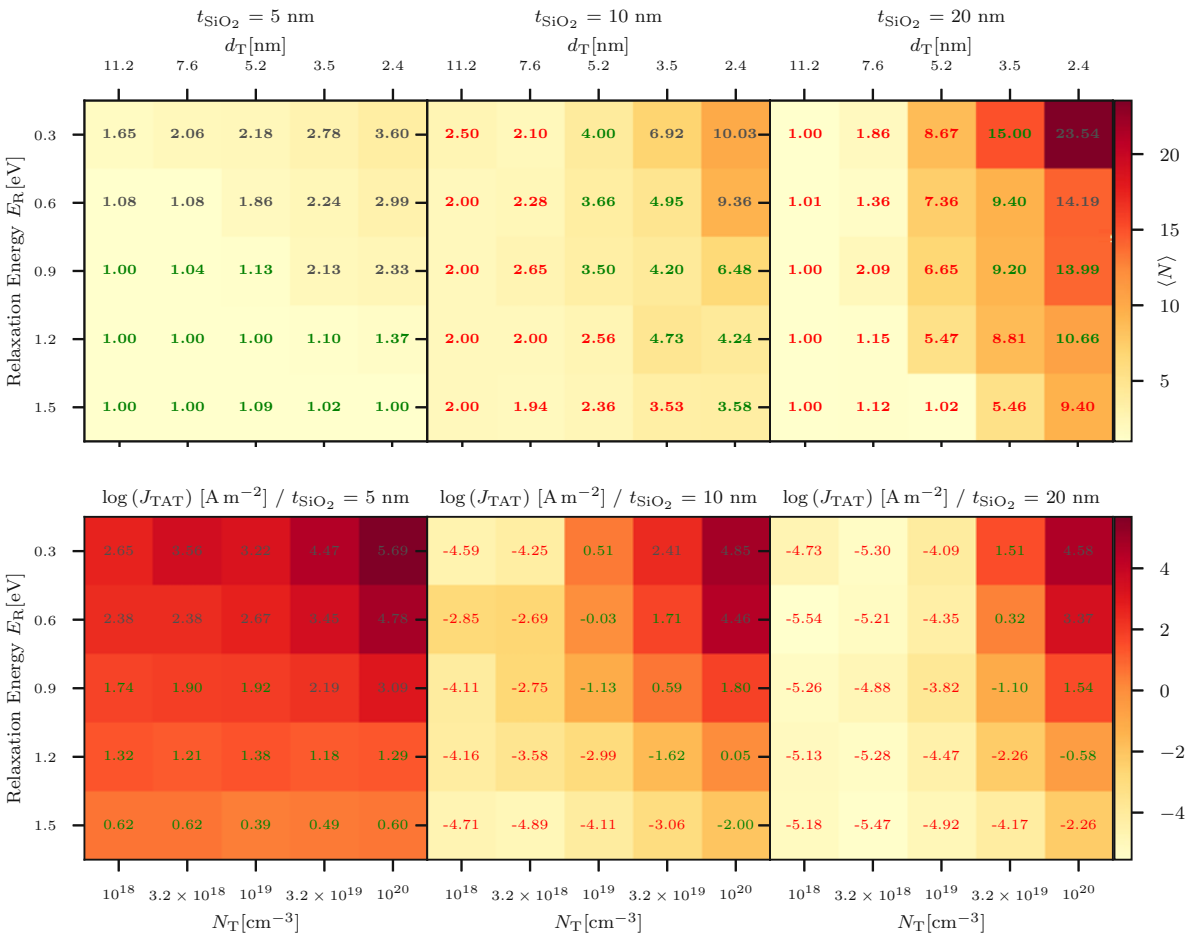

Figure 4.13. The average number of defects $\langle N \rangle$ in a TAT percolation path shown for $E_{ox} \approx 4\,MV\,cm^{-1}$ depends mainly on E_R and the distance between the defects **(top)**. The corresponding current densities **(bottom)** reveal that only larger densities ($N_T > 10^{19}\,cm^{-3}$) at lower relaxation energies ($E_R < 0.9\,eV$) endanger the low power limit for logic circuits of $10^{-2}\,A\,cm^{-2}$ (black values) via a multi-TAT percolation path. For thicker oxides **(center)** and **(right)** multi-TAT presents a leakage threat only for memory applications (green values), while most other leakage paths are negligible (red values). (taken from [CSJ4])

applied in the simulation, resulting in comparable oxide field strengths at $T = 300\,K$. The steady-state TAT currents were then analyzed with the modified Dijkstra algorithm

as discussed above. Figure 4.13 shows the resulting average number of defects $\langle N \rangle$ for the three oxide thicknesses together with the associated steady-state current densities at intermediate field strength of $E_{ox} \approx 4\,\mathrm{MV\,cm^{-1}}$. The black colored $\langle N \rangle$ indicate the parameter tuples (E_R,N_T) resulting in significant leakage current densities above a low power limit of $10^{-2}\,\mathrm{A\,cm^{-2}}$ for logic devices [248], while the green numbers indicate current densities between 10^{-6} to $10^{-2}\,\mathrm{A\,cm^{-2}}$ which can be considered moderate leakage currents in RAM applications while the red fields with current densities below $10^{-6}\,\mathrm{A\,cm^{-2}}$ are not considered to contribute to a relevant leakage current. Thus, it can be seen that only the thinnest oxide exhibits relevant multi-TAT currents for the logic current limit at realistic bulk defect parameters ($E_R > 0.9\,\mathrm{eV}$, $N_T < 10^{20}\,\mathrm{cm^{-3}}$). Multi-TAT leakage current densities relevant for logic applications are only observed for medium densities $N_T \geq 10^{19}\,\mathrm{cm^{-3}}$ for the 10 nm oxide, with more defects in the leakage paths on average. In the thickest oxide multi-TAT leakage can be considered relevant only for the highest densities at low E_R, thereby resulting in hopping over more than 10 traps.

A detailed spatial resolution of the multi-TAT percolation paths in the different gate stacks is provided in the band diagrams in Figure 4.14 at $E_R = 0.9\,\mathrm{eV}$ and $N_T = 10^{19}\,\mathrm{cm^{-3}}$ (central field in Figure 4.13).

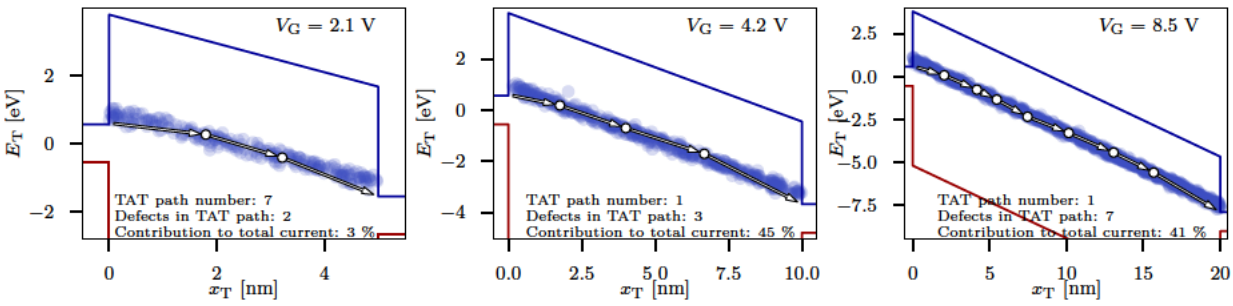

Figure 4.14. Multi-TAT percolation paths are shown for $E_R = 0.9\,\mathrm{eV}$ and $N_T = 10^{19}\,\mathrm{cm^{-3}}$ as extracted by the modified Dijkstra algorithm. While in the thinnest gate stack only one path with more than 1 defect contributes a small fraction of the total current **(left)**, a large fraction of the total current is conducted over multiple traps in the thicker gate stacks **(center)** and **(right)**. Nonetheless, the current densities decay significantly with more defects involved in the hopping mechanism, rendering the total current densities a minor threat for leakage currents in the thicker insulators. (taken from [CSJ4])

4.8 Effective Single Defect Decomposition

Finding a correct and unique set of defect parameters to compute energetic barriers, c.f. (4.31), that yield charge transfer rates to reproduce the exponentially decaying recovery data obtained from electrical measurements, e.g. MSM sequences Section 2.1.3, is referred to as spectral- or Multi-Exponential Analysis (MEA). As explained in detail by Istratov *et. al* [249], a unique solution can only be derived with adequate Signal-to-Noise Ratio (SNR), as the signal decomposition is mathematically an ill-posed problem.

Sufficient variation of experimental parameters, e.g. T, V_G and a correct hypothesis (model) in combination with a reasonably accurate initial guess of the parameters are required to mitigate the numerical instabilities typically arising within MEA. In this section, a new numerical method for MEA, as imposed by the problem of finding two-state NMP defect parameters that explains experimental MSM data obtained in large area MOSFETs, is presented. Due to its inherent decomposition of parameter space, this method has been termed Effective Single Defect Decomposition (ESiD) [CSJ6].

A common assumption for the distribution of the defect parameters in previous works was a uniform [240] or linearly decaying [109] spatial defect density distribution N_T with a Gaussian distribution in the energetic dimensions, which for a two-state NMP model yields the parameter tuple

$$P = \left(\overline{E}_T, \sigma_{E_T}, \overline{E}_R, \sigma_{E_R}, R, x_T, N_T\right) \tag{4.69}$$

subject to minimize the error between computed and measured ΔV_{th}. The naive approach of optimization using local gradient based or iterative minimization schemes, e.g. a Nelder-Mead method [250], is simple to use, however, does not constrain the parameter space and usually requires an excellent initial guess if numerous local minima are present as is typical for highly nonlinear problems like MEA of BTI data. In case of insulators with more than one defect band of the form (4.69), which is subject to charge capture and thus alters the observed ΔV_{th}, the optimization becomes even more tedious due to the extended parameter space.

Additionally, a parameter cross-correlation in the NMP model between the curvature ratio R and relaxation energy E_R leads to similar energetic barriers, not resolvable by an experimental parameter variation [CSJ6]. Hence, in-line with ab-initio calculations [81], the curvature ration is fixed to $R = 1$ and removed from the parameter space (4.69) that is optimized. As the measured ΔV_{th} is a result of the superposition of a large defect ensemble it can be expressed as

$$\Delta V_{th}(t) = \int_{\Omega} N(\vec{p})\, \delta V_{th}(t, \vec{p})\, \mathrm{d}\vec{p} \tag{4.70}$$

with the weight or distribution function $N(\vec{p})$ of the defect parameter vector $\vec{p} = (E_T, E_R, x_T)$ within the parameter space Ω and the response function $\delta V_{th}(t, \vec{p})$. For the definition of the estimator on a discrete time t_i defined by the measurement input, the parameter space is discretized as p_j on a grid within a reasonable range. In our approach, a non-negative least square (NNLS) estimator is then used to infer the underlying distribution function $N(\vec{p})$ from the experimental degradation $\Delta V_{th}(t, V_G, T)$. Mathematically, this estimator can be cast as [CSJ6]:

$$\vec{N} = \underset{\boldsymbol{N} \geq 0}{\operatorname{argmin}} \left\| \boldsymbol{\delta V} \cdot \boldsymbol{N} - \Delta \vec{V} \right\|_2^2 \tag{4.71}$$

with the response matrix $(\delta \boldsymbol{V})_{ij} = \delta V_{\mathrm{th}}(t_i, p_j)$ and the observation vector $\Delta \vec{V}_i = \Delta V_{\mathrm{th}}(t_i)$. Note that a restriction to semi-positive values for the distribution function is necessary for physical reasons, since a negative density would be nonsensical. Minimization of this estimator, however, may result in a discontinuous discrete distribution function, as no restriction is given on the shape of $\boldsymbol{N}$. Nonetheless, a physical distribution function requires smoothness, therefore a Tikhonov regularization term [251] is added to the estimator yielding [CSJ6]

$$\vec{N} = \underset{\boldsymbol{N}\geq 0}{\arg\min} \left\| \delta \boldsymbol{V} \cdot \boldsymbol{N} - \Delta \vec{V} \right\|_2^2 + \gamma^2 \|\boldsymbol{N}\|_2^2. \tag{4.72}$$

As γ is a free parameter its variation for the optimum regularization has to be chosen sensibly. A too low value of γ results in a low error, but at the same time a large density and thus over-fitting of the problem. On the other hand, if γ has a too large value, the estimator is too heavily regularized. Thus, the "sweet spot" in between these two regimes has to be evaluated by the variation of γ. In Figure 4.15 the impact of the regularization parameter γ can be seen with its optimum at the"corner" point of the normalized error, together with the absolute error and defect density evolution during the iteration of the estimator. The new ESiD algorithm has proven to reproduce

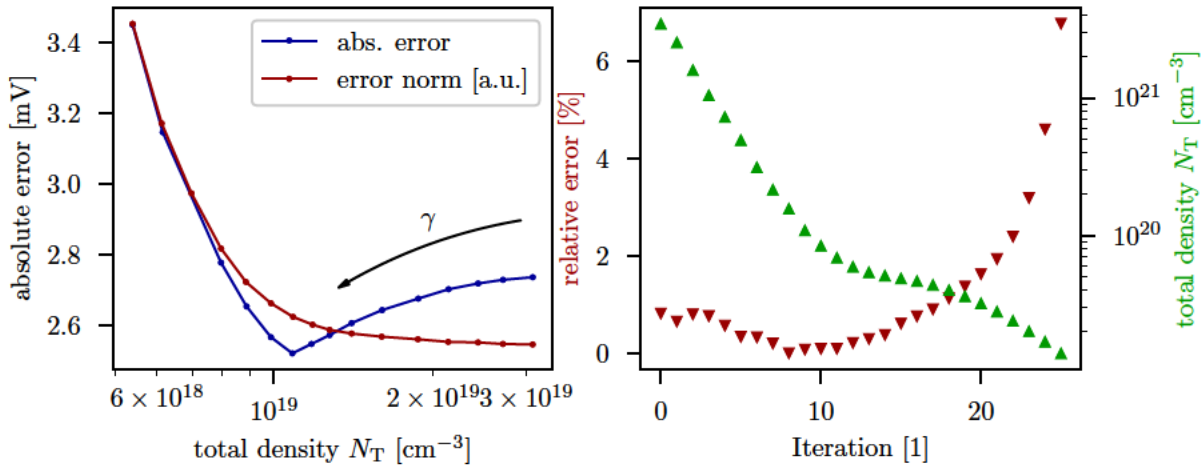

Figure 4.15. The impact of the variation of the Tikhonov parameter γ shows an optimum point at the corner point of the mean absolute error as exemplary shown for a Si/SiON transistor **(left)** (reproduced from [CSJ6]). The error increases rapidly when the density is reduced further during the iterations of the ESiD algorithm for too low densities as shown for a SiC DMOS.

MSM data on an established Si/SiON technology including n- and p-MOS transistors, with two different gate oxide thicknesses. The thereby extracted defect parameters are both consistent over the investigated process variations and with ab-initio calculations for suspected defect candidates in this widely studied material combination [CSJ6]. Also a consistency with parameters from a single defect characterization has been demonstrated. This renders the ESiD method the most promising approach to extract physical defect densities from MSM data obtained from SiC/SiO_2 MOS devices, with

its large defect densities and a multitude of potential defect candidates and therefore overlaid parameter distribution functions [CSJ6].

Its application for a comparison of SiC DMOS technologies will be shown in Section 5.1.2. For the extraction of defect parameters based on measured TAT currents, the method is only applicable when the multi-TAT term in (4.56) can be ignored as then the non-linear coupling of the system of equations for the defect occupations vanishes. With the inclusion of the multi-TAT term, a least square optimization method employing a simplex algorithm, as discussed at the beginning of this section, is used throughout this work.

4.9 Summary

To summarize, within this chapter an NMP framework has been derived for calculating both charge trapping and charge hopping currents based on an efficient and minimal parameter modeling approach. Therefore, analytical expressions for a simple two-state NMP model to explain charge transfer between oxide defects and carrier reservoirs have been derived to enable large scale defect charge transfer computation. This approach has been implemented in the Compact Physics Framework (Comphy) for an efficient computation of both ΔV_{th} and I_{G} as a result of the NMP charge transitions to and from defects in MOS stacks. Finally, the relevance of multi-TAT currents is quantified and it is found that defects with small E_{R} at relatively large N_{T} are required to conduct a significant current over multiple defects in 5 to 20 nm thick dielectrics. To enable an efficient defect parameter extraction for BTI and single-TAT studies a novel ESiD method is presented.

Chapter 5

Measurements, Simulations and Results

BTI and gate-leakage currents are considered major reliability threats responsible for device parameter degradation in SiC MOSFETs. Their characterization and simulation by accurate models are presented within this section. The Si-face interface of SiC to its deposited or grown native oxide has been intensively studied in the past. Thus, investigations of charge trapping by inelastic tunneling processes as presented here, mainly focusing on lateral MOS test structures and commercially available DMOS devices.

First, BTI is analyzed on lateral MOSFET test-structures by employing a bias pulse technique to separate fast and slow degradation components for both pBTI and nBTI degradation. Based on these findings different DMOS technologies are characterized by a large measurement data set and, using the newly developed ESiD algorithm, therefrom defect parameters are extracted which reveal similarities, but also differences among the defect bands in the SiC MOSFETs.

In the second section, gate leakage currents are analyzed based on enhanced temperature activated TAT currents observed at low to medium field strengths employing a SiC/SiO_2 MOSCAP, a MOSFET, and a MIM capacitor with ZrO_2, as used in RAM applications. The newly proposed TAT model is demonstrated and reveals details about the charge trapping kinetics within these structures and by a comparison of the defect parameters with ab-initio computations, a class of defects is identified as TAT transition centers in both binary oxides.

5.1 Bias Temperature Instabilities in SiC MOSFETs

The results within this section have been previously published in [CSC1],[CSJ2] and [CSC3].

This section aims to reveal the underlying physical mechanisms that cause the main features of BTI as observed in SiC MOSFETs, which are frequently compared to BTI in Si technologies [92, CSC2, 94] by applying the same characterization and data analysis methods. For this purpose, defect parameters are extracted by device

scale simulations and restricted to be consistent within bounds defined by ab-initio calculations of likely defect candidates. Similarities and differences among different SiC DMOSFET technologies and Si based MOSFETs in terms of the origin of BTI are also discussed.

5.1.1 Lateral Test Structures

Some of the advantages of studying the impact of charge trapping as the main reason for V_{th} and R_{on} shifts on lateral structures include:

- A uniform electric field distribution across the oxide can be assumed for small enough drain bias.
- Geometrical effects, e.g. edge effects due to trench sidewalls, can be neglected.
- A small contact resistance is assumed and an additional series resistance as in vertical device architectures is not expected to influence on the ΔV_{th} extraction.
- The band offsets and other material parameters, e.g. transition region width between SiC and SiO_2, are best studied for the Si-face SiC/SiO_2 interface, compared to a-face, c-face or m-face surface planes.

Hence, planar SiC/SiO_2 MOSFETs with channel dimensions of W×L = 100×2, 4 and 6 µm^2 and an oxide layer with a thickness of about 70 nm have been investigated. After the oxide deposition, the devices have received an annealing process step in NO ambient.

An initial $I_D(V_G)$ curve to convert the measured drain current into ΔV_{th} is recorded as shown in Figure 2.2 on a pristine device for each BTI stress sequence. To determine the threshold voltage shift with a reduced perturbation of the $I_D(V_G)$-curve due to charge trapping during the gate bias sweep, these time-zero transfer characteristics are measured at a rate of $R = 50\,\mathrm{V\,s^{-1}}$ and within a narrow bias range of only up to about 1 V above the threshold voltage. The selected sweep rate is the fastest for the chosen current limit of $I_{max} = 1\,\mu\mathrm{A}$ for the ultra-low noise Defect Probing Instrument (DPI) used for this characterization. A constant current criterion of $I_D = 100\,\mathrm{nA}$ is used to convert I_D to ΔV_{th} and the drain bias has been scaled with L by V_D = 0.1, 0.2 and 0.3 V. Without any additional delay after recording the pristine $I_D(V_G)$ characteristics, an eMSM scheme is applied with stress times ranging from $t_{str} = 10^{-6}$ to 10^4 s and recovery times $t_{rec} = 10$ to 10^5 s with the first measurement point extracted after $t^{delay} = 100\,\mu\mathrm{s}$. For the PBTI characterization, the stress bias has been selected as V_G^s = 30, 37.5 and 45 V, resulting in approximate oxide stress fields of $E_{ox}^{str} \approx 3.5$, 4.6 and 5.7 MV cm^{-1}. The recovery bias V_G^r is chosen according to the extracted $V_{th,0} \approx 4.4\,\mathrm{V}$. All measurements have been conducted on the custom-built low-noise DPI presented in Section 2.3 and each eMSM scheme is recorded on a fresh n-MOSFET.

The material parameters that were used to calculate the electrostatic quantities in Comphy (c.f. Section 4.6.1) are listed in Table 5.1 for the channel substrate and in

Table 5.2 for the insulating layer. The transition of the band edges between the channel and the oxide is assumed to be abrupt and the band edges are thus linearly interpolated for the simulation within the first 5 Å as shown in the band diagrams in Figure 5.1.

quantity		ref.	value	unit
$E_{G,0}$	band gap at 0 K	[23]	3.36	eV
$E_{G,1}$	temperature coefficient	[252, 253]	-3.3×10^{-4}	eV K^{-1}
m_l	lateral el. eff. mass	[254, 30]	0.33 m_e	kg
$m_{t,0}$	transversal el. eff. mass	[254, 30]	0.42 m_e	kg
$m_a ... m_i$	coeff. for eff. mass val. band	[34]	see ref	1
N_{cv0}	band weight	[23]	2.54×10^{19}	cm^{-3}
M_c	conduction band minima	[23]	3	1
$\varepsilon_{r,chan}$	relative permittivity channel	[23]	9.76	1
$\Delta E_{w,0}$	channel/gate work. func. diff.	[23]	-1.2	eV
$N_{a,chan}$	acceptor doping concentration		2×10^{17}	cm^{-3}
$N_{d,chan}$	donor doping concentration		10^{10}	cm^{-3}

Table 5.1. Channel parameters to calculate the electrostatic quantities in Comphy. Note that m_e donates the electron mass.

quantity		ref.	value	unit
E_G	band gap		9.0	eV
E_{off}	channel/oxide E_v offset	[23]	-4.68	eV
m_t	tunneling mass	[255]	0.42 m_e	kg
$\varepsilon_{r,ox}$	rel. permittivity oxide		3.9	1
t_{ox}	thickness of the oxide layer		70	nm

Table 5.2. Input quantities used for the SiO_2 layer. Note that m_e donates the electron mass.

For the extraction of the defect parameters, defects are considered uniformly distributed on an equidistant spatial grid x_T and normally distributed on a equidistant energetic grid (E_R, E_T). Each grid point (x_T, E_R, E_T) is weighed by this distribution to yield the selected total defect density N_T, with the grid parameters given in Table 5.3. Using these settings, the defect parameters of two bands are extracted by minimizing the

parameter		value	unit
ΔE_T	trap energy level	0.1	eV
ΔS	relaxation energy level	0.1	eV
Δx_T	spatial distribution	0.05	nm
p_{tol}	cut-off probability	10^{-4}	1

Table 5.3. Grid parameters used in Comphy. The distance between the points are given for the three dimensional grid together with a cut-off probability p_{tol} for the Gaussian tails.

difference between the simulation results and the measurement data by a Nelder-Mead

least-square minimization algorithm [250] as implemented in *scipy*. As initial guess, a shallow defect band extracted on Si/SiO_2 technology [240] has been used and with E_T close to $E_{c,SiC}$ that is sampled up to 3 nm into the oxide. A good agreement with the measurement data for the tails of the recovery traces is revealed in Figure 5.1 (top). For the calculation of the remaining fast recovering ΔV_{th} defects with small relaxation energies and located within the transition region at a distance of up to 5 Å from the interface have been introduced, resulting in a fast electron trap band (EB). These defects define the charge transfer kinetics as required to explain the fast recovering component of ΔV_{th} and lead to degradation of $\Delta V_{th} > 2$ V for the longest stress phases. Note that the small E_R used in the fast EB effectively yield transition rates that can also be approximated by employing the extended-SRH model, as discussed in Chapter 4 and in detail by Ruch *et. al* [213]. To investigate the impact of bias switches to the depletion and accumulation

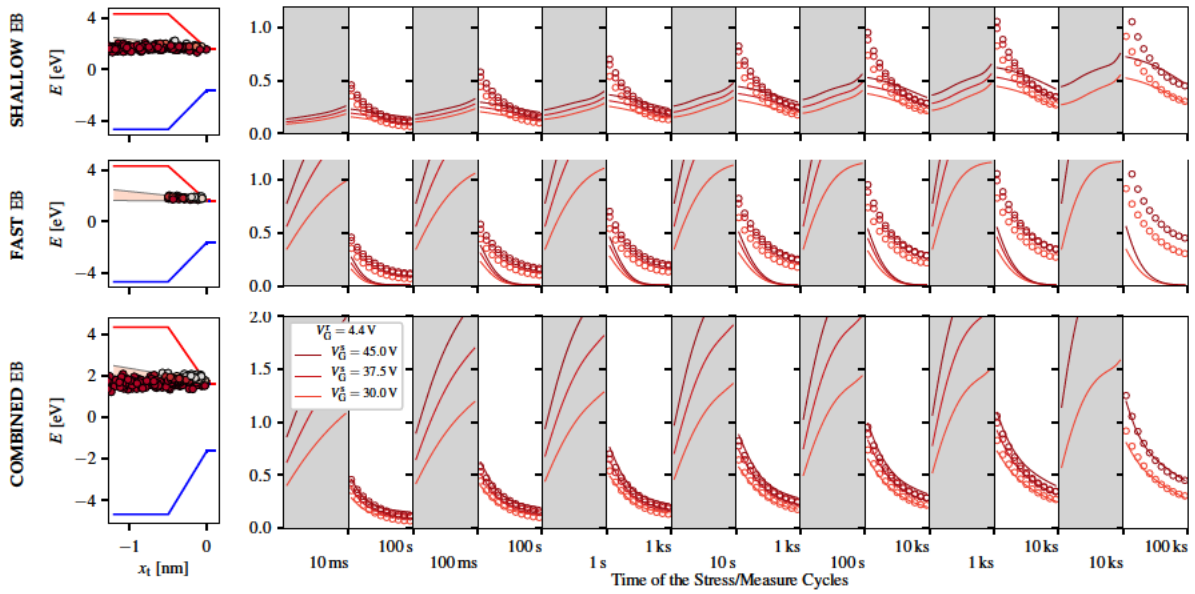

Figure 5.1. The measured positive ΔV_{th} (circles) of three MSM measurement schemes employing three different positive stress biases at a temperature of $T = 30$ °C, is well described by the calibrated simulation (lines) **(bottom)**. Thereby, two defect bands are used, as indicated in the band-diagrams, of which one (shallow electron trap band) accounts for the slowly degrading and recovering ΔV_{th} part **(top)**, and the other (fast electron trap band) for the fast component of ΔV_{th} degradation and recovery **(center)**. Note that the shallow defects which explain the tails of the recovery traces employ similar parameters as extracted for Si-based devices in [240]. (taken from [CSC1])

regime, as for instance proposed in [91] for an evaluation of V_{th} shifts in parallel for many devices, pulsed MSM sequences have also been measured and included in the fitting routine, as shown in Figure 5.2. Thereby, a pulse at a bias level in the depletion ($V_G^P = 0$ V) or accumulation ($V_G^P = -5$ V) regime is applied after the stress phase before the recovery phase is started for $t^P = 10$ s. Initially, only the pulse is applied without stress to investigate the impact of the pulse on the pristine device.

parameter	fast EB	shallow EB	HB 1	HB 2	unit
$\overline{E}_T \pm \sigma_{E_T}$	1.87 ± 0.08	1.73 ± 0.17	-1.12 ± 0.24	-1.77 ± 0.04	eV
$\overline{E}_R \pm \sigma_{E_R}$	$0 \quad +0.85$	4.93 ± 1.95	$5.2 \quad \pm 4.89$	$0 \quad +1.55$	eV
R	0.9	0.437	1.19	0.6	1
N_T	2.8×10^{19}	3.44×10^{19}	1.26×10^{19}	7.3×10^{18}	cm^{-3}

Table 5.4. Four defect bands are employed for reproducing a large variation of PBTI and NBTI characteristics of lateral SiC-MOSFETs. The electron traps are concentrated around the conduction band edge, while the whole traps reach further into the band gap from the valence band edge. For both types, a fast defect band (fast EB and HB2) with low E_R is used to reproduce the interfacial defect characteristics.

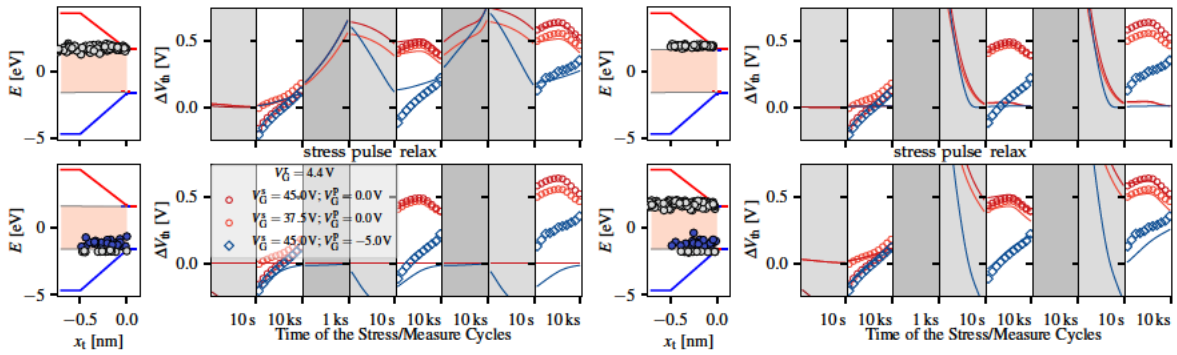

Figure 5.2. A pulsed MSM scheme is used to separate the contributions of fast and slow recovering ΔV_{th}.To this end a pulse with $V_G = 0\,V$ or $-5\,V$ is applied after the stress sequence for 10 s and before the recovery trace is recorded. The resulting recovery traces show a reverse characteristic for the depletion regime pulse (V_G= 0 V), which is completely reconstructed by the shallow electron trap band in the simulation **(top, left)**. The fast traps are emptied by both pulse biases **(top, right)**. The accumulation regime pulse enables hole trapping close to the valence band, that shifts the recovery traces to more negative ΔV_{th}, which is accounted for by two additional hole trapping bands **(bottom, left)**. A superposition of all bands explains the characteristic recovery traces for all conditions **(bottom, right)**. (taken from [CSC1])

When splitting the contributions of the defect bands in the simulation, it is revealed that the shallow EB solely accounts for the characteristic recovery traces for a pulse bias of $V_G^P = 0\,V$, shown in Figure 5.2 (top). Note the degradation of ΔV_{th} at the beginning of the recovery traces. This increasing ΔV_{th} at recovery conditions is a result of electron capture of a small fraction of defects in the shallow EB, that previously emitted charge during the pulse phase. Quite to the contrary, all defects in the fast band emit the previously captured electrons during the pulse duration. Furthermore, the application of an accumulation pulse results in a different recovery characteristic, starting at negative ΔV_{th}. This NBTI characteristics is a result of hole capture and can be accounted for by the introduction of two hole trap bands (HB1, HB2) with parameters listed in Table 5.4. These bands together with the two EBs are able to reproduce the peculiar ΔV_{th} recovery at all pulse conditions shown in Figure 5.2 (bottom).

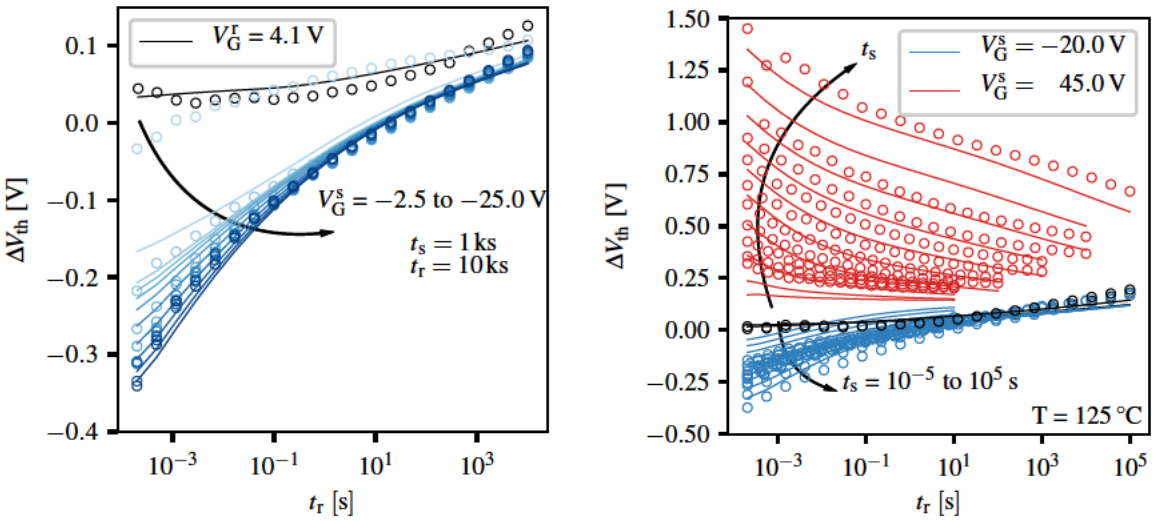

Figure 5.3. A ramped voltage stress (RVS) MSM scheme to capture the bias dependence of NBTI at $T = 30\,°C$ **(left)**. Initially a readout is performed without prior stress for 10^5 s (black) showing that electron capture is already happening at the readout voltage close to V_{th}. The temperature activation of the charge transfer kinetics in the simulation (lines) for both positive and negative bias stress is confirmed by a good agreement of the recovery trends when compared to the measurement data (circles) **(right)**. (taken from [CSC1])

Moreover, the NBTI bias dependence is extracted by measuring a RVS MSM scheme with an initial readout at the recovery bias and stress bias variation in the range of $V_G^s = -2.5$ to -25 V at fixed stress time of $t^s = 1$ ks and readout time of $t^r = 10$ ks, as shown in Figure 5.3 (left). It has to be noted that even if the extraction of NBTI in an nMOS is operation relevant when bipolar gate drivers are used, a large fraction of defects capturing holes at negative bias already have emitted their charge before the read-out phase. Hence, only a small fraction of defects contributing to NBTI is experimentally accessible with MSM sequences conducted in n-channel MOSFETs. Note that the NBTI results on experimental pMOS structures investigated in [256] show significantly larger V_{th} shifts compared to those of the n-MOSFETs presented in this work.

The accurate reproduction of the temperature activation in the simulation is mainly influenced by the relaxation energy E_R within the NMP model as shown in Figure 5.3 (right) for both PBTI and NBTI MSM sequences. Again, in Figure 5.3, the impact of an initial readout phase at $V_G \approx V_{th}$ prior to the stress phase is shown by the black line. This readout shows that already the application of the readout bias leads to electron trapping and hence V_{th} shifts of more than $\Delta V_{th} = 0.1$ V for $t^{read} = 10$ ks.

To further strengthen the hypothesis of the shallow EB band being an intrinsic property of the oxide, a PBTI MSM sequence has been measured on a commercially available trench MOSFET [257, 258]. The inset of Figure 5.4 shows the initial transfer characteristics used to extract ΔV_{th} with steeper SS and lower V_{th} compared to the lateral device. Thus, the device electrostatics in Comphy have been adapted for the reduced initial V_{th} by changing the channel doping concentration to compensate for the

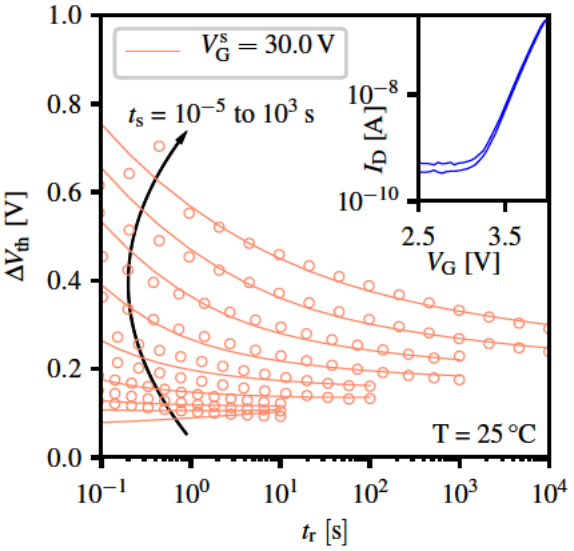

Figure 5.4. Recovery traces on a trench MOS can be reconstructed with the same defect parameters for the long-term tails, but require an increased defect density for the fast EB. Although, a higher mobility and *SS* (c.f. $I_D(V_G)$ curve in inset) is reached on the a-face interface compared to lateral MOSFETs, the short term degradation is slightly increased.(taken from [CSC1])

difference. The first point of the recovery trace could not be resolved below 100 ms due to the large input capacitance of the trench device. As shown, the long-term recovery behavior is again captured well by the simulation and can solely be described by the shallow EB with the same parameters as given in Table 5.4. Increasing the defect density of the fast EB by about a factor of 1.5, finally leads to a reasonable agreement of the computed short term ΔV_{th} with the measurement. The increased density thereby compensates for the different interfacial properties obtained on Si-face when compared to a-face terminated SiC MOSFETs. It has to be emphasized that the comparatively large PBTI shifts in SiC MOSFETs does not contradict the fact that PBTI is almost negligible in Si/SiO_2 technologies, as the active defects are not accessible in the Si based devices due to the difference of about 0.3 eV in the conduction band offsets between Si/SiO_2 and SiC/SiO_2 [259]. A comparison of the PBTI degradation of different SiC technologies [CSC2] to Si-based MOSFETs is shown in Figure 5.5 together with a comparison of the AERs available in both systems. In order to acquire only the long-term BTI component for the SiC characterization, a preconditioning scheme employing negative pulses has been used to remove the fast degrading and recovering components. Thus, the long-term degradation shows a similar trend as in the Si technology with an increased absolute ΔV_{th} of up to a factor of 200.

5.1.2 Comparison of different DMOS Technologies

As large differences in V_{th} shifts have been reported for different SiC MOSFETs [260, 92] for both negative and positive BTI, three different n-channel DMOSFETs from two vendors are analyzed in terms of their BTI recovery trends and defect distributions

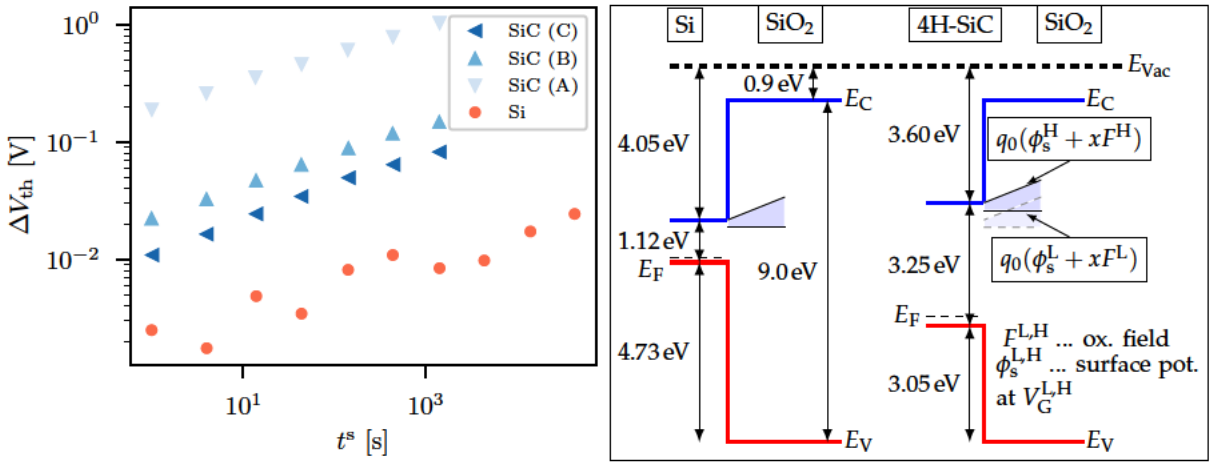

Figure 5.5. PBTI quantified by ΔV_{th} over stress time of different SiC MOSFETs compared to a Si MOSFET with 8 to 200 times larger degradation in the SiC MOSFETs with a similar time evolution trend **(left)** (reproduced from [CSC2]). Assuming that the same bulk SiO_2 defects are present in both device types, the enhanced PBTI can be explained as a result of the energetically elevated AER within the oxide for positive bias operation **(right)** (taken from [CSC1]).

that explain each peculiar ΔV_{th} recovery characteristics. The differences may arise from various influences during device manufacturing such as POA under different nitrogen containing precursors (NO, NO_2, NH_3) and annealing temperatures or channel counter-doping for increased mobility [53, 54] and off-axis epitaxial growth.

With the same argument as in Section 5.1.1 that the Si-face SiC/SiO_2 interface is best studied compared to other SiC surface terminations, three different DMOSFET devices are analyzed. Thereby two technologies are the second (T1/G2) [261] and third generation (T1/G3) [262] of the same vendor, and the third one is the first generation of a different vendor (T2/G1) [263]. In order to guarantee comparability, devices with similar oxide thicknesses were chosen, differing only in a few nanometers, so that the applied stress biases result in similar electric field strengths.

Contrary to the lateral test structures, the measurement setup used to extract V_{th} shifts [151] consists of a feedback loop, in which an operational amplifier forces a constant drain current of $I_D = 1\,mA$ through the channel by regulating V_G at fixed V_D (c.f. Figure 2.7 (right)). Besides the direct readout of $\Delta V_{th}(t) = V_G(t) - V_G(0)$, an additional advantage is that the first read-out can be conducted after only $t^{delay} \approx 1\,\mu s$. Two types of MSM schemes are used to characterize the short and long-term ΔV_{th} shifts. For operation relevant short term shifts, an AC MSM scheme [87] is used (c.f. Figure 2.4 (top)), in which an AC stress signal is applied for $t_{str} = 100\,ms$ at a frequency of $f = 50\,kHz$ at a constant high V_G^H and low bias V_G^L. This stress phase is interrupted at different points within the last AC signal period, and a recovery trace is recorded for 10 ms by forcing the constant threshold current through the channel as described above. This scheme is repeated for 20 different interruption points that are logarithmically distributed across the high and low phase of the last AC period of the stress phase. The total AC stress MSM sequence has then been permuted for different elevated

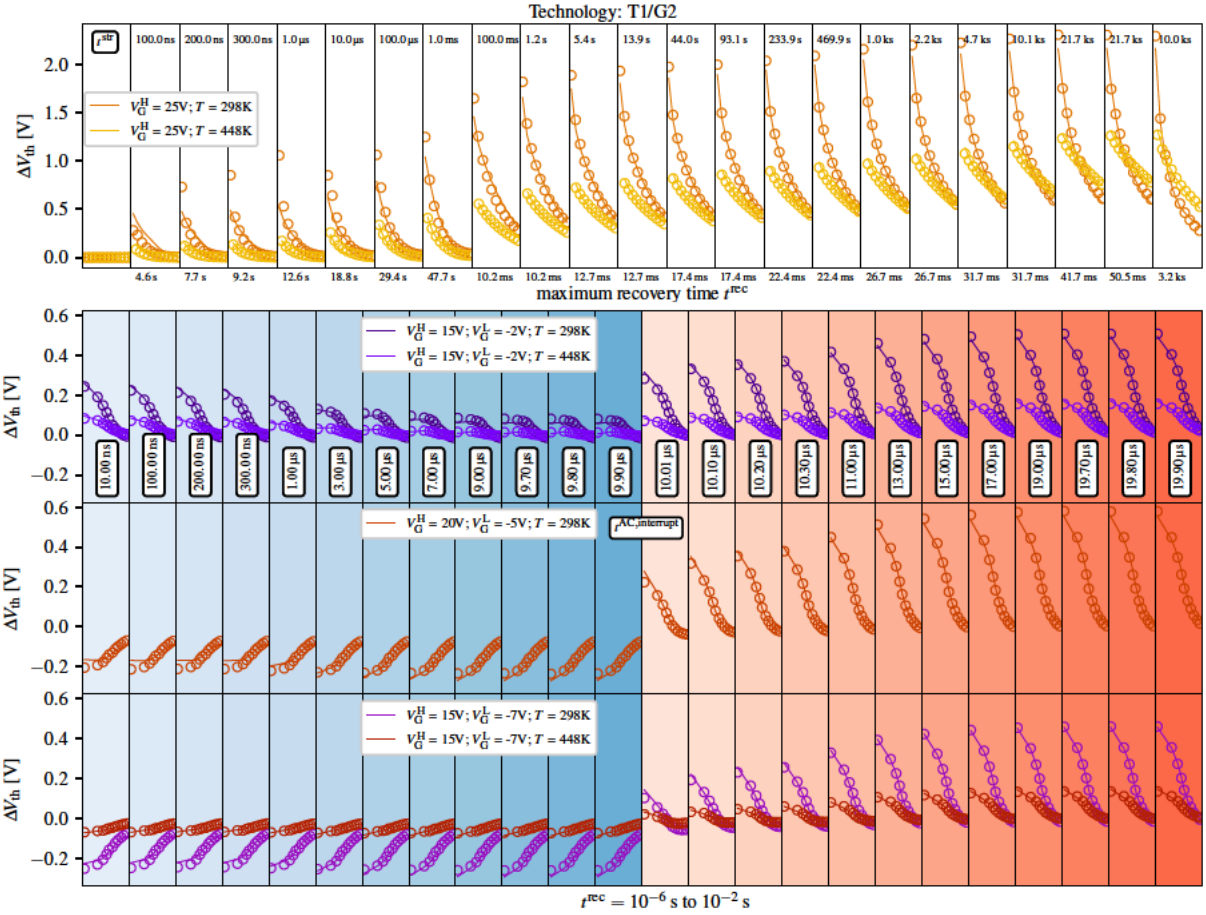

Figure 5.6. A comparison of recovery traces of V_{th} of measurements (circles) and simulations (lines) of DC MSM sequence **(top)** for stress times of $t^{str} = 10^{-7}$ to 10^{4} s at constant stress bias of $V_{G,str} = 25$ V and two $T = 298$ and 448 K is shown for varying maximum recovery times t^{rec}. Note that the first point of recovery is measured at $t^{delay} = 1$ µs only after the stress period. The first phase shown is a relaxation phase with constant I_D forced through the channel via the feedback loop, showing no significant ΔV_{th}. Recovery traces after short term bipolar AC stress at a constant stress time of 100 ms at 50 kHz and varying V_G^H and V_G^L are reproduced in detail by the simulation **(bottom)**. The increasing intensity of the background color indicates the advanced time within the last AC period of the stress signal before the interruption for V_G^L (blue) and V_G^H (red). (taken from [CSJ2]).

operation voltages of $V_G^H = 15$ and 20 V and $V_G^L = -2$, -5 and -7 V. While this sequence covers all the short term drifts of V_{th} expected during an AC signal period at regular operation, additionally DC CVS MSM sequences (c.f. Figure 2.4) with increased stress bias ($V_G^{str} = 25$ V) have been measured to capture the long-term degradation. In order to justify the extrapolation of ΔV_{th} beyond the experimental time window and to obtain the temperature activation of charge trapping, all sequences have been repeated at $T = 448$ K.

For calculating ΔV_{th}, as described in Section 5.1.1, Comphy is calibrated to the device electrostatics of each device using the channel material parameters given in Table 5.1. Additionally, as also proposed by Ito *et. al* [264], fixed positive charges, as given in Table 5.5, have to be used to compensate for the deviation from an ideal device

Symbol	Quantity	T1/G2	T1/G3	T2/G1	Unit
Q_f	fixed Charge	2×10^{11}	1.4×10^{12}	0	$C\,cm^{-2}$
t_{ox}	oxide thickness	37	33	33	nm

Table 5.5. Parameters used for calibrating the electrostatic of each device. A fixed positive charge rigidly shifts the electrostatic parameters V_{th} and V_{fb} towards more negative values.

Layer	E_T range	ΔE_T	E_R range	ΔE_R	x_T range	Δx_T
oxide	−3–3 eV	50 meV	0.1–5 eV	70 meV	0.6–3 nm	0.1 nm
interface	−2.2–2.2 eV	34 meV	0.1–3 eV	70 meV	0.0–0.5 nm	0.1 nm

Table 5.6. Grid parameters used for the ESiD extraction method. An oxide layer accounts for border traps considered as a bulk SiO_2 property, while the interface layer accounts for defects within the transition region from bulk SiC to bulk SiO_2.

characteristic, c.f. CV measurements in Figure 2.3. It should be noted that the exact origin of these fixed positive charges is subject of ongoing research. In the work of Rescher [198], process splits were performed during device manufacturing and thereby it has been revealed by measuring CV curves after each processing step during the gate stack formation that the poly-Si gate deposition and its subsequent annealing step results in the largest deviations from the ideal CV characteristics. This led to the the hypothesis that the passivation of Si-dangling bonds at the poly-Si/SiO_2 interface in forming gas leads to H^+ accumulation within the SiO_2 layer and thus to a positive charge build up.

Contrary to the simplex optimization approach used for the lateral devices, the ESiD algorithm is employed to extract defect parameters that can explain the indicated V_{th} recovery over the bias and temperature space. As discussed in Section 4.8, a major advantage of this algorithm is that no initial distribution has to be assumed for the defect parameters and respective densities, and thus no initial guess is required. Besides this improvement over the iterative optimization scheme, the computational effort is significantly reduced, as only a few iterations for varying the regularization parameter γ, c.f. Figure 4.15 are required. Quite to the contrary, for the bands optimized by the simplex method, the parameter space increases by four parameters, E_T and E_R mean and standard deviations when assuming Gaussian distributed defect bands, for each additional band. Thus, the optimization in this large parameter space rapidly becomes cumbersome. Here it has to be emphasized that only the application of the ESiD allows to extract defect parameters for the large amount of data acquired by AC and DC MSM schemes with bias and temperature variations. The computational expenses for ESiD are, however, larger than for Si based MOSFETs as an increased defect parameter grid is required due to the AER covering a larger fraction of the entire SiO_2 bandgap. As can be seen in Table 5.6, the parameter grid spanned for the ESiD extraction has been chosen to be split into two layers for electron and hole traps each. The first layer (interfacial layer) spans the range from 0 to 0.5 nm from the SiC/SiO_2 interface and is introduced

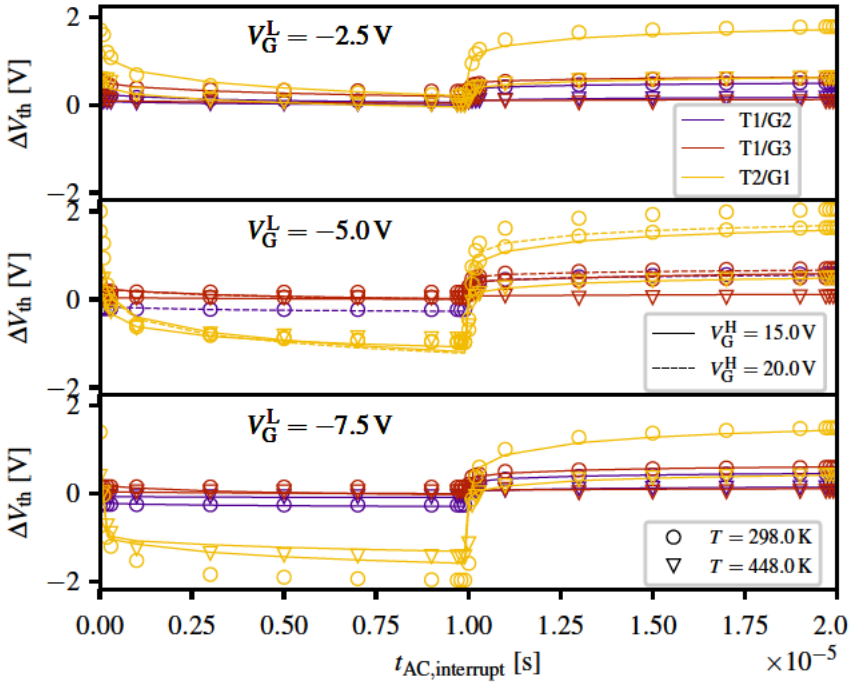

Figure 5.7. The first points of the AC MSM recovery periods are shown for different V_G^L with each symbol (measurement) interrupted at different times during the last AC stress period, e.g. the first point refers to an interruption of the AC signal after 10^{-8} s during the V_G^L phase. The lines indicate the points of simulation, which are connected for a better guidance to the eye. Large differences in the quantitative characteristics can be seen, i.e. T1/G3 shows no negative V_{th} shifts for the applied V_G^L, while T2/G1 exhibits large shifts of $\Delta V_{th} \approx 2\,V$ in positive and negative bias range. (taken from [CSJ2])

to account for the changing stoichiometric composition and therefore interface defect properties as well as to allow for increased defect densities in the transition region from bulk-SiC to bulk-SiO_2, c.f. Figure 3.3. Additionally, a second layer (oxide trap layer) covering the range of 0.6 to 3.0 nm accounts for border traps, as a bulk-SiO_2 property. Note that any further extension to larger distances within the oxide is not meaningful, as the tunneling probability in the transitions rates (4.29) and (4.30) decreases exponentially with increasing distance, as shown in [CST1]. The optimization of the defect parameters by the simulation with the calibrated device and material parameters allows to achieve an excellent agreement between the transient simulation with the measurement data, as exemplary shown for T1/G2 in Figure 5.6. A comparison of the short-term ΔV_{th} characteristics is shown in Figure 5.7 by comparing the first point of each AC MSM recovery trace at the different interruption times $t_{AC,interrupt}$. The largest degradation can be observed in T2/G1 for both negative and positive stress bias, as well as for the long-term DC PBTI characterization. More negative ΔV_{th} at more negative V_G^L can be seen in both T1/G2 and T2/G1, however, negative ΔV_{th} is not noticeable in T1/G3 at all. The positive V_{th} shift values of T1/G3 are well below 0.5 V and slightly smaller than those observed for its preceding technology generation (T1/G2).

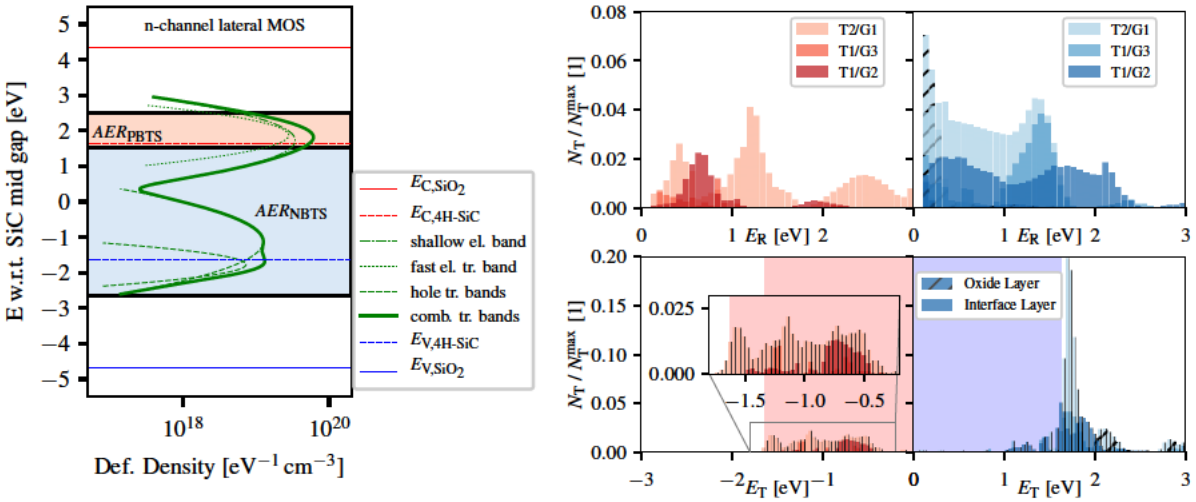

Figure 5.8. The thermodynamic trap levels according to the Gaussian distributions that were used for reproducing ΔV_{th} in the lateral MOSFETs **(left)**. A comparison of the distributions of the extracted defect parameters of the three DMOSFET technologies is shown in the right panel. (taken from [CSC1] and [CSJ2])

5.1.3 Defect Parameters

In order to explain the observed positive V_{th} in the lateral test MOSFETs, as well as for all three DMOSFETs, acceptor-like defects in the vicinity of the conduction band edge are required, as the AER spans from $E_{c,SiC}$ towards larger energies at PBTI conditions. All technologies therefore show distinct peaks, above $E_{c,SiC}$ with varying densities, i.e. N_T for electron traps in T2/G1 and lateral MOSFET are about four times higher compared to those in T1/G2 and T1/G3, as can be seen in Figure 5.8 together with their assignments to the employed layers. Also donor-like defects in the lower half of the SiC band-gap are prevalent and distributed over a wide energetic area towards $E_{v,SiC}$, except for T1/G3, which does not require a notable amount of hole traps, consistent with the absence of NBTI in this technology. The extracted relaxation energies are relatively low compared to those extracted for Si-based technologies employing a plasma-nitrided oxide [CSJ6, CSC5]. For the relaxation energies it has to be mentioned that the extracted values in Table 5.4 are considered as too large. This arises from not pinning R to a value of 1 which together with the parameter correlation of R and E_R, as mentioned in Section 4.8, leads to the overestimated values for E_R. By fixing R to 1 and correcting for the correlation, the mean relaxation energy of the shallow electron trap band reduces to E_R = 1.82 eV, which is comparable to those for the electron traps extracted in the ESiD spectra with larger E_R, shown in Figure 5.8 that are considered as oxide defects. Additionally, the fast EB as well as the ESiD spectra with E_R values smaller than 1 eV are associated with interface traps, as these defects exhibit significantly smaller E_R [213] compared to structures considered for oxide traps [81]. The thermodynamic trap levels of several defect candidates, which have been extracted from DFT calculations found in the literature, are shown in Figure 5.9 together with the AERs for an intermediate stress oxide field of 6 MV cm^{-1}, which covers all presented CTLs. It has to be noted, however,

that the CTL only represents a thermodynamic property and the charge transfer kinetics depend on the relaxation energy of the defect as well. Also, what is not represented by this graph is the formation energy of the defect candidates, which determines the probability of formation and therefore is correlated to the defect densities in a real device. Finally, the (E_T, E_R) maps for the DMOSFETs shown in Figure 5.10 show a strong correlation for the electron traps extracted with two major distributions, i.e. defect types, and in part also for the donor-like defects within the lower half of the SiC bandgap. A possible origin for the different densities extracted for the electron traps with low E_R values situated at the conduction band edge is charge trapping at N-complexed defects, as the amount of accumulated N at the interface has been correlated with increasing numbers of interface traps with charge transition levels close to $E_{c,SiC}$ [206]. This seems also plausible when considering the fact that N is a suitable dopand with relatively small activation energy in SiC.

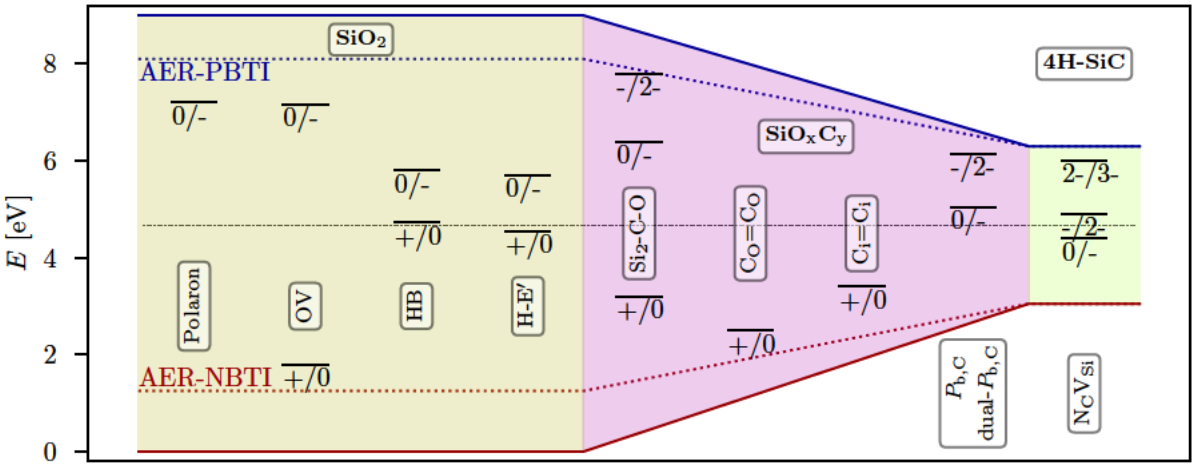

Figure 5.9. A comparison of defect CTLs extracted from DFT calculation in literature are shown for bulk-SiO_2 (dark-green), the interface layer SiO_xC_y and bulk SiC. All candidates lie within or close to the trap-levels extracted by our simulations, c.f. Figure 5.8. The AER is shown for a maximum interface distance of 3 nm at $|E_{ox}| = 6\,\mathrm{MV\,cm^{-1}}$ and covers all shown CTLs at PBTI and NBTI conditions. The defect levels were extracted from literature as follows: polaron [182, CSJ7]; OV, HB, H-E′ [81, 177]; Si_2-C-O [191], C_O=C_O, C_i=C_i [189]; $P_{b,C}$ [193]; N_CV_{Si} [202]

As the only left "free" parameters in calculating the transition rates (4.29) and (4.30) are the capture-cross sections for electron and hole trapping $\sigma_{n,p}$, their relevance on the parameter extraction is briefly discussed in the following. Therefore, the impact of a σ variation is studied, in steps of one order of magnitude to $10^{-14}\,\mathrm{cm^2}$ and $10^{-16}\,\mathrm{cm^2}$ [265] from the originally used values of $\sigma_{n,p} = 10^{-15}\,\mathrm{cm^2}$ [71, 213]. For both alterations of σ, the ESiD extraction has been repeatedly applied, with the results shown in Figure 5.11. It becomes evident that the thermodynamic trap level is not significantly influenced by the selection of σ, with only minor deviations of the two main distributions around $E_{c,SiC}$. On the other hand, the distribution of E_R with larger mean values shifts by about 0.5 eV towards smaller values with decreasing σ, while the lower E_R distribution is less affected. The change of E_R is effectively compensated by the change of charge transfer

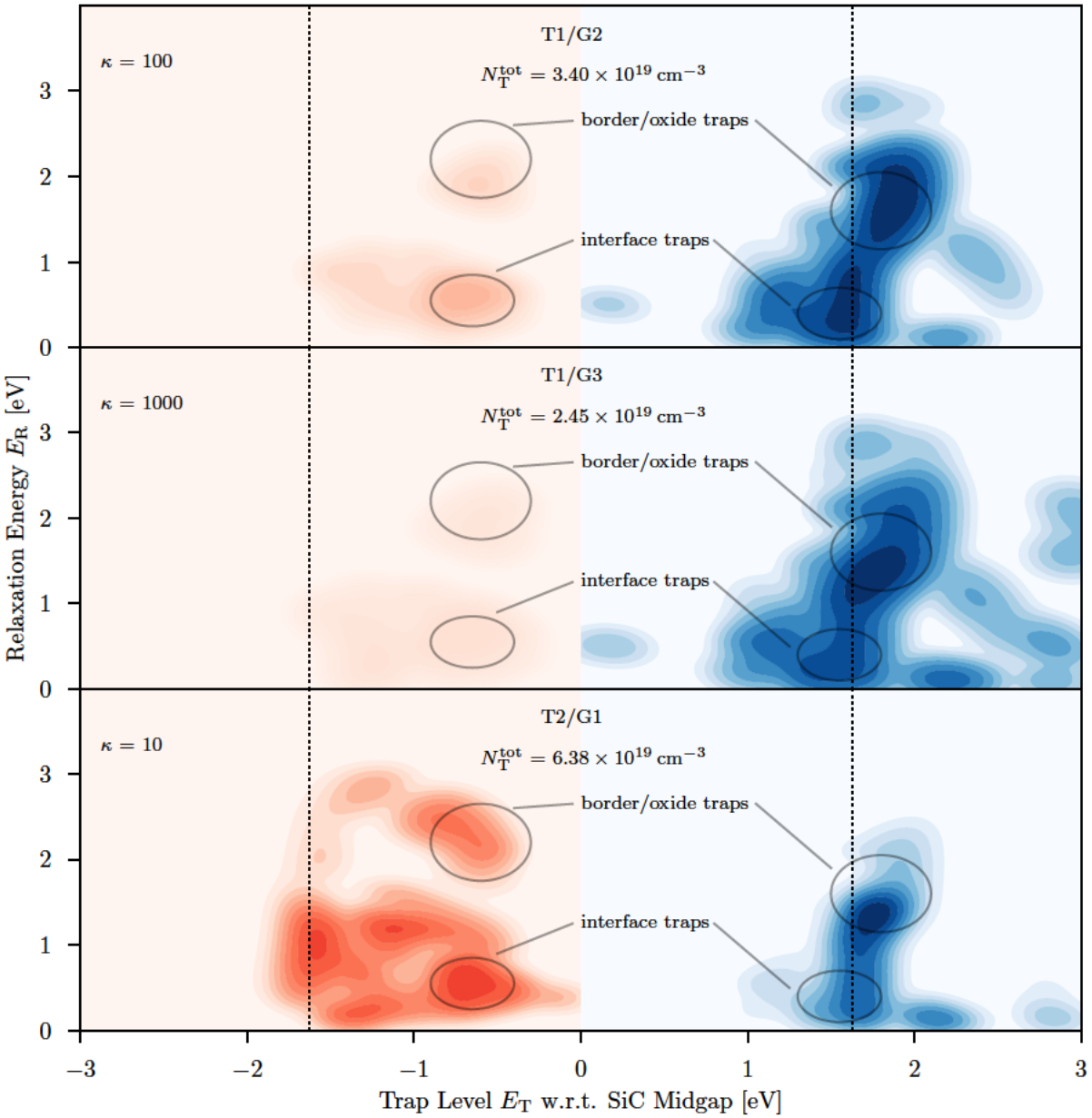

Figure 5.10. The extracted defect distributions are shown in a (E_T, E_R) parameter map. A detailed visualization is achieved by scaling the defect densities by $\log_{10}(1+\kappa N_T/N_T^{max})$ / $\log_{10}(1+\kappa)$ with κ as denoted in the panels. Compared to its preceding technology T1/G2 **(top)**, T1/G3 exhibits a negligible number of defects in the lower half of E_G, while similar densities are seen for the two distributions close to E_C. This two-fold distribution is also extracted on T2/G1 **(bottom)**, with increased density, and additionally a widespread hole trap contribution compared to T1/G2 and T1/G3. The two electron trap distributions represent a commonality among all three technologies. (adapted from [CSJ2]).

kinetics due to the altered σ value, with no loss in the ESiD accuracy. Even though a large variation of two orders of magnitude in σ is shown, the resulting deviation of E_R is low, which is a result of the exponential dependence of the rates on E_R. As the relaxation energy extracted within the simulation is typically compared to ab-initio

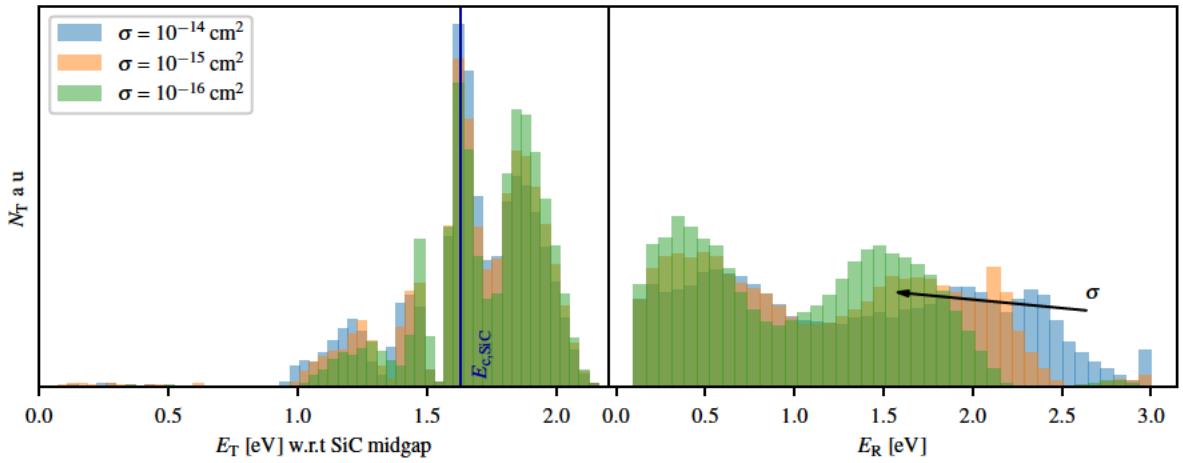

Figure 5.11. The dependence of E_T **(left)** and E_R **(right)** on a variation of the capture cross section σ is shown for the electron trap interfacial layer of T1/G2. A clear compensation of the rate kinetics with lower E_R for smaller σ can be observed for the large E_R defect distribution, while smaller E_R distributions and both E_T peaks remain largely un-affected.

calculations, the compensation effect seen between E_R and σ can be minimized by targeting consistency between the two computational methods.

5.1.4 Temperature Activation of Electron Emission

An non-intuitive feature of the V_{th} recovery previously reported by Puschkarsky *et. al*, is the less pronounced degradation observed for higher T [87], as shown in detail in Figure 5.12. Such an inverse recovery temperature acceleration contradicts observations from NBTI on Si/SiO_2 MOS devices, however, has also been reported for PBTI on n-channel Si/SiON [CSJ6]. As for the Si/SiON technology, in the SiC/SiO_2 device this phenomenon can be explained by a pronounced temperature activation for the electron emission, compared to that for the capture process, which does lead to a higher degradation during the stress phase, as shown in Figure 5.12. For the long-term recovery, a crossover between the recovery curves is observed which leads to larger observable degradation at the higher T after longer recovery times. This phenomena is also well captured by the NMP charge transfer kinetics, with the extracted defect parametrization for the DMOSFETs. In Figure 5.13 the time to reach ΔV_{th}= 0.6 V on the lateral devices is plotted for different stress bias and temperatures. The same inverse T behaviour is observed, however, with a strong dependence on the readout time t^{delay} and V_G^s, as the effect is most pronounced for an intermediate V_G^s = 37.5 V ($E_{ox} \approx 5\,MV\,cm^{-1}$), and decays for lower and higher field strengths.

5.1.5 Capture and Emission Time Maps

While the (E_T,E_R) map, c.f. Figure 5.10, represents a full picture of the defect properties, which in turn allows to compute ΔV_{th} for arbitrary input signals $V_G(t,T)$, a direct readout of ΔV_{th} from the map for a specific input signal is not possible. Therefore,

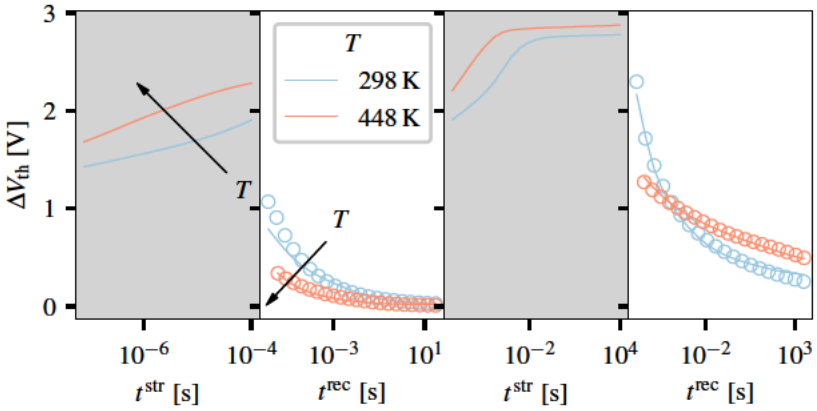

Figure 5.12. The first and the last stress and recovery phases of the full MSM sequence are shown. An interesting feature of the recovery is the enhanced T-activation for electron emission, resulting in a crossover point of the recovery traces of the two temperatures after t_{str}=10 ks. (taken from [CSJ2])

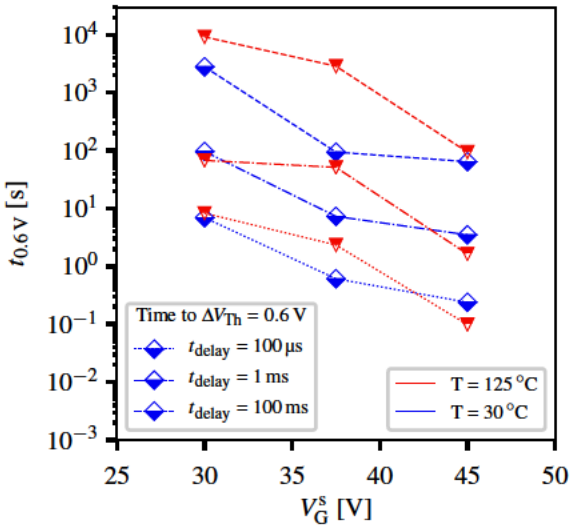

Figure 5.13. The time $t_{0.6\,V}$ to reach ΔV_{th} = 0.6 V is shown for different readout delays for the lateral MOSFETs. The unambigous trend that for most of the (t_{delay},V_G^s) combinations the degradation of 0.6 V (arbitrary chosen) is exceeded after a longer period is again a result of more pronounced temperature activation of the emission compared to electron capture. However, the effect also strongly depends on the selected t_{delay}. (taken from [CSC1])

Capture Emission Time (CET) maps can be used for a direct representation of the degradation for a specific V_G^L, V_G^H and T. A large set of experimentally extracted CET and activation energy maps is shown in previous works of Puschkarsky *et. al* [87, 94, 266]. The main features within these maps are consistent with the previous explanation of a slow and fast degrading and recovering BTI component, transferring into two peaks within these maps. These peculiarities in CET maps extracted from SiC MOSFETs are also prevalent in the lateral test structures, as shown in Figure 5.14 for the experimentally extracted and simulated CET maps.

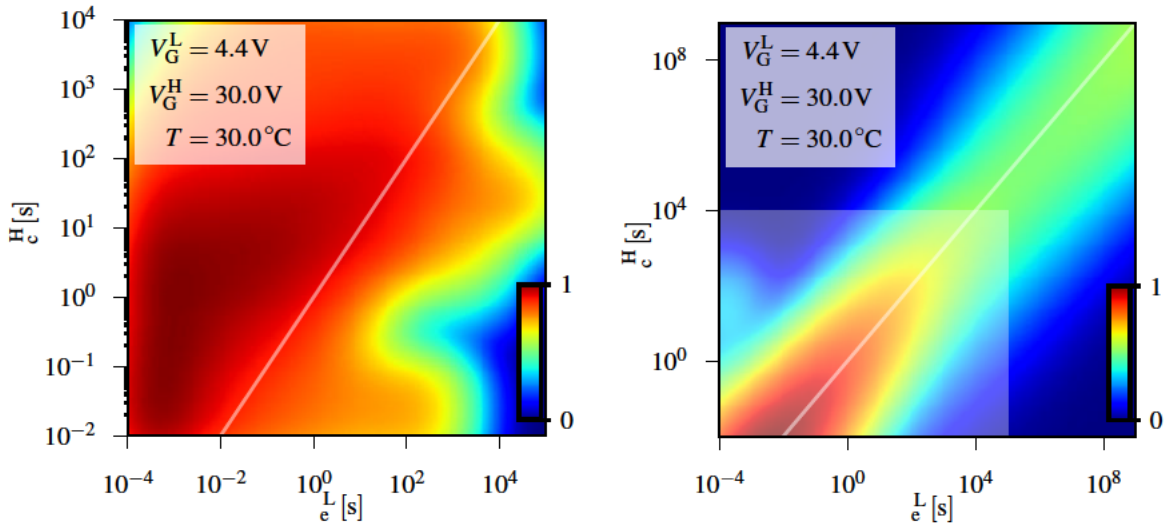

Figure 5.14. The experimentally extracted CET map of lateral MOSFETs **(left)** agrees with the simulation **(right)** in the main features for the noted $V_G^L \approx V_{th}$, $V_G^H = 30\,V$ and $T = 30\,°C$. A peak in the time constant distribution is visible above the $\tau_c^H = \tau_e^L$ diagonal with a decreasing density towards larger τ_c^H and τ_e^L. For the calculated CET map, $\log_{10}\left(1+\kappa V_{th}/V_{th}^{max}\right)$ / $\log_{10}\left(1+\kappa\right)$ with $\kappa = 1000$ has been used to visualize the relatively small contribution of the defects with larger charge transition time constants. The experimental window is represented by the shaded area in the simulated map. (taken from [CSC1])

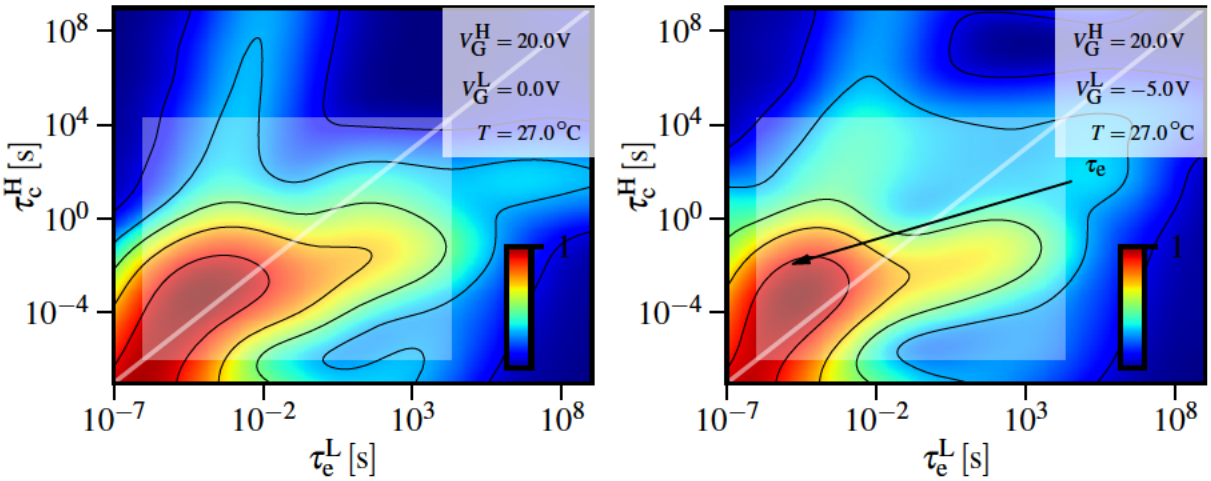

Figure 5.15. A comparison of unipolar AC ($V_G^L = 0\,V$) **(left)** with a bipolar operation $V_G^L = -5\,V$ **(right)** shows the shift of the distribution of charge transtion time constants towards lower emission times, leading to less observable ΔV_{th}. The fast degrading component recovers fast enough and parts of the slow-degrading component is also shifted towards smaller emission times, leading to a smaller overall PBTI due to charge accumulated in electron traps.(taken from [CSC3])

As a bipolar operation of SiC DMOSFETs is recommended [267] as it increases the long term stability of V_{th}, i.e. it reduces long-term BTI, the CET maps of T1/G2 are shown for $V_G^L = 0\,V$ compared to $V_G^L = -5\,V$ in Figure 5.15. The electron trapping time distributions shift towards smaller τ_e^L, which leads to the ascribed effect of enhanced

electron emission at the fast electron traps, c.f. pulsed MSM in Section 5.1.1. This observation has led to the introduction of preconditioning schemes [91, 92] to primarily measure long term BTI effects.

5.1.6 Reliable Prediction of ΔV_{th}

The extrapolation of ΔV_{th} under arbitrary bias and temperature operating conditions is in some works still performed based on fitting a power-law to the measured ΔV_{th} [268]. However, it lacks of any physical justification, e.g. ΔV_{th} never saturates, and in the case of SiC MOSFETs even more than one branch of a power law is needed to describe the different regimes of degradation. This fact is emphasized in Figure 5.16 for a constant voltage DC stress bias, leading to a severe overestimation of the degradation. The application of a Gaussian distribution of charge capture and emission times [55] might be justified in the case of only one defect type accounting for the observed ΔV_{th}, however, in the case of different distributions present, c.f. Section 5.1.4, it leads to an underestimation of ΔV_{th}. Both empirical methods require in any case different parameters for different read-out delays when measuring ΔV_{th}. On the contrary, with a carefully calibrated physical defect model, ΔV_{th} can be predicted for arbitrary input signals and readout delays accurately, shown in Figure 5.16 (right).

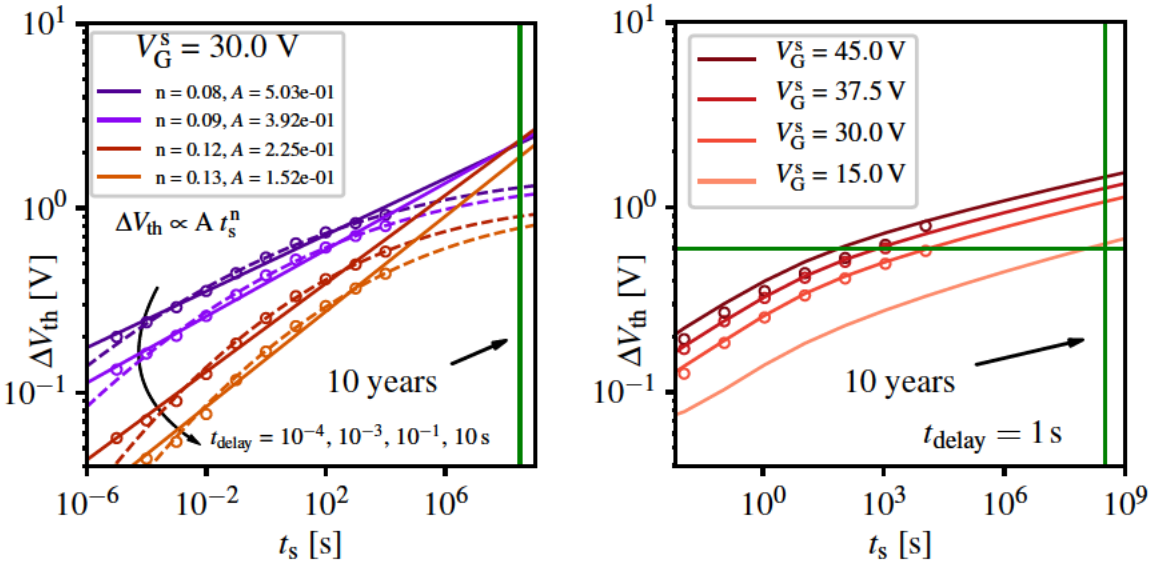

Figure 5.16. Extrapolation of ΔV_{th} with a simple empirical power-law (solid lines) **(left)** lacks not only of physical justification, but also severely overestimates the V_{th} degradation, as the slopes over stress time start to decay after 10^{-1} to 10^{1} s. The strong dependence of the readout time is also not captured by a single power-law exponent. A fit with a simple Gaussian distribution for charge transition times (dashed lines) explains the extracted V_{th} more accurate, however, underestimates degradation at lifetimes. On the contrary, the calculation of V_{th} with a calibrated physical defect model captures the degradation and slopes well for arbitrary bias conditions and measurement delays **(right)**. (taken from [CSC1])

A precondition for the calculation of a valid extrapolation of ΔV_{th} at operating conditions of a MOSFET is the careful design of the stress conditions of the defect parameter extraction. The temperature and stress bias need to be increased to allow to capture charge transition times that are accelerated enough to be shifted into the experimental time window. This acceleration is shown in Figure 5.17 for the harshest PBTI stress conditions ($V_G^H = 25\,V$, T=448 K), which shows a larger defect occupation after the interpolation time of about 100 ks, compared to the occupation after a device lifetime of 10 years at operation conditions ($V_G^H = 20\,V$, T=300 K). Based on the calibration of the

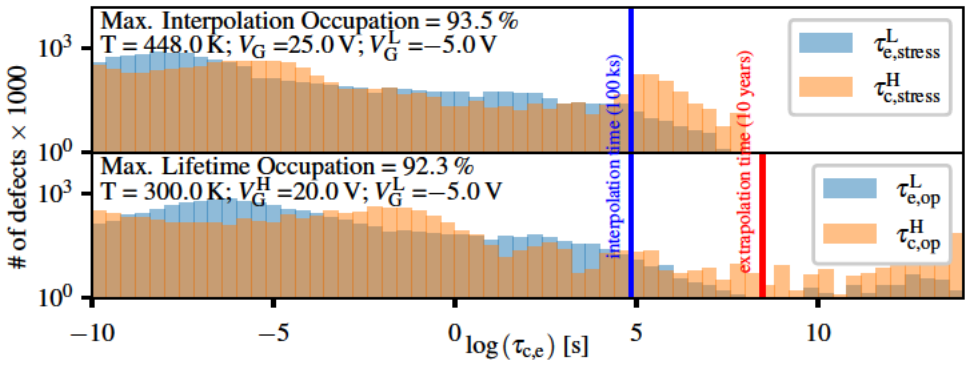

Figure 5.17. A comparison of charge transition time distribution of defects active at harshest stress condition **(top)** with the according distribution for recommended operation of the MOSFET **(bottom)** shows a larger occupation of the defects, i.e. more defects with smaller τ_c^H that are likely occupied after the interpolation time, compared to a lifetime of about 10 years at the operation condition. This renders the computation of ΔV_{th} after such a long lifetime period at operation condition valid.(taken from [CSC3])

DMOSFET technologies in Comphy, a lifetime prediction is presented in Figure 5.18 for each DMOSFET for different digital AC gate signals, as typically applied, considering a continuous operation. For this, the occupation of the defects has been calculated based on (4.60). It becomes clear that the wide distributions of defects with increased densities for T2/G1 leads to the most pronounced drifts of V_{th}, as well as to the largest variation. In contrast, the small densities and absence of hole traps in T1/G3 leads to relatively small drifts during stress, and as low as about 0.2 V only after 10 years, when read out after 10^{-4} µs. Exemplarily shown for T1/G2 is the variation for different (V_G^L,V_G^H) bias combinations with a maximum of about 2 V degradation for unipolar positive bias operation, which refers to the value at the end of the V_G^H phase during the AC period. For all three devices bipolar operation leads to a significantly reduced V_{th} shift when an AC signal is applied and readout is performed at $V_G \approx V_{th}$.

When comparing the overdrive voltage dependence $V_{ov} = V_G - V_{th,0}$ dependence of ΔV_{th} and on-state resistance shift ΔR_{on} at different V_G^L, as shown in Figure 5.19, a minimum of about 8 mΩ increase in R_{on} is predicted after 10 years of continuous operation at the maximum recommended bias conditions. R_{on} is thereby computed from an initially recorded $I_D(V_G)$-curve with only a small deviation depending on the method of $I_D(V_G)$ recording, e.g. continuous sweep or pulsed $I_D(V_G)$ measurement, as discussed and shown in [CSJ1]. The continuous $I_D(V_G)$ characteristics is used for the

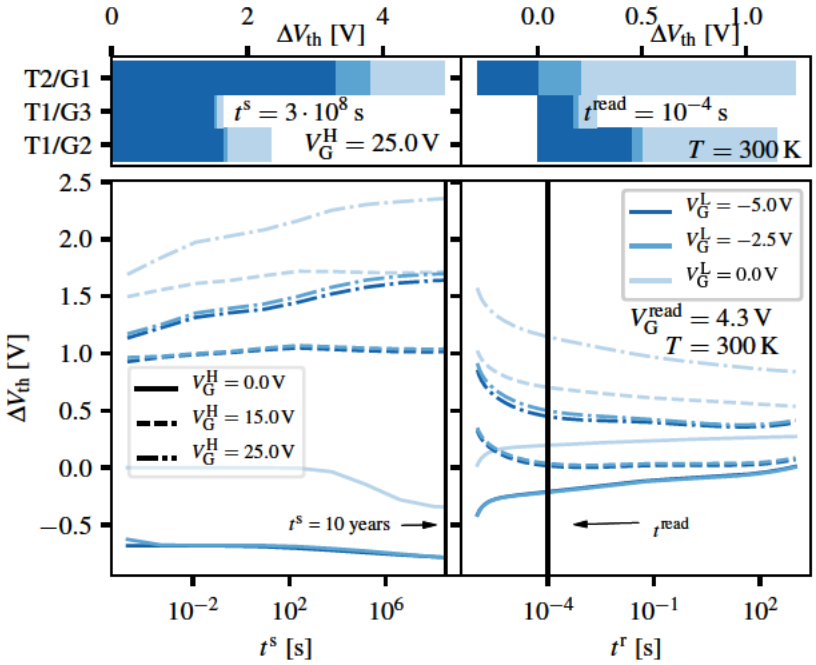

Figure 5.18. An extrapolation of ΔV_{th} analytically computed for bipolar AC stress (f=50 kHz, duty cycle = 0.5) for T1/G2 is shown up to a device lifetime of 10 years for different (V_G^L, V_G^H) **(bottom, left)**. A maximum of $\Delta V_{th} \approx 2$ V is observed for $V_G^L = 0$ V, which is reduced by a factor of 2 for recommended operation ($V_G^L = -5$ V, $V_G^H = 15$ V). A large fraction of the degradation recovers within a short time for readout at $V_G \approx V_{th}$ **(bottom, right)**. The comparison of stress and read-out V_{th} extrapolation of the three technologies **(top)** suggests highest stability for T1/G3, as a result of low electron trap densities and the absence of hole traps. (taken from [CSJ2]).

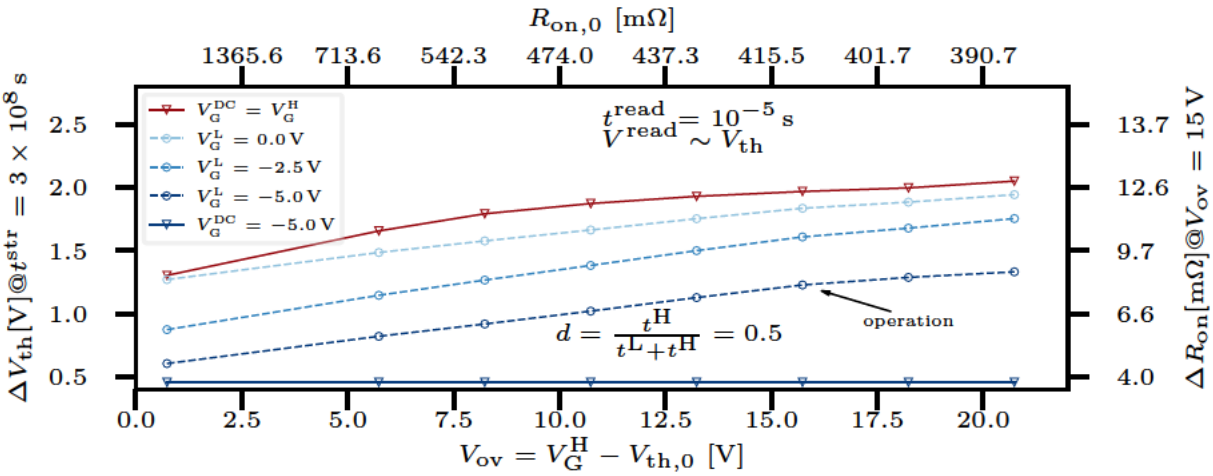

Figure 5.19. A comparison of the overdrive voltage dependence of the V_{th} and R_{on} degradation for a duty cycle of $d = 0.5$ for T1/G2 after 10 years and 10 µs readout time at V_{th}. An initial $I_D(V_G)$ characteristic is used to calculate R_{on} and ΔR_{on}within a range of $\Delta R_{on} \approx 8$ to 13 mΩ for different V_G^L at the largest V_{ov}. This translates to a minor static on state loss increase of less than 1 W considering a constant maximum current as given in the datasheet.(taken from [CSC3])

R_{on} calculation in Figure 5.19, as a readout time of 10 µs after the stress phase, as used for the extrapolation of V_{th} is expected to compensate for potential accumulation pulses during the pulsed $I_D(V_G)$ sweep. With the small static degradation of R_{on} predicted by the simulation, a minor increase of the static on-state losses P_{on} of less than 1 W at continuous current operation at the maximum value according to the datasheet of 10 A can be expected. Finally, in Figure 5.20 the duty cycle $d = t^H / \left(t^H + t^L\right)$ dependence of ΔV_{th} shows only a minor variation of about 0.2 V for relevant d in the range 0.1 to 0.9 for all V_G^L, V_G^H permutations, with larger deviations only obtained for the DC operation cases at constant $V_G = V_G^L$ and $V_G = V_G^H$. This leads to the conclusion that no major deviation due to BTI is predicted for variable high / low voltage conversion operation within a power converter circuit.

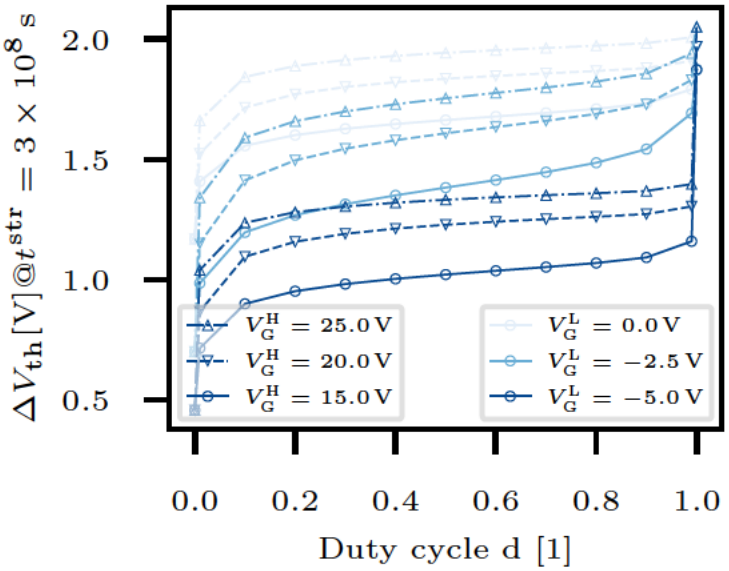

Figure 5.20. Duty cycle d dependence of ΔV_{th} after 10 years of operation at varying V_G^L, V_G^H shows a minor variation over d except for the DC cases. A V_G^L of −5 V significantly reduces the degradation by more than 0.5 V for any V_G^H, when compared to non-negative V_G^L.(taken from [CSC3])

5.1.7 Summary

BTI in different SiC MOSFETs has been reproduced in detail by a device scale model employing physical defect parameters. The parameters for defects causing the long-term degradation are similar to those extracted in Si-based MOSFETs. However, the obtained defect densities are increased due to the different conduction band offsets in SiC/SiO_2, which enables a larger fraction of shallow electron traps to be charged during device operation. These defects are considered an intrinsic property of SiO_2. Together with fast electron traps, the defects close to the SiC conduction band are a common feature extracted in three commercially available DMOSFETs and a lateral test MOSFET, however, vary quantitatively in the extracted densities. The two components, i.e. fast and shallow EB, have been demonstrated to be separable by accumulation pulses and

the optimum operation condition employing bipolar gate drive bias has been explained by the extracted defect charge transition times. These electron trap properties have recently also been confirmed by TCAD simulations employing a detailed four-state NMP model [269]. Furthermore, based on carefully calibrated simulation parameters and including data from accelerated stress experiments, static degradation extrapolation is performed. It predicts that the low on-state resistance and power loss increase can be considered as no major threat in SiC MOSFETs. Although a unique defect candidate cannot be identified with the presented methods, a parameter range is defined in the presented work that can help to further pin down suspected defect structures by single defect characterization in future works.

5.2 Trap-Assisted Tunneling Currents

The results within this section have been previously published in [CSJ4] and [CSJ7].

As outlined in Chapter 1, time-zero leakage currents through dielectrics in MOSFETs or storage capacitors, as well as through back-end of line inter-layer insulators can increase the device power consumption and accelerate the aging of the dielectric. In defective dielectrics, these currents can be enhanced already at low to medium field strengths due to trap-assisted conduction. A detailed understanding of these TAT currents and the properties of the defects that act as transition centers is required in order to both set countermeasures, i.e. optimized material selection and processing, and to include the effects to realistically replicate the device behavior in simulations. Therefore, this section aims to make use of the developed NMP based TAT model from Chapter 4 to explain TAT in SiC MOS technologies reported in previous works [119, 120]. The employed model is further verified by simulation of well explored currents in $TiN/ZrO_2/TiN$ (TZT) structures, as reported also in [270, 111], in detail. The obtained defect parameters to replicate the measured TAT currents can interestingly both be attributed to polarons in the two binary oxides, i.e. SiO_2 and ZrO_2 via comparison to DFT calculations. Finally, the modeling approach is analyzed in terms of the impact of multi-TAT, parameter variation, stochastic properties and computational efficiency.

5.2.1 Tunnel Currents in SiC MOSCAPs

The temperature activated tunneling currents in SiC MOSCAPs reported by Moens *et. al* [120] have been suspected to originate from a trap-assisted conduction due to oxide defects in the vicinity of the interface between the SiC substrate and the thermally grown and 53 nm thick SiO_2 serving as gate oxide. With a moderate doping concentration of $N_D = 10^{16}\,cm^{-3}$ and an n^+-doped poly-Si gate contact, these devices are expected to show similar leakage currents as commercially available MOSFETs. The gate currents have been measured over a wide temperature range of $T = 25$ to 245 °C for oxide field strengths of up to $9\,MV\,cm^{-1}$ at positive gate bias. Increased temperature activation in the regime of $E_{ox} = 5$ to $8\,MV\,cm^{-1}$ has been observed, when compared to FN

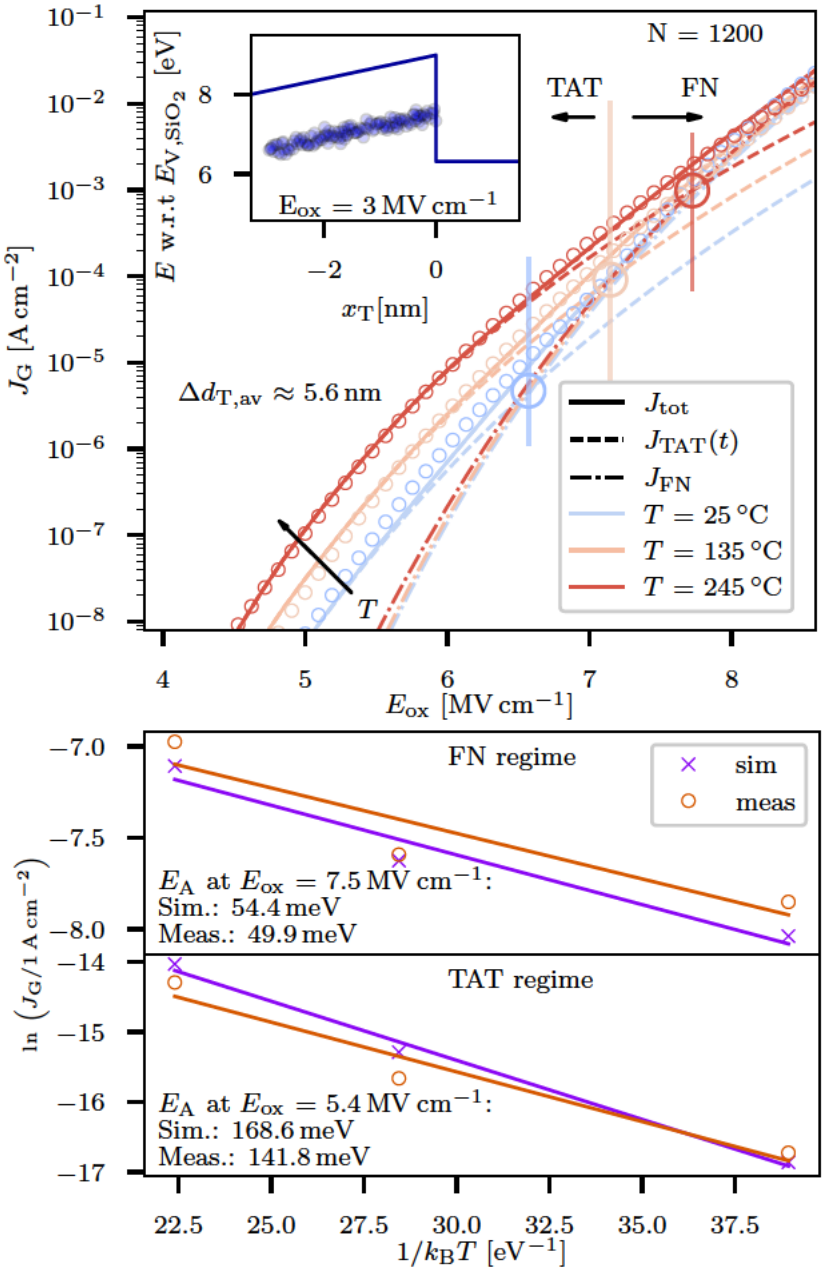

Figure 5.21. $I_G\,(V_G)$ characteristics of SiC MOSCAPs as extracted from the measurement data in [120] **(top)** (circles). The mean values of the simulated transient TAT currents (dashed) as computed by the new TAT model, together with band to band currents as calculated with the Tsu-Esaki model (dash-dotted) and the total currents (solid) as the sum of both contributions are also shown. This total current is in excellent agreement with the data over the entire bias regime. The thermal activation in the TAT and FN regime is accurately captured by the model as shown in the FN plots **(bottom)**. (taken from [CSJ7])

tunneling with negligible T activation which dominates the measured currents at higher fields. To calculate the TAT currents, the device reliability simulator Comphy has been set up by using the same material parameters for the channel substrate as in Table 5.1. A single defect band has been used, with parameters that have been optimized to reproduce the reported measurement data. A least square method based on

a Nelder-Mead algorithm as implemented in the scipy package of Python has been used for this purpose. Figure 5.21 shows the simulation results compared to the measured characteristics with excellent agreement for both, the TAT regime, as computed by the proposed TAT model, as well as the FN regime, calculated by the Tsu-Esaki model. Note that the shown simulations have been performed with $N = 1200$ defects for $M = 100$ slices, and the resulting current densities refer to the average values over M slices at each T. Most importantly, the temperature activation is accurately captured by the TAT calculation as can be seen in the bottom panel of Figure 5.21.

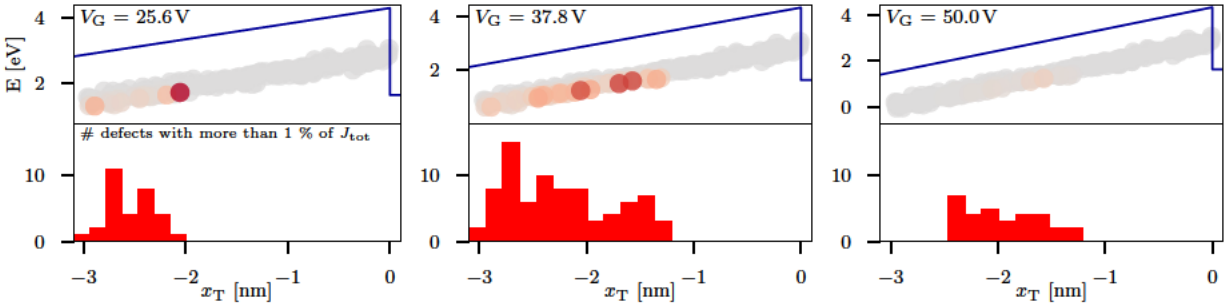

Figure 5.22. The spatial distribution of the defects contributing to the total current shown for low V_G at the limit of the measurement resolution **(left)** between a distance of 2 to 3 nm from the channel interface. At intermediate V_G **(center)**, the shift of the effective trap level towards lower energies results in a shift of the conduction towards lower distances. In the FN regime **(right)** only a few defects contribute more than 1 % to the total current density. The more intense red color indicates a larger contribution to the total current. (taken from [CSJ7])

By analyzing the simulation, the hypothesis of Moens *et. al* of electron capture from the channel at defects within the first few nm of the oxide and further emission to the insulator conduction band can be confirmed. Figure 5.22 shows a spatial resolution of the defects´ current conduction contribution at the intermediate $T = 135\,°C$ that is concentrated within 1 to 3 nm distance from the channel. For lower gate bias, the conducting defects are located further away from the interface. Due to the effective trap level shift with increasing field strengths, the distribution of conducting traps shifts towards the interface. Above about $V_G = 45\,V$, the total current is dominated by direct band to band tunneling, i.e. FN conduction. It should be noted that the defect band has been sampled up to a maximum distance of 3 nm. This distance does not indicate an abrupt stop of the defect distribution but simply reflects the fact that the set-in of the measured current starts at about $V_G = 25\,V$ due to the limited current resolution of available measurement tools. This set-in point, hence, defines the maximum distance, at which the current conduction is observed, and thus sampling further into the oxide has no impact on the computed currents within the relevant bias range. The electron drift within the insulator, upon emission from the defect to the oxide conduction band, can be considered instantaneous within each simulation time step. This assumption is justified, as typical drift velocities in SiO_2 exceed drift velocities of $v_D \approx 10^7\,cm\,s^{-1}$ at $E_{ox} > 1\,MV\,cm^{-1}$ [271] and therefore a drift time of less than 1 ps in a 100 nm oxide can be expected. Such a drift time is orders of magnitude faster than time-scales that

can be measured by ultra-fast current measurement setups with resolutions in the µs regime [151].

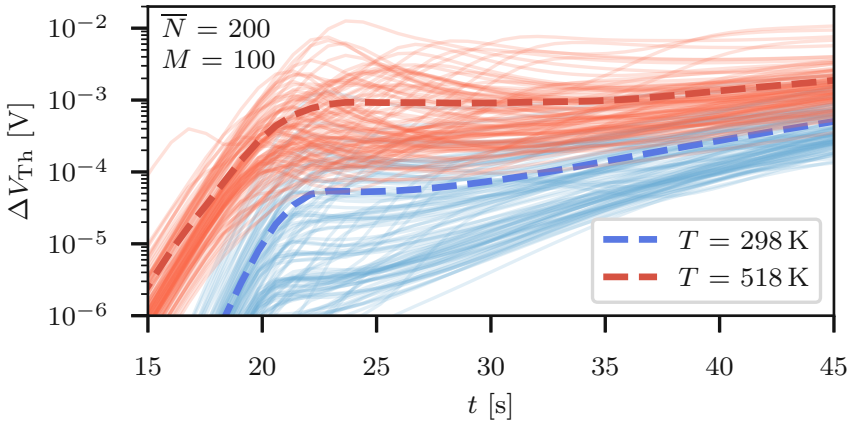

Figure 5.23. The mean transient shifts (dashed) of the threshold voltage, which are proportional to the defect occupations are shown for $\overline{N} = 200$ at the minimum and maximum T, together with their statistical distribution within $M = 100$ slabs (solid). The time range of 15 to 20 s refers to the set in point of the current conduction at about $V_G = 25$ V, c.f. Figure 5.21. The low defect occupation leads in all simulations to $\Delta V_{th} < 10$ mV and therefore renders the defect band responsible for TAT insignificant for BTI. (taken from [CSJ7])

Furthermore, the simulated currents are in steady-state, i.e. the electron is captured from the channel at the defect site and instantaneously emitted to the insulator conduction band within one time-step. This is caused by capture and emission times which are orders of magnitude smaller than the selected time steps. For example, at $V_G \approx 28$ V and $T = 298$ K, the capture time from the channel $\tau_{c,chan}$ as well as the emission time to the gate $\tau_{e,gate}$ are in the range of 10^{-4} s which is significantly smaller than the time step of 1 s. Additionally, no charge builds up in the TAT defect band with defect occupations $f_T < 10^{-4}$ for all (V_G, T), which translates to minor threshold voltage shifts $\Delta V_{th} < 10$ mV at all time steps, as shown in Figure 5.23. With such low ΔV_{th}, which is about a factor of 100 smaller than ΔV_{th} observed in SiC MOSFETs, the TAT defect band can be considered to have no impact on charge trapping, i.e. no contribution to BTI within the time regime of ms to s is expected.

Band	$\langle E_T \rangle$	σ_{E_T}	$\langle E_R \rangle^*$	σ_{E_R}	$x_{T,max}$	N_T
TAT	2.85 eV	0.1 eV	0.89 eV	0.11 eV	3.0 nm	$7.6 \times 10^{18}\,\mathrm{cm}^{-3}$
polarons (DFT)	2.53 eV	0.23 eV	1.06 eV	0.23 eV	-	-

Table 5.7. The defect parameters of the two-state NMP model as obtained for technology 1 from Comphy (TAT) and DFT (polarons) are listed. Note that the thermodynamic trap-levels E_T are referred to the SiC mid-gap level. $^*\langle R \rangle^{DFT} = 1.35$ recalculated with the E_R-R correlation (5.1) for R = 1 as denoted in Figure 5.26.

In Table 5.7, the extracted parameters needed to describe the observed TAT currents are listed. Contrary to defects that are typically responsible for charge trapping, the

distance of the thermodynamic trap level to the channel conduction band edge is relatively large for this trap band. At the same time low relaxation energies are obtained in comparison to oxide defects that are suspected to cause BTI in technologies employing SiO_2 layers [81, 178, 177].

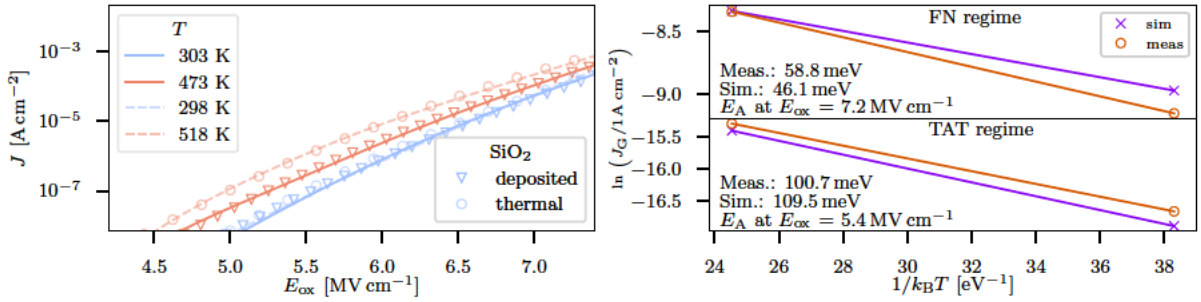

Figure 5.24. The reported tunneling currents on MOSCAPs [120] employing thermally grown 53 nm thick oxide (circles) are compared to the measurement data extracted from poly-Si/SiO_2/SiC MOSFETs with a deposited 70 nm thick oxide (triangles) **(left)**. The simulations (lines) for both structures are performed with the same defect parameters (Table 5.7) and agree with the measured I_G (V_G) characteristics. As in the case of the MOSCAPs, c.f. Figure 5.21, the thermal activation of TAT as shown in the FN plots **(right)** is well captured by the simulation.(taken from [CSJ7])

As the oxide of the MOSCAPs reported in [120] is thermally grown silica, it potentially exhibits a different stoichiometric composition compared to a deposited SiO_2 layer, which is used in trench MOSFET fabrication. Such a different composition could potentially be introduced from residues of the TEOS [45] based precursor. Also, different structural properties of the oxide due to altered process temperatures can be expected. To investigate the impact of a different oxide deposition process on the oxide defect band, the gate leakage measurements have been repeated on lateral MOSFETs employing a 70 nm thick SiO_2 layer, which was passivated after CVD oxide deposition in NO ambient. Note, that the different surface termination of the a-face on trench MOSFETs compared to the Si-face on lateral devices could modify the band alignments between SiC and SiO_2 [23] and therefore an investigation of leakage currents in trench MOSFETs was deliberately avoided for this study. The leakage currents of the MOSFETs with gate area $W \times L = 1.95\,mm^2$ have been measured with an Agilent B1500 Parameter Analyzer and a Keithley 708B Switching Matrix Mainframe by sweeping the gate bias from 20 to 60 V at a rate of $33\,mV\,s^{-1}$ with a step size of 10 mV at a constant drain bias of V_D= 0.1 V and grounded source terminal for two temperatures T = 303 and 473 K. The resulting sweeps are shown in Figure 5.24 together with those of the MOSCAPs as a reference. Despite the modified gate stack configuration, the simulations performed with the same defect parameters can accurately reproduce the gate leakage characteristics of the n-MOSFETs with the slightly thicker oxide. In this way, the temperature activation in the TAT and the FN regime show perfect agreement, as can be seen from the FN plots. Thus, it can be concluded that deposited and thermally grown oxides show similar time-zero gate leakage performance in the positive bias regime.

The hypothesis of a narrow spatial defect distribution in SiC/SiO_2 MOSFETs that enables the leakage current has already been presented earlier by Chbili *et. al* [119]. The simulations performed in this work agree with their observation and confirm the suggestion of a "sweet spot" for conduction. Thus, a certain spatial position x_T and a thermodynamic trap-level E_T are required to enable leakage currents in the tens of nm thick oxide. Additionally, in the work of Fiorenza *et. al* [117], a similar mechanism is reported for NBTI, however, due to the transient decay of the gate currents shown in their work, these currents are more likely caused by charge trapping.

At higher oxide fields above $8\,\mathrm{MV\,cm^{-1}}$, impact ionization is reported to play a crucial role in SiO_2 [121] and should be considered in an expanded transient modeling approach. Nonetheless, the scope of the herein presented model is limited to time-zero characterization, thus also neglecting time dependent SILC, which may stem from defect generation, or reconfiguration of oxide defects which can open up a leakage path [130]. However, these effects are considered to be negligible within the short time ranges in which the gate bias sweeps are performed on pristine devices.

5.2.2 Tunnel Currents in TZT Structures

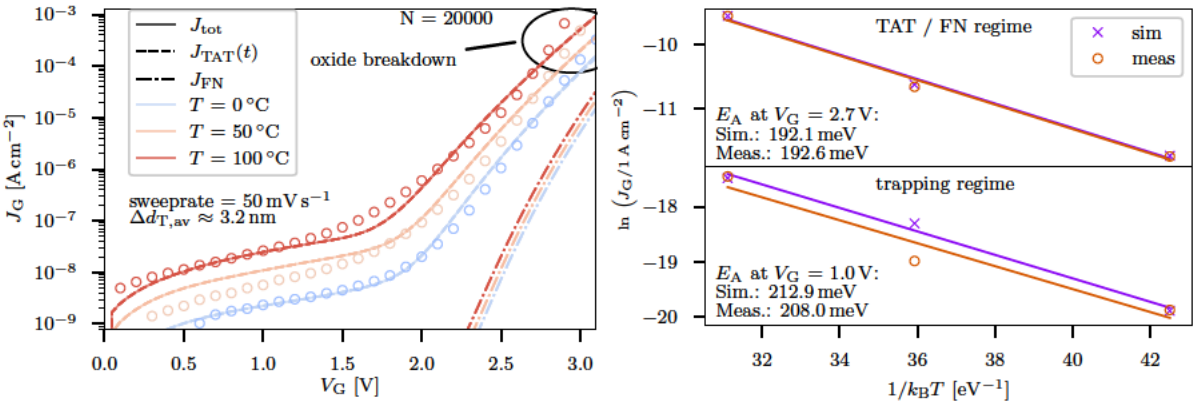

Figure 5.25. The MIM structures with single layered ZrO_2 show two branches in the TAT currents **(left)**. The low to medium gate bias leakage currents up to $V_G \approx 1.5$ V appear due to charges captured from the channel at defects energetically aligned to the Fermi-Level. This branch is not a steady-state current, but rather a transient current **(dashed lines)**. The second steeper branch above $V_G \approx 2$ V, on the other hand, shows TAT-FN characteristics in steady-state like as for the MOS structures shown in Figure 5.21. The temperature activation of both regimes **(right)** shows apparent activation energies around 200 meV and is well captured by the simulations. (taken from [CSJ7])

For further validation of the proposed TAT model, a well explored dielectric leakage mechanism as observed in $TiN/ZrO_2/TiN$ (TZT) capacitors, is investigated. These structures have been established in DRAMs as storage capacitors [272]. Besides the advantages that lower supply voltages can be used by employing the high-k dielectric, while conserving the necessary electric field to store and erase charges at physically thicker layers compared to low-k dielectrics, large thermally activated leakage currents

have been reported in TZT stacks at low and medium field strengths [270, 273]. These detrimental leakage currents limit further down-scaling of the devices.

In order to explain the different slopes and thermal activation of the currents in the low and medium field strengths regimes, Jegert *et. al* used a kinetic Monte Carlo approach to explain the TAT currents [245]. This modeling approach based on a Gillespie algorithm [274] has the advantage of straight forward acquisition of a solution of charge transfer reactions using a stochastic probability density function that is equivalent to solving the Master equation deterministically, as in the herein presented approach. However, it comes at the cost of an inexact time sampling for reactions that show time constants distributed over many decades. This might be the reason why their modeling fails to explain the low field transient currents and only captures one component of the TAT mechanism. Additionally, elastic tunneling has been used for defect to defect charge transfer and inelastic tunneling for the reactions between defects and reservoirs, which seems non-physical, see discussion in Chapter 4. For the verification of the multi-TAT model, data of capacitors with 8 nm thick ZrO_2 contacted with TiN electrodes with an area of about $10^{-4}\,cm^2$, as reported in [111], has been used as a reference, which is equivalent to the data presented in [245]. As shown in Figure 5.25 the multi-TAT model described in Chapter 4 can explain both the shallow sloped currents at $V_G < 1.7\,V$, as well as the steeper slopes in the tunnel current for $V_G > 1.7\,V$. At oxide fields above $E_{ox} \approx 3.5\,MV\,cm^{-1}$ ($V_G \approx 2.5\,V$) the onset of oxide breakthrough can be seen, which explains the increasing slopes of the leakage current, compared to decreasing slopes of TAT currents in the simulation.

Band	$\langle E_T \rangle$	σ_{E_T}	$\langle E_R \rangle$	σ_{E_R}	$x_{T,max.}$	N_T
TAT band	1.09 eV	0.1 eV	0.76 eV	0.1 eV	-	$3 \times 10^{19}\,cm^{-3}$
polarons (DFT)	1.24 eV	0.2 eV	0.7 eV	0.15 eV	-	-
charge trapping band	0.35 eV	0.12 eV	2.6 eV	0.1 eV	-	$6 \times 10^{19}\,cm^{-3}$

Table 5.8. The NMP parameters extracted by the TAT model to explain the leakage currents of TZT capacitors compared to those obtained from DFT calculations are given. Note that the thermodynamic trap levels E_T are referred to the TiN work function level.

In order to explain the measurement data, two defect bands are required with parameters shown in Table 5.8. The lower slope currents at low field strengths are thereby explained by the "trapping" band, with mean $E_T = 0.35\,eV$ above the TiN conduction band edge, and mean relaxation energies of $E_R = 2.6\,eV$. These relatively large relaxation energies for defects deep in the ZrO_2 band gap in combination with aligned thermodynamic trap levels to the electrode conduction band edge leads to a transient charge trapping current which decays with increasing time at a constant bias level. The relaxation energies are too large to allow for a conduction towards the second TiN contact and defect levels are too deep to emit electrons to the ZrO_2 conduction band. Thus, the Shockley-Ramo current for charge capture is measured. These observations are fully consistent with the measurement data reported in [245, 270] as "transient" or

"relaxation" currents. For the steeper slope currents at medium field strenghts, the same conduction mechanism is responsible that has been observed for the SiC MOSCAPs and MOSFETs. The TAT defect band in between the conduction band edges of the electrode and oxide with relatively low relaxation energies enables a steady-state TAT current, with electrons captured at the defects and instantaneously, i.e. within the time scales defined by the sweep rate of 50 mV s^{-1}, emitted to the ZrO_2 conduction band.

5.2.3 The Role of Polarons

The DFT calculations presented within this section were performed by Dominic Waldhoer.

When taking a closer look at the NMP defect parameters in Table 5.7 and Table 5.8 of the defects that are necessary to replicate the measured leakage currents in both technologies, two common features can be observed. First, the thermodynamic trap level E_T lies in between the conduction bands of the reservoir electrode or semiconductor channel, respectively, and the insulator. Second, the relaxation energies which mainly impact the charge trapping kinetics are small when compared to common oxide defect structures considered responsible for charge trapping [81, 178, 177], whose relaxation energies are in the range of 1.5 to 4 eV, c.f. also Section 5.1. Considering these prerequisites, a class of defects widely studied by ab-initio methods in binary oxides [275, 276, 277, 227, 182, 278, 184], the so-called polaron has to be taken into account as a potential defect structure candidate. In a-SiO_2 polarons are associated with electrons trapped at an elongated O-Si-O bond. The self-trapped electron, as the polaron is also named in SiO_2, fullfills the requirement of a small relaxation energy with E_R = 0.72 to 1.7 eV as for instance calculated in [182]. However, in the work of El-Sayed *et. al* only a small number of these elongated O-Si-O bonds have been calculated. Therefore, an extension towards a larger statistical data set is required to capture the distributed defect properties in amorphous silica as discussed in [CSJ7] and also in the following. For this purpose, by applying a melt-and-quench technique within a molecular dynamics (MD) calculation including 216 atoms in a 3x3x3 supercell of β-crystobalite, models of a-SiO_2 structures have been prepared. The exact procedure and parameters used for the MD calculations employing Reax-FF force fields to model the interactions between the individual atomic species are explained in detail in [182]. A further relaxation of the atomic positions and cell vectors of the prepared sample structures was then calculated within DFT [279] to reduce the atomic forces below a threshold of 25 meV $Å^{-1}$ and the internal stress below 0.01 GPa. For this, a Gaussian Plane wave method within the CP2K code [280] has been used and to expand the electron density and wavefunctions a double-ζ Goedecker-Teter-Hutter [281] basis set has been employed. For an accurate calculation of the electronic structure, the non-local hybrid exchange-correlation (XD) potential PBE0_TC_LRC [282] has been used. These calculations resulted in a single-particle bandgap of 8.1 eV in good agreement with the experimentally observed gap in thin SiO_2 films of about 8.9 eV [283]. To reduce the high computational costs for the accurate calculation of the Hartree-Fock exchange integral, it has been approximated by a small auxiliary basis set within the Auxiliary Density Matrix method [284].

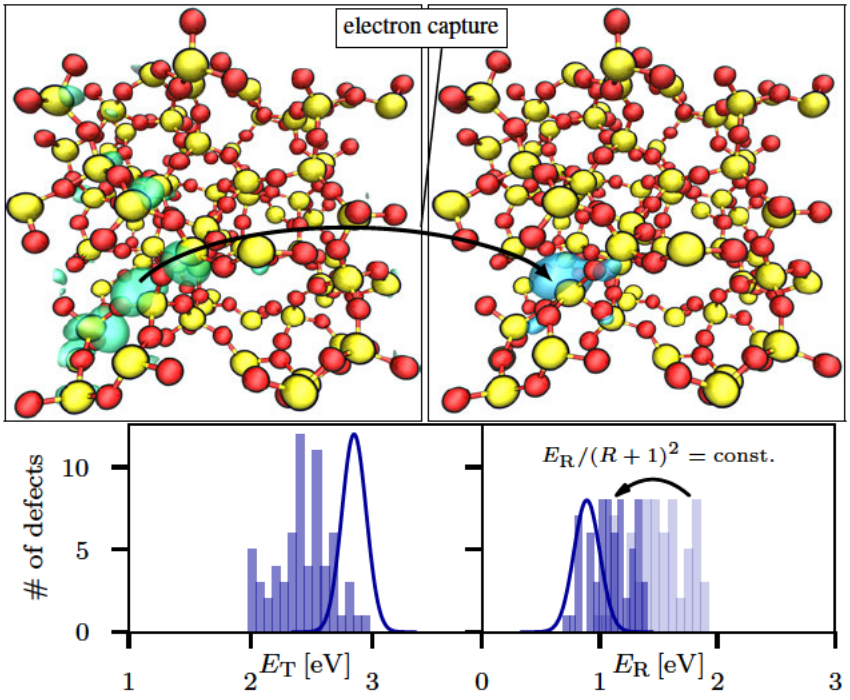

Figure 5.26. A sample of an a-SiO_2 structure is shown within a ball-and-stick representation with Si atoms in yellow and oxygen atoms in red. The lowest unoccupied orbital **(top, left)** collapses to a localized wave-function upon the capture of an electron **(top, right)** at elongated Si-O-Si bonds, which act as the polaron trapping sites in this structure. The distribution of the NMP defect parameters **(bottom)** obtained from DFT (histogram) are compared with those used in Comphy to explain the experimental data (lines), c.f. Table 5.7, and show reasonable consistency. (taken from [CSJ7])

The resulting disordered atomic structures contain partially-localized empty states in the vicinity to the conduction band edge of SiO_2, as shown in Figure 5.26 (top left). Upon electron injection these wavefunctions collapse onto a single Si atom [285] which together with a structural relaxation results in the localized polaron state, shown in the right panel of Figure 5.26. The energy that is dissipated to the energy reservoir, i.e. the surrounding thermal bath, during this relaxation process directly gives the relaxation energy E_R, while the thermodynamic trap levels E_T have been derived by employing the methodology presented in [286]. As spurious electrostatic self-interaction occurs in charged cells with periodic boundaries, a Makov-Payne correction scheme [287] has been used for its compensation. Both statistical distributions of the charge transfer parameters (E_T, E_R) are shown in the bottom panel of Figure 5.26 together with the bands used in Comphy and listed in Table 5.7. A reasonably good agreement between the E_T used for the TAT calculation and the DFT calculations is observed. As for the relaxation energy, due to a slightly higher value of the curvature ratio of $R^{DFT} = 1.35$, a transformation due to the parameter correlation of the relaxation energies with curvature ratios as explained in Section 4.8 is required for comparison with the two-state NMP parameters.

The correlation is given by [CSJ6]:

$$\frac{E_R^{DFT}}{(R^{DFT}+1)^2} \approx \frac{E_R^{corr}}{(R^{Comphy}+1)^2} \approx constant \tag{5.1}$$

and when applied it indeed results in an excellent agreement between E_R^{DFT} and E_R^{corr}. Thus, polarons are considered to be a likely defect candidate responsible for the observed TAT currents in SiO_2.

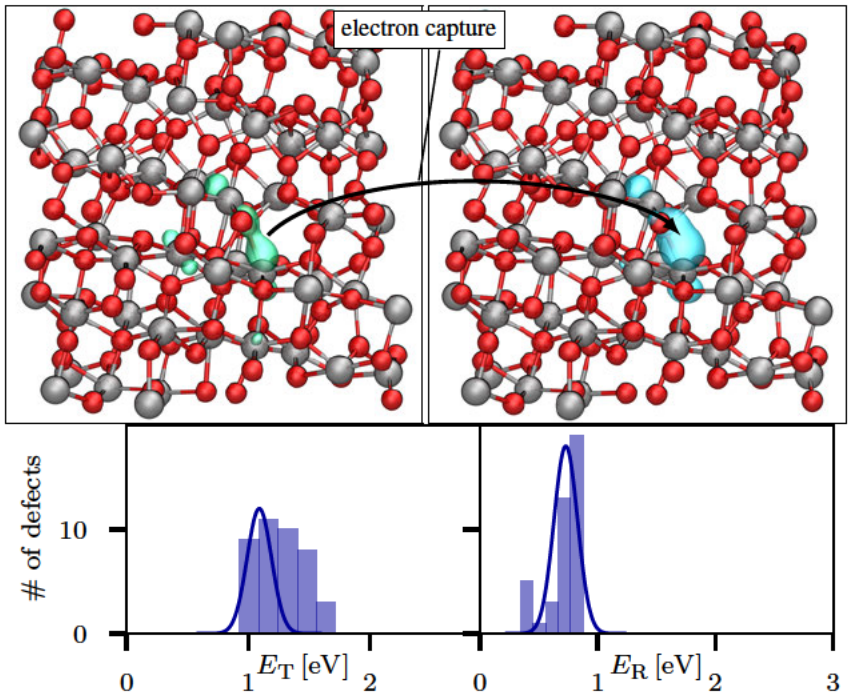

Figure 5.27. A sample of a partially re-crystallized ZrO_2 structure is shown within a ball-and-stick representation with Zr atoms in gray and oxygen atoms in red. The lowest unoccupied orbital **(top, left)** collapses to a strongly localized wave-function upon the capture of an electron **(top, right)** at the polaron which acts as trapping site in this structure. The distribution of the NMP defect parameters **(bottom)** obtained from DFT (histogram) are compared with those used in Comphy (lines) to explain the experimental data, c.f. Table 5.8, and as in the case of the SiO_2 polaron study an excellent agreement can be observed. (taken from [CSJ7])

In order to create a-ZrO_2 models by MD simulations, a similar method as for the SiO_2 models was applied by using Buckingham-like force fields that have been parameterized for high-k $ZrHfO_4$ alloys [288] from 3 x 3 x 3 cubic ZrO_2 cells. Varying quench rates in the range of 5 to 20 K ps^{-1} have been employed to achieve different grades of crystallinity throughout the samples, as ZrO_2 is known to partially recrystallize during device processing [289]. In the resulting structures shown in Figure 5.27, the crystal planes can be clearly identified, however, with local spatial distortions of the atoms. For the DFT calculation, the same parameters and models have been used as described above for the SiO_2 models. Thereby, a bandgap of 5.9 eV was computed which shows excellent agreement to values reported from experiments, e.g. E_G = 5.8 eV [290]. Local oxygen deficiencies lead to a precursor site for polarons, shown in Figure 5.27 (top

left). Here, electrons can localize to form a polaron state as can be seen in the right panel. These observations agree well with those obtained from other non-glass forming oxides [184, 289]. When comparing the statistical distribution of the charge transfer parameters calculated within DFT as in the case of SiO_2 to the TAT band parameters for the TZT structures used in Comphy, the good agreement is evident.

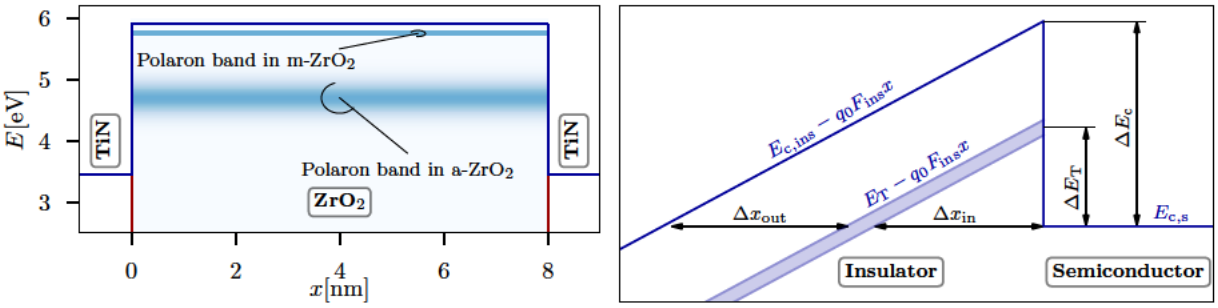

Figure 5.28. Polarons in amorphous zirconia fulfill the requirements for forming an efficient TAT conduction path, while in monoclinic ZrO_2 the E_T of the band becomes discrete (very narrowly distributed) and too close to the conduction band edge **(left)**. For a generic formation of a TAT path, the defect level for a given oxide field F_{ins} needs to be aligned with the conduction band of the semiconductor **(right)**. (taken from [CSJ7])

Since both structures investigated herein employ binary oxides and show a strong indication for a polaron-assisted leakage current, the question arises, whether this mechanism can generally be expected in gate stacks or capacitors employing SiO_2, ZrO_2 or the structurally very similar HfO_2. One prerequisite for a defect band to contribute to an electron TAT current is that the thermodynamic trap level lies in between the conduction bands of the electrode and the insulator or, for a hole TAT current in between the valence bands. In the following the conditions for an electron TAT current will be described while similar considerations apply to a hole TAT current. This energetic alignment of the trap-level is observed in non-crystalline materials, as shown for the a-ZrO_2 defect level distribution as obtained from DFT in Figure 5.28 (left). By analyzing a few samples of the model that have fully recrystallized, these show a defect band with very narrow distribution in the vicinity of the insulator conduction band, as shown in the same figure for monoclinic ZrO_2 (m-ZrO_2). In general, the polaron band is expected to be a bulk property of the oxides and therefore it is likely that it shows a uniform defect density. In contrast, the density of interfacial defects typically decays towards the bulk oxide. With the preconditions of an amorphous dielectric layer in the material system and a homogeneous density of such a bulk defect band, some approximate numbers shall be given to define an energetic and spatial range where polarons can play a role to enable TAT currents. As for the energetic alignment of the trap level, its distance $\Delta E_T = E_T - E_{c,s}$ to the insulator conduction band $E_{c,ins}$ needs to be aligned to the conduction band edge, i.e. in a first order approximation, the Fermi-Level. Furthermore, the defect needs to be located at a distance Δx_{in} of the electrode, as schematically shown in Figure 5.28. From this, with $\Delta E_T - q_0 \Delta x_{in} F_{ins} = 0$ the first energetic precondition is

obtained as

$$\Delta E_T = q_0 \Delta x_{in} F_{ins}. \tag{5.2}$$

Both the distance for tunneling to the defect as well as the distance Δx_{out} for tunneling to the insulator $E_{c,ins}$ from the defect need to be sufficiently small, as the tunneling probability decays exponentially. The relation for the full tunneling distance is given by

$$\Delta E_c = q_0 \left(\Delta x_{in} + \Delta x_{out}\right) F_{ins}. \tag{5.3}$$

When eliminating F_{ins} by inserting (5.2) in (5.3), the relation $\Delta x_{out} = \Delta x_{in} \left(\Delta E_c / \Delta E_T - 1\right)$ for the output distance as a function of the input distance gives the second energetic condition as defined by the ratio of conduction band edge distance and trap level difference. Assuming a maximum field strength of F_{ins} = 10 MV cm^{-1}, which a high quality insulator can sustain, and a conservative maximum tunneling distance of 2 nm together with the conservative condition that $\Delta x_{in} = \Delta x_{out}$ then leads to $\Delta E_c = 2\Delta E_T$ with ΔE_T = 2 eV. Based on these assumptions, both ΔE_T and ΔE_c - ΔE_T are required to be smaller than 2 eV to efficiently enable TAT currents. It has to be noted that additionally sufficiently fast charge transfer kinetics as enabled by the relatively small relaxation energies are needed, as observed for polarons. Hence, the conclusion is drawn that polarons in gate stacks based on amorphous or polycrystalline binary oxides are likely to enable trap assisted tunneling currents.

5.2.4 Model Verification

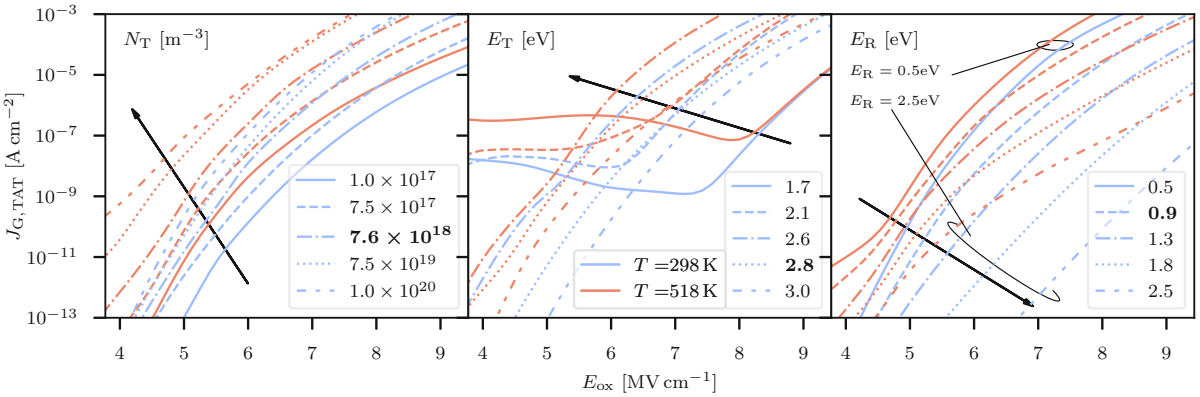

Figure 5.29. Impact of the parameters on the total TAT current is shown. N_T **(left)**, E_T **(center)** and E_R **(right)** are varied by a wide range around the extracted defect parameters from Table 5.7 in **bold** for a constant defect number $\overline{N}$ = 200. While J_G scales with N_T, the shape of the characteristics is strongly influenced by the mean trap level E_T. A wide variation of E_R shows the strong influence of this parameter on the temperature activation of the current. (taken from [CSJ7])

In the past three sections, the capabilities of the TAT model to reproduce measured currents and the consistency of the employed NMP parameters with DFT calculations

have been demonstrated. Within this section, an overview of the impact of the individual model parameters together with the stochastic properties of the Monte Carlo sampling approach as well as the relevance of multi-TAT shall be discussed. In Figure 5.29, the impact of a variation of the defect density N_T, trap level E_T and relaxation energy E_R on the $I_G\,(V_G)$ characteristic is shown for the minimum and maximum T. Here, the parameters are varied around the extracted values given in Table 5.7. Note that only simulations of single slabs with $\overline{N} = 200$ defects are shown, and therefore a stochastic variation of the presented results is expected. A scaling effect of the current density is mainly obtained from the N_T variation, with minor impact on the $I_G\,(V_G)$ shape. A more complex behavior is observed for the trap-level variation, as a shift towards the channel conduction band ($E_{c,SiC} = 1.62\,\text{eV}$) can lead to severe charge trapping currents with shallow sloped TAT currents at $E_T = 1.7$ and $2.1\,\text{eV}$, while a further increase of the trap level leads to smaller current densities at a higher bias set-in point for the currents, c.f. discussion in the previous section. The relaxation energy mainly impacts the charge transfer kinetics, and can drastically change the shape of the $I_G\,(V_G)$ curves, as not steady-state but transient currents are observed for larger E_R. Additionally, increased E_R leads to increased thermal activation of J_G, while a relaxation energy reduction creates the opposite effect.

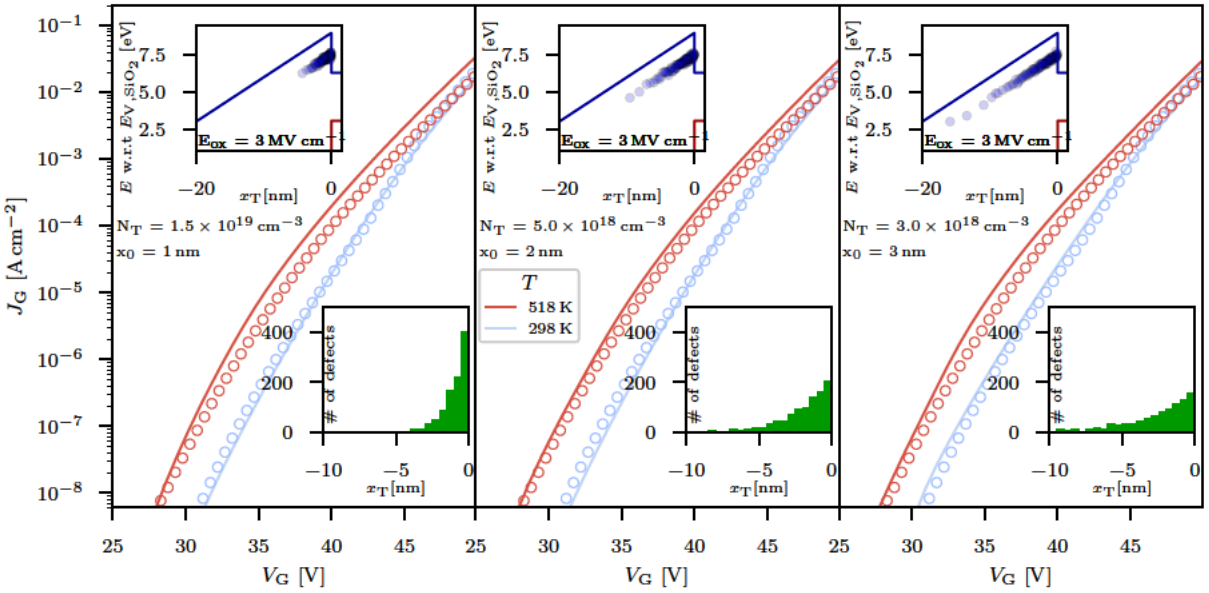

Figure 5.30. The effect of non-uniform spatial defect distribution, as proposed in literature, is shown for the polaron trap band with different scaling parameters $x_0 = 1$, 2 and 3 nm. The total densities (calculated within the extension of the band) decrease from $N_T = 1.5 \times 10^{19}\,\text{cm}^{-3}$ to $3 \times 10^{18}\,\text{cm}^{-3}$ with increasing x_0 in order to reproduce the experimental data. This effect is therefore considered to be of second order and since polarons are a bulk-SiO_2 property, a uniform distribution is likely.

Close to the interface, the defect density is likely no longer uniformly distributed but is expected to increase due to the stoichiometric disorder and strains present within interfacial layers. Thus, the TAT currents are calculated for an exponentially decaying distribution, as shown in Figure 5.30 with $N_T\,(x) = N_T\,(0)\exp\,(-x/x_0)$ for scaling

parameters of $x_0 = 1, 2$ and 3 nm. As a result, the reproduction of the currents requires a defect density variation of $N_T = 1.5 \times 10^{19}$, 5×10^{18} and $3 \times 10^{18}\,\mathrm{cm}^{-3}$ for increasing x_0 respectively. Note that these N_T are calculated within the maximum distance of the defect band. However, the density in the relevant distance for polaron conduction is fairly constant at about $8 \times 10^{18}\,\mathrm{cm}^{-3}$, rendering the spatial defect density distribution a second order effect for the bulk polaron defects.

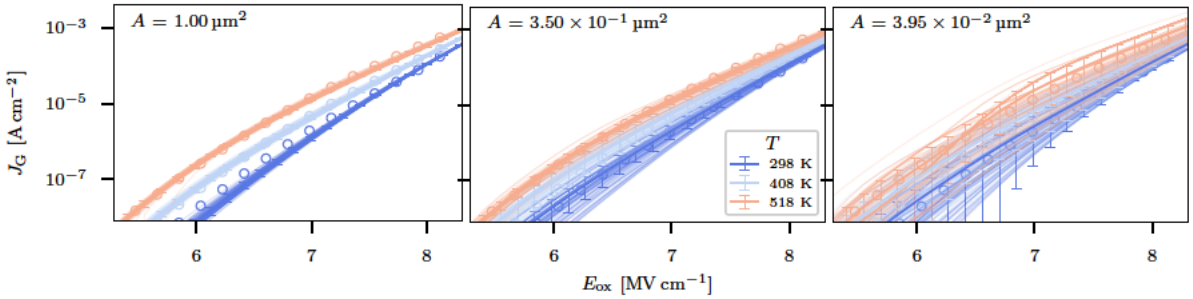

Figure 5.31. A comparison of the variance of gate leakage currents is shown for different total gate contact areas $A = MA_i$ with $M = 100$ samples each as computed by the charge-hopping model. The mean values (thick) lines are in good agreement with the experimental data for all $A \approx 1$ and $3.5 \times 10^{-1}\,\mu\mathrm{m}^2$ **(left)**, **(center)**, which correspond to a defect number $\overline{N} = 1200$ **(left)** and $\overline{N} = 200$, respectively. Quite to the contrary, the error bars representing the standard errors of the M calculations increase from the smallest variation in the largest device up to a large variance in the smallest device with only $\overline{N} = 80$ defects within one sample at $A \approx 3.95 \times 10^{-2}\,\mu\mathrm{m}^2$, as a result of the stronger impact of the Poisson distribution of the actual defect number. While the simulated areas are orders of magnitude smaller than a typical device area required to measure leakage currents in the fA regime, the large area current density can already be explained with $\overline{N} = 1200$ at reasonable accuracy. (taken from [CSJ7])

Another important aspect of the simulation accuracy is the stochastic variability due to Monte Carlo sampling. The stochastic properties of the extracted defect band of the SiC MOSCAPs are therefore shown in Figure 5.31 for different numbers of average defects $\overline{N} = 1200$, 200 and 80 defects with $M = 100$ samples each. While for the largest defect numbers no significant variations from the mean values can be observed, the smaller defect numbers result in large variability, as indicated by the error bars, representing standard errors. Alternatively, the results can also be interpreted in terms of large to small area device variability. Hence, the impact of the Poisson distributed number of defects introduces an additional stochastic variation for smaller defect numbers, an effect typically observed in small area devices. Even though the largest number of defects used for the simulation with a repetition of $M = 100$ yields only a total device area of $A = A_i M \approx 1\,\mu\mathrm{m}^2$ with $A_i = N/N_T x_{max}$, the variance around the mean value is small enough for an accurate representation of a large area device with electrode areas in the mm^2 range. Such large devices are inevitable to accurately resolve the measured tunneling current densities, as commercially available measurement equipment provides at best a current resolution in the tens of fA range.

As already discussed in Section 4.7, multi-TAT is unlikely to occur within the polaron band, as electrons are instantaneously transmitted to the insulator conduction

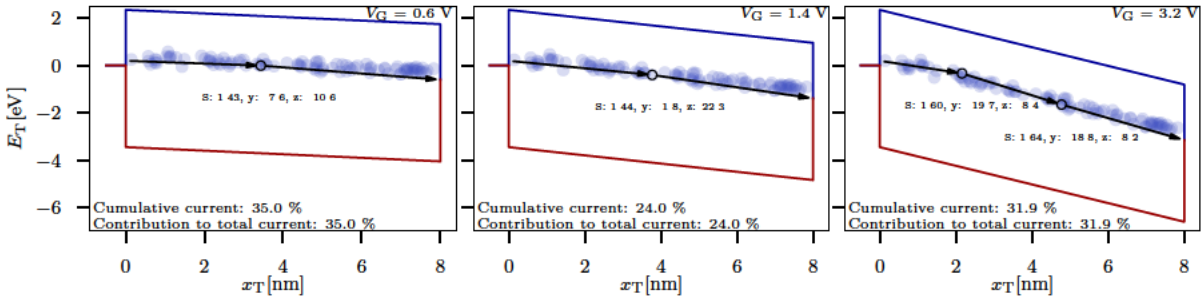

Figure 5.32. The most dominant percolation paths for the charge trapping band of the TZT capacitors are shown, as extracted by the modified Dijkstra algorithm at low **(left)** to intermediate gate bias **(center)**, **(right)**. At the larger bias, a third of the total current is conducted over two defects (multi-TAT), while at lower biases only one defect is involved in the TAT current (single-TAT). However, multi-TAT does not play a major role in the conduction, as the majority of the I_G is conducted over single defects of the polaron band at increased V_G.

band after being captured from the reservoir electrode. Thus, the contribution of the "trapping" band with lower E_T and E_R within a range as typically observed for oxide defects is investigated with Dijkstra's algorithm for multi-trap assisted percolation. As can be seen from Figure 5.32, indeed multi-TAT percolation over two defects is obtained at a voltage of 3.2 V. However, at this relatively high bias, the polaron assisted tunneling current dominates the observed leakage current in the TZT capacitor. Therefore, within the investigated technologies, multi-TAT conduction plays a subordinate role. Nonetheless, a general conclusion about whether the effect can be neglected or not, cannot be drawn from these studies.

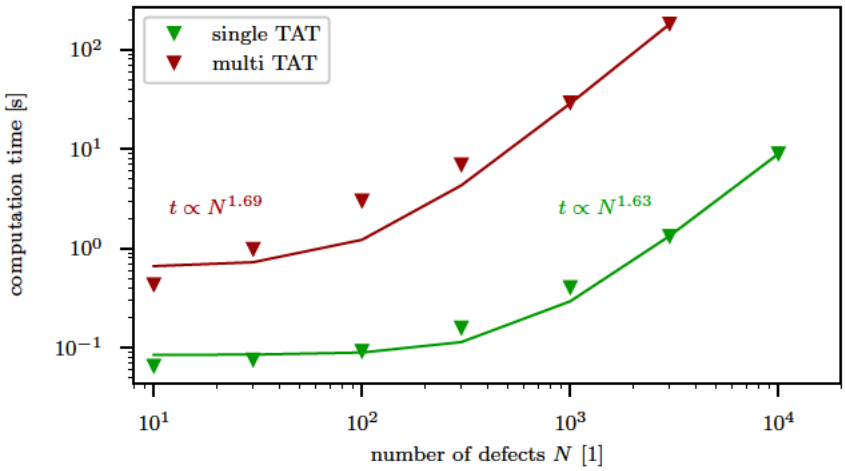

Figure 5.33. A performance comparison between multi-TAT (red) and single TAT (green) computation shows a similar exponential proportionality on the number of defects accounted for and the simulation execution time. The benchmark has been performed on a *Intel core i7 (10th gen.), 16Gb RAM* personal computer, for 30 simulation time steps.

The introduction of the non-linear coupling within the Master equation (4.10) requires the iterative solution of the system through a Newton scheme, whose convergence behavior depends on the initial value of the iteration and the defect coupling. When

comparing the computation of the full formulation with the computational effort for the decoupled (single-TAT) formulation, the computational cost is reduced by a factor of about 10 to 100 if the multi-TAT mechanism is neglected.

5.2.5 Summary

The leakage mechanisms of SiC/SiO_2 MOSCAPs and MOSFETs have been analyzed in detail by employing a detailed TAT model together with the WKB based Tsu-Esaki model for band-to-band tunneling. All important characteristics describing the involved charge transfer kinetics, e.g. temperature activation and transient shapes of $I_G\,(V_G)$, have been accurately reproduced when using only material parameters and physical defect parameters. These parameters agree well with those obtained by DFT for polarons in SiO_2. Further verification of the TAT model by accurately characterized leakage characteristics of TZT capacitors allows to identify two defect bands responsible for TAT, of which the first is responsible for transient charge trapping currents. The leakage currents caused by the second band show similar characteristics as for the polaron band in SiO_2. Furthermore, the parameters of the second defect band perfectly match the defect properties obtained with DFT computations of polarons in partially re-crystallized ZrO_2 models. Thus, polarons in general are likely to lead to TAT currents in many material systems employing amorphous binary oxides as components of their gate stacks. This stems from their favorable energetic trap level alignment within the insulator that is in between the electrode and insulator conduction band edges.

5.3 Conclusions

To the best of the author´s knowledge, modeling efforts related to charge-trapping in SiC MOSFETs have either been limited to empirical approaches, describing the time dependent degradation by a power-law, or to the extraction of capture and emission activation energy maps from measurement data. Going significantly beyond these efforts, BTI modeling presented here is based on device level simulations, relying solely on physical material parameters to parameterize two-state NMP transitions in large ensembles of pre-existing oxide and interfacial defects. Based on a novel effective single defect extraction algorithm, large experimental data sets have been used to extract defect parameters in different DMOS technologies, which are comparable in their electron trap distributions, but significantly differ in their hole trap distributions and thus NBTI characteristics. Due to the large variety of defects that can potentially form in SiC/SiO_2 MOSFETs and the wide active energy range allowing for defects almost in the entire SiO_2 bandgap to get charged and discharged, no single candidate can be identified to explain the defect distributions common among the technologies.

A novel approach for modeling TAT currents based on a deterministic solution of the hopping Master equation has been proposed and parameterized to explain leakage currents in SiC/SiO_2 structures in detail. Additionally, the model has been validated by

reproducing well explored leakage characteristics in TZT capacitors. The parameters determining the charge transfer kinetics allow for a comparison to ab-initio calculations, rendering polarons likely defect structures to enable TAT currents in material systems employing amorphous binary oxides as dielectric layers.

Chapter 6

Summary and Outlook

A synopsis of the results of this thesis concludes with the advances for the research field presented in the summary of this chapter. Based on the used methods and obtained results, suggestions for future extensions of this work related to unresolved challenges of characterizing and modeling SiC MOSFET reliability are finally discussed.

6.1 Summary

A large set of data characterizing **BTI in different SiC** based MOSFETs has been **reproduced by device level simulation of threshold voltage shifts**. For this, a two-state non-radiative multi-phonon model has been employed to accurately describe the kinetics of charge capture and emission at pre-existing structural defects. This model as implemented into the simulation framework Comphy **solely relies on physical material parameters** to calculate the ideal MOS electrostatics. To extract defect parameters from the extensive data set, with many potential defect distributions present at a large number of total defects, a **novel ESiD algorithm** has been used. This method has enabled the physical parametrization of the NMP model, which allowed to obtain **similarities of parameter distributions for electron traps** among the investigated **lateral channel SiC MOS devices** and comparable bulk oxide defects as extracted in **Si based MOSFETs** employing the same native oxide, i.e. SiO_2. Furthermore, these electron traps were demonstrated to be present in DMOS technologies of different manufacturers and generations with varying densities. However, large **differences in the hole trap densities** amongst the technologies have been obtained. The calibration of the reliability framework Comphy further enabled the **extrapolation of** $\Delta V_{\mathrm{th}}/\Delta R_{\mathrm{on}}$ of the DMOS technologies beyond typical experimental time-scales for operation relevant AC gate drive signals, rendering **bi-polar gate drive signals** with small negative off bias as the **most stable operation condition**.

In the second part of the work, a **novel TAT modeling** approach has been developed, including both defect to reservoir and **defect to defect charge transfer** reactions by employing a reduced NMP parametrization. These multi-TAT transitions have been shown to presumably play a **negligible role in most MOS gate stacks**, by an evaluation

following the implementation of the model in Comphy. Quite to the contrary, TAT currents via single defects have been accurately reproduced in technologies employing SiC/SiO_2 and ZrO_2 based capacitors. The defect parameters used in both technologies excellently fit those obtained for polarons with DFT. This renders **polarons a likely charge transition center to enable TAT currents in binary oxides** quite in general.

6.2 Outlook

Irrespective of the progress made in the field for describing BTI and TAT based on the defect centric NMP modeling approaches, there is still a number of potential improvements to the presented methods and models to fully model SiC MOSFETs reliability issues and the most important considered are outlined in the following:

- The post-stress recovery of V_{th} for **NBTI characterization** is commonly studied **on p-channel MOSFETs**. However, these devices are rarely needed in power switch applications and therefore such studies are rare for SiC MOSFETs. Thus, extending NBTI studies to SiC pMOS would allow to capture a larger fraction of defects in the lower half of the SiC bandgap and in the vicinity of the valence band edge due to the significantly slower charge transfer kinetics obtainable.
- A previously reported **switching cycle dependence of BTI in SiC trench MOSFETs** [95, 97] cannot be captured by a two-state NMP model, and requires further studies to reveal the underlying mechanism, e.g. as presented in [99].
- Recently, **optical emission** following bias switches from the accumulation to the inversion regime has been **correlated with BTI** in SiC trench MOSFETs [291, CSJ8]. The characterization of radiative transitions contributing to BTI allows for detailed studies of the parameters of the involved defects, e.g. charge transition levels.
- A **single defect study**, employing **TDDS or RTN** measurements, could reveal the stochastic properties of charge transfer kinetics and allow for a more detailed investigation of the defects NMP parameters. As in Si-based MOSFETs an extension to a four-state NMP model could be used to explain the underlying reactions. Although there is no obvious obstacle for an experimental scaling of the channel geometry, such studies have not been presented for SiC MOSFETs.
- The new TAT modeling approach allows studying **BTI and TAT in parallel** within one technology. However, for this appropriate test structures have to be designed with large enough gate area to measure small leakage currents and smaller structures that allow for detailed BTI studies.
- Additionally, the TAT model may be applied to explain leakage currents in other technologies, such as **thick inter-layer dielectrics**. An extension of the model to include defect generation, i.e. time evolution of defect densities, would extend its **applicability to SILC and to impact ionization** and allow to explain **TDDB**.

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List of Publications

Scientific Journals

[CSJ1] Maximilian Feil, Andreas Huerner, Katja Puschkarsky, **Christian Schleich**, Thomas Aichinger, Wolfgang Gustin, Hans Reisinger, and Tibor Grasser. "The Impact of Interfacial Charge Trapping on the Reproducibility of Measurements of Silicon Carbide MOSFET Device Parameters". In: *Crystals* 10.12 (2020). invited, pp. 1143-1–1143-14. DOI: 10.3390/cryst10121143. URL: https://www.iue.tuwien.ac.at/pdf/ib_2020/JB2020_Feil_1.pdf.

[CSJ2] **Christian Schleich**, Dominic Waldhör, Katja Anna Waschneck, Maximilian Feil, H. Reisinger, Tibor Grasser, and Michael Waltl. "Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies". In: *IEEE Transactions on Electron Devices* 68.8 (2021), pp. 4057–4063. DOI: 10.1109/TED.2021.3092295. URL: https://www.iue.tuwien.ac.at/pdf/ib_2021/JB2021_Schleich_1.pdf.

[CSJ3] Alexander Vasilev, Markus Jech, Alexander Grill, Gerhard Rzepa, **Christian Schleich**, Stanislav Tyaginov, Alexander Makarov, Gregor Pobegen, Tibor Grasser, and Michael Waltl. "TCAD Modeling of Temperature Activation of the Hysteresis Characteristics of Lateral 4H-SiC MOSFETs". In: *IEEE Transactions on Electron Devices* (2022), pp. 1–6. DOI: 10.1109/TED.2022.3166123.

[CSJ4] **Christian Schleich**, Dominic Waldhör, Theresia Knobloch, Weifeng Zhou, Bernhard Stampfer, Jakob Michl, Michael Waltl, and Tibor Grasser. "Single- Versus Multi-Step Trap Assisted Tunneling Currents - Part I: Theory". In: *IEEE Transactions on Electron Devices* 69.8 (2022), pp. 4479–4485. DOI: 10.1109/TED.2022.3185966.

[CSJ5] Theresia Knobloch, Yury Illarionov, Fabian Ducry, **Christian Schleich**, Stefan Wachter, Kenji Watanabe, Takashi Taniguchi, Thomas Müller, Michael Waltl, Mario Lanza, M. I. Vexler, Mathieu Luisier, and Tibor Grasser. "The Performance Limits of Hexagonal Boron Nitride as an Insulator for Scaled CMOS Devices Based on Two-Dimensional Materials". In: *Nature Electron-*

ics 4.2 (2021), pp. 98–108. DOI: 10.1038/s41928-020-00529-x. URL: https://www.iue.tuwien.ac.at/pdf/ib_2021/JB2021_Knobloch_1.pdf.

[CSJ6] Dominic Waldhör, **Christian Schleich**, Jakob Michl, Bernhard Stampfer, Konstantinos Tselios, Eleftherios Ioannidis, H. Enichlmair, Michael Waltl, and Tibor Grasser. "Toward Automated Defect Extraction From Bias Temperature Instability Measurements". In: *IEEE Transactions on Electron Devices* 68.8 (2021), pp. 4057–4063. DOI: 10.1109/TED.2021.3091966. URL: https://www.iue.tuwien.ac.at/pdf/ib_2021/JB2021_Waldhoer_1.pdf.

[CSJ7] **Christian Schleich**, Dominic Waldhör, Al-Moatasem El-Sayed, Konstantinos Tselios, Ben Kaczer, Tibor Grasser, and Michael Waltl. "Single- Versus Multi-Step Trap Assisted Tunneling Currents - Part II: The Role of Polarons". In: *IEEE Transactions on Electron Devices* 69.8 (2022), pp. 4486–4493. DOI: 10.1109/TED.2022.3185965.

[CSJ8] Maximilian Feil, Hans Reisinger, Andre Kabakow, Thomas Aichinger, **Christian Schleich**, Aleksandr Vasilev, Dominic Waldhoer, Michael Waltl, Wolfgang Gustin, and Tibor Grasser. "Electrically Stimulated Optical Spectroscopy of Interface Defects in Wide-Bandgap Field-Effect Transistors". In: *Communications Physics* (). submitted.

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[CSC2] Judith Berens, M. Weger, Gregor Pobegen, T. Aichinger, Gerald Rescher, **Christian Schleich**, and Tibor Grasser. "Similarities and Differences of BTI in SiC and Si Power MOSFETs". In: *Proceedings of the IEEE International Reliability Physics Symposium (IRPS)*. talk: IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA - virtual; 2020-03-29 – 2020-04-02. 2020, pp. 1–6. ISBN: 978-1-7281-3200-6. DOI: 10.1109/IRPS45951.2020.9129259. URL: https://www.iue.tuwien.ac.at/pdf/ib_2020/CP2020_Berens_1.pdf.

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Master Thesis

[CST1] **Christian Schleich**. "Charakterisierung und Modellierung von SiC Transistoren". MA thesis. Institut für Mikroelektronik, 2019.

Curriculum Vitae

Personal Information

Name	Christian Schleich
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Education

since 02/2019	**PhD Candidate** at Institute for Microelectronics, TU Wien, Austria; Primary Supervisor: Univ.Prof. Dipl.-Ing. Dr.techn. Tibor Grasser Title of Dissertation: Modeling of Defect Related Reliability Phenomena in SiC Power-MOSFETs
03/2017 - 02/2019	**Master's Degree in Microelectronics and Photonics (With Distinction)** Institute for Microelectronics, TU Wien, Austria; Primary Supervisor: Univ.Prof. Dipl.-Ing. Dr.techn. Tibor Grasser Faculty of Electrical Engineering and Information Technology, TU Wien, Austria Thesis: Characterization and Modeling of SiC MOSFETs
10/2013 - 02/2017	**Bachelor's Degree in Electrical Engineering and Information Technology (With Distinction)** Faculty of Electrical Engineering and Information Technology, TU Wien, Austria
09/2001 - 06/2006	**HTBLA Braunau** Electronics / Technical Informatics

Awards

11/2020	**Price for Master Thesis of the City of Vienna (Diplomarbeitspreis der Stadt Wien)**
2013 - 2016	**Three Annual Merit Scholarships (Leistungsstipendien)** Faculty of Electrical Engineering and Information Technology, TU Wien, Austria

Employment

since 02/2019	**Research Projectassistant** Christian Doppler Laboratory for SDS at the Institute for Microelectronics, TU Wien, Austria
2015 - 2019	**Student Assistant** Institute for Microelectronics, TU Wien, Austria
08/2014-09/2014	**Technical Training Engineer** EV Group Europe & Asia/Pacific GmbH
03/2010-09/2013	**Technical Support Engineer** EV Group Europe & Asia/Pacific GmbH
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